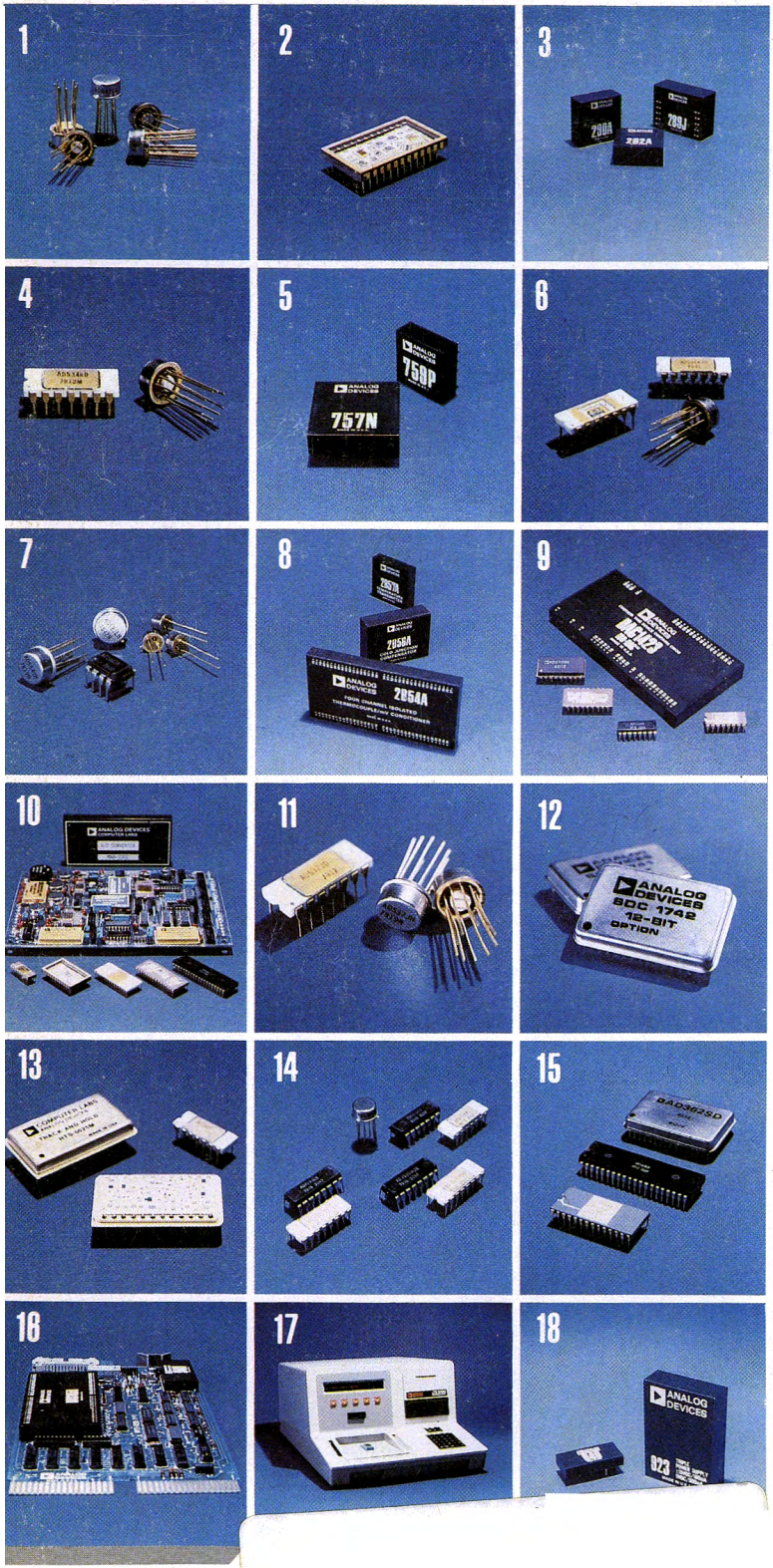

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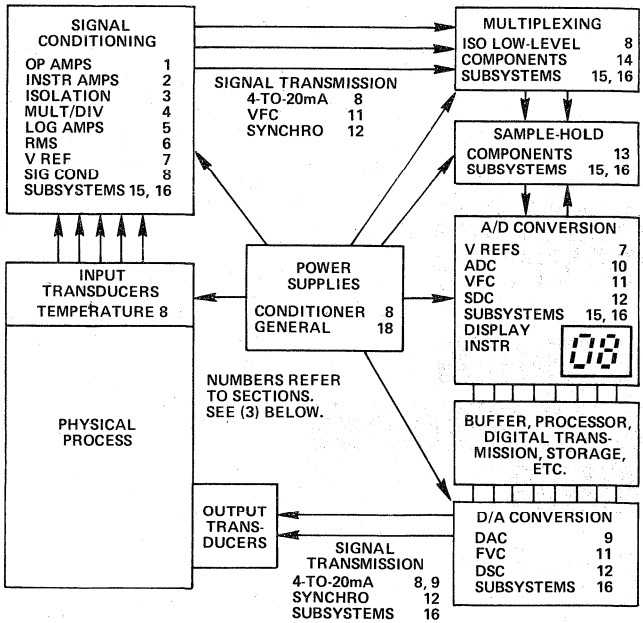

HOW TO FIND IT

This is a catalog of our entire line of IC and modular data-acquisition components and subsystems for measurement and control. It contains data sheets for all the products recommended for new designs, and—on page vii—a list of products not catalogued here, but still available; data sheets are available upon request. This catalog is designed to make it easy to find and choose any product listed here.

1. **If you know the model number,** look up its page number in the alphabetic/numeric listing inside the front cover.

2. **If you know the function,** go directly to the numbered section listed for the function, using the "bleed tabs" at the right. Each section has a Table of Contents and a Selection Guide, which also suggests other sections where similar functions might be found.

3. **If you know the function but can't find the right words,** you will probably find it, together with its location in the catalog, in the above block diagram of a generalized real-world process.

4. **Choosing a device:** Each Section starts with a Selection Guide, which compares each device with others of the same class. With it, you can pick out the device(s) having the performance and features nearest to what you need and turn immediately to the indicated page number(s) for complete data.

5. **Understanding:** Following most of the Selection Guides, there are "Orientation" sections, which include definitions of terms, for added understanding of the devices and how to select them.

If it isn't here . . . Ask! We'll be happy to give you information on our MACSYM intelligent computer-based Measurement And Control SYsteMs, our digital panel-instrument line, our integrated-circuit chips, and any other aspects of our products, processes, and prices. Just get in touch with Analog Devices or the nearest office.

Device Testing: If you use linear ICs, you may be interested in our LTS-2000 Linear Test Systems, described in Section 17.

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DATA ACQUISITION COMPONENTS AND SUBSYSTEMS CATALOG

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Specifications and prices shown in this catalog are subject to change without notice.

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General Introduction

Analog Devices designs, manufactures, and sells worldwide sophisticated electronic components and subsystems for use in precision measurement and control. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including bipolar, I^2L, CMOS, and hybrid integrated circuits, and assembled products in the form of potted modules, printed-circuit boards, and instrument packages. The list on the Cover is a summary of our IC and modular component and subsystem classes. The Complete Contents, starting on page v, provides a detailed panorama of these products.

State-of-the-art technologies have been utilized (and, in many cases, invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Fifteen years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens the leadership position of Analog Devices in data-acquisition products.

MAJOR PROGRESS

Since the publication of the last complete *Data Acquisition Products Catalog*, in 1978, our components and subsystems have been augmented by several major lines: high-speed "video" a/d and d/a converters, signal-conditioning and current-loop products for transducers, and computer-based automatic testing equipment for analog ("linear")-circuit users. In addition, we have introduced a number of landmark integrated-circuit products, including a complete true-12-bit microprocessor-compatible IC a/d converter (the AD574) and a complete single-supply internally referenced voltage-output 8-bit microprocessor-compatible d/a converter on a single monolithic chip (the AD558).

TECHNICAL SUPPORT

Analog Devices offers extensive technical literature, which discusses the technology and applications of products for precision measurement and control. Besides comprehensive data sheets, of which there are many outstanding examples in this book, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and two serial publications: *Analog Productlog*, which provides brief information on new products being introduced, and *Analog Dialogue*, our technical journal, which provides in-depth discussions of new developments in analog and digital circuit technology as applied to data-acquisition and control. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to data-book catalogs—such as this one—we also publish several short-form catalogs, including a *Short-Form Guide* to our entire product line. You will find our publications described on page ix.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our sales offices are listed on pages x and xi.

STANDARDS

Many products comply with MIL-STD-883B and/or other customer requirements. Analog Devices Semiconductor has complete capabilities for 100% screening of devices per Methods 5004 and 5005 of MIL-STD-883B; generic data is available on many of our products. Our CMOS facility in the Republic of Ireland has received plant approval from the European standardization authority; its quality-assurance procedures and capabilities have met the standards of CECC (CENELEC Electronic Components Committee), which are essentially compatible with what are known in the U.S.A. as MIL-M-38510 and MIL-STD-883B.

G.S.A. LISTING

Many products in this catalog are covered under G.S.A. contracts. If your organization is qualified to purchase on G.S.A. contracts, see your Analog Devices sales engineer or write on letterhead to the Analog Devices Sales Department for a copy of the Analog Devices "Authorized Federal Supply Schedule Price List."

PRODUCTS NOT CATALOGUED HERE

To make this catalog maximally useful to designers of new equipment, without its attaining unwieldy size, we have limited its contents to those products most likely to be used for the design of new circuits and systems. If the data sheet for a product you are interested in is not here, turn to page vii, where you will find a list of older products for which data sheets are available upon request. On page viii, you will find a guide to substitutions for products no longer available.

PRICES

At Analog Devices, we recognize that prices of our products are an important consideration in making a choice among our many available product families. To this end, we believe that prices should be both stable and available. However, in the present economy, with its unpredictable costs of materials and energy, curent price information at the time a catalog goes to the printer may be out of date within a few months after publication. Rather than publish possibly misleading information, we have for the time being decided not to publish prices in this catalog. As always, current price lists and/or price quotations are available upon request from our sales offices.

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●New product since 1979 *Data Acquisition Products Catalog Supplement*

Product Families Not Catalogued Here (But Still Available)

The information published in this catalog is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs or in designs for which they are uniquely suitable. Data sheets on these products are available upon request.

2N3954
2N5900
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ADC-16Q
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DAC-QM
DAC-QS
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DAC-10Z
DGM1040
MDA-F
MDA-8H
MDA-10Z
MDA-11MF
MDA-LB
MDA-LD
MDA-UB
MDA-UD
SCDX1623
SCM1677
SERDEX
SHA-1A
SHA-3
SHA-4
SHA-5
SHA-6
SHA-1114
SHA-1134
SMC1007
SMX1004
SMX2607
SRX1005
SRX2605
SSCT1621
STX1003
STX2603
TSDC1608–1611

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column below are no longer available. In many cases, comparable functions and performance may be obtained with newer models, but — as a rule — they are not directly interchangeable. The closest recommended equivalent, physically and electrically, is listed in the right-hand column.

Model	Closest Recommended Equivalent
47	48
101 (module)	45
102	48
106	118
107	118
108	52
110	48
114	119
115	43
120	50
142	48
143	52
149	50
161	165
170	171
220	234
274J	286J
282J	292A
283J	292A
301 (module)	52
302	310
602J10	610
602J100	610
602K100	610
901	904
AD501	AD511
AD505	AD509
AD508	AD517
AD513	AD503
AD516	AD506
AD551	AD553
AD555	AD7519
ADC1121	AD7550
ADM501	ADM501/506
ADP501	ADP511
DAC1122	AD7541
DAC-10H	DAC-10Z
MDA-10H	MDA-10Z

Operational Amplifiers

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AD515J/K/L Electrometer IC Op Amps	1-45
AD517J/K/L/S High-Accuracy Low Drift IC Op Amps	1-51
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AD540J/K/S FET-Input IC Op Amps	1-61
AD542J/K/L/S Trimmed Implanted FET (TRIFET) IC Op Amps	1-65
AD544J/K/L/S Trimmed Implanted FET (TRIFET) IC Op Amps	1-69
AD545J/K/L/M Low Bias Current FET IC Op Amps	1-73
AD642J/K/L/S Dual AD542 Trimmed Implanted FET (TRIFET) Op Amps ●	1-77
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AD OP-07/A/D/C/E High-Accuracy Low-Drift IC Op Amps●	1-83
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52J/K High-Accuracy Low-Bias FET-Input Modules	1-97
171J/K High-Output Modules	1-99
235J/K/L Inverting Chopper-Stabilized Modules	1-103
261J/K Noninverting Chopper Op Amps	1-107

●New product since 1979 *Data-Acquisition Products Catalog Supplement.*

Selection Guide
Operational Amplifiers

In this Selection Guide, operational amplifier families are divided into the following categories:

1. General-Purpose ICs (see also selected high-accuracy versions in Category 5.)
2. FET-Input, Low-Bias Current ICs and Modules
3. FET-Input *Dual* ICs
4. Electrometer IC and Modules
5. High-Accuracy Low-Drift ICs and Modules
6. High-Accuracy Low-Drift Chopper-Amplifier Modules
7. Fast Wideband ICs and Modules
8. High-Output Modules
9. Isolated Op-Amp Modules

The brief specifications given are key for the device category. Complete and detailed specifications for further comparison can be found on the data sheets. Information on selection principles and definitions of the specifications can be found in the pages that follow.

All specifications are typical at rated supply voltage and load, and $T_A = 25°C$, unless noted otherwise.

1. General Purpose IC's	Offset Voltage mV max	$\Delta E_{OS}/\Delta T$† $\mu V/°C$ max	Bias Current nA max	Slew Rate V/μs	Page
AD301A/201A/101A†#	7.5/2/2	30/15/15	250/75/75	0.5 to 10*	1-17
AD741/741C† Internal Comp	5.0/6.0	No Spec.	500	0.5	1-79

2. FET-Input Low Bias Current IC's and Module	Bias Current pA max	Offset Voltage mV max	$\Delta E_{OS}/\Delta T$‡ $\mu V/°C$ max	Slew Rate V/μs	Page
AD515J/K/L	0.3/0.15/0.075	3/1/1	50/15/25	0.3 min	1-45
AD545J/K/L/M	2/1/1/1	1/1/0.5/0.25	25/15/5/3	0.3 min	1-73
52J/K Module	3	0.5	3/1	0.25 min	1-97
AD506J/K/L/S	15/10/5/10	3.5/1.5/1/1.5	75/25/10/50	3.0 min	1-21
AD503J/K/S	15/10/10	50/20/20	75/25/50	3.0 min	1-21
AD542J/K/L/S TRIFET #	50/25/25/25	2/1/0.5/1	20/10/5/15	3.0	1-65
AD544J/K/L/S TRIFET #	50/25/25/25	2/1/0.5/1	20/10/5/15	8 min	1-69
AD540J/K/S #	50/25/25	50/20/20	75/25/50	6.0	1-61

3. FET-Input Dual IC TRIFET	Bias Current pA max	Offset Voltage mV max	$\Delta E_{OS}/\Delta T$‡ $\mu V/°C$ max	Slew Rate V/μs	Page
AD642J/K/L/S #●	75/35/35/35	2/1/0.5/1	20/10/5/15	3.0	1-65

4. Electrometer IC and Modules	Bias Current fA max	Offset Voltage mV max	$\Delta E_{OS}/\Delta T$ ‡ $\mu V/°C$ max	Slew Rate V/ms min	Page
310J/K Inverting Module	10	10	30/10	0.4	**
311J/K Noninverting Module	10	10	30/10	0.4	**
AD515J/K/L IC Differential	300/150/75	3/1/1	50/15/25	300	1-45

5. High Accuracy Low-Drift IC's and Module	Offset mV max	$\Delta E_{OS}/\Delta T$†, ‡ $\mu V/°C$ max	Bias Current nA max	Slew Rate V/μs	Page
AD OP-07/A/D/C/E† #●	0.075/0.025/0.15/ 0.15/0.075	1.3/0.6/2.5/1.8/1.3	±3.0/2.0/12/7/4	0.17	1-83
AD517J/K/L/S #	0.15/0.075/0.05/0.075	3/1.8/1.3/1.8	5/2/1/2	0.1	1-51
AD510J/K/L/S #	0.1/0.05/0.025/0.05	3/1/0.5/1	25/13/10/13	0.1	1-41
AD504J/K/L/M/S #	2.5/1.5/0.5/0.5/0.5	5/3/1/0.5/1 nulled	200/100/80/80/80	0.12 to 2.5*	1-25
52J/K Module	0.5	3/1	0.003	0.25 min	1-97
AD301AL† #	0.5	5.0	30	0.5 to 10*	1-17
AD741J/K/L/S #	3/2/0.5/2	20/15/5/15 untrimmed	200/75/50/75	0.5	1-79

6. High Accuracy Low-Drift Chopper Amplifier Modules	Offset μV max	$\Delta E_{OS}/\Delta T$‡ $\mu V/^{\circ}C$ max	Bias Current pA max	Slew Rate V/μs	Page
235J/K/L Inverting	25/25/15	0.5/0.25/0.1	100/50/50	0.3	1-103
261J/K Low-Noise, Noninverting	25	0.3/0.1	300	100V/s	1-107

7. Fast, Wideband IC's and Modules	Settling Time to 0.1%, μs	Slew Rate V/μs, min	$\Delta E_{OS}/\Delta T$†, ‡ $\mu V/^{\circ}C$ max	I_{BIAS} nA max	Page
50J/K Module	0.1 (INV, max)	500 (INV)	50/15	2	1-93
51A/B‡ Module (-25°C to +85°C)	0.15 (INV, max) 0 to +70°C	400 (INV)	50/20	2	1-93
(-55°C to +100°C Operating)	0.25 (INV, 0.05%) -25°C to +85°C				
HOS-050/050A† TO-8	0.08 (INV)	300 (INV)	150/35	2	1-89
48J/K Fast Settling Module	0.5 (0.01%, max)	110 (INV)	50/15	0.05/0.025	1-91
AD509J/K/S IC	0.2/0.5 max/0.5 max	80/80/100	20 typ/30/30	250/200/200	1-37
AD518J/K/S IC #	0.8	50	10 typ/15/20	500/250/250	1-57
AD507J/K/S IC	0.9	20/25/20	15 typ/15/20	25/15/15	1-33

8. High-Output Modules	E_{OUT} F.S. (min)	I_{OUT} F.S. (min)	$\Delta E_{OS}/\Delta T$‡ $\mu V/^{\circ}C$ max	I_{BIAS} pA max	Page
171J/K	±140V	±10mA	50/15	50/20	1-99
50J/K	±10V	±100mA	50/15	2000	1-93
51A/B‡ -25°C to +85°C (Spec.) (-55°C to +100°C Oper.)	±10V	±100mA	50/20	2000	1-93
HOS-050/050A† TO-8	±10V	±100mA	150/35	2000	1-89

9. Isolated Op Amp Modules		Page
277J/K/A	Inverting, noninverting, differential op-amp applications, Input offset drift 3/1/1$\mu V/^{\circ}C$ (nulled), bias current 20nA max, CMR 160dB min at dc, 120dB min at 60Hz, max CMV 3500V rms (60Hz, 1 min), ±2500V peak or dc, continuous, isolated power output, ±15mA @ ±15V.	3-7

*Inverting—Actual value depends on compensation.
†301A, 301AL, 0 to +70°C; 201A, -25°C to +85°C; 101A, -55°C to +125°C; 741C, 0 to +70°C; 741, -55°C to +125°C; HOS, -55°C to +125°C; AD OP-07D/C/E, 0 to 70°C; AD OP-07/A, -55°C to +125°C.
‡Temperature range suffixes (e.g. AD504J/K/L/M/S) J/K/L/M, 0 to +70°C; S, -55°C to +125°C; 51A/B, 277A, -25°C to +85°C.
#Monolithic chips available with guaranteed performance for precision hybrids. Information available upon request. All but AD642 and AD OP-07 can be found in 1979 Chip Catalog, available upon request.
•New product since 1979 *Data Acquisition Products Catalog Supplement.*
**Data sheet available upon request.

Orientation
Operational Amplifiers

The amplifiers listed in this catalog are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more-general requirements in electronic circuits. The technical data included here*cover the properties of some 20 op-amp families, comprising about 75 distinct types. Some are general purpose, others provide near-optimum performance for specific classes of applications.

They differ in a variety of ways, for example, circuit technology, circuit architecture, input properties, output properties, operating temperature range, degree of isolation, and in terms of the many performance specifications. Some are high-performance modules, most are monolithic ICs, some are hybrid ICs.

BACKGROUND

The operational amplifier is today the most-widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control), and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 1-16 a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. It should come as no surprise to successful users of Analog Devices op amps that a number of the references are to the applications sections of data sheets included in this catalog.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.* Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.

2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.* Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to translate these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishining the circuit architecture, (2) defining the permance levels, and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier, or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks", and linear circuit books, as well as in application notes and data sheets.

2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of parameters, and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high-frequency performance and transient behavior of the op-amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist, which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.

3. The designer must then relate acceptable performance of the op-amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows the next section.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier.

*In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request.

Chopper stabilized amplifiers, for example, are not generally applicable where differential inputs are required.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, DC offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gain-bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If DC information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and all of the "drift" specifications may usually be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where DC information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

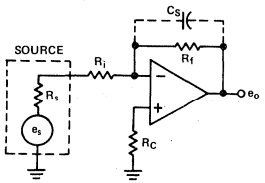
1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_s, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier R_{cm}.

2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy. For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b), and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for



$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i\right]$$ For $R_C = 0$ and $R_s \ll R_i$

Signal; Input Drift Error = V_d

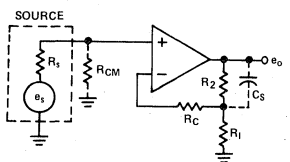
$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\frac{R_f + R_i}{R_f} + i_d R_i\right]$$ For $R_C = R_i R_f/(R_i + R_f)$ and $R_s \ll R_i$

Signal; Input Drift Error = V_d

Input Impedance $R_{IN} \approx R_i$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1A. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_b R_s\right]$$ for $R_C = 0$

Signal; Drift Error = V_d

$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_d R_s\right]$$ for $R_C = R_s - \frac{R_i R_2}{R_i + R_2}$

Signal; Drift Error = V_d

Input Impedance $R_{IN} \approx R_{CM}$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1B. Noninverting Configuration

increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

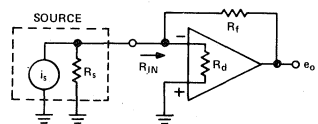
Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from +25°C need be considered. For example, over the range of −25 to +85°C, the maximum temperature excursion (ΔT) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm},



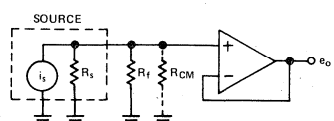
$$e_o = -R_f\left[i_s + e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b\right]$$

Signal; Drift error = $I\epsilon$

Input Impedance $R_{IN} = \left(\frac{R_f R_d}{R_f + R_d}\right)\left(\frac{1}{1 + A\beta}\right)$

where $1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s \quad R_d}$ $\% \text{ Drift Error} = \frac{100\ I\epsilon}{i_s}$

Figure 2A. Current Amplifier



$$e_o = R_f i_s + e_{os} + i_b R_f$$ for $R_s > R_f$

Signal; Drift Error = V_d

Input Impedance $R_{IN} \approx R_f$

$$\% \text{ Drift Error} = \frac{100V_d}{R_f\ i_s}$$

Figure 2B. Voltage Amplifier with Sampling Resistor

for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T} \left(\frac{R_f + R_s}{R_f R_s} \right) + \frac{\Delta i_B}{\Delta T} \right] \Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μsec, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm, and stray capacitance, C_S, were one picofarad then the closed loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in turn is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_s will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

For greater emphasis wideband applications can be separated into two categories – steady state and transient. Since the amplifier requirements for the two are somewhat different; these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is DC coupling required?* If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.

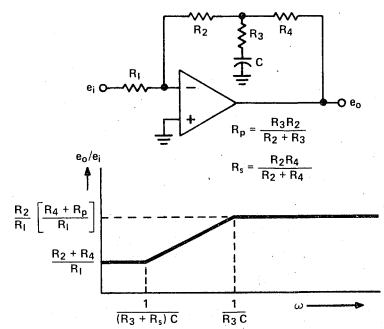


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, f_{c1}(−3dB). For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta = A/G$). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

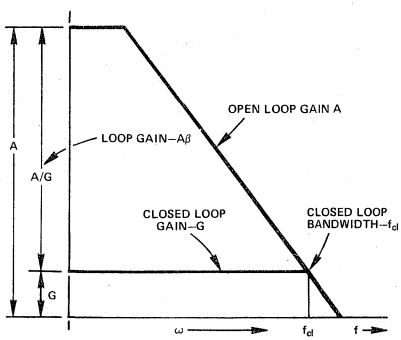


Figure 4. Closed Loop Bandwidth and Loop Gain

a. Closed loop gain stability = $\Delta G/G$
$\Delta G/G = (\Delta A/A)\ [1/(1 + A\beta)]$ where $\Delta A/A$ is the open loop gain stability, usually about 1%/°C.

b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, usually 200 to 5000 ohms.

c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?* You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier.

For some monolithic amplifier designs available today their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

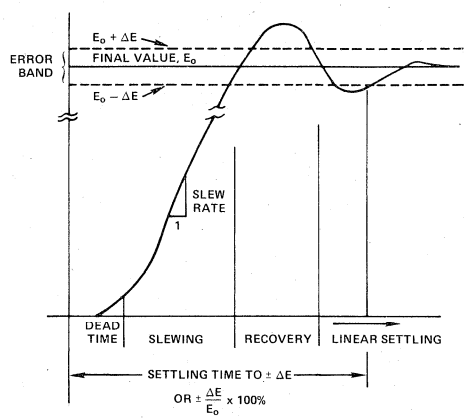


Figure 5. Typical Settling Time Characteristics

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

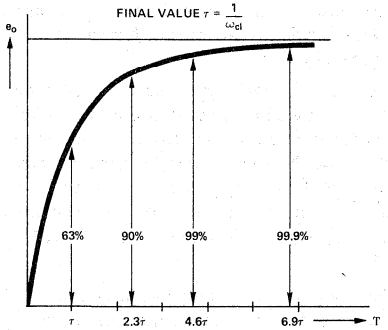


Figure 6. Step Response for Linear 6dB/Octave Amplifier

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:

$e_n = \sqrt{4KTBR}$

where e_n = the rms value of the noise voltage

K = Boltzman's Constant (1.38×10^{23} joules/°K)

T = absolute temperature of the resistance, °K

B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldy for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

(1) Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n \text{ (rms)} = (40nV/\sqrt{Hz})\left(\sqrt{\frac{R}{100k\Omega}\ (BW)}\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

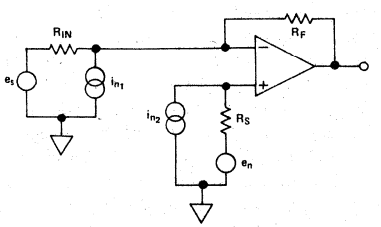
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 7A illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a RMS fashion.

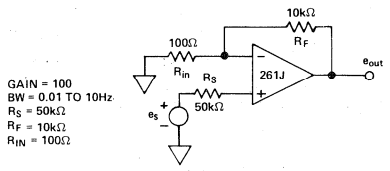


COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4KTBR_{IN}}\ (R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4KTBR_S}\ (R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4KTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\ (R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\ (R_F/R_{IN}+1)$

$$\text{TOTAL NOISE} = \sqrt{(e_{R_{IN}}\ G)^2 + [e_{R_S}\ (G+1)]^2 + e^2{}_{R_F} + (i_{n_1}\ R_F)^2 + [(i_{n_2}\ R_S)\ (G+1)]^2 + [e_n\ (G+1)]^2}$$

Figure 7A. Noise Components

Figure 7B illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, model 261J, the lowest noise non-inverting chopper type amplifier is being used with a 50kΩ source impedance. The two major noise sources, in addition to the 261J input voltage noise of 1μV p-p, are the Johnson noise (58μV p-p) and current noise (100μV p-p).



1) RESISTOR NOISE: $R_F \rightarrow 13nV/\sqrt{Hz}$
$R_{IN} \rightarrow (1.3nV/\sqrt{Hz})\ 100$
$R_S \rightarrow (28nV/\sqrt{Hz})\ 101 = 2.8\mu V/\sqrt{Hz}$
TOTAL RESISTOR NOISE IN 10Hz BW =
$(2.8\mu V/\sqrt{Hz})\ \sqrt{10Hz}\ 6.6\mu V\ p\text{-}p/\mu V\ rms = 58\mu V\ p\text{-}p$

2) AMPLIFIER CURRENT NOISE: (20pA p-p) (50k) (101) = 100μV p-p
(20pA p-p) (10k) = 0.2μV p-p

3) AMPLIFIER VOLTAGE NOISE: (1μV p-p) (101) = 100μV p-p

TOTAL OUTPUT NOISE = $\sqrt{(100)^2 + (100)^2 + (58)^2} \approx 150\mu V\ p\text{-}p$

Figure 7B. Design Example

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide, in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations. In general, IC's can be distinguished from modules by the "AD" prefix.

Temperature Range and Nomenclature. Analog Devices operational-amplifier nomenclature uses suffixes to permit ready identification of the temperature range for which device operation to meet critical specifications has been designed or selected. The most popular range comprises the "commercial" temperatures from 0 to 70°C; it is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD741L). Also popular is the "military" range, −55°C to +125°C, designated by S, T, U, (e.g., AD510S); not all families have types with specified performance in this range. There are a few types designed for operation in the "industrial" range, −25°C to +85°C, designated by A, B (e.g., model 51B). Wide-range types will generally meet the same or better specs in a narrower temperature range. A few types are second-sources for products originally introduced by other manufacturers. In those instances, the generic nomenclature is used (AD741C) or enlarged upon, if superior selections are offered (e.g., AD301AL).

There are nine divisions by class of application, based on optimization of one or more key specifications. Versions of many devices in this class are available to meet requirements of MIL-STD-883B; the availability of such devices will be noted on the data sheets.

1. *General-Purpose ICs.* Amplifiers in this group include our lowest-cost devices. They are best-suited for general purpose designs with moderate drift requirements, down to 5μV/°C max (AD301AL), and gain-bandwidth to 8MHz (AD301A). Typical applications include summing, inverting, impedance buffering (followers), and active filtering. They are also useful for developing nonlinear transfer functions, with appropriate external circuitry.

Bipolar monolithic technology is used for all types. The AD741 is internally compensated; it does not require external capacitance for frequency compensation. On the other hand, the AD301A's ability to be externally compensated, by either lag or feedforward circuitry, permits circuits with a wide range of dynamic performance characteristics to be handled. Extended-temperature-range equivalents are the AD101A, AD201A, and AD741.

2. *Low Bias-Current, High Input-Impedance, FET-Input ICs and Modules.* These types use the inherently high impedance and low leakage current of junction field-effect transistors (FET's) to deal with configurations that either provide the measurement of low currents or require the use of high-resistance circuitry.

Typical applications range from general-purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to measurements with high-impedance transducers, such as photomultipliers, flame detectors, pH cells, and radiation detectors.

The performance range is from the 75fA (75×10^{-15} A) maximum bias current of the AD515L electrometer to the 50pA max of the general purpose, lowest-cost AD540J. The AD542 is a low-cost, laser-wafer-trimmed (LWT) monolithic implanted FET input amplifier with low offset and drift. The AD544 is similar, but has higher speed. Low bias current does not necessarily imply large voltage offsets; the AD515K combines a 150fA (0.15pA) max bias current with 1.0mV max offset and 15μV/°C max voltage drift; comparable figures for model 52K are 3pA, 0.5mV, and 1μV/°C.

Extended-temperature-range equivalents are AD503S, AD506S, AD540S, AD542S, and AD544S.

Except for Model 52J/K, the types in this group either are completely monolithic or employ matched FET's and a special bipolar amplifier chip designed to accommodate the input FET's electrically. In nearly all the IC's, thin-film resistors are deposited on the chip at critical circuit locations to ensure stability; low offsets and drift are achieved by laser-trimming of circuit balance. All FET-input op amps from Analog Devices are manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmed-up bias current). Our published max bias-current specification applies to either input (some manufacturers call "bias current" the *average* of the two input currents). Bias current of junction FET's approximately doubles for every 10°C increase of temperature.

3. *FET-Input Dual ICs.* The AD642 is a single-chip pair of trimmed implanted-FET-input (TRIFET) op amps similar to the AD542, with low warmed-up bias current (35pA max − K, L, S), low offset voltage (0.5mV max − L), low offset-voltage drift (5μV/°C max − L), and excellent V_{os} matching (0.25mV max − L). Besides applications calling for more than one FET-

input op amp at low cost per function, the AD642 is especially useful in applications calling for matched duals, such as log-ratio amplifiers, FET-input instrumentation amplifiers, and buffering of differential signals.

4. *Electrometers.* This class comprises the lowest bias-current devices, the AD515 ICs and models 310 and 311 modules. The AD515L, with its 75fA input bias current, 1mV max offset, and 25μV/°C offset tempco, has differential inputs, and can be used in voltage measurements at high impedance, as a follower, or in current measurements, as an inverter, or even differentially.

The 310K is primarily an inverting amplifier, with 10fA (10^{-14} A) max bias current at the negative input (±1nA at the positive input), 10mV offset voltage (adjustable to zero), and 10μV°C tempco; the 311K is primarily non-inverting, with the same specifications, and the 10fA max bias current is specified for the *positive* input. This type can be used differentially but asymmetrically; an example is the 311 as a follower-with-gain, using low-value resistors in the feedback network).

These amplifiers differ from the AD515 in design technique, as well as in manufacturing technology. The 310 and 311 are a unique pair of amplifiers that achieve their outstanding input specifications with *parametric-amplifier* inputs. A high-frequency carrier, applied to a varactor bridge, is modulated by the differential input voltage of the amplifier, transformer-coupled, amplified, and demodulated. Although it intrinsically has noise-free amplification, a parametric circuit also has substantial input capacitance — 30pF differential for model 310, vs. 2.4pF total for AD515 — always a consideration in low-current measurement, because of the long charging time at low currents. On the other hand, the 310/311 can withstand fault voltages up to ±300V between the inputs. Noise is also a consideration in low-level amplifiers. Typical current noise for the AD515 is 3fA (peak-to-peak) in the 0.1 to 10Hz band; current noise for the 310/311 is 1fA (peak-to-peak) in the 0.01 to 1Hz band. Corresponding voltage noise if 4μV p-p (AD515, 0.1 to 10Hz) and 10μV p-p (310/311, 0.01 to 1Hz).

These amplifiers do not have standard extended-temperature-range equivalents. Data sheets for 310/311 are available.

5. *High-Accuracy Low-Drift Differential-Input ICs and Modules.* "Chopperless" low-drift designs with differential inputs, optimized for voltage offset and drift, dc open-loop gain, and CMR, should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators, and for impedance buffer designs.

Performance of internally compensated premium amplifiers in this group ranges from the ADOP-07A's 25μV max offset voltage and 0.6μV/°C drift, and the AD517L's 50μV max offset voltage and 1.3μV/°C drift, combined with 1nA max bias current (1.5nA max over the temperature range), and CMR of 110dB min, to the low-cost AD741L's maximum offset of 0.5mV and max offset tempco of 5μV/°C, with 100nA max bias current over the temperature range, and CMR of 90dB min. The best overall performer in this group in high impedance applications is the FET-input model 52K, which combines low offset and drift (0.5mV and 1μV/°C) with 3pA bias current. The ADOP-07 is a superior second source to other OP-07 families; for example, ADOP-07AH has minimum gain of 3×10^6 V/V compared to 3×10^5 V/V.

Among *uncompensated* op amps, the premium range is from the AD504M, with 0.5mV maximum offset voltage, 0.5μV/°C max drift, 100nA max bias current over the temperature range, and 110dB CMR, to the low-cost AD301AL, with max offset of 0.5mV, max drift of 5μV/°C, max bias current of 45nA over the temperature range, and minimum CMR of 90dB. For applications in which low noise is essential, the AD504M has 100%-tested guaranteed maximum voltage noise of 0.6μV p-p, for the frequency range 0.1 to 10Hz, and maximum spot noise of 13, 10, and 9nV/$\sqrt{\text{Hz}}$ and 1.3, 0.6, and 0.3pA/$\sqrt{\text{Hz}}$, at 10Hz, 100Hz, and 1000Hz, respectively.

External dynamic compensation permits considerably greater bandwidths, at higher gains, than are available with the compensated AD517 and AD510 families. For example, with a 3.9pF compensating capacitor, the AD504's typical small-signal bandwidth is 100kHz at a gain of 200, vs. 1.5kHz for the internally compensated AD510; under the same conditions, the full-power bandwidth of the AD504 is 30kHz, vs. 1.5kHz for the AD510. With feedforward compensation, the AD301AL has a full-power bandwidth in excess of 150kHz, for inverting applications.

Except for model 52, all of the amplifiers in this class are monolithic*. The AD741J/K/L and the AD301AL are selected from production lots of the generic AD741 and AD101A types. The AD504, AD510, and AD517 are thermally balanced for low drift and high gain (independent of output loading), with inputs that are bootstrapped for high CMR and protected against overloads to prevent bias-current degradation due to reverse breakdown. Thin-film resistors, deposited on the chip, are another key to the stability of these amplifiers. The AD510 and the AD517 employ super-beta input transistors to achieve low bias current, and they are laser-trimmed at the wafer-probe stage (LWT) to achieve their excellent offset-voltage specifications at low cost. Since the bias currents are always of one polarity, they can be nulled at a given temperature with simple circuitry; and the change over the temperature range will be considerably less than for low-cost FET-input amplifiers having comparable specifications.

Extended-temperature-range equivalents are AD504S, AD510S, AD714S, and AD517S.

6. *High-Accuracy Modules Using Chopper Techniques.* The amplifiers in this class are widely accepted as the best choice when it is essential to maintain low voltage offsets and bias currents with time and temperature or whenever external offset adjustments are not practical in the application. Using carrier modulation techniques, these designs achieve drifts to 0.1μV/°C and long-term stability to ½μV/mo. Typical applications include error-summing amplifiers for servo loops, pre-

*In the AD510, the compensating capacitor is bonded to the header, alongside the monolithic amplifier chip.

cision regulators, and input amplifiers for laboratory-grade metering instruments and test equipment.

Two forms of amplifier are available. The *noninverting chopper-amplifier* (261 family) is a high gain feedback amplifier, containing a MOSFET chopper, optimized for follower-with-gain applications. The chopper converts the difference between the dc or low-frequency input voltage, at high impedance, and the feedback voltage to a high-frequency square-wave, amplifies it with no drift, and demodulates and filters the result to produce an output waveform that is an amplified version of the input. The closed-loop gain is determined by the attenuation ratio of the feedback resistor-pair.

The initial offset is ±25μV max (trimmable to zero), with average drift-vs.-temperature of 0.1μV/°C max (model 261K). Bias current is respectable, at 300pA max, with a tempco of 10pA/°C max, to minimize errors with high-impedance sources.

Maximum noise voltage is 0.4μV peak-to-peak, from 0.01 to 1.0Hz, and 1.0μV, from 0.01 to 10Hz. Small-signal bandwidth, established by an external compensating capacitor that is chosen as a function of gain, is 100Hz.

Inverting chopper-stabilized amplifiers (235 family) employ narrow-band chopper amplifiers to measure the summing-point voltage of the main amplifier (which should be at a null), chop, amplify, filter, and feed to the positive input of the main amplifier an amplified correction signal. Thus, the offset voltage and drift of the main amplifier (including the effects of input bias current) are reduced by the gain of the chopper amplifier, without a corresponding reduction of bandwidth.

Chopper and chopper-stabilized amplifiers should be considered when long-term stability must be maintained with time and temperature, and wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include amplification of microvolt-level signals, precision integration, and analog computing.

These amplifiers do not have standard extended-temperature-range equivalents.

7. *Wide Bandwidth, Fast-Settling ICs and Modules.* High-speed op amps are characterized by high slewing rates, fast settling time, and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data, in buffers, d/a converters, and multiplexer circuitry; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimal distortion, since the large-signal bandwidth is closely related to the slewing rate.

The products in this category with outstanding specifications are models HOS-050, 50J/K, and 48J/K. Settling of the hybrid HOS-050 is to within 0.01% in 300ns in the inverting connection. Model 50's max slewing rate is 500V/μs inverting, 400V/μs noninverting, and small-signal unity-gain bandwidth is 70MHz; full-power bandwidth is 8MHz, min. In addition, all of these devices will deliver ±100mA of output current at ±10V, an important factor in video and line-driver circuitry, and in driving capacitive loads. For example, the current required to sustain 500V/μs in a 100pF load is I = C dV/dt = 50mA. Model 48J/K is optimized for settling time: 500ns maximum to 0.01%, inverting or non-inverting, with output of ±20mA at ±10V.

There are three families of monolithic ICs listed in this category, with slewing rates ranging from 25V/μs min to 100V/μs min. The AD509S is the fastest slewing (100V/μs min) and settling (500ns min to 0.1% and 2.5μs min to 0.01%). The AD507K is the best all-around performer, with small-signal bandwidth of 35MHz, slewing rate of 25V/μs min, and typical settling to 0.1% within 900ns, in addition to open-loop dc gain of 10^5 min, drift of 15μV/°C max, and bias current of 15nA max. The AD518J is the lowest in cost, yet it slews at 50V/μs min, and typically settles to within 0.1% in 800ns, with single-capacitor compensation.

Extended-temperature-range equivalents are models 51A/B, AD507S, AD509S, and AD518S.

8. *Differential FET-Input High-Out Modules.* This beefy group includes models HOS-050, 50, 51, and 171. The hybrid HOS-050 and models 50 and 51 will furnish up to ±100mA at ±10V out. In addition both are excellent wideband amplifiers. Besides the applications suggested for them in the wide-bandwidth category, they are useful for such applications as current booster/buffer for op amps dealing with low-level signals—either outside the loop or inside the loop. They are protected against short circuits.

For extended-temperature-range operation, models 51A/B operate from -25°C to +85°C and HOS-050 operates over the -55°C to +125°C range.

The model 171 has a large output voltage swing, ±140V at ±10mA, when used with ±150V supplies. However, it need not operate symmetrically; any combination of power-supply voltages between the limits of 15 to +300V for the positive side and -15 to -300V for the negative side is acceptable (including single-supply operation), provided that the total voltage across the amplifier is within the range of 30 to 300V. The output will swing to within 10V of the V_S^+ and V_S^- supply rails. The output and both inputs are protected against short circuits to common or to either supply. Model 171K has an open-loop gain of 10^6 min, offset of 1mV, drift of 15μV/°C max, bias current of 20pA max, CMR of 100dB min, unity-gain small-signal bandwidth of 3MHz, and slewing rate of 10V/μs. Typical applications include high compliance-voltage current source, high-voltage follower-with-gain, high-voltage integrator, differential amplifier for high-common-mode-voltage bridge applications, and high-voltage reference supply.

Model 171 does not have standard extended-temperature-range equivalents.

9. *Isolated Operational Amplifier Module.* Model 277 combines a high-performance uncommitted operational-amplifier

input stage with a precision, isolated output stage, an isolated dual ±15V power supply, and transformer-coupled isolation circuitry, to form a versatile isolation amplifier. It is rated to withstand input/output common-mode voltage of 3500V rms max (60Hz, 1 minute), and peak continuous ac or dc of ±2500V max, and has input-output CMR of 160dB min at dc and 120dB min at 60Hz, with leakage current of 1μA @ CMV of 115V rms, 60Hz ($Z_L = 10^{12}\Omega \| 16pF$).

The input-stage performance makes many op-amp applications feasible: ±1μV/°C max offset tempco (trimmed, model 277K), bias current of ±20nA max, open-loop gain of 106dB min. In addition, isolated power output of ±15mA max at ±15V, referred to input common, is available for auxiliary front-end circuitry. The output stage has gain of 1V/V, nonlinearity of 0.05% max, 1.5kHz full-power bandwidth, and 50μV/°C offset tempco.

Typical applications for the 277 include general isolated op-amp circuitry, programmable-gain isolated amplifier, isolated power source and amplifier for bridge measurements, instrumentation amplifier, instrumentation-grade process-signal isolator, and current-shunt measurements.

The extended-temperature-range equivalent of models 277J/K is model 277A.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage
Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, in some applications, such as voltage comparators, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection
An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is often expressed logarithmically: CMR (in dB) = $20 \log_{10}$ (CMRR).

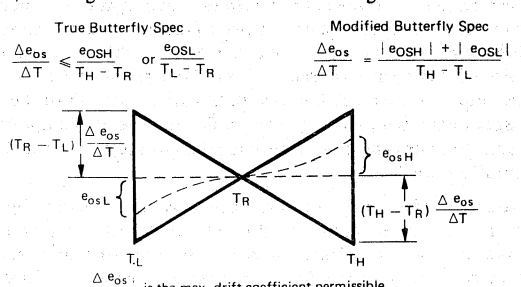
The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified (on the other hand, the incremental CMR may be less in the neightborhood of large CMV). Published CMR specifications for op amps pertain to very low-frequency voltages, unless specified otherwise; CMR decreased with increasing frequency.

Common-Mode Voltage, Maximum
For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connection.

Drift vs. Supply
Offset voltage, bias current, and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature
Offset voltage, bias current, and difference current all change, or "drift", from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature ranges); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more-) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drifts in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less



than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").

The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time
Offset voltage, bias current, and difference current change with time as components age. It is important to realize that drift with time is random, and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift for a chopper-stabilized amplifier might be quoted at 1μV/day, whereas cumulative drift over 30 days might not exceed 5μV, or 15μV in a year (e.g., model 235). A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response
The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. There is no industry-wide accepted value for the distortion level which determines the full-linear-response limitation, but we use 3% as a maximum acceptable limit for modules.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more-serious effect (often overlooked) is an effect equivalent to a dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often of interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current
Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average.* For single-ended amplifiers (i.e., chopper types), bias current refers to the current at the input terminal.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature* (some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" spec used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current
Difference current is defined as the difference between the bias currents at the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

Input Impedance
Differential input impedance is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the non-inverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage
Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise
Input voltage- and current-noise characteristics can be speci-

fied and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. The primary difference is that, when evaluating noise performance, bandwidth must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise", resistor noise, or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some types, spectral-density plots or "spot noise", at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain

Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response.*

Overload Recovery

Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output

Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate

The slewing rate of an amplifier, usually in volts per microsecond ($V/\mu s$), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response

Unity-gain small-signal response is the frequency at which the open-loop gain falls to 1V/V, or 0dB under a specified compensation condition. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification. For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and non-inverting configurations. However, if feedforward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

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"Specifying and Measuring a Low-Noise FET-Input IC Op Amp" by Bill Maxwell, ANALOG DIALOGUE 8-2, 1974

USEFUL TUTORIAL MATERIAL IN DATA SHEETS

Electrometer Circuitry, see AD515 and Models 310/311

High-Speed Amplifiers, see AD518 and Models 50/51

Low-Drift Differential Op Amp Performance, see AD504

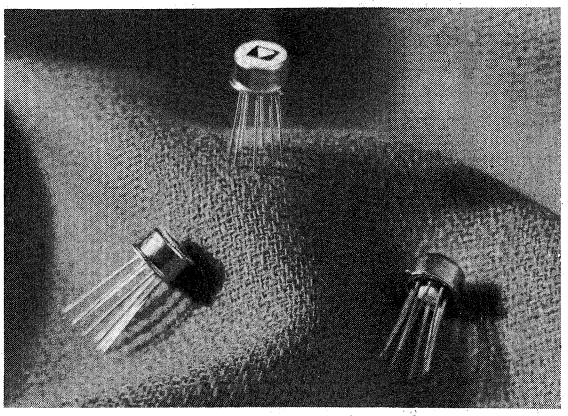
Low-Level Applications of Chopper-Stabilized Amplifiers:
Inverting, see Models 234, 235
Non-Inverting, see Model 261

General Purpose Low Cost IC Operational Amplifier

AD101A, AD201A, AD301A, AD301AL

FEATURES

- Low Bias and Offset Current
- Single Capacitor External Compensation for Operating Flexibility
- Nullable Offset Voltage
- No Latch-Up
- Fully Short Circuit Protected
- Wide Operating Voltage Range

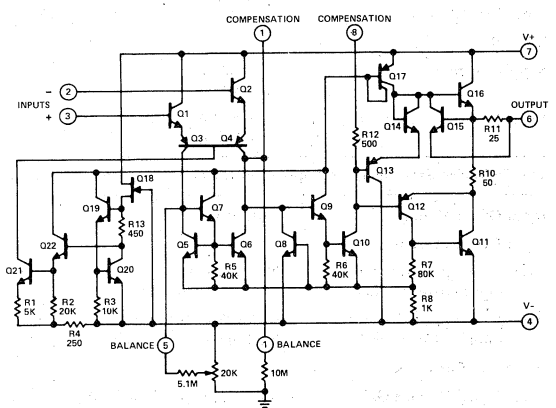


GENERAL DESCRIPTION

The Analog Devices AD101A, AD201A, AD301A and AD301AL are high performance monolithic operational amplifiers. All the circuits feature full short circuit protection, external offset voltage nulling, wide operating voltage range, and the total absence or "latch-up". Because frequency compensation is performed externally with a single capacitor (30pF maximum), the AD101A, AD201A, AD301A and AD301AL provide greater flexibility than internally compensated amplifiers since the degree of compensation can be fitted to the specific system application.

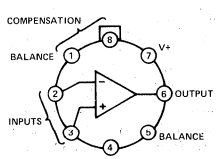
The AD101A and AD201A have identical specifications in the TO-99 package; the former guaranteed over the −55°C to +125°C temperature range, and the latter over −25°C to +85°C. The AD201A is also available in the mini-DIP package for high performance operation over the 0 to +70°C temperature range. The AD301A is specified for operation over the 0 to +70°C temperature range in both the TO-99 and mini-DIP packages. The AD301AL is the highest accuracy version of this series. Improved processing and additional electrical testing allow the user to achieve precision performance at low cost. The device provides substantially increased accuracy by reducing errors due to offset voltage (0.5mV max), offset voltage drift (5.0μV/°C max), bias current (30nA max), offset current (5nA max), voltage gain (80,000 min), PSRR (90dB min), and CMRR (90dB min). The AD301AL is also specified from 0 to +70°C and is available in the TO-99 can or 8-pin mini-DIP.

SCHEMATIC DIAGRAM

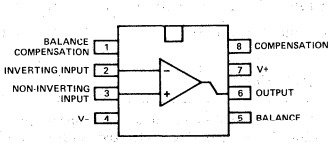


CONNECTION DIAGRAMS (TOP VIEW)

TO-99



Mini-DIP

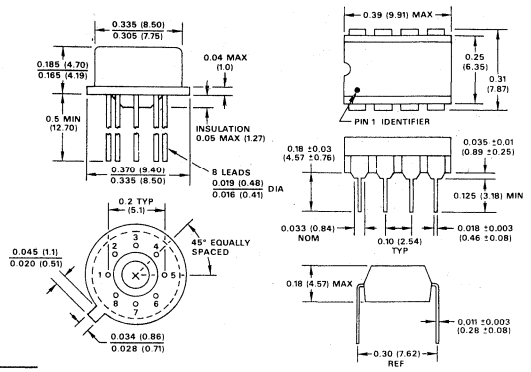


SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

ABSOLUTE MAXIMUM RATINGS	AD101A, AD201A, AD301A, AD301AL unless otherwise specified
Supply Voltage	
AD101A, AD201A	±22V
AD301A, AD301AL	±18V
Power Dissipation[1]	
TO-99 (Metal Can)	500mW
Dual In-Line (Mini-DIP)	500mW
Differential Input Voltage	±30V
Input Voltage[2]	±15V
Output Short Circuit Duration[3]	Indefinite
Operating Temperature Range	
AD101A	-55°C to +125°C
AD201A (TO-99)	-25°C to +85°C
AD201A (Mini-DIP)	0 to +70°C
AD301A, AD301AL	0 to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60sec)	300°C

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99 (H) MINI-DIP (N)

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)[4]

Parameter	Conditions	AD101A/AD201A Min	AD101A/AD201A Typ	AD101A/AD201A Max	AD301A Min	AD301A Typ	AD301A Max	AD301AL Min	AD301AL Typ	AD301AL Max	Units
Input Offset Voltage	$R_S \leq 50k\Omega$		0.7	2.0		2.0	7.5		0.3	0.5	mV
Input Offset Current			1.5	10		3	50		3	5	nA
Input Bias Current			30	75		70	250		15	30	nA
Input Resistance		1.5	4		0.5	2		1.5	4		MΩ
Supply Current	V_S = ±20V		1.8	3.0							mA
	V_S = ±15V					1.8	3.0		1.8	3	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	50	160		25	160		80	300		V/mV
The Following Specifications Apply Over the Operating Temperature Ranges[4]											
Input Offset Voltage	$R_S \leq 50k\Omega$			3.0			10		0.5	1	mV
Input Offset Current				20			70		5	10	nA
Average Temp. Coefficient of Input Offset Voltage	$T_A(min) \leq T_A \leq T_A(max)$		3.0	15		6.0	30		2	5	μV/°C
Average Temp. Coefficient of Input Offset Current	+25°C$\leq T_A \leq T_A$(max)		0.01	0.1		0.01	0.3		0.01	0.1	nA/°C
	T_A (min)$\leq T_A \leq$+25°C		0.02	0.2		0.02	0.6		0.01	0.1	nA/°C
Input Bias Current				100			300		30	45	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	25			15			40	100		V/mV
Input Voltage Range	V_S = ±20V	±15									V
	V_S = ±15V				±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	90		90	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	96		90	100		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±14		±12	±14		±12	±14		V
	V_S = ±15V, R_L = 2kΩ	±10	±13		±10	±13		±10	±13		V
Supply Current	$T_A = T_A$(max), V_S = ±20V		1.2	2.5					1.8	3	mA

[1] The maximum desirable junction temperature of the AD101A is +150°C; that of the AD201A, AD301A and AD301AL is +100°C. For operating at elevated temperatures, devices must be derated based upon a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. The thermal resistance of the Dual In-Line package is +160°C/W, junction to ambient.

[2] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

[3] For the AD301A and AD301AL continuous short circuit is allowed for case temperatures to +70°C and ambient temperatures to +55°C.

[4] Unless otherwise specified, these specifications apply for supply voltages and ambient temperatures of ±5V to ±20V and -55°C to +125°C for the AD101A, ±5V to ±20V and -25°C to +85°C for the AD201AH (0 to +70°C for the AD201AN), and ±5V to ±15V and 0 to +70°C for the AD301A and AD301AL.

Specifications subject to change without notice.

ORDERING GUIDE

MODEL	TEMP RANGE	ORDER NUMBER
AD301AL	0 to +70°C	AD301AL*
AD201A	−25°C to +85°C	AD201A*
AD301A	0 to +70°C	AD301A*
AD101A	−55°C to +125°C	AD101AH

* Add package type letter: H = TO-99, N = Mini-DIP

FREQUENCY COMPENSATION CIRCUITS

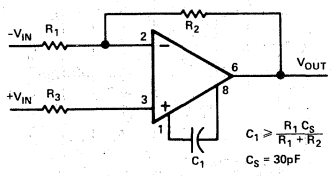


Figure 1. Single Pole Compensation

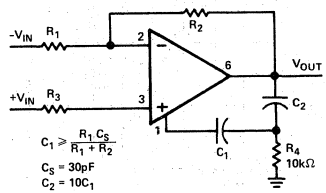


Figure 2. Two Pole Compensation

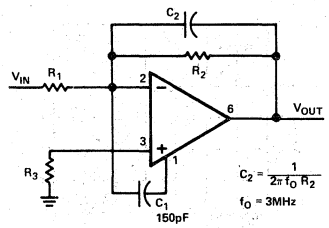
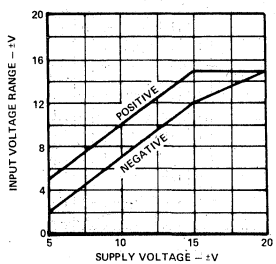
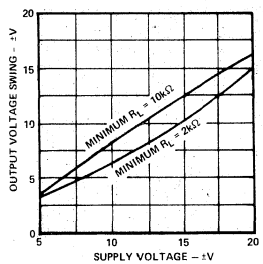


Figure 3. Feedforward Compensation

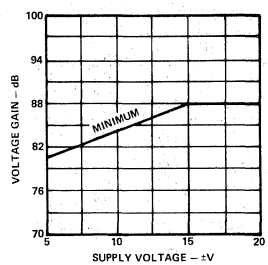
GUARANTEED PERFORMANCE CURVES (Curves apply over the Operating Temperature Ranges)



Input Voltage Range

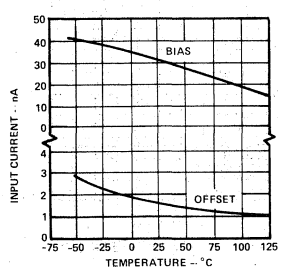


Output Swing

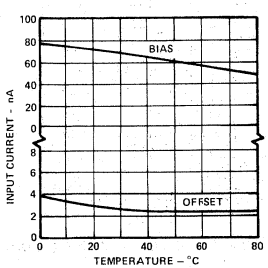


Voltage Gain

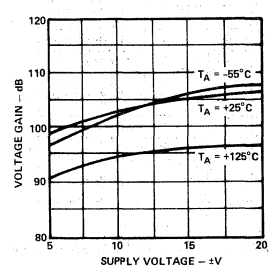
TYPICAL PERFORMANCE CURVES[4]



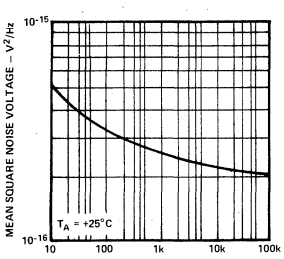
Input Current AD101A, AD201A



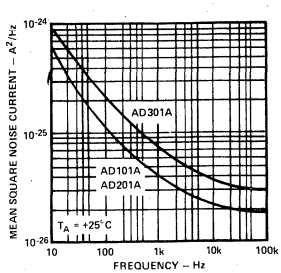
Input Current – AD301A



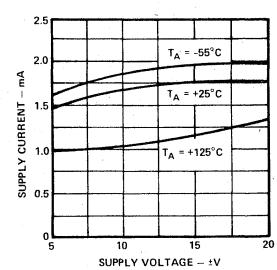
Voltage Gain



Input Noise Voltage

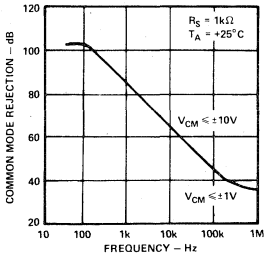


Input Noise Current

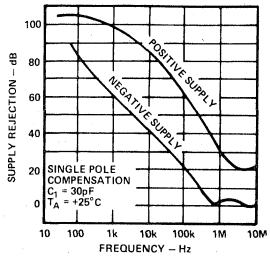


Supply Current

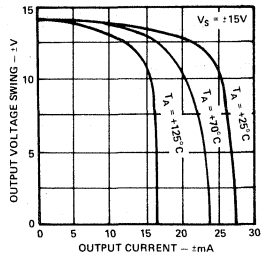
TYPICAL PERFORMANCE CURVES



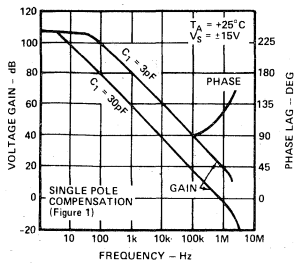
Common Mode Rejection



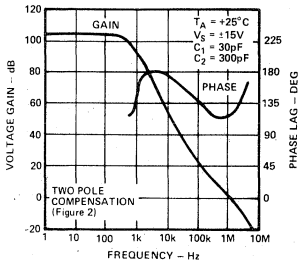
Power Supply Rejection



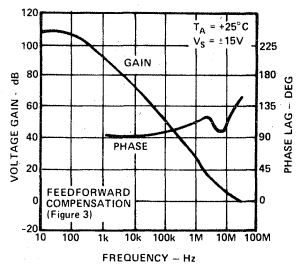
Current Limiting



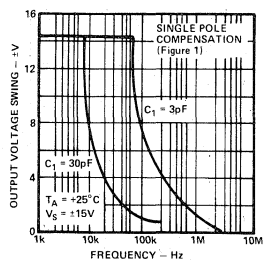
Open Loop Frequency Response



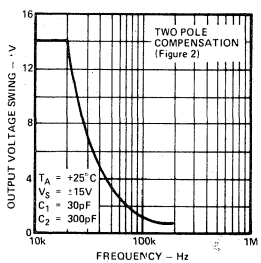
Open Loop Frequency Response



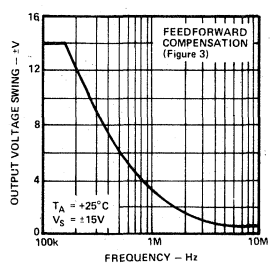
Open Loop Frequency Response



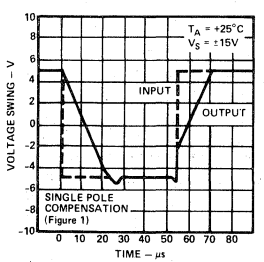
Large Signal Frequency Response



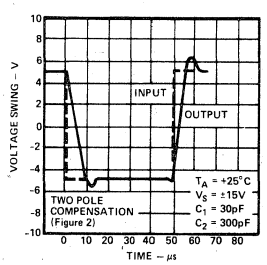
Large Signal Frequency Response



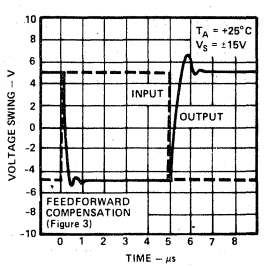
Large Signal Frequency Response



Voltage Follower Pulse Response



Voltage Follower Pulse Response



Inverter Pulse Response

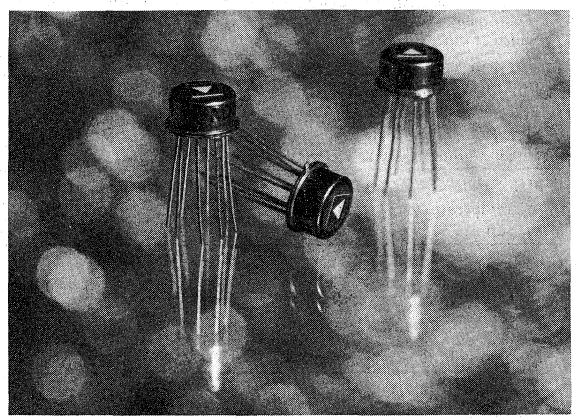
ANALOG DEVICES

High Accuracy Low Offset IC FET-Input Op Amps

AD503, AD506

FEATURES

Low I_b: 15pA max (AD503J, AD506J)
5pA max (AD506L)
Low V_{OS}: 1mV max (AD506L)
Low Drift: 25μV/°C max (AD503K, AD506K)
10μV/°C max (AD506L)



PRODUCT DESCRIPTION

The AD503J/AD506J, AD503K/AD506K, AD506L and AD503S/AD506S are IC FET input op amps that provide the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The devices achieve maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. They are free from latch-up and are short circuit protected. No external compensation is required as the internal 6dB/octave rolloff provides stability in closed loop applications.

The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance. The AD506, with specifications otherwise similar to the AD503, offers significant improvement in offset voltage and nulled offset voltage drift by supplementing the AD503 configuration with internal laser trimming of thin film resistors to provide typical offset voltages below 1mV.

The AD503 and AD506 are especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the noninverting "buffer" connection is used). The AD503 and AD506 IC FET input amplifiers, therefore, are of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

All the circuits are supplied in the TO-99 package; the AD503J, K and AD506J, K and L are specified for 0 to +70°C temperature range operation; the AD503S and AD506S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD503 and AD506 op amps meet their published input bias current and offset voltage specs after full warmup. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD503 and AD506 are specified as a maximum for *either* input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Offset voltage nulling of the AD503 and AD506 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±0.8μV/°C per millivolt of nulled offset for the AD506 and ±2.0μV/°C per millivolt of nulled offset for the AD503, compared to several times this for other IC FET op amps.
4. The gain of the AD503 and AD506 is measured with the offset voltage nulled. Nulling a FET input op amp can cause the gain to decrease below its specified limit. The gain of the AD503 and AD506 is fully guaranteed with the offset voltage both nulled and unnulled.
5. Bootstrapping of the input FET's achieves a superior CMRR of 80dB, while reducing bias currents and maintaining them constant through the CMV range.
6. To maximize the reliability inherent in IC construction, every AD503/AD506 receives a stabilization bake for 24 hours at 150°C. All guaranteed dc parameters are 100% computer tested, including offset voltage drift. AC performance and noise parameters are continually reviewed.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/μs min (6.0V/μs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10μs	*	*
INPUT OFFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs. Temperature, T_A = min to max	75μV/°C max (30μV/°C typ)	25μV/°C max (10μV/°C typ)	50μV/°C max (20μV/°C typ)
vs. Supply, T_A = min to max	400μV/V max (200μV/V typ)	200μV/V max (100μV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	$10^{11}\Omega \| 2pF$	*	*
Common Mode	$10^{12}\Omega \| 2pF$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*
5Hz to 50kHz	5.0μV (rms)	*	*
f = 1kHz (spot noise)	$30.0nV/\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

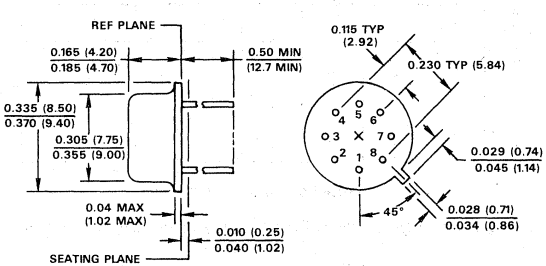
NOTES:
[1] Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2] A conservative design would not exceed 500pF of load capacitance.
[3] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4] Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[5] See comments in Input Considerations section.

*Specifications same as for AD503J.
**Specifications same as for AD503K.
Specifications subject to change without notice.

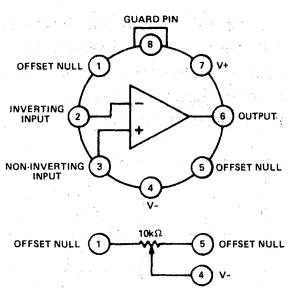
AD506J	AD506K	AD506L	AD506S
*	**	75,000 min (100,000 typ)	**
*	**	50,000 min	25,000 min
*	*	*	*
*	*	*	*
1000pF	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
3.5mV max (1.0mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.4mV typ)	1.5mV max (0.5mV typ)
*	**	10μV/°C max (5μV/°C typ)	50μV/°C max (20μV/°C typ)
**	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)
*	**	5pA max (2pA typ)	**
*	*	*	*
*	*	*	*
40μV (p-p)	*	*	*
8μV (rms)	*	6μV (rms)	*
80nV/√Hz	*	25nV/√Hz	*
±4V	*	*	*
*	*	*	*
*	**	**	**
*	*	*	*
*	*	*	±(5 to 22)V
7mA max (5mA typ)	*	*	*
*	*	*	-55°C to +125°C
*	*	*	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS



APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 and AD506 specify maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced in the AD503 and AD506 by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

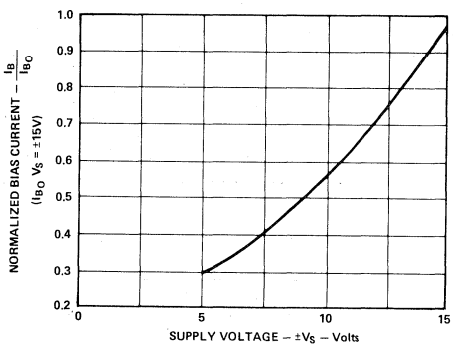


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD503K and AD506K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

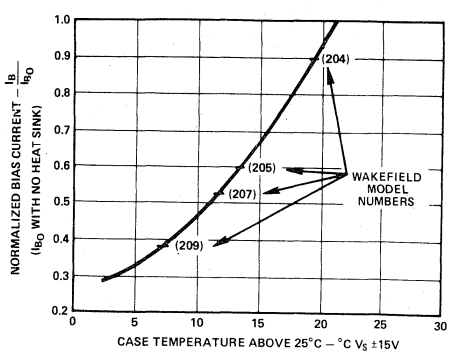


Figure 2. Normalized Bias Current vs. Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503/AD506K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

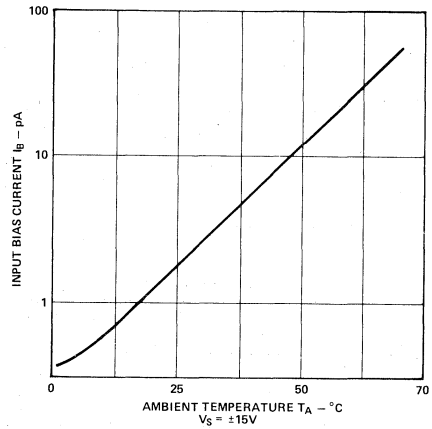


Figure 3. Input Bias Current vs. Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 volts and negative common mode inputs to $-V_S$ are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed $V_{CM} = V_S$.

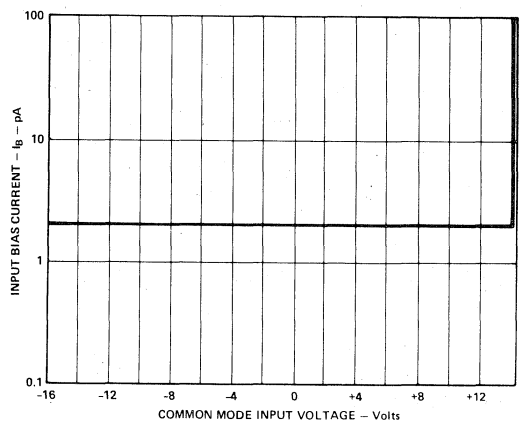


Figure 4. Input Bias Current vs. Common Mode Voltage

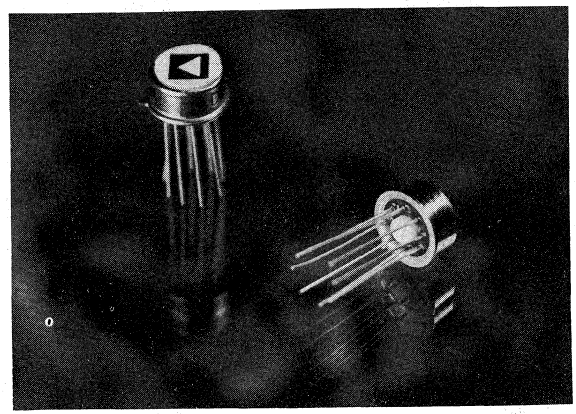
Like most other FET input op amps, the AD503 and AD506 display a degraded bias current specification when operated at moderate differential input voltages. The AD503 maintains its specified bias current up to a differential input voltage of ±3V typically, while the AD506's bias current performance is not significantly degraded for $V_{diff} \leqslant 4V$ typically. Above $V_{diff} = \pm 3V$ in the AD503 and $V_{diff} = \pm 4V$ in the AD506, the bias current will increase to approximately 400μA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase $100\mu A/V_{diff}$ (in volts), and other parameters may suffer degradation.

ANALOG DEVICES

High Accuracy IC Operational Amplifier

AD504

FEATURES
Low V_{OS}: 500μV max (AD504M)
High Gain: 10^6 min (AD504L, M, S)
Low Drift: 0.5μV/°C max (AD504M)
Free of Popcorn Noise



PRODUCT DESCRIPTION

The Analog Devices AD504J, K, L, M and S IC operational amplifiers provide ultra-low drift and extremely high gain, comparable to that of modular amplifiers, for precision applications. A new double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than 10^6, offset voltage drift of less than 1μV/°C, small signal unity gain bandwidth of 300kHz, and slew rate of 0.12V/μs. Because of monolithic construction, the cost of the AD504 is significantly below that of modules, and becomes even lower with larger quantity requirements. The amplifier is externally compensated for unity gain with a single 470pF capacitor; no compensation is required for gains above 500. The inputs are fully protected, which permits differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits to ground and/or either supply voltage, and is capable of driving 1000pF of load capacitance. The AD504J, K, L and M are supplied in the hermetically sealed TO-99 package, and are specified for operation over the 0 to +70°C temperature range. The AD504S is specified over the −55°C to +125°C temperature range and is also supplied in the TO-99 package.

PRODUCT HIGHLIGHTS

1. Fully guaranteed and 100% tested 1μV/°C maximum voltage drift combined with voltage offset of 500μV (AD504L).
2. Fully protected input ($\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, and is of critical importance in this type of device whose overall performance is strongly dependent upon front-end stability.
3. Single capacitor compensation eliminates elaborate stabilizing networks while providing flexibility not possible with an internally compensated op amp. This feature allows bandwidth to be optimized by the user for his particular application.
4. High gain is maintained independent of offset nulling, power supply voltage and load resistance.
5. Bootstrapping of the critical input transistor quad produces CMRR and PSRR compatible with the tight 1μV/°C drift. CMRR and PSRR are both in the vicinity of 120dB.
6. Noise performance is closely monitored at Outgoing QC to ensure compatibility with the low error budgets afforded by the performance of all other parameters.
7. Every AD504 receives a stabilization bake for 24 hours at 150°C to ensure reliability and long term stability.
8. The 100 piece price of the AD504 is 1/3 to 1/2 less than that of modular low drift operational amplifiers, and is competitive with the price of less accurate IC op amps.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

PARAMETER	AD504J	AD504K	AD504L
OPEN LOOP GAIN			
V_{OS} = ±10V, $R_L \geq 2k\Omega$	250,000 min (4 x 10^6 typ)	500,000 min (4 x 10^6 typ)	10^6 min (8 x 10^6 typ)
$T_{min} \leq T_A \leq T_{max}$	125,000 min (10^6 typ)	250,000 min (10^6 typ)	500,000 min (10^6 typ)
OUTPUT CHARACTERISTICS			
Voltage at $R_L \geq 2k\Omega$, $T_{min} \leq T_A \leq T_{max}$	±10V min (±13V typ)	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal, C_c = 390pF	300kHz	*	*
Full Power Response, C_c = 390pF	1.5kHz	*	*
Slew Rate, Unity Gain, C_c = 390pF	0.12V/μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leq 10k$	2.5mV max (0.5mV typ)	1.5mV max (0.5mV typ)	0.5mV max (0.2mV typ)
vs Temp, $T_{min} \leq T_A \leq T_{max}$, V_{OS} nulled	5.0μV/°C max (0.5μV/°C typ)	3.0μV/°C max (0.5μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
$T_{min} \leq T_A \leq T_{max}$, V_{OS} unnulled†	10μV/°C max (1.5μV/°C typ)	5.0μV/°C max (1.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
vs Supply	25μV/V max	15μV/V max	10μV/V max
@ $T_{min} \leq T_A \leq T_{max}$	40μV/V	25μV/V max	15μV/V max
vs Time	20μV/mo	15μV/mo	10μV/mo
INPUT OFFSET CURRENT			
@ T_A = 25°C	40nA max	15nA max	10nA max
INPUT BIAS CURRENT			
Initial	200nA max	100nA max	80nA max
T_{min} to T_{max}	300nA max	150nA max	100nA max
vs Temp, T_{min} to T_{max}	300pA/°C	250pA/°C	200pA/°C
INPUT IMPEDANCE			
Differential	0.5MΩ	1.0MΩ	1.3MΩ
Common Mode	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.01 to 10Hz	1.0μV (p-p)	*	*
100Hz	10nV/√Hz(rms)	*	*
1kHz	8nV/√Hz(rms)	*	*
Current, 0.01 to 10Hz	50pA(p-p)	*	*
100Hz	0.6pA/√Hz(rms)	*	*
1kHz	0.5pA/√Hz(rms)	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, Max Safe	$\pm V_S$	*	*
Common Mode Rejection, V_{IN} = ±10V	94dB min (120dB typ)	100dB min (120dB typ)	110dB min (120dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
TEMPERATURE RANGE			
Operating, Rated Performance (T_{min} to T_{max})	0 to +70°C	*	*
Storage	−65°C to +150°C	*	*

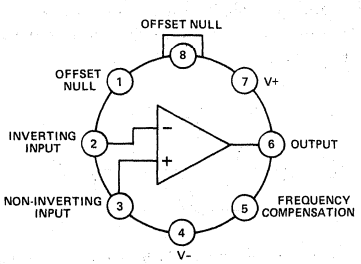
*Specifications same as for AD504J.
†This parameter is not 100% tested. Typically, 90% of the units meet this limit.
Specifications subject to change without notice.

NOTE
Analog Devices 100% tests and guarantees all specified maximum and minimum limits. Certain parameters, because of the relative difficulty and cost of 100% testing, have been specified as "typical" numbers. At ADI, "typical" numbers are subjected to rigid statistical sampling and outgoing quality control procedures, resulting in "typicals" that are indicative of the performance that can be expected by the user.

AD504M	AD504S(AD504S/883)
10^6 min (8 x 10^6 typ)	10^6 min (8 x 10^6 typ)
500,000 min (10^6 typ)	250,000 min
*	*
*	*
*	*
*	*
*	*
*	*
*	*
0.5mV max (0.2mV typ)	0.5mV max
0.5μV/°C max (0.2μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
1.0μV/°C max (0.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
10μV/V max	10μV/V max
15μV/V max	20μV/V max
10μV/mo	10μV/mo
10nA max	10nA max
80nA max	80nA max
100nA max	200nA max
200pA/°C	200pA/°C
1.3MΩ	1.3MΩ
*	*
0.6μV (p-p) max	*
10nV/$\sqrt{Hz}$ max	*
9nV/$\sqrt{Hz}$ max	*
1.3pA/$\sqrt{Hz}$ max	*
0.6pA/$\sqrt{Hz}$ max	*
0.3pA/$\sqrt{Hz}$ max	*
*	*
110dB min (120dB typ)	110dB min (120dB typ)
*	*
*	*
±3.0mA max (±1.5mA typ)	±3mA max (±1.5mA typ)
*	-55°C to +125°C
*	-65°C to +150°C

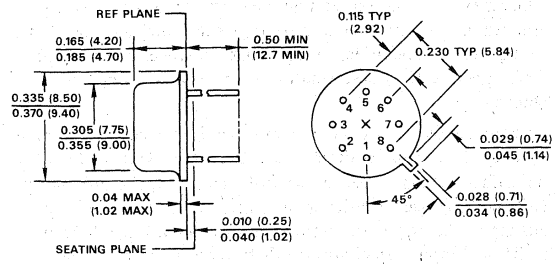
**AD504S/883 minimum order is 10 pieces.

TO-99 PIN CONFIGURATION

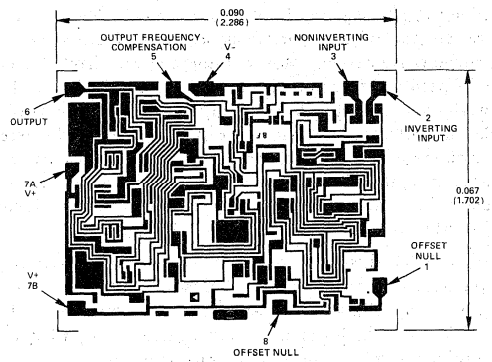


OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



BONDING DIAGRAM



The AD504 is also available in chip form. See the Analog Devices Chip Catalog for details.

MIL-STANDARD-883

The AD504S/883 has the same electrical specifications as the AD504S, but it is subjected to the 100% screening requirements specified in MIL-STD-883, Method 5004, Class B.

This procedure includes . . . . . .

(1) Pre-Cap Visual Inspection:
Method 2010, Condition B

(2) Stabilization Bake:
Method 1008, Condition C,
24 hours @ +150°C

(3) Temperature Cycle:
Method 1010, Condition C,
-65°C to +150°C, 10 cycles

(4) Constant Acceleration:
Method 2001, Condition E,
30,000 g, Y_1 orientation

(5) Hermeticity, Gross Leak:
Method 1014, Condition C,
Steps 1 and 2

(6) Hermeticity, Fine Leak:
Method 1014, Condition A,
5 x 10^{-8} atm/cc/sec

(7) Burn-In:
Method 1015, 160 hours @ +125°C

(8) Final Electrical Tests

(9) External Visual:
Method 2009

OFFSET VOLTAGE DRIFT AND NULLING

Most differential operational amplifiers have provisions for adjusting the initial offset voltage to zero with an external trim potentiometer. It is often not realized that there is a resulting increase in voltage drift which accompanies this initial offset adjustment. The increased voltage drift can often be safely ignored in conventional amplifiers, since it may be a small percentage of the specified voltage drift. However, the voltage drift of the AD504 is so small that this effect cannot be ignored.

To achieve low drift over temperature, it is necessary to maintain equal current densities in the input pair. Unless the initial offset nulling circuit is carefully arranged, the nulling circuits will themselves drift with temperature. The resulting change in the input transistor current *ratio* will produce an additional input offset voltage drift. This drift component can actually be larger than the unnulled drift.

Typically, IC op amps are nulled by using an external potentiometer to adjust the ratio of two resistances. These resistances are part of a network from which the input stage emitter currents are derived. Most commercially available op amps use diffused resistors in their internal nulling circuitry, which typically display large positive temperature coefficients of the order of 2000ppm/°C. As a result of the failure of the external potentiometer resistance to track the diffused resistors over temperature, the two resistance branches will drift relative to one another. This will cause a change in the emitter current ratio and induce an offset drift with temperature.

In the AD504, this problem is reduced an order of magnitude by the use of thin film resistors deposited on the monolithic amplifier chip. These resistors, which make up the critical bias network from which the input stage emitter current balance is determined, display typical temperature coefficients of less than 200ppm/°C, an order of magnitude improvement over diffused types. Thus, when the initial offset of the AD504 is trimmed using a low TC pot in combination with the thin film network, the drift induced by nulling even relatively large offsets is extremely small. This means that AD504 units of all three grades (J, K, L) will typically yield significantly better temperature performance in nulled applications than an all-diffused amplifier with comparable initial offset.

Since the intrinsic offset drift of the amplifier is improved by nulling, the direct measurement of any additional drift induced by differing temperature coefficients of resistors would be extremely difficult. However, the *induced* offset drift can be established by calculating the change in the emitter current ratio brought about by the differing TC's of resistances. From the change in this ratio, the offset voltage contribution at any temperature can be easily calculated.

A simple computer program was written to calculate induced offset drift as a function of initial offset voltage nulled. This calculation was made assuming zero TC of the amplifier resistors, and TC's of 200ppm/°C and 2000ppm/°C for the null pot. These results are very nearly equivalent to the case where the pot has zero temperature coefficient and the amplifier resistors drift. The results of these calculations are summarized graphically in Figure 1.

Figure 1 shows the variation of induced voltage drift with nulled offset voltage for:

a. AD504 op amp.
b. 725 typ op amp.

Note that as a result of nulling 1.4mV of offset, *the AD504 induces 30X less offset drift (only 0.05μV/°C) than the 725 type op amp* with its actual diffused resistor values and the recommended 100k pot to trim the offset. Actual induced drifts from this source for the AD504 may be even lower in the practical case when metal film resistors or pots are used for nulling, since their TC's tend to closely *match* the negative TC's of the thin film resistors on the AD504 chip.

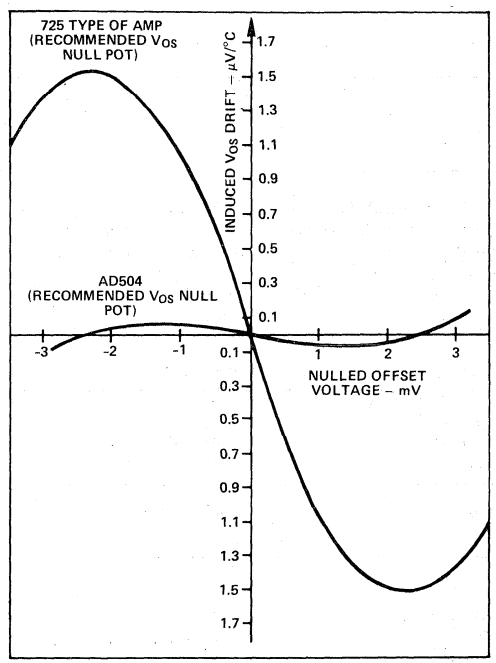


Figure 1. Induced Offset Drift vs. Nulled Offset Using Manufacturer's Recommended Adjustment Potentiometer

NULLING THE AD504

Since calculations show that superior drift performance can be realized with the AD504, special care should be taken to null it in the most advantageous manner. Using the actual values of resistors in the AD504, it is possible to calculate, under worst case conditions, that the total adjustment rage of the AD504 is approximately 8mV. Since the amplifier may often be trimmed to within 1μV, this represents an adjustment of 1 part in 8000. This type of accuracy would require a pot with 0.0125% resolution and stability. Because of the problems of obtaining a pot of this stability, a slightly more sophisticated nulling operation is recommended for applications where offset drift is critical (see Figure 2a).

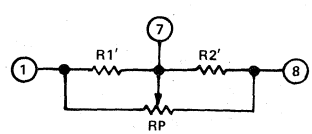


Figure 2a. High Resolution, High Stability Nulling Circuit

NULLING PROCEDURE

1. Null the offset to zero using a commercially available pot (suggest $R_P = 10k\Omega$).
2. Measure pot halves R1 and R2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}, \quad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Insert R1′ and R2′ (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (R_P) to fine tune the trim.

For applications in which stringent nulling is not required, the user may choose a simplified nulling scheme as shown in Figure 2b. For best results the wiper of the potentiometer should be connected directly to pin 7 of the op amp. This is true for both nulling schemes.

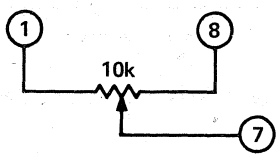


Figure 2b. Simplified Nulling Circuit

INPUT BIAS CURRENT

The input bias current vs. temperature characteristic is displayed in Figure 3.

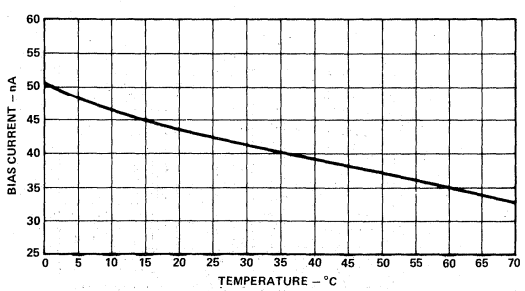


Figure 3. Input Bias Current vs. Temperature

GAIN PERFORMANCE

Most commercially available monolithic op amps have gain characteristics that vary considerably with:

1. Offset Nulling.
2. Load Resistance.
3. Supply Voltage.

Careful design allows the AD504 to maintain gain well in excess of 10^6, independent of nulling, load or supply voltage.

Nulling – The gain of a 741 op amp varies considerably with nulling (see Figure 4).

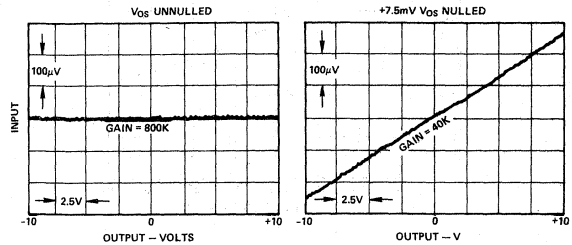


Figure 4. Gain Error Voltage Before and After Nulling a Typical 741 Op Amp

The gain of the AD504 is independent of nulling.

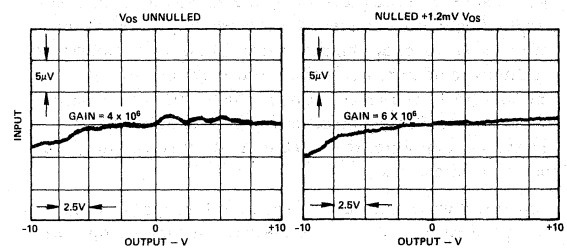


Figure 5. Gain Error Voltage Before and After Nulling the AD504

Load Resistance – The gain of the AD504 is flat with load resistance to 1kΩ loads and below.

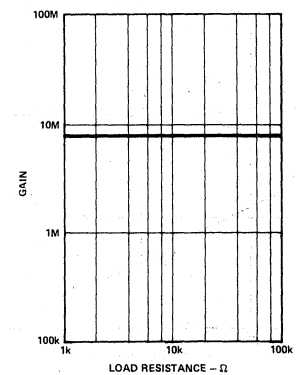


Figure 6. Gain vs. Load Resistance

Supply Voltage – The gain of the AD504 stays well above 1M down to $V_S = \pm 5V$.

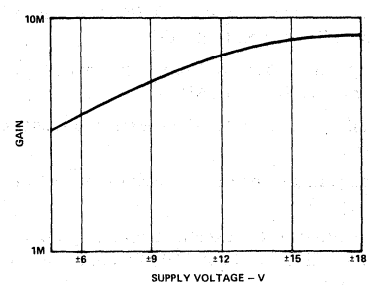


Figure 7. Gain vs. Supply Voltage

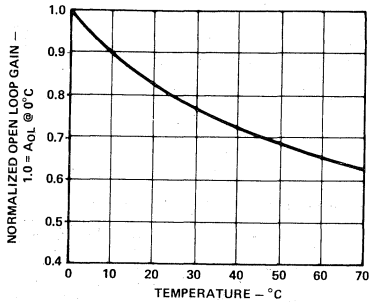


Figure 8. Normalized Open Loop Gain vs. Temperature

NOISE CHARACTERISTICS

An op amp with the precision of the AD504 must have correspondingly low noise levels if the user is to take advantage of its exceptional dc characteristics. Of primary importance in this type of amplifier is the absence of popcorn noise and minimum I/f or "flicker" noise in the 0.01Hz to 10Hz frequency band. Sample noise testing is done on every lot to guarantee that better than 90% of all devices will meet the noise specifications.

Separate voltage and current noise levels referred to the input are specified to enable the designer to calculate or optimize signal-to-noise ratio based on any desired source resistance. The spot noise figures are useful in determining total wideband noise over any desired bandwidth (see Figure 9).

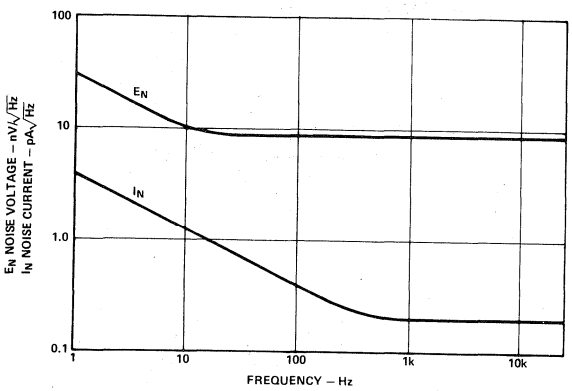


Figure 9. Spot Noise vs. Frequency

The key to success in using the AD504 in precision low noise applications is "attention to detail".

Here are a few reminders to help the user achieve optimum noise performance from the AD504.

1. Use metal film resistors in the source and feedback networks.
2. Use fixed resistors instead of potentiometers for nulling or gain setting.
3. Take advantage of the excellent common-mode noise rejection qualities of the AD504 by connecting the input differentially.
4. Limit the bandwidth of the system to the minimum possible consistent with the desired response time.
5. Use input guarding to reduce capacitive and leakage noise pickup.
6. Avoid ground loops and proximity to strong magnetic or electro-static fields, etc.

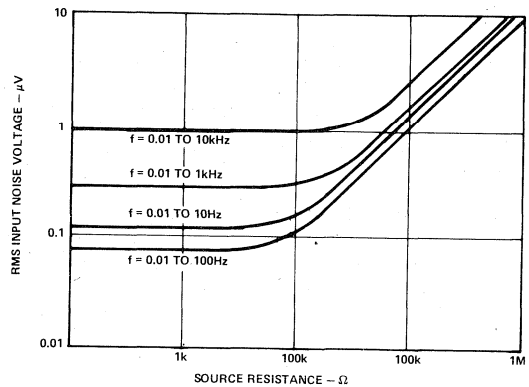


Figure 10. RMS Noise vs. Source Resistance

DYNAMIC PERFORMANCE

The dynamic performance of the AD504, although comparable to most general purpose op amps, is superior to most low drift op amps. Figure 11 shows the small signal frequency response for both open and closed loop gains for a variety of compensating values. Note that the circuit is completely stable for C_C = 390pF with a -3dB bandwidth of 300kHz; with C_C = 0, the -3dB bandwidth is 50kHz at a gain of 2000.

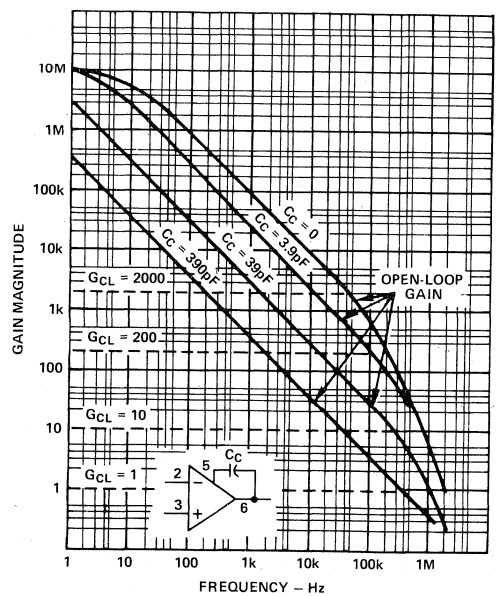


Figure 11. Small Signal Gain vs. Frequency

More important, at unity gain (390pF), full power bandwidth is (Figure 12) 2kHz which corresponds to a 0.12V/μs slew rate. At a gain of 10 (39pF), it increases to 20kHz, corresponding to 1.2V/μs, a considerable improvement over "725 type" amplifiers.

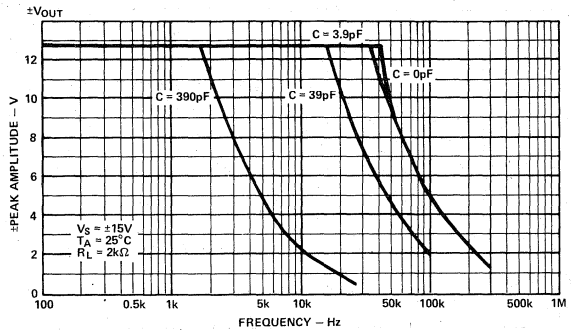


Figure 12. Output Voltage Swing vs. Frequency

Figure 13 shows the voltage follower step response for $V_S = \pm 15V$, $R_L = 2k\Omega$, $C_L = 200pF$ and $C_C = 390pF$.

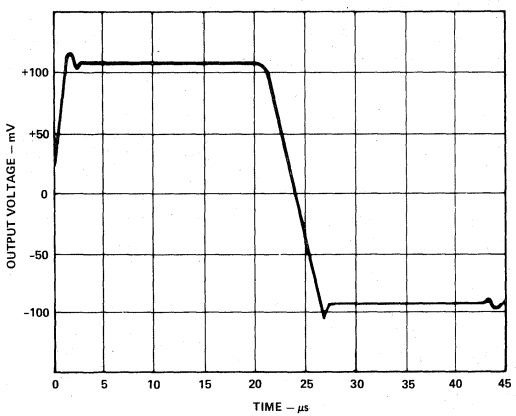


Figure 13. Voltage Follower Step Response

The common mode rejection of the AD504 is typically 120dB, and is shown as a function of frequency in Figure 14.

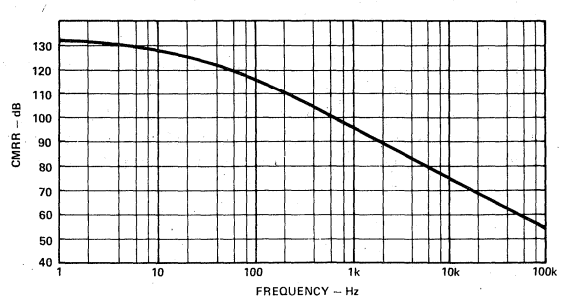


Figure 14. CMRR vs. Frequency

The power supply rejection ratio of the AD504 is shown in Figure 15.

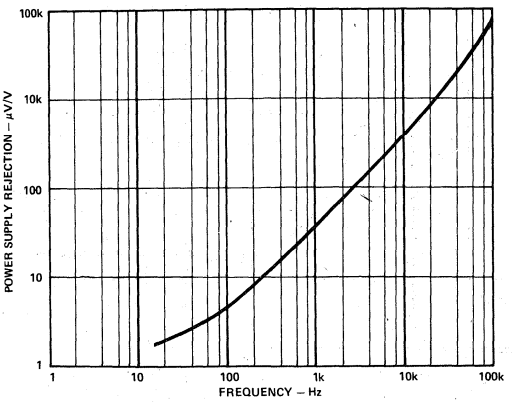


Figure 15. PSRR vs. Frequency

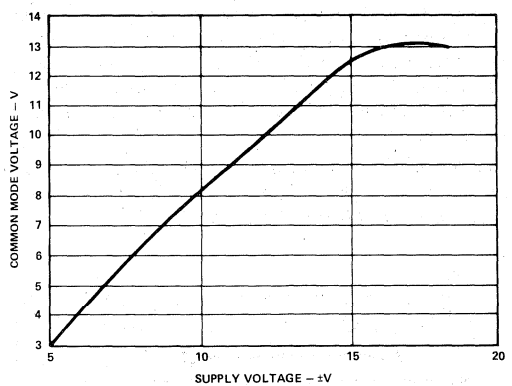


Figure 16. CMV Range vs. Supply Voltage

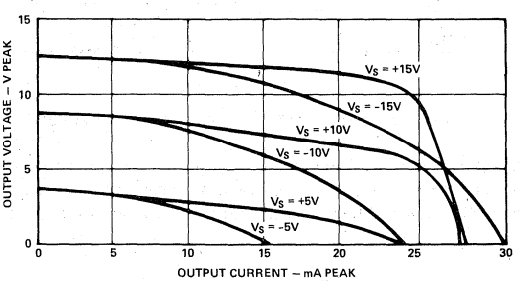


Figure 17. Output Characteristics

THERMAL PERFORMANCE

Temperature Gradients

Most modular and hybrid operational amplifiers are extremely sensitive to thermal gradients. The transient offset voltage response to thermal shock for a high performance modular op amp is shown in Figure 18.

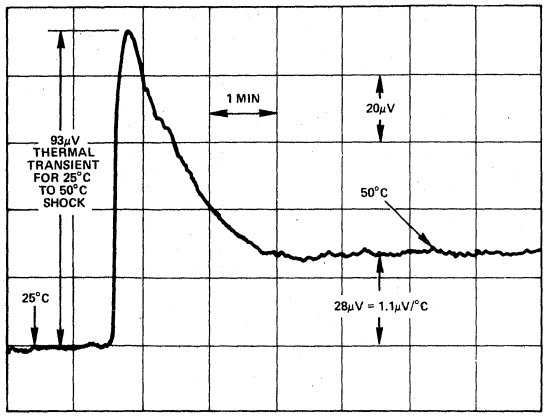


Figure 18. Response to Thermal Shock for High Performance Modular Op Amp

The graph shows the transient offset voltage resulting from a thermal shock when the amplifier's temperature is abruptly changed from 25°C to 50°C by dipping it into a hot silicon oil bath. Note the large overshoot (approximately 60μV) and long settling time (2.5 minutes). Also note the hysteresis of about 30μV.

Monolithic technology affords the AD504 significant improvements in this area. Thermal transients in the AD504 are small and over with quickly (see Figure 19).

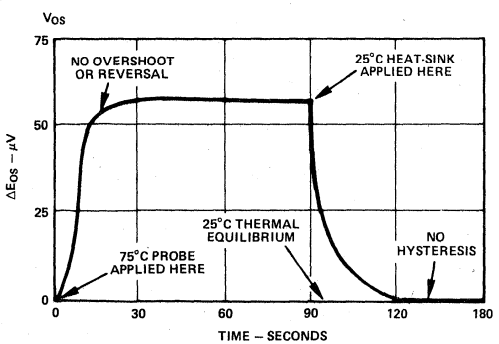


Figure 19. Response to Thermal Shock for AD504

In Figure 19, a 50°C step change in ambient temperature, applied to the can via a room temperature heat sink, then a 75°C thermal probe and back to the heat sink, results in settling to the final value within 30 seconds, for both increases and decreases in temperature. Note that the offset goes directly to its final value, with no spikes or hysteresis.

Warmup Drift

Modular and hybrid op amps have historically been plagued by excessive thermal time constants. Figure 20 shows the typical warmup drift of a high performance modular op amp.

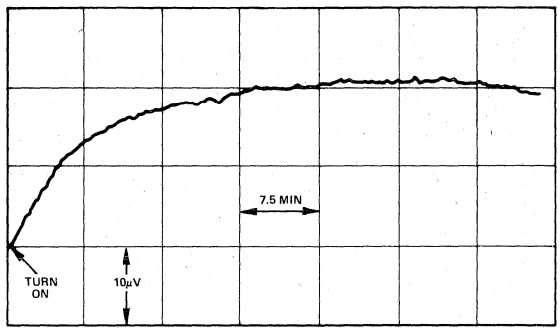


Figure 20. Warmup Voltage Drift for High Performance Modular Op Amp

Note that although warmup drift is low (20μV), it requires a long time to settle (>20 minutes).

Monolithic technology results in significant reduction of thermal time constants (see Figure 21).

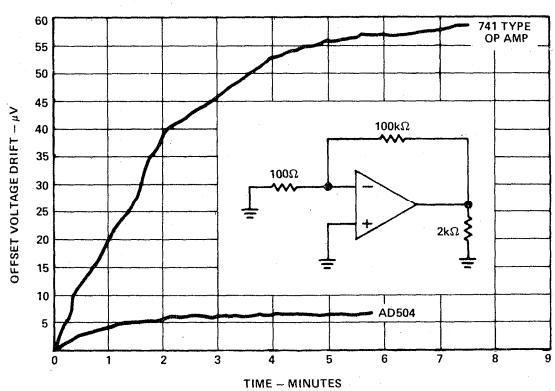


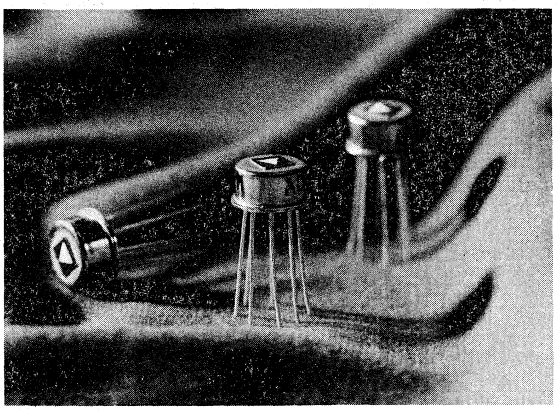
Figure 21. Warmup Voltage Drift for AD504 and 741 Type Op Amp

Note that warmup drift remains low (10μV), but that the thermal time constant decreases significantly to about 2 minutes. If a heat sink were used, total settling time would be completed within 30 seconds. Note that the 741 type op amp has a significantly longer warmup drift and thermal time constant.

IC, Wideband, Fast Slewing, General Purpose Operational Amplifier

AD507

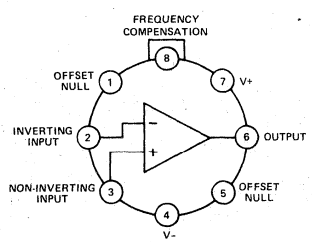
FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive



PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the full military temperature range, −55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.



TO-99 PIN CONFIGURATION

PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.
5. To take full advantage of the inherent high reliability of IC's, every AD507S receives a 24 hour stabilization bake at +150°C.

MIL-STANDARD-883

The AD507S/883 has the same electrical specifications as the AD507S, but is subjected to the 100% screening requirements specified in MIL-STD-883, Method 5004, Class B.

This procedure includes:

1. Pre-Cap Visual Inspection: Method 2010, Condition B.
2. Stabilization Bake: Method 1008, Condition C, 24 hours @ +150°C.
3. Temperature Cycle: Method 1010, Condition C, -65°C to +150°C, 10 cycles.
4. Centrifuge: Method 2001, Condition E, 30,000 g, Y_1 orientation.
5. Hermeticity, Gross Leak: Method 1014, Condition C, steps 1 and 2.
6. Hermeticity, Fine Leak: Method 1014, Condition A, 5×10^{-8} atm/cc/sec.
7. Burn-In: Method 1015, 160 hours @ +125°C.
8. Final Electrical Test.
9. External Visual: Method 2009.

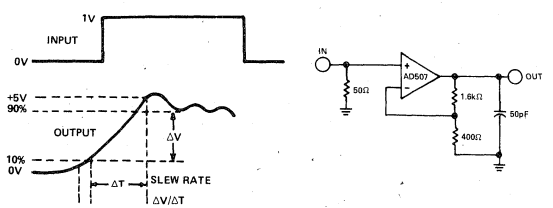
SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S(AD507S/883)**
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T min to T max	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	12nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Operating	−25°C to +85°C	*	−65°C to +150°C
Storage	−65°C to +150°C	*	*

*Specifications same as AD507J.

**AD507S/883 minimum order 10 pieces.

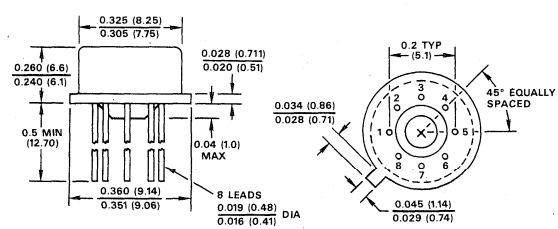
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

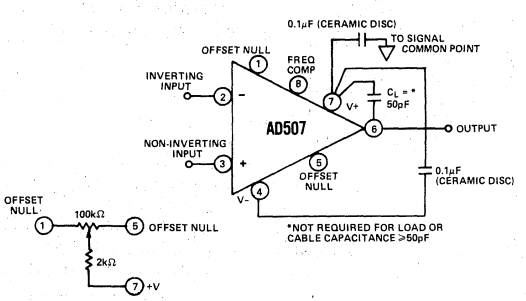


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

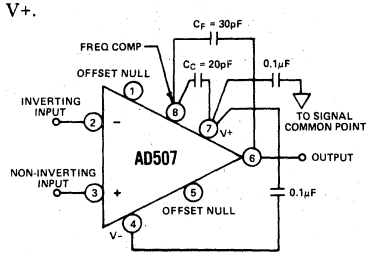


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

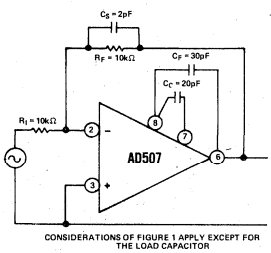
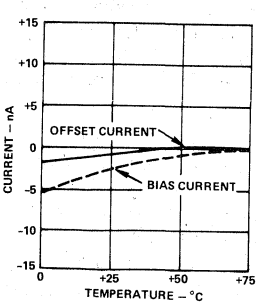
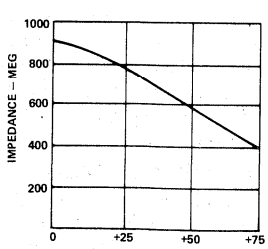


Figure 3. Fast Settling Time Configuration

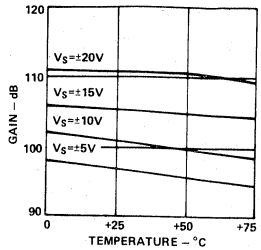
TYPICAL PERFORMANCE CURVES



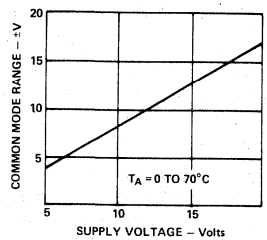
Input Bias Current and Offset Current vs Temperature



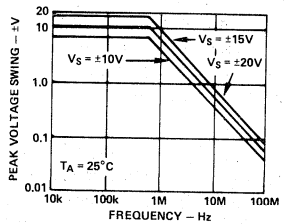
Input Impedance vs Temperature



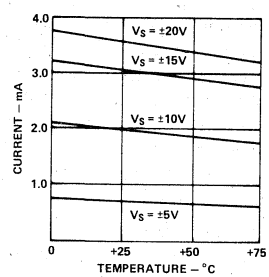
Open Loop Voltage Gain vs Temperature



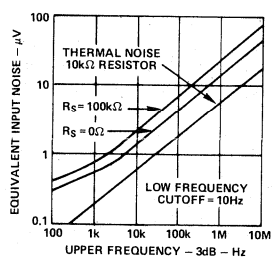
Common Mode Voltage Range vs Supply Voltage



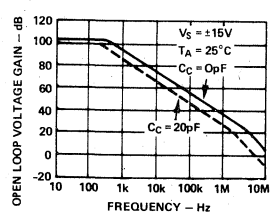
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

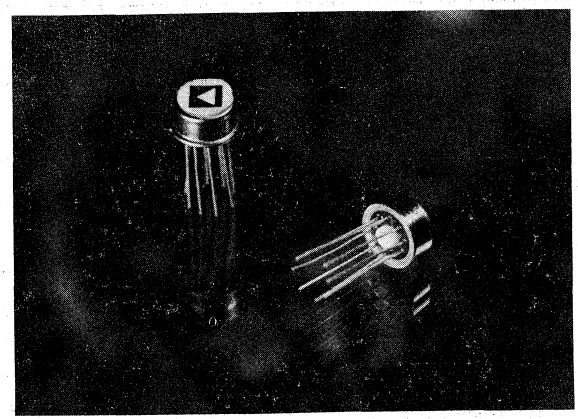
AD509

FEATURES

Fast Settling Time (100% Tested)
0.1% in 500ns max
0.01% in 2.5μs max
High Slew Rate: 100V/μs min
Low I_{OS}: 25nA max
Guaranteed V_{OS} Drift: 30μV/°C max
High CMRR: 80dB min
Drives 500pF
Low Price

APPLICATIONS

D/A and A/D Conversion
Wideband Amplifiers
Multiplexers
Pulse Amplifiers



PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. The AD509K and AD509S are 100% tested and guaranteed to settle to 0.1% in 500ns max and 0.01% in 2.5μs max, with typical performance that is twice as fast. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD509K and AD509S are 100% tested and guaranteed to settle to 0.01% of its final value in less than 2.5μs.
2. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains; thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
3. The AD509 will drive capacitive loads of 500pF without any deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
4. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

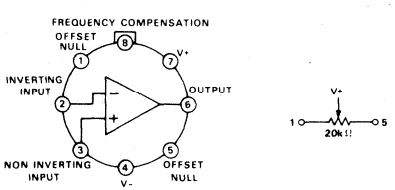
MODEL	AD509J	AD509K	AD509S
OPEN LOOP GAIN			
R_L = 2kΩ	7,500 min (15,000 typ)	10,000 min (15,000 typ)	**
@ T_A = min to max	5,000 min	7,500 min	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	20MHz	*	*
Full Power Response, V_O = ±10V	120kHz min (1.6MHz typ)	150kHz min (2.0MHz typ)	**
Slew Rate, R_L = 2kΩ, V_o = ±10V, C_L = 50pF	80V/μs min (120V/μs typ)	*	100V/μs min (120V/μs typ)
Settling Time			
to 0.1%	200ns	500ns max (200ns typ)	**
to 0.01%	1.0μs	2.5μs max (1.0μs typ)	**
INPUT OFFSET VOLTAGE			
Initial	10mV max (5mV typ)	8mV max (4mV typ)	**
T_A = min to max	14mV max	11mV max	**
Avg vs. Temperature, T_A = min to max	20μV/°C	30μV/°C max (20μV/°C typ)	**
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**
INPUT BIAS CURRENT			
Initial	250nA max (125nA typ)	200nA max (100nA typ)	**
T_A = min to max	500nA max	400nA max	**
INPUT OFFSET CURRENT			
Initial	50nA max (20nA typ)	25nA max (10nA typ)	**
T_A = min to max	100nA max	50nA max	**
INPUT IMPEDANCE			
Differential	40MΩ min (100MΩ typ)	50MΩ min (100MΩ typ)	**
INPUT VOLTAGE RANGE			
Differential, max safe	±15V	*	*
Common Mode Voltage Range			
T_A = min to max	±10V	*	*
Common Mode Rejection, V_{cm} = ±5V			
T_A = min to max	74dB min (90dB typ)	80dB min (90dB typ)	**
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	19nV/√Hz	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	6mA max (4mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*

*Specification same as AD509J.
**Specification same as AD509K.
Specifications and prices subject to change without notice.

PIN CONFIGURATION & PHYSICAL DIMENSIONS

Dimensions shown in inches and (mm).

TO-99



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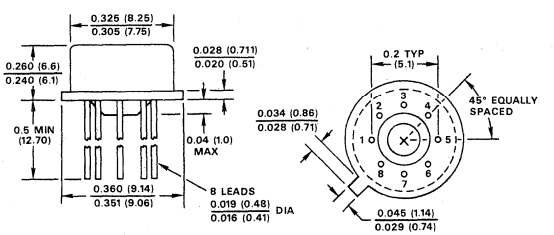


APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

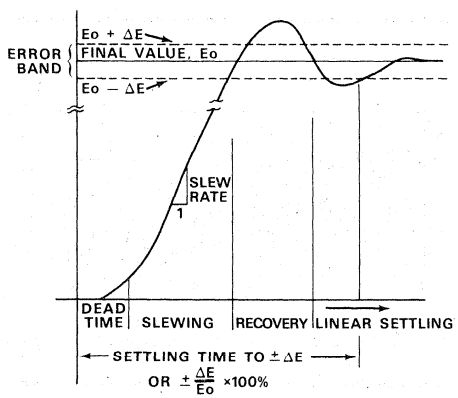


Figure 1. Settling Time

The AD509K and AD509S are 100% tested and guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs (see Test Circuit, Figure 2). Note that the devices are tested compensated, at a gain of one, with a 50pF capacitive load. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope

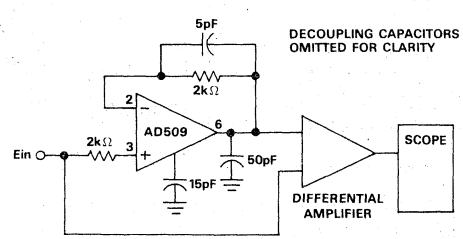


Figure 2. AD509 Settling Time Test Circuit

display. The resultant waveform of ($E_O - E_{in}$) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

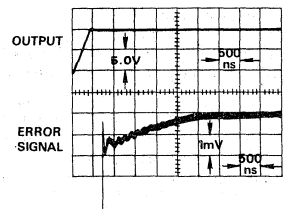


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

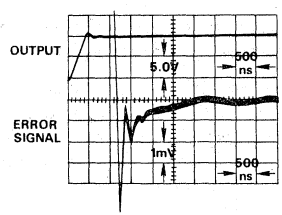


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are.....

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

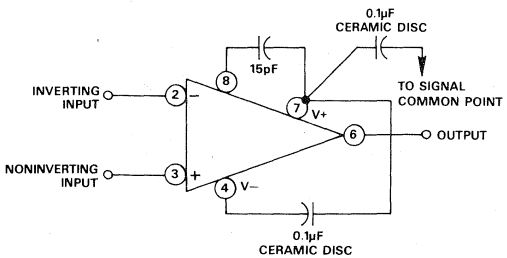


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

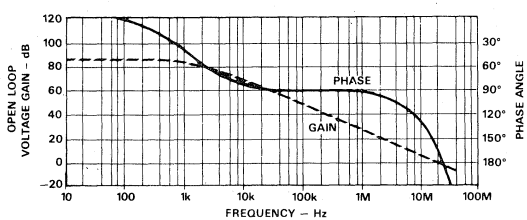


Figure 6. Open Loop Frequency and Phase Response

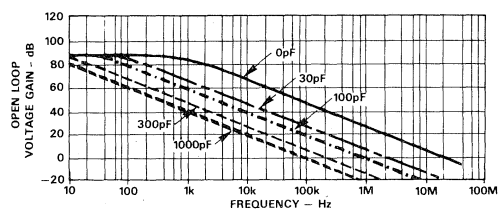


Figure 7. Open Loop Frequency Response for Various C_C's

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST CURRENT-OUTPUT D-TO-A CONVERTERS

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-to-voltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_s \text{ TOTAL} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to ±0.1% or ±0.01% of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

Figure 8 shows the AD509K connected as an output amplifier with the AD565K, high speed 12-bit IC digital-to-analog converter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.

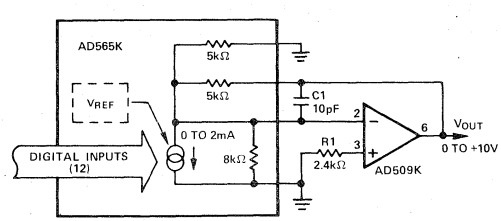


Figure 8. AD507 as an Output Amplifier for a Fast Current-Output D-to-A Converter

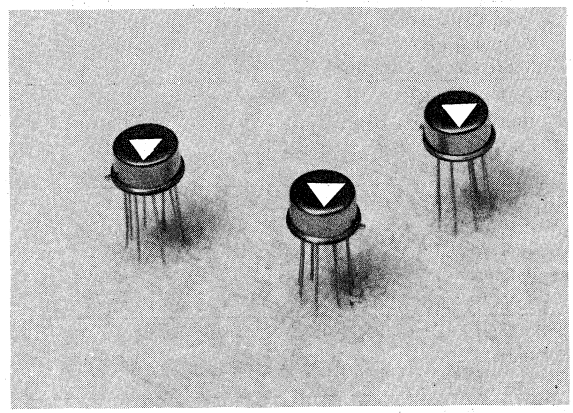
ANALOG DEVICES

Low Cost, Laser Trimmed, Precision IC Op Amp

AD510

FEATURES

Low Cost
Low V_{OS}: 25μV max (AD510L), 100μV max (AD510J)
Low V_{OS} Drift: 0.5μV/°C max (AD510L)
Internally Compensated
High Open Loop Gain: 10^6 min
Low Noise: 1μV p-p 0.01 to 10Hz



PRODUCT DESCRIPTION

The AD510 is the first low cost high accuracy IC op amp available. Analog Devices' precise thermally-balanced layout combined with high-yield IC processing provides truly superlative op amp performance at the lowest possible cost. The device is internally compensated, thus eliminating the need for an additional external capacitor.

A truly precision device, the AD510 achieves laser trimmed offset voltages less than 25μV max and offset voltage drifts of 0.5μV/°C max (nulled). Bias currents and offset currents are available at less than 10nA and 2.5nA respectively, while open loop gain is maintained at over 1,000,000, even under loaded conditions. Designed along a thermal axis, the AD510 is unaffected by thermal gradients across the monolithic chip caused by current loading.

The AD510 has fully protected inputs, permitting differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits and drives 1000pF of load capacitance without oscillation.

The AD510 is specifically designed for applications requiring high precision at the lowest possible cost, such as bridge instruments, stable references, followers and analog computation. Packaged in a hermetically-sealed TO-99 metal can, the AD510 is available in three versions of performance (J, K and L) over the commercial temperature range, 0 to +70°C and one version (S) over the full military temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

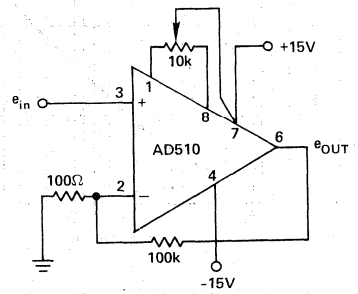
1. Offset voltage drift is guaranteed and 100% tested on all models with a controlled temperature drift bath with the offset voltage nulled. Offset voltage on the AD510L is tested following a 3 minute warm-up.
2. The AD510 offers fully protected input (to $\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, a critical factor in high accuracy op amps where overall performance is strongly dependent on front-end stability.
3. Internal compensation eliminates the need for elaborate and costly stabilizing networks, often required by many high accuracy IC op amps.
4. A thermally balanced layout maintains high gain (1,000,000 min, K, L and S) independent of offset nulling, power supply voltage and output loading.
5. Bootstrapping of critical input transistors produces CMRR and PSRR of 110dB min and 100dB min, respectively.
6. Every AD510 receives a 24 hour stabilization bake at 150°C and a 48 hour burn-in at 125°C to ensure reliability and long term stability.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD510J	AD510K	AD510L	AD510S
OPEN LOOP GAIN				
V_{OS} = ±10V, R_L > 2kΩ	250,000 min	10^6 min	**	**
T_{min} to T_{max}	125,000 min	500,000 min	**	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	300kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leq 10k\Omega$	100μV max	50μV max	25μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.0μV/°C max	0.5μV/°C	**
vs. Supply	25μV/V max	10μV/V max	**	**
T_{min} to T_{max}	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	5nA max	4nA max	2.5nA max	**
T_{min} to T_{max}	8nA max	6nA max	4nA max	10nA max
INPUT BIAS CURRENT				
Initial	25nA max	13nA max	10nA max	**
T_{min} to T_{max}	40nA max	20nA max	15nA max	30nA max
vs. Temp, T_{min} to T_{max}	±100pA/°C	±50pA/°C	±40pA/°C	**
INPUT IMPEDANCE				
Differential	4MΩ	6MΩ	**	**
Common Mode	100MΩ‖4pF	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	1μV p-p	*	*	*
f = 10Hz	$18nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$13nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$10nV/\sqrt{Hz}$	*	*	*
Current, f = 10Hz	$0.5pA/\sqrt{Hz}$	*	*	*
f = 100Hz	$0.3pA/\sqrt{Hz}$	*	*	*
f = 1kHz	$0.3pA/\sqrt{Hz}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

NOTES:
*Specifications same as AD510J
**Specifications same as AD510K
Specifications subject to change without notice.

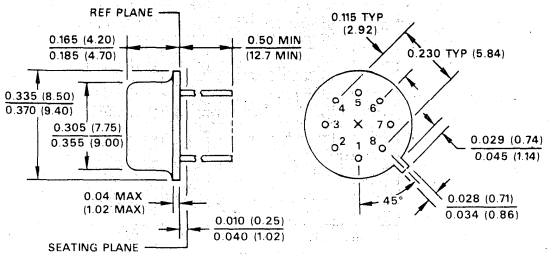
TYPICAL NON-INVERTING AMPLIFIER CONFIGURATION



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

TO–99



NULLING THE AD510

Nulling the AD510 can be achieved using the high resolution circuit of Figure 1.

1. Null the offset to zero using a commercially available pot (approximately 10kΩ).
2. Measure pot halves, R_1 and R_2.
3. Calculate . . . $R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}$ $R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$
4. Insert R_1' and R_2' (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (r_p) to fine tune the trim.

Nulling to within 1 microvolt can be achieved using this technique. For best results, the wiper of the potentiometer should be connected directly to pin 7 of the op amp.

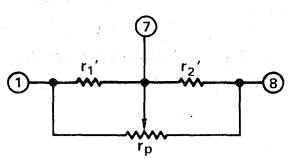


Figure 1. High Resolution, High Stability Nulling Circuit

THE AD510L IN A SIMPLE INSTRUMENTATION AMPLIFIER

The circuit of Figure 2 illustrates a simple instrumentation amplifier suitable for use with strain gauges, thermocouples and other transducers. It provides high input impedance to ground at each of the differential input terminals and excellent common mode rejection.

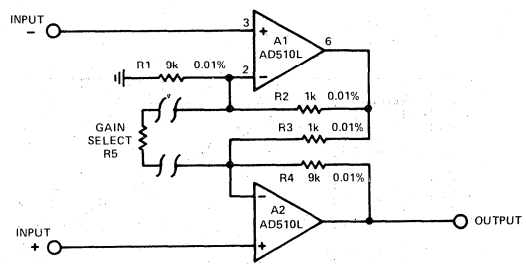


Figure 2. Instrumentation Amplifier

The configuration shown is designed for a gain of 10, however the gain can be varied upwards by adding a gain select resistor R_5. In operation, amplifier A_1 provides a gain of 10/9 for signals at the negative input terminal. This output feeds the inverting amplifier A_2, which has a gain of 9, resulting in an overall gain of 10. For signals at the positive input, the output of A_1 is at ground potential and the amplifier A_2 provides a gain of 10. Thus, the circuit has a gain of 10 for differential signals and 0 for common mode signals; the very high CMRR and open loop gain of the AD510L automatically produces common mode rejection of at least 25,000 at dc at a gain of 10 and over 1,000,000 at a gain of 1000. The common mode rejection, of course, depends upon the resistor ratios and their specified tolerance. Less accurate resistors can be used if the network is trimmed.

For gains of 10 the frequency response is down 3dB at 500kHz, for gains of 1000, 2kHz. Full output of ±10V can be attained up to 1800Hz.

The common mode rejection at 60Hz is limited by the finite gain bandwidth of A_1 causing a phase lag on the negative input signal. At 60Hz the CMRR measures 72dB at a gain of 1000 and 62dB at a gain of 10.

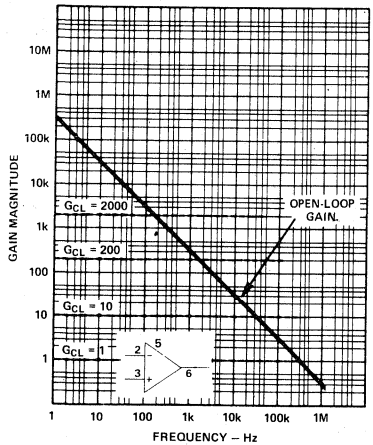


Figure 3. Small Signal Gain vs. Frequency

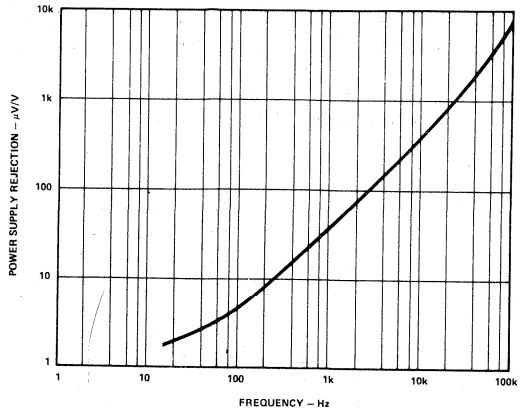


Figure 4. PSRR vs. Frequency

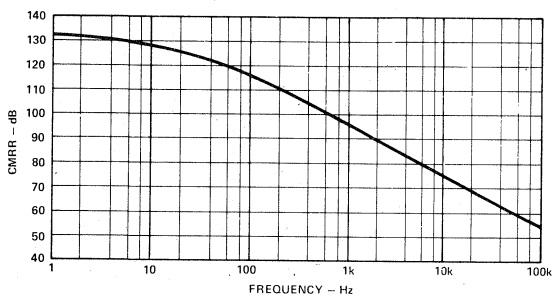


Figure 5. CMRR vs. Frequency

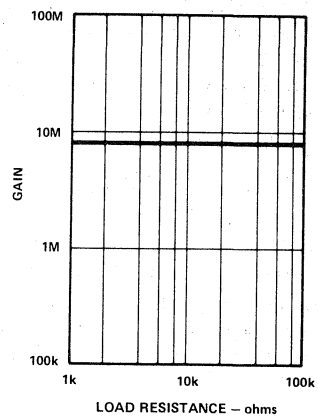


Figure 6. Gain vs. Load Resistance

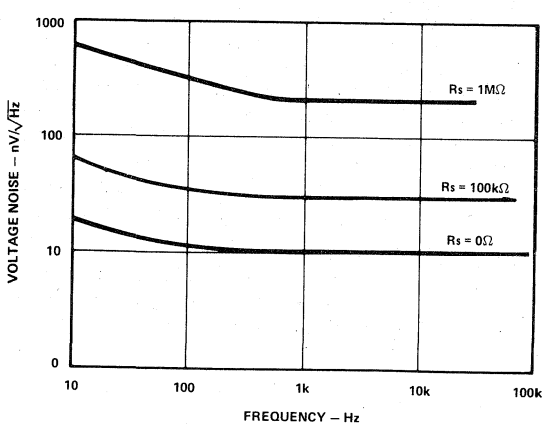


Figure 7. Voltage Noise vs. Frequency

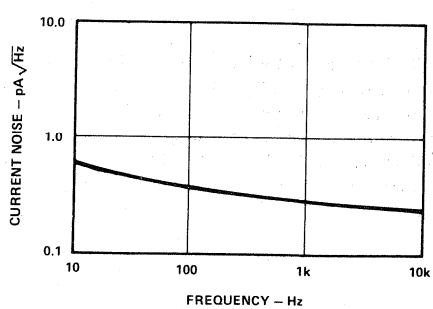


Figure 8. Current Noise vs. Frequency

ANALOG DEVICES

Precision, Low-Power FET-Input Electrometer Op Amp

AD515

FEATURES

Ultra Low Bias Current: 0.075pA max (AD515L)
0.150pA max (AD515K)
0.300pA max (AD515J)

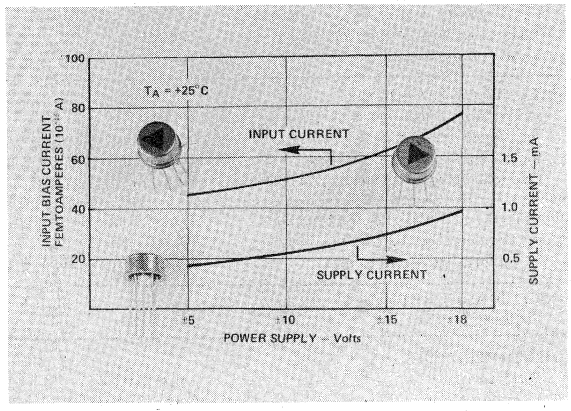
Low Power: 1.5mA max Quiescent Current (0.8mA typ)

Low Offset Voltage: 1.0mV max (AD515 K & L)

Low Drift: 15μV/°C max (AD515K)

Low Noise: 4μV p-p, 0.1 to 10Hz

Low Cost



PRODUCT DESCRIPTION

The AD515 series of FET-input operational amplifiers are second generation electrometer designs offering the lowest input bias currents available in any standard operational amplifier. The AD515 also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultra-low bias current circuits. All devices are internally compensated, free of latch-up, and short circuit protected.

The AD515 delivers a new level of versatility and precision to a wide variety of electrometer and very high impedance buffer measurement situations, including photo-current detection, vacuum ion-gauge measurement, long term precision integration, and low drift sample/hold applications. The device is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515 with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The 10^{15} ohm common mode input impedance, resulting from a solid bootstrap input stage, insures that the input bias current is essentially independent of common mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD515 is available in three versions of bias current and offset voltage, the "J", "K", and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The AD515 provides the lowest bias currents available in an integrated circuit amplifier.
   - The ultra low input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15 volt supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±5 volt supplies, input bias current can typically be brought below 50fA.
2. The input offset voltage on all grades is laser trimmed to a level typically less than 500μV.
   - The offset voltage drift is the lowest available in an FET electrometer amplifier.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per millivolt).
3. The low quiescent current drain of 0.8mA typical and 1.5mA maximum, which is among the lowest available in operational amplifier designs of any type, keeps self-heating effects to a minimum and renders the AD515 suitable for a wide range of remote probe situations.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one Megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristic.
5. Every AD515 receives a 24 hour stabilization bake at +150°C, to ensure reliability and long term stability.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

MODEL	AD515J	AD515K	AD515L
OPEN LOOP GAIN (Note 1)			
V_{out} = ± 10V, $R_L \geq 2k\Omega$	20,000V/V min	40,000V/V min	25,000V/V min
$R_L \geq 10k\Omega$	40,000V/V min	100,000V/V min	50,000V/V min
T_A = min to max $R_L \geq 2k\Omega$	15,000V/V min	40,000V/V min	25,000V/V min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*
Load Capacitance (Note 2)	1000pF	*	*
Short Circuit Current	10mA min (25mA typ)	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	350kHz	*	*
Full Power Response	5kHz min (16kHz typ)	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (1.0V/μs typ)	*	*
Overload Recovery Inverting Unity Gain	100μs max (16μs typ)	*	*
INPUT OFFSET VOLTAGE (Note 3)	3.0mV max (0.4mV typ)	1.0mV max (0.4mV typ)	1.0mV max (0.4mV typ)
vs. Temperature, T_A = min to max	50μV/°C max	15μV/°C max	25μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	100μV/V max	200μV/V max
INPUT BIAS CURRENT			
Either Input (Note 4)	300fA max	150fA max	75fA max
INPUT IMPEDANCE			
Differential	$1.6pF \| 10^{13}\Omega$	*	*
Common Mode	$0.8pF \| 10^{15}\Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	4.0μV (p-p)	*	*
f = 10Hz	$75nV/\sqrt{Hz}$	*	*
f = 100Hz	$55nV/\sqrt{Hz}$	*	*
f = 1kHz	$50nV/\sqrt{Hz}$	*	*
Current, 0.1 to 10Hz	0.003pA (p-p)	*	*
10Hz to 10kHz	0.01pA rms	*	*
INPUT VOLTAGE RANGE			
Differential	±20V min	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	66dB min (94dB typ)	80dB min	70dB min
Maximum Safe Input Voltage (Note 5)	$\pm V_S$	*	*
POWER SUPPLY			
Rated Performance	±15V typ	*	*
Operating	±5V min (±18V max)	*	*
Quiescent Current	1.5mA max (0.8mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	*
Storage	−65°C to +150°C	*	*

*Specifications same as AD515J.

NOTES:

1. Open Loop Gain is specified with or without nulling of V_{OS}.
2. A conservative design would not exceed 750pF of load capacitance.
3. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
4. Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
5. If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage. See next page.

Specifications subject to change without notice.

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515 can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultra-low input currents of the AD515. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pick-up and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515 is brought out separately to pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

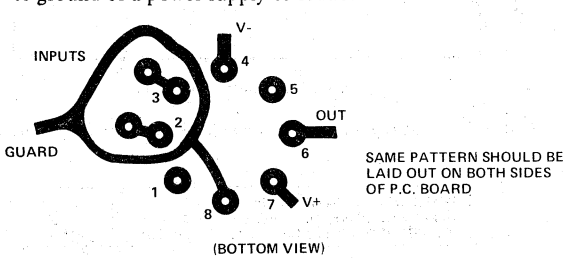


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515 can deliver. The best performance will be realized by using a teflon IC socket for the AD515; but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

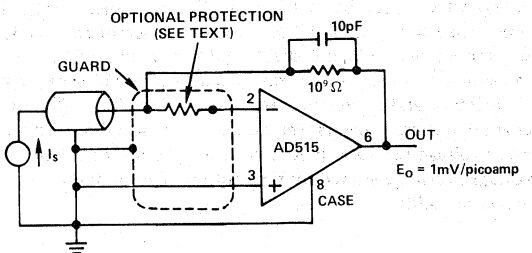


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

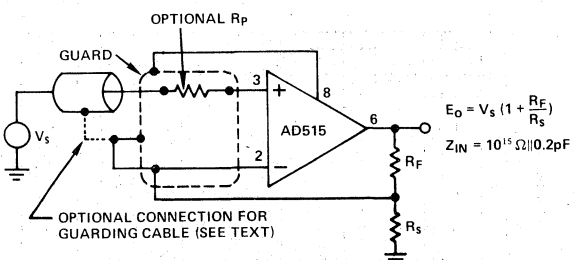


Figure 3. Very High Impedance Non-Inverting Amplifier

INPUT PROTECTION

The AD515 is guaranteed for a maximum safe input potential equal to the power supply potential. The unique bootstrapped input stage design also allows differential input voltages of up to ±20 volts (or within 10 volts of the sum of the supplies) while maintaining the full differential input resistance of $10^{13}\Omega$, as shown in Figure 10. This makes the AD515 suitable for low speed comparator situations employing a direct connection to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD515 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.5mA (for example, 200kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515 virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise, and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration-free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant such as Amphenol 21-537 will reduce the noise, but short rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other objects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is normally about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will de-stabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Non-inverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may destabilize and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

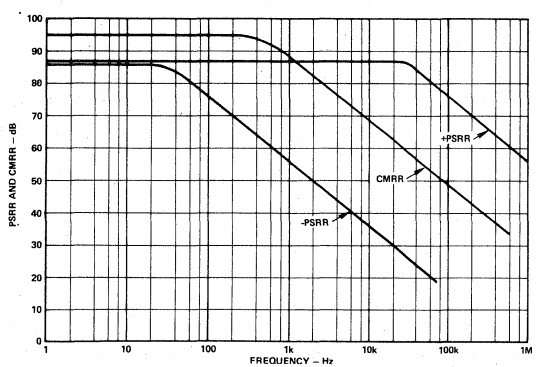


Figure 4. PSRR and CMRR Versus Frequency

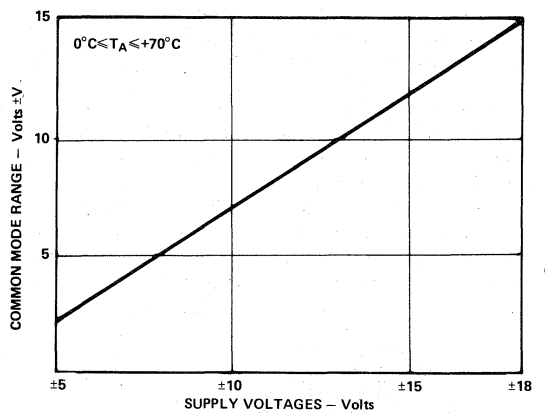


Figure 6. Input Common Mode Range Versus Supply Voltage

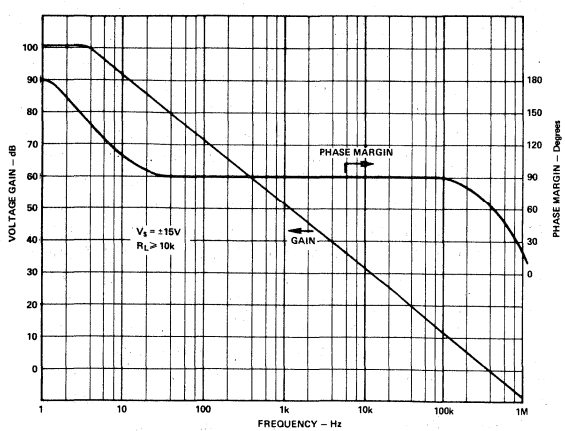


Figure 5. Open Loop Frequency Response

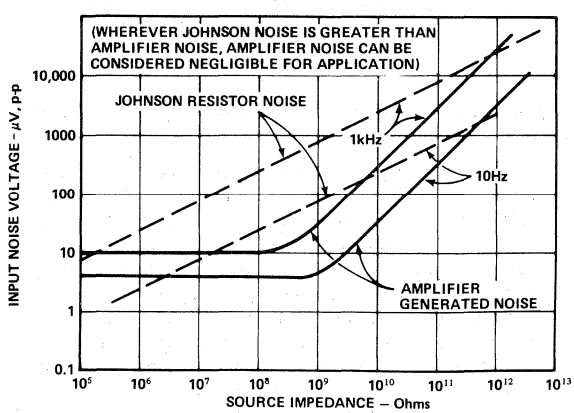


Figure 7. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515 offers the lowest input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515 and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515 has been reduced to a level much lower than that of any other electrometer-grade device, but additional performance improvement can be gained by lowering the supply voltages, to ±5 volts if possible. The effects of this are shown in Figure 8, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many dc performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load impedance to be at least 10kΩ.

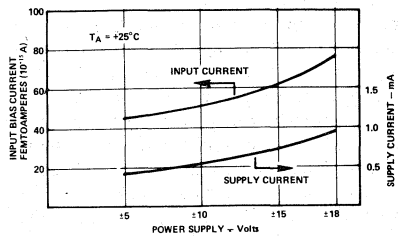


Figure 8. Input Bias Current and Supply Current Versus Supply Voltage

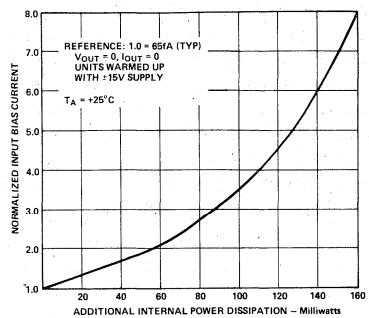


Figure 9. Input Bias Current Versus Additional Power Dissipation

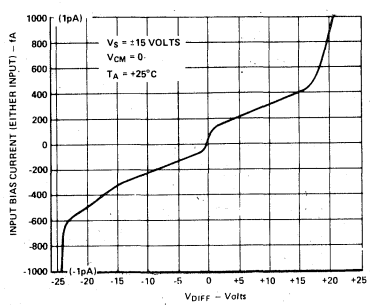
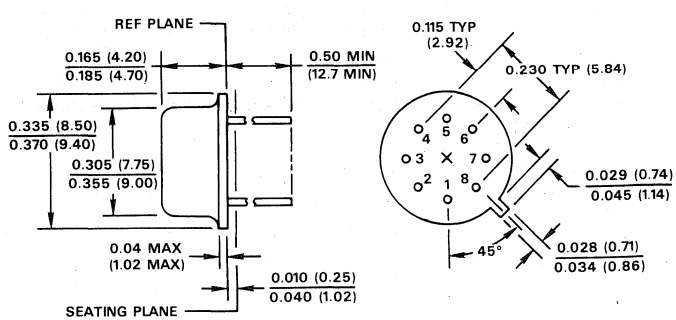


Figure 10. Input Bias Current Versus Differential Input Voltage

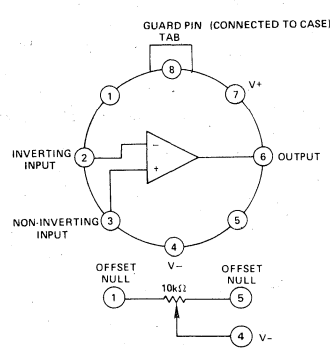
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



TOP VIEW

AD515 CIRCUIT APPLICATION NOTES

The AD515 is quite simple to apply to a wide variety of applications because of the pre-trimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High-megohm resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high-megohm resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515 is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515 are significant only above $10^{11}\Omega$.

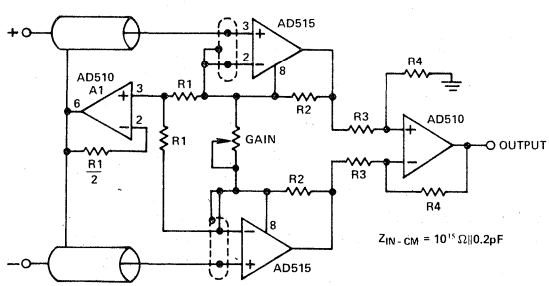


Figure 11. Very High Impedance Instrumentation Amplifier

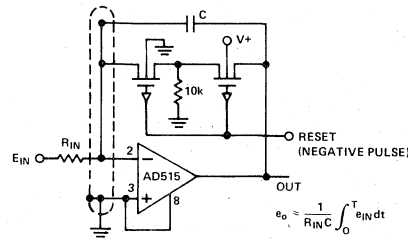


Figure 12. Low Drift Integrator and Low-Leakage Guarded Reset

LOW-LEVEL CURRENT TO VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515 makes the tradeoff easier.

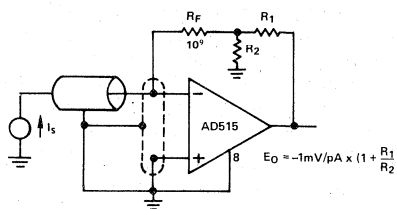


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the non-inverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD521 instrumentation amplifier converts the floating differential signal to a single-ended output.

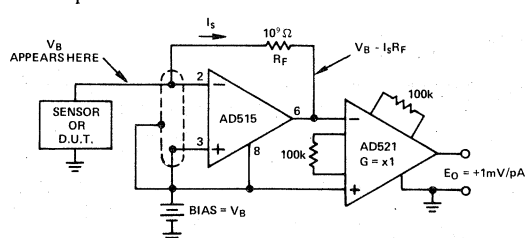


Figure 14. Current-to-Voltage Converters with Grounded Bias and Sensor

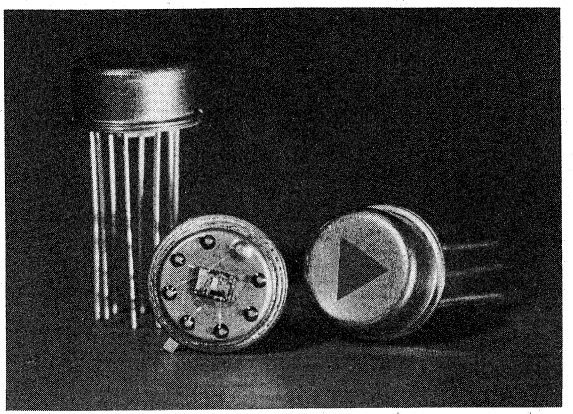
ANALOG DEVICES

Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

Low Input Bias Current: 1nA max (AD517L)
Low Input Offset Current: 0.25nA max (AD517L)
Low V_{OS}: 50μV max (AD517L), 150μV max (AD517J)
Low V_{OS} Drift: 1.3μV/°C (AD517L)
Internal Compensation
Low Cost



PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 50μV and offset voltage drifts less than 1.3μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the full military temperature range, -55°C to +125°C. The AD517S is also available with full processing to the requirements of MIL-STD-883, Level B.

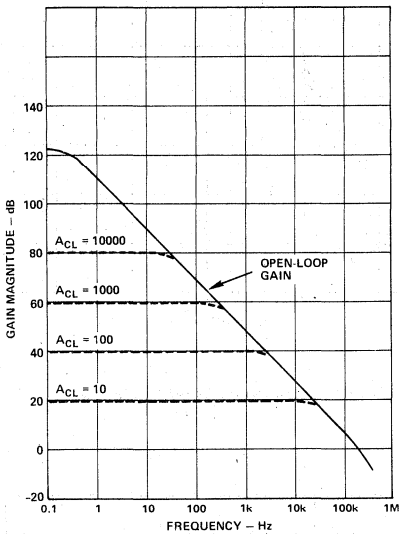
PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models. Testing is performed following a 5 minute warm-up period.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.
7. Every AD517 receives a 24 hour stabilization bake at +150°C, and a 48 hour burn-in at +125°C to ensure reliability and long-term stability.

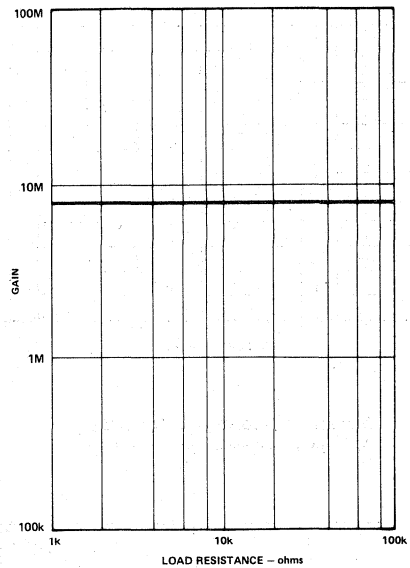
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD517J	AD517K	AD517L	AD517S[1]
OPEN LOOP GAIN				
V_O = ±10V, $R_L \geq 2k\Omega$	10^6 min	*	*	*
T_{min} to T_{max}	500,000 min	*	*	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	250kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leq 10k\Omega$	150μV max	75μV max	50μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.8μV/°C max	1.3μV/°C max	**
vs. Supply	25μV/V max	10μV/V max	**	**
(T_{min} to T_{max})	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	1nA max	0.75nA max	0.25nA max	**
T_{min} to T_{max}	1.5nA max	1.25nA max	0.4nA max	2nA max
INPUT BIAS CURRENT				
Initial	5nA max	2nA max	1nA max	**
T_{min} to T_{max}	8nA max	3.5nA max	1.5nA max	10nA max
vs. Temp, T_{min} to T_{max}	±20pA/°C	±10pA/°C	±4pA/°C	**
INPUT IMPEDANCE				
Differential	15MΩ‖1.5pF	20MΩ‖1.5pF	**	**
Common Mode	$2.0 \times 10^{11}\ \Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	2μV p-p	*	*	*
f = 10Hz	$35nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$25nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$20nV/\sqrt{Hz}$	*	*	*
Current, f = 10Hz	$0.05pA/\sqrt{Hz}$	*	*	*
f = 100Hz	$0.03pA/\sqrt{Hz}$	*	*	*
f = 1kHz	$0.03pA/\sqrt{Hz}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max Safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB min	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

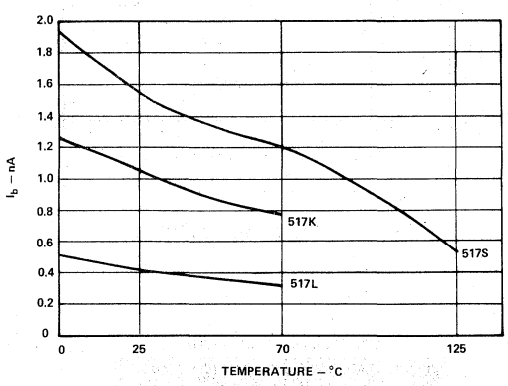
NOTES
*Specifications same as AD517J
**Specifications same as AD517K
[1] The AD517S is available fully processed and screened to the requirements of MIL-STD-883, Level B.
Specifications subject to change without notice.



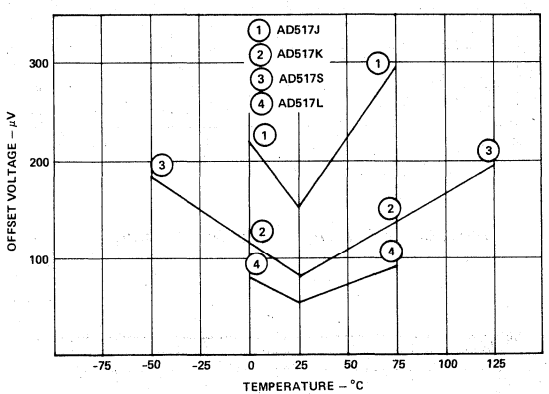
Small-Signal Gain vs. Frequency



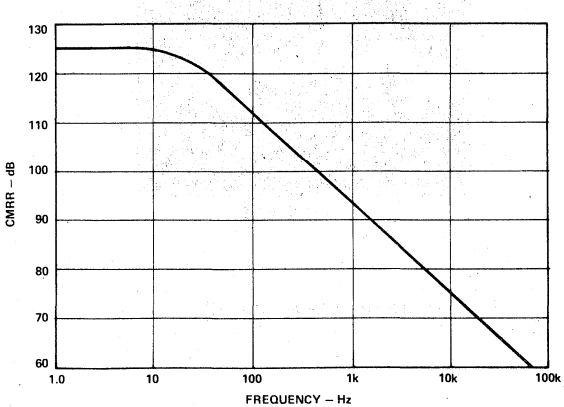
Open-Loop Gain vs. Load Resistance



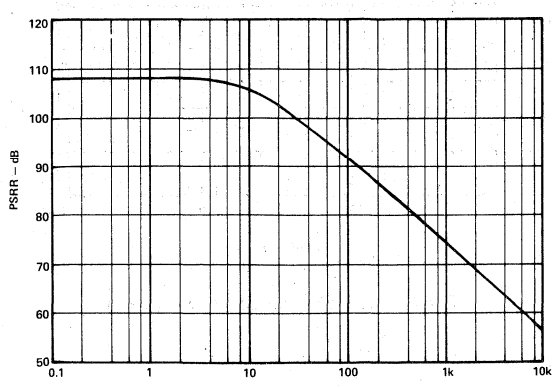
Input Bias Current vs. Temperature



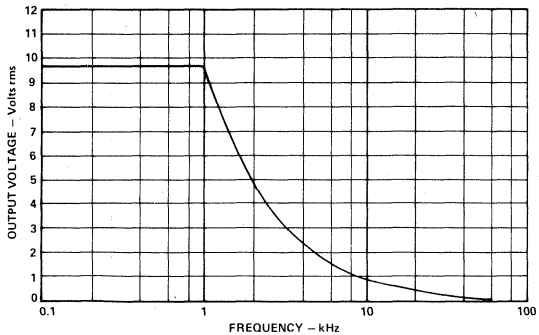
Untrimmed Offset Voltage vs. Temperature



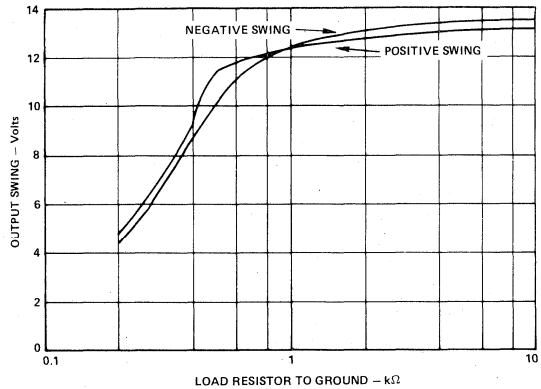
CMRR vs. Frequency



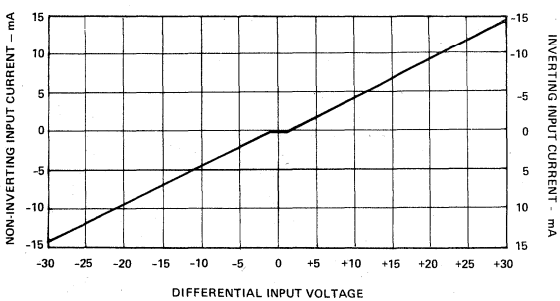
PSRR vs. Frequency



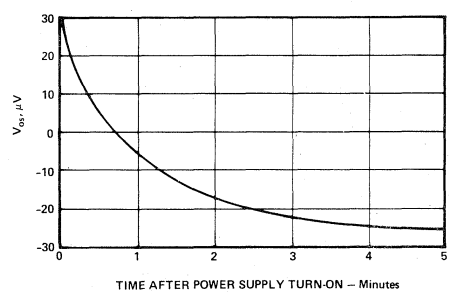
Maximum Undistorted Output vs. Frequency (Distortion ≤ 1%)



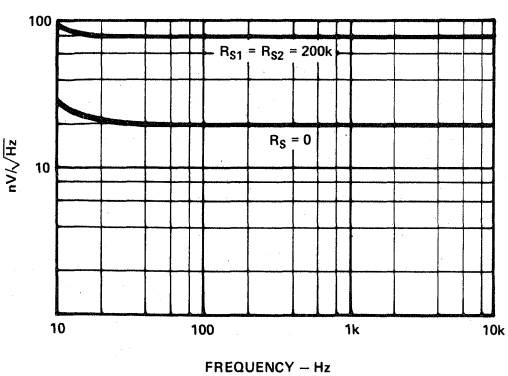
Output Voltage vs. Load Resistance



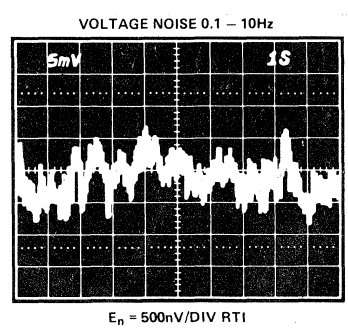
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

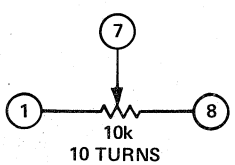
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

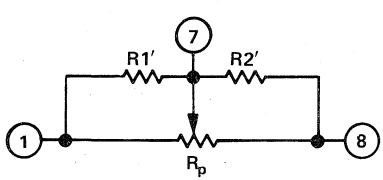
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega,}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

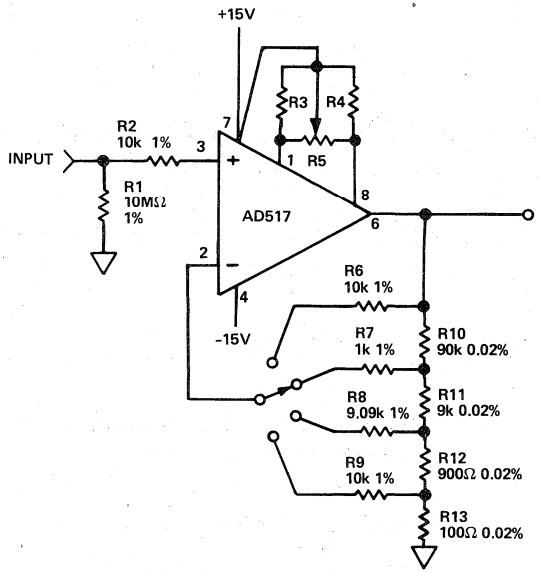


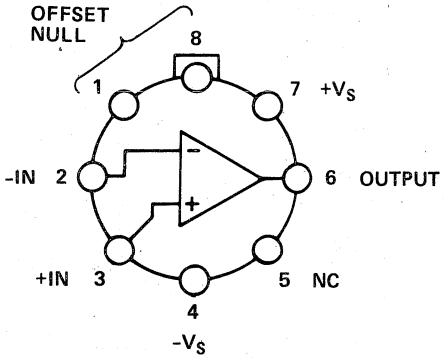
Figure 2. Stable Instrument Input Amplifier

Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

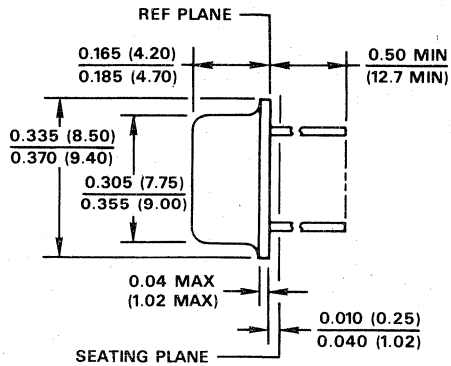
PIN CONFIGURATION



TOP VIEW

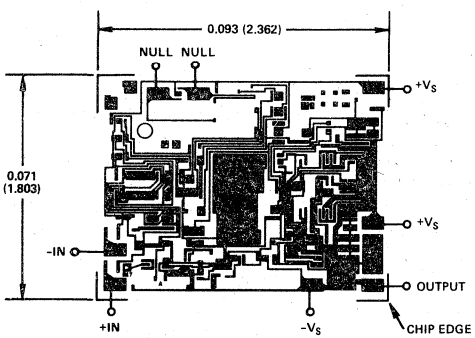
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



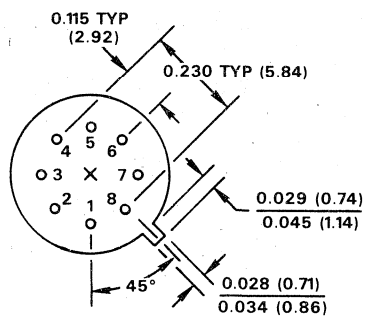
CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD517 IS AVAILABLE IN LASER-TRIMMED CHIP FORM. CONSULT CHIP CATALOG FOR DETAILS.

TO-99



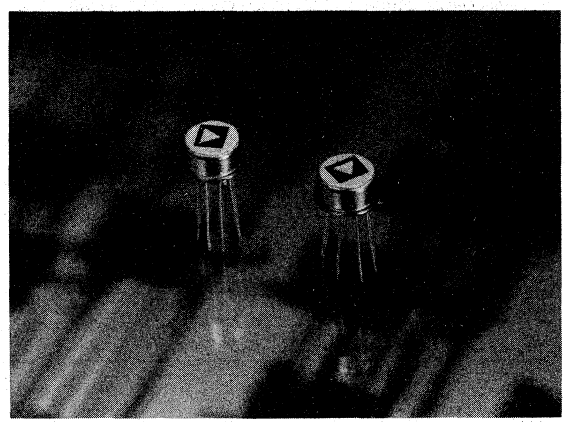
ANALOG DEVICES

Low Cost, High Speed, IC Operational Amplifier

AD518

FEATURES

- Low Cost
- High Slew Rate: 70V/μs
- Wide Bandwidth: 12MHz
- 60° Phase Margin (At Unity Gain Crossover)
- Drives 300pF Load
- Guaranteed Low Offset Drift: 15μV/°C Max (AD518K)
- Pin Compatible With 118-Type Op Amp Series
- MIL-STD-883 Availability



PRODUCT DESCRIPTION

The AD518J, AD518K, and AD518S are high speed precision monolithic operational amplifiers designed for applications where slew rate and wide bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μs, and a typical bandwidth of 12MHz. In addition, in inverting applications external feedforward compensation may be added to increase the slew rate to over 100V/μs, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μs with a single external capacitor.

The AD518's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2mV, maximum offset drifts of 15μV/°C, and offset currents below 50nA max.

The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with D/A and A/D converters, as well as active filters, sample-and-hold circuits, and as a general purpose, fast, wideband amplifier. The AD518 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to +70°C temperature range; the AD518S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD518 offers the user high speed performance and flexibility previously unavailable at low cost . . . . . .
   - Internal compensation for unity gain applications
   - Capability to increase slew rate to over 100V/μs and double the bandwidth by an external feedforward technique
   - Capability to reduce settling time to under 1μs to 0.1% with a single external capacitor
   - Differential input capability
2. The phase margin of the AD518, uncompensated at the unity gain crossover frequency, is 60°, providing unconditional stability for all conditions. This conservative phase margin represents a clear improvement over that of the 118 series IC op amps currently available.
3. The static performance of the AD518 is consistent with its excellent dynamic performance, providing offset voltage drift under 15μV/°C, CMRR of 80dB, and offset current below 50nA.
4. Every AD518 receives a 24 hour stabilization bake at +150°C to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

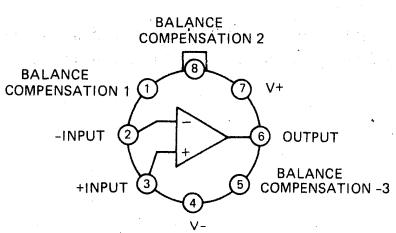
PARAMETER	AD518J	AD518K	AD518S
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, V_O = ±10V	25,000 min (100,000 typ)	50,000 min (100,000 typ)	50,000 min (100,000 typ)
@ T_A = min to max	20,000 min	25,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*
Current @ V_O = ±10V	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	12MHz	*	*
Slew Rate, Unity Gain	50V/μs min (70V/μs typ)	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800ns	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	10mV max (4mV typ)	4mV max (2mV typ)	4mV max (2mV typ)
@ T_A = min to max	15mV max	6mV max	6mV max
Avg vs. Temp, T_A = min to max	10μV/°C	15μV/°C max (5μV/°C typ)	20μV/°C max (10μV/°C typ)
Avg vs. Supply, T_A = min to max	65dB min (80dB typ)	80dB min (90dB typ)	80dB min (90dB typ)
INPUT BIAS CURRENT			
Initial	500nA max (120nA typ)	250nA max (120nA typ)	250nA max (120nA typ)
@ T_A = min to max	750nA max	400nA max	400nA max
INPUT OFFSET CURRENT			
Initial	200nA max (30nA typ)	50nA max (6nA typ)	50nA max (6nA typ)
@ T_A = min to max	300nA max	100nA max	100nA max
INPUT IMPEDANCE			
Differential	0.5MΩ min (3.0MΩ typ)	*	*
INPUT VOLTAGE RANGE †			
Common Mode, max safe	$\pm V_S$	*	*
Operating, V_S = ±15V	±11.5V	*	*
Common Mode Rejection Ratio	70dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	10mA max (5mA typ)	7mA max (5mA typ)	7mA max (5mA typ)
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

† The inputs are shunted with back-to-back diodes; if the differential input may exceed ±1 volt, a resistor should be used to limit the input current to 10mA.

*Specifications same as AD518J.

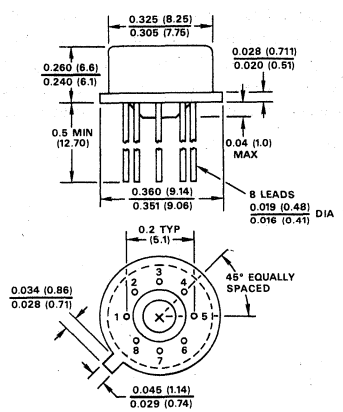
Specifications and prices subject to change without notice.

PIN CONFIGURATION
Top View



OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

TO-99



STABILITY & PHASE MARGIN

Perhaps one of the most meaningful ways to express the relative stability of a closed loop amplifier is in terms of phase margin. Phase margin is measured at that frequency where the open loop gain of the amplifier becomes unity or 0dB. It is the additional amount of phase shift that, if introduced in the loop, would make the loop unstable.

At very low frequencies the gain of most operational amplifiers is generally large. Moreover, the amplifier output signal is very nearly in phase with the differential input signal. This output is, therefore, nearly 180° out of phase with the feedback signal applied to the inverting input. At sufficiently high frequencies the gain of the amplifier begins to decrease as a function of frequency, with the resulting consequence of a lagging phase characteristic. That is, as the gain falls with increasing frequency, the phase of the output signal at a given frequency will lag the phase of the input signal. The phase shift depends most critically on the slope of the gain curve with respect to the logarithm of the frequency at the frequency where the phase is measured. If the gain changes more rapidly than 12dB/octave over a substantial frequency range, the minimum resulting phase shift may exceed 180°.

To insure amplifier stability, it is necessary that the phase shift near the unity gain frequency (12MHz in the AD518) is less than 180°. Moreover, it is generally required that the phase shift be substantially below the critical stability point to insure proper system performance. If the unity gain phase shift approaches 180°, the system will be on the verge of oscillation. As a result, there will be a large peak in the closed loop response near the unity loop gain frequency. This sharply peaked frequency response generally causes an undesirable small signal transient response with a poorly damped overshoot.

The term *phase margin* refers to the difference between 180° and the actual frequency-dependent phase shift at the system unity gain frequency. It is the margin between the actual system phase shift and the critical phase shift at which oscillation will occur. Not only does it indicate the relative immunity to oscillation, but it also gives some indication about the peaking and overshoot that can be expected.

The simple pole or frequency response of a single R-C network has a gain slope of 6dB/octave. This response has an associated phase shift which is asymptotic to −90°. Linear systems which are dominated by this characteristic in their open loop response are stable. They show no overshoot or ringing in their small signal transient response. Additional poles, either above or below the unity loop gain frequency, will add phase shift. As phase shift increases up to a lagging phase of about 120°, representing a 60° phase margin, little or no peaking will result. As the unity gain phase shift increases, peaking becomes more and more evident. For example, as the phase shift reaches 160° (20° of phase margin), between 9 and 10dB of peaking will occur.

The AD518 has been designed for a 60° phase margin at the unity gain crossover frequency, for absolute stability and absence of ringing and overshoot. (Note the transient response of the AD518 in Figure 1.) Note also in Figure 2 that the phase shift at 12MHz, the unity gain crossover frequency, is 120°, representing 60° of phase margin.

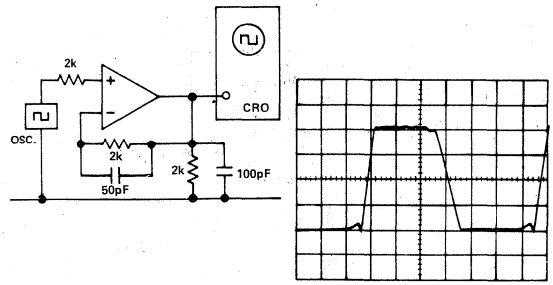


Figure 1. Transient Response of the AD518

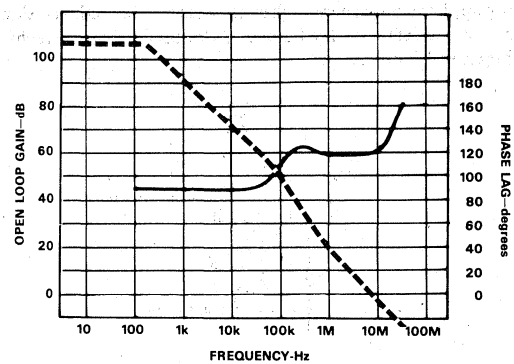


Figure 2. Amplitude and Phase Response of the AD518

THE FLEXIBILITY OF THE AD518

MINIMUM SETTLING TIME APPLICATIONS

For applications where a minimum settling time is desired, the settling time of the AD518 may be reduced significantly by employing the compensation scheme suggested in Figure 3.

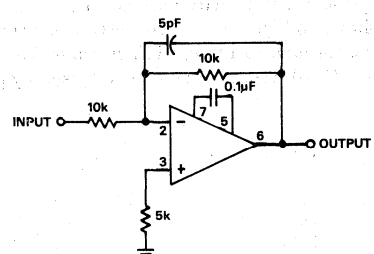


Figure 3. Minimum Settling Time Compensation

Using the 0.1μF capacitor from Pin 5 to V+ (Pin 7), the settling time to 0.1% is reduced from 2μs to 800ns.

HIGHER BANDWIDTH OR HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD518 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 4.

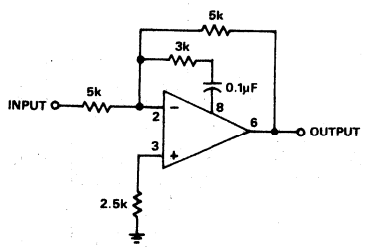


Figure 4. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD518 may be nearly doubled using the technique shown in Figure 5.

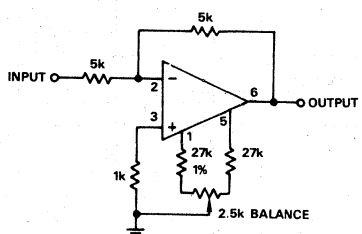


Figure 5. High Slew Rate Configuration

Note that the techniques of Figures 4 and 5 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/μs.

USING THE AD518

The connection scheme employed when using the AD518 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1μF bypass capacitors shown in Figure 6 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V– 0.1μF capacitor equalizes the supply grounds, while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

When using the AD518, this decoupling configuration should be used in conjunction with the configuration of Figures 3, 4 and 5, depending on the specific application.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

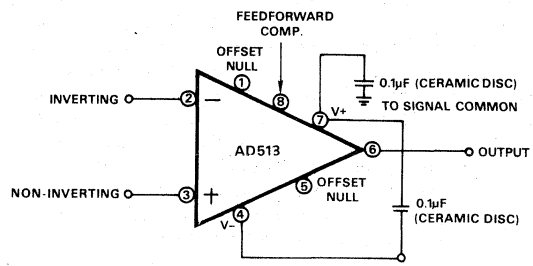
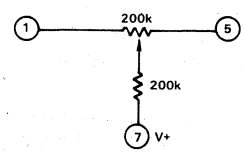


Figure 6. General Purpose Connection Diagram

NULLING THE AD518



OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

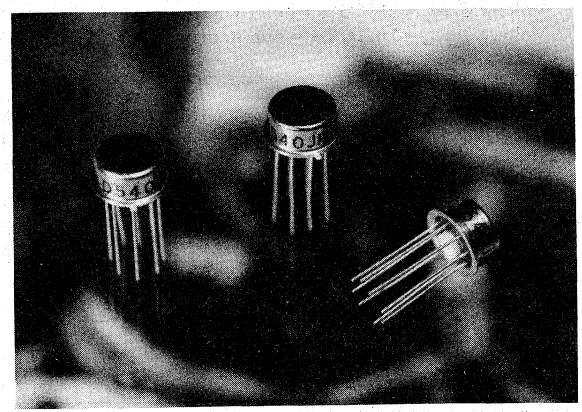
AD507	35MHz Gain Bandwidth Slew Rate of 25V/μs min Bias Current of 15nA max Offset Voltage Drift of 15μV/°C max
AD509	Settles to 0.01% in 1μs Settles to 0.1% in 200ns Slew Rate of 100V/μs min

ANALOG DEVICES

High Accuracy, Low Cost, FET-Input Operational Amplifier

AD540

FEATURES
Low Cost
Low I_b: 25pA max (K)
Low V_{OS}: 20mV max (K)
Low V_{OS} Drift: 25μV/°C max (K)
High Differential Input Voltage Capability: ±20V



PRODUCT DESCRIPTION

The AD540 is the lowest cost, high accuracy FET-input op amp available which provides the user with low bias currents, high overall performance, and accurately specified predictable operation. The device offers maximum bias currents as low as 25pA, offset voltages below 20mV, maximum offset voltage drift below 25μV/°C and a minimum gain of 50,000.

All devices are free from latchup and are short-circuit protected. No external compensation is required as the internal 6dB/octave roll-off provides stability in closed loop applications.

The AD540 is suggested for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.

All versions of the AD540 are supplied in the hermetically-sealed, 8-pin, TO-99 package. The AD540J and AD540K are specified for 0 to +70°C applications, while the AD540S is offered for operation over the full military temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD540 op amp meets specified input bias current and offset voltage values after full warm-up. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD540 are specified as a maximum for either input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Unlike many FET-input op amps, the AD540 allows a maximum differential input voltage of ±20V dc. Standard "bootstrapped" FET-input op amps permit maximum differential input voltages of only about ±3V.
4. Offset nulling of the AD540 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±2.0μV/°C per millivolt of nulled offset, compared to several times this for other IC FET op amps.
5. The gain of the AD540 is measured with the offset voltage nulled. Nulling a FET-input op amp can cause the gain to decrease below its specified limit. The gain of the AD540 is fully guaranteed with the offset voltage both nulled and unnulled.
6. To maximize the reliability inherent in IC construction, every AD540 receives a 24 hour stabilization bake at +150°C.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD540J	AD540K	AD540S
OPEN LOOP GAIN (Note 1)			
V_{out} = ±10V, $R_L \geq 2k\Omega$	20,000 min	50,000 min	**
T_A = min to max	15,000 min	25,000 min	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	6.0V/μs	*	*
INPUT OFFSET VOLTAGE (Note 2)	50mV max	20mV max	**
vs. Temperature	75μV/°C max	25μV/°C max	50μV/°C max
vs. Supply, T_A = min to max	400μV/V max	300μV/V max	**
INPUT BIAS CURRENT			
Either Input (Note 3)	50pA max	25pA max	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential (Note 4)	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	70dB min	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*

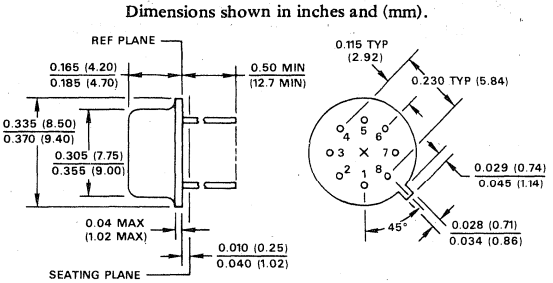
NOTE:
1. Open Loop Gain is specified with V_{OS} both nulled and unnulled.
2. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
3. Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
4. Defined as voltage between inputs, such that neither exceeds ±10V from ground.

* Specifications same as AD540J.
** Specifications same as AD540K.

Specifications subject to change without notice.

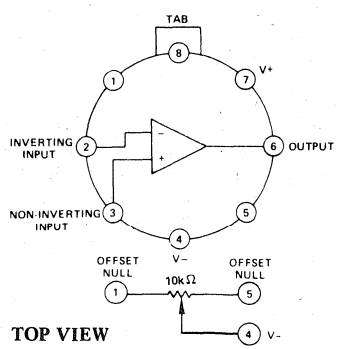
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



TOP VIEW

APPLYING THE AD540

The AD540 is especially designed for low cost applications involving the measurement of low level currents or small voltages from high impedance sources in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the non-inverting "buffer" connection is used). The AD540 FET-input operational amplifier is, therefore, of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

APPLICATIONS CONSIDERATIONS

BIAS CURRENTS. Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed-up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the maximum bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed-up operating unit.

The AD540 specifies maximum bias current at either input after warm-up, thus giving the user the values he expected.

IMPROVING BIAS CURRENT BEYOND GUARANTEED VALUES. Bias currents can be substantially reduced in the AD540 by decreasing the junction temperature of the devices. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

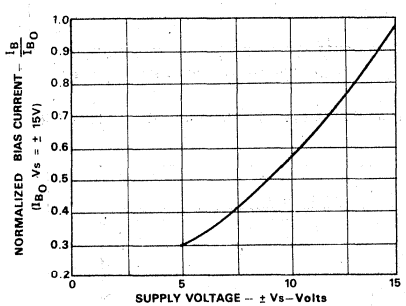


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD540K at ±5V reduces the warmed-up bias current by 70% to a typical value of 8pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading. Note that the use of the Model 209 heat sink reduces warmed-up bias current by 60% to 10pA in the AD540K.

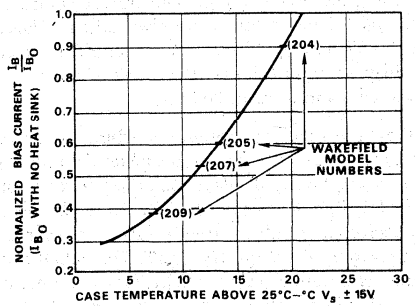


Figure 2. Normalized Bias Current vs. Case Temperature

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

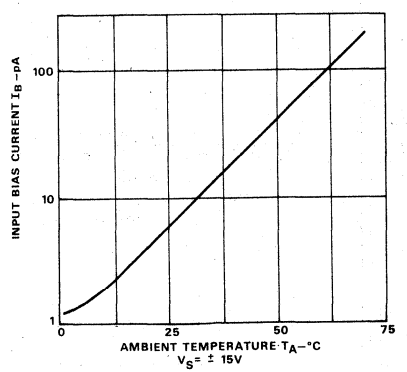


Figure 3. Input Bias Current vs. Temperature

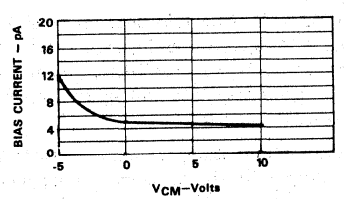


Figure 4. Bias Current vs. Common Mode Voltage.

INPUT CONSIDERATIONS. Unlike some FET-input operational amplifiers, the AD540 accommodates differential input voltages of up to ±20V....without any degradation in bias current. In certain time-dependent applications, such as charge amplifiers and integrators, large differential input voltages temporarily occur which may exceed the rated value of a typical FET op amp (approximately ±3V differential).

By utilizing un-bootstrapped FET's at the inputs, the AD540 assures the user of expected performance at large differential input voltages....without the use of protective diodes or resistors.

OFFSET VOLTAGE DRIFT. Most commercially available IC FET op amps are nulled by adjusting the FET operating currents, causing the offset voltage temperature coefficients to vary 3 to 6μV/°C per millivolt of offset nulled. Thus a conventional FET op amp with 20mV initial offset, when nulled may display an additional offset drift of 60 to 120μV/°C, in addition to its nulled value.

The AD540 achieves nulling without disturbing the operating currents of the FET's, thus allowing a substantial reduction in drift. Figure 5 graphically displays the offset drift performance of the AD540, nulled and unnulled. As can be seen, nulling the device can result in either positive or negative offset drifts given by the slope $\Delta V_{OS}/\Delta T$. The nulled curves represent the maximum changes in drift, indicating performance considerably better than many other IC FET op amps which null V_{OS} by varying the operating currents of the FET's.

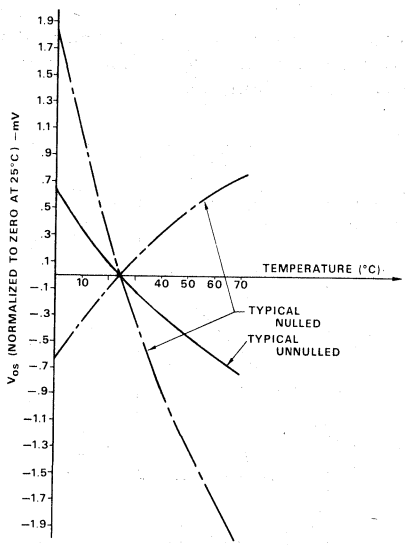


Figure 5. V_{OS} vs. Temperature

NOISE PERFORMANCE. The noise spectral density vs. frequency for the AD540 is given in Figure 6. The curve shows approximately 300nV/$\sqrt{\text{Hz}}$ at 10Hz, declining in a 1/f fashion (1/f for power, 1/$\sqrt{f}$ for voltage) to approximately 12nV/$\sqrt{\text{Hz}}$ at higher frequencies.

Current noise in the AD540 is approximately 0.001pA/$\sqrt{\text{Hz}}$ at low frequencies. Above 300Hz, the current noise generated by the op amp increases at a 3dB/octave rate, determined by $\omega e_n C_{in}$, where e_n = spectral noise density and C_{in} = input capacitance. In most practical applications, the current noise from source or feedback resistors will be larger than the low frequency current noise from the amplifier.

At high frequencies, the total circuit current noise is equal to $\omega e_n C$, where C is the sum of all input and feedback capacitors. In well-shielded circuits, C is usually 10 to 100pF, so that the $\omega e_n C$ can be a significant factor. Thus the user should attempt to minimize C.

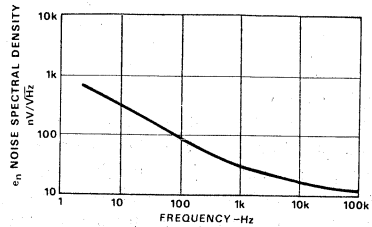


Figure 6. Noise Spectral Density vs. Frequency

DYNAMIC PERFORMANCE. The AD540 is internally compensated to achieve a –3dB bandwidth of 1MHz (see Figure 7). At unity gain the full power bandwidth is 50kHz minimum, and typically 100kHz. Slew rates are 3V/μs minimum and 6V/μs typical (see Figure 8 and Figure 9).

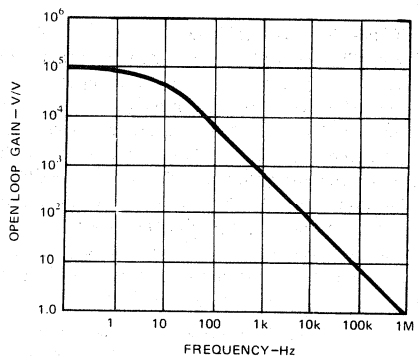


Figure 7. Small Signal Gain vs. Frequency

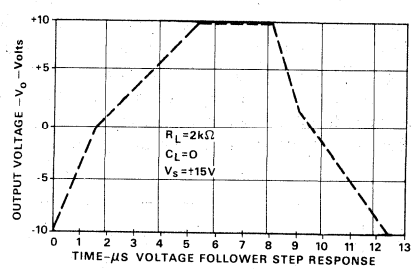


Figure 8. Voltage Follower Step Response

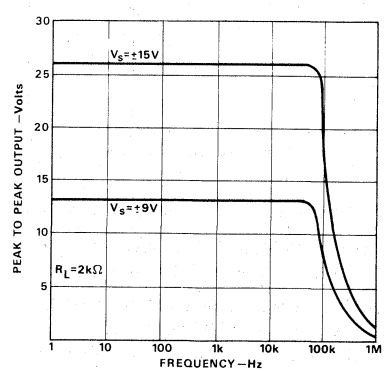


Figure 9. P-P Output vs. Frequency

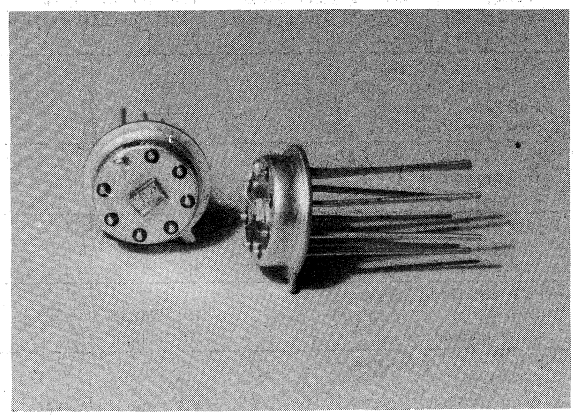
ANALOG DEVICES

Precision Low Cost BI-FET Op Amp

AD542

FEATURES

- **Low Bias Current: 25pA max, warmed-up (AD542K,L), 50pA max (AD542J)**
- **Low Offset Voltage: 0.5mV max (AD542L), 1.0mV max (AD542K)**
- **Low Offset Voltage Drift: 5μV/°C max (AD542L), 10μV/°C max (AD542K) 20μV/°C max (AD542J)**
- **Low Quiescent Current: 1.5mA max**
- **Low Price**



PRODUCT DESCRIPTION

The AD542 is a precision, monolithic FET-input operational amplifier fabricated with the most advanced BI-FET and laser trimming technologies. The AD542 offers bias currents significantly lower than currently available BI-FET devices: 25pA max, warmed-up for the AD542K and L, 50pA max for the AD545J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD542L and 1.0mV on the AD542K utilizing Analog's exclusive laser-wafer-trimming (LWT) process. When combined with the AD542's low offset voltage drift (5μV/°C max for "L", 10μV/°C max for "K"), these features offer the user IC performance truly superior to existing BI-FET op amps – and at low, BI-FET pricing.

The key to BI-FET technology is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFET's on a monolithic bi-polar chip. Analog Devices optimizes the BI-FET process to produce bias currents lower than other popular BI-FET op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1 – 10Hz), and low quiescent current.

The AD542 is recommended for any operational amplifier application requiring excellent dc performance at low and moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain—even under heavy loading—ensures better than "12-bit" linearity in high impedance buffer applications. Additionally, bandwidth and slew rate are much increased over presently available precision, bipolar op amps.

The AD542 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C military operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved BI-FET processing on the AD542 results in the lowest bias current available in a BI-FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD542 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD542L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (Offset voltage drift can increase an additional 3μV/°C per mV of offset nulled.)
5. Low voltage noise (2μV, p-p), and low offset voltage drift enhance the AD542's performance as a precision op amp.
6. The 1.5mA max quiescent current enables the device to be used in numerous portable applications where low battery drain is essential. This is achieved without sacrificing open loop gain or the ability to drive up to a 10mA load.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD542J	AD542K	AD542L	AD542S
OPEN LOOP GAIN[1]				
V_{out} = ±10V, $R_L \geq 1k\Omega$	50,000 min	150,000 min	**	**
$R_L \geq 2k\Omega$	100,000 min	300,000 min	**	**
T_A = min to max	100,000 min	300,000 min	**	**
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.0MHz	*	*	*
Full Power Response	50kHz	*	*	*
Slew Rate, Unity Gain	3.0V/μs	*	*	*
INPUT OFFSET VOLTAGE[2]	2.0mV max	1.0mV max	0.5mV max	**
vs. Temperature	20μV/°C max	10μV/°C max	5μV/°C max	15μV/°C max
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT				
Either Input[3]	50pA max	25pA max	**	**
Input Offset Current	5pA	2pA	**	**
INPUT IMPEDANCE				
Differential	$10^{10}\Omega \| 2pF$	*	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[4]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{in} = ±10V	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	1.5mA max	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2μV p-p	*	*	*
10Hz	70nV/√Hz	*	*	*
100Hz	45nV/√Hz	*	*	*
1kHz	30nV/√Hz	*	*	*
10kHz	25nV/√Hz	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*

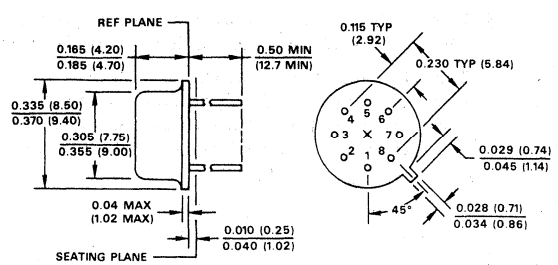
NOTES:
[1] Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[4] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as AD542J.
**Specifications same as AD542K.

Specifications subject to change without notice.

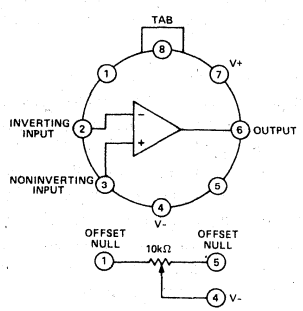
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



TOP VIEW

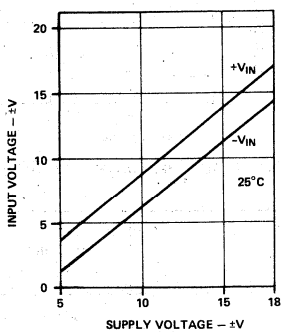


Figure 1. Input Voltage Range

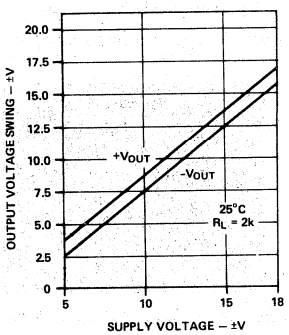


Figure 2. Output Swing

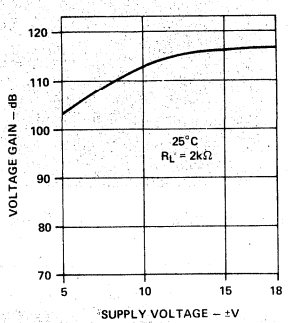


Figure 3. Voltage Gain

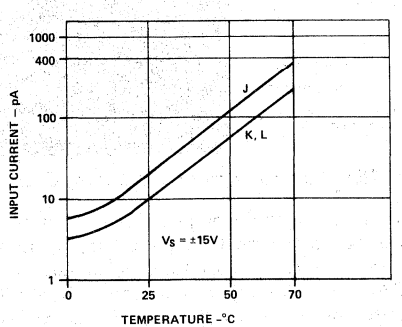


Figure 4a. Input Current vs. Temperature

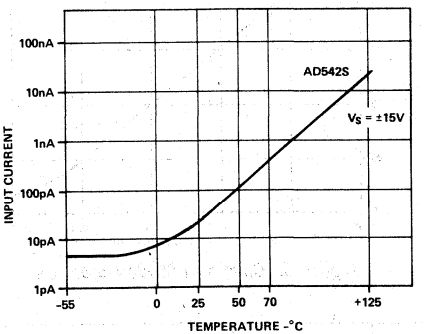


Figure 4b. Input Current vs. Temperature

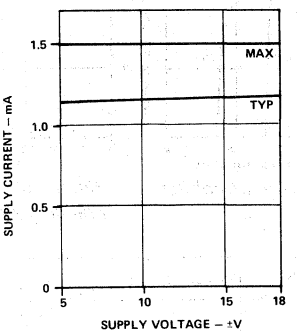


Figure 5. Supply Current

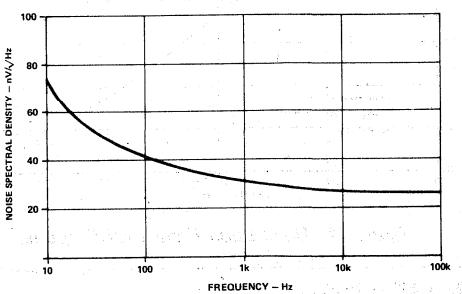


Figure 6. Input Noise Voltage, Spectral Density

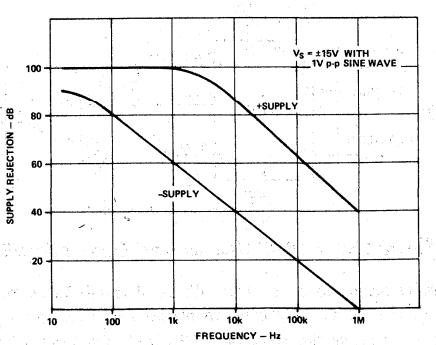


Figure 7. Power Supply Rejection

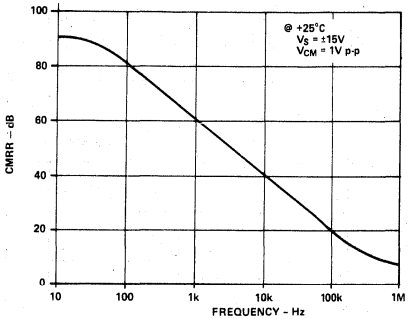


Figure 8. Common Mode Rejection

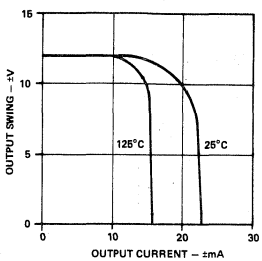


Figure 9. Current Limiting

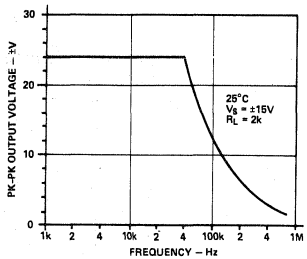


Figure 10. Large Signal Frequency Response

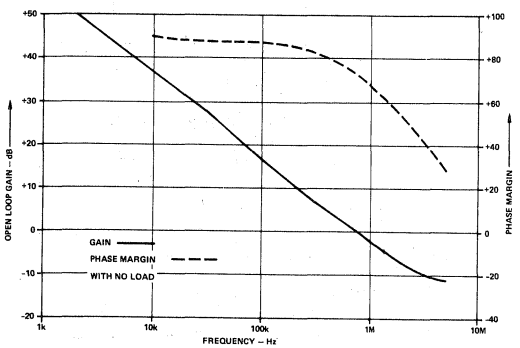


Figure 11. Open Loop Frequency Response

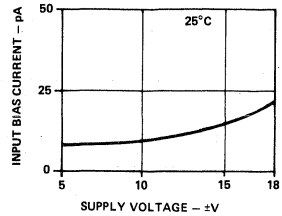


Figure 12. Input Bias Current vs. Supply Voltage

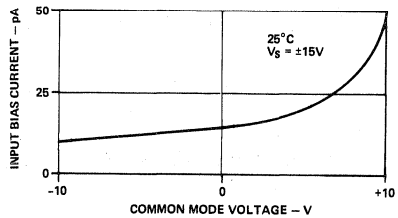


Figure 13. Input Bias Current vs. CMV

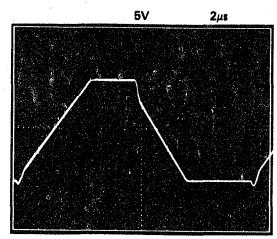


Figure 14a. Unity Gain Follower Pulse Response

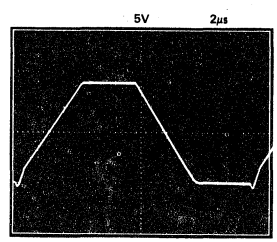


Figure 14b. Unity Gain Inverter Pulse Response

APPLICATION

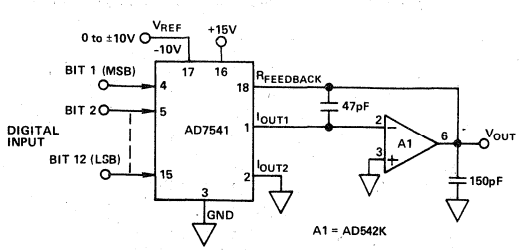


Figure 15a. AD542 Used as DAC Output Amplifier

The 1MHz bandwidth and low offset of the AD542 make it an excellent choice as an output amplifier for current-output D/A converters such as the AD7541, 12-bit CMOS DAC (1.8mV of amplifier offset could result in non-monotonic operation).

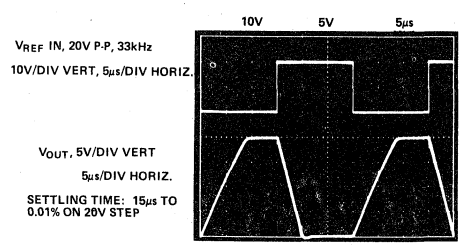


Figure 15b. Voltage Output DAC Settling Characteristic

The photo above shows the output of the circuit of Figure 15a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

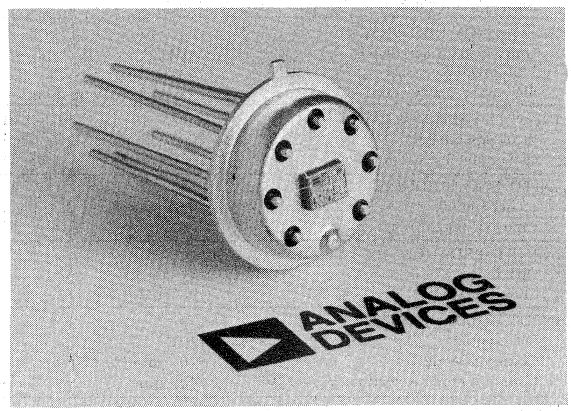
ANALOG DEVICES

High Speed Implanted FET-Input Op Amp

AD544

FEATURES

Low Bias Current: 25pA max, warmed-up
Low Offset Voltage: 500μV max
Low Offset Voltage Drift: 5μV/°C max
Low Input Voltage Noise: 2μV p-p
Low Quiescent Current: 2.5mA max
High Slew Rate: 13V/μs
Fast Settling to ±0.01%: 3μs



PRODUCT DESCRIPTION

The AD544 is a high speed monolithic FET-input operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD544 offers bias currents significantly lower than currently available monolithic FET-input devices: 25pA max, warmed-up for the AD544K and L, 50pA max for the AD544J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD544L and 1.0mV on the AD544K utilizing Analog's exclusive laser-wafer-trimming (LWT) process. When combined with the AD544's low offset voltage drift (5μV/°C max for "L", 10μV/°C max for "K"), these features offer the user IC performance truly superior to existing FET-input op amps—and at low, monolithic pricing.

The key technology required for monolithic JFET-input op amps is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFET's on a monolithic bipolar chip. Analog Devices optimizes the process to produce bias currents lower than other popular FET-input op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1—10Hz), and low quiescent current.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low cost. The 2MHz bandwidth and low offset of the AD544 make it an excellent choice as an output amplifier for current output D/A Converters such as the AD7541, 12-Bit CMOS DAC. High common mode rejection (80dB, min on the "K" and "L" versions) and open-loop gain ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the −55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing on the AD544 results in the lowest bias current available in a high speed monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD544 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD544L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (Offset voltage drift can increase an additional 3μV/°C per mV of offset nulled.)
5. Low voltage noise (2μV, p-p), and low offset voltage drift enhance the AD544's performance as a precision op amp.
6. The 2.5mA max quiescent current enables the device to be used in numerous portable applications where low battery drain is essential. This is achieved without sacrificing open loop gain or the ability to drive up to a 10mA load.
7. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD544J	AD544K	AD544L	AD544S[1]
OPEN LOOP GAIN[2]				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	30,000 min	50,000 min	**	**
T_A = min to max R_L = 2kΩ	20,000 min	40,000 min	**	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	2.0MHz	*	*	*
Full Power Response	200kHz	*	*	*
Slew Rate, Unity Gain	13.0V/μs (8.0V/μs min)	*	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	0.5mV max	**
vs. Temperature	20μV/°C max	10μV/°C max	5μV/°C max	15μV/°C max
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT				
Either Input[4]	50pA max	25pA max	**	**
Input Offset Current	5pA	2pA	**	**
INPUT IMPEDANCE				
Differential	$10^{10}\Omega$||2pF	*	*	*
Common Mode	$10^{11}\Omega$||2pF	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	74dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	2.5mA max (1.8mA typ)	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2μV p-p	*	*	*
10Hz	35nV/√Hz	*	*	*
100Hz	22nV/√Hz	*	*	*
1kHz	18nV/√Hz	*	*	*
10kHz	16nV/√Hz	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

NOTES

[1] The AD544S/883 is an AD544S which is inspected and processed to the full requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

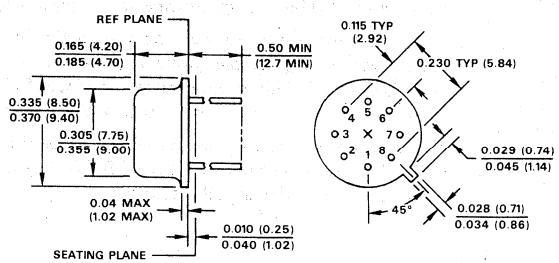
*Specifications same as AD544J.

**Specifications same as AD544K.

Specifications subject to change without notice.

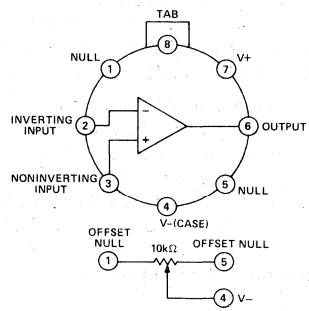
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



TOP VIEW

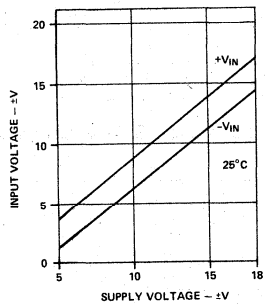


Figure 1. Input Voltage Range

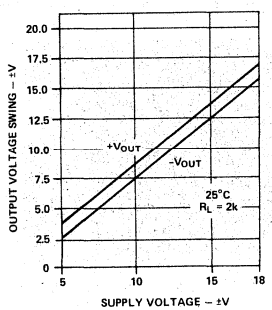


Figure 2. Output Swing

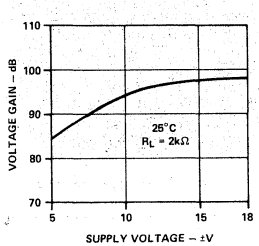


Figure 3. Voltage Gain

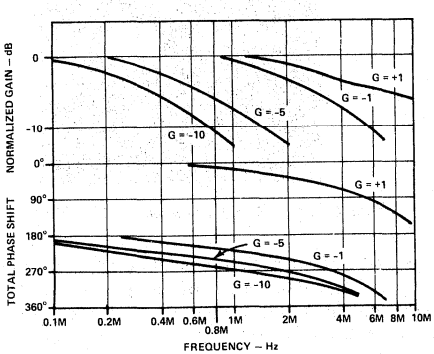


Figure 4. Closed Loop Gain & Phase vs. Frequency

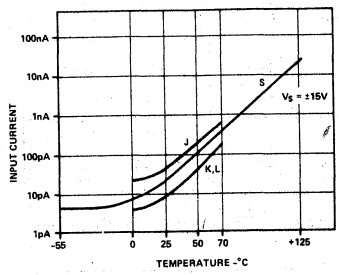


Figure 5. Input Current vs. Temperature

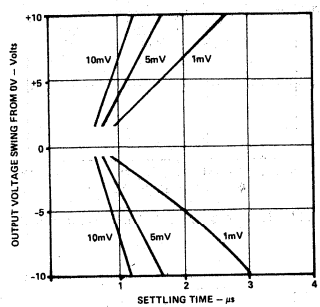


Figure 6. Output Settling Time vs. Output Swing and Error (Circuit of Figure 15a)

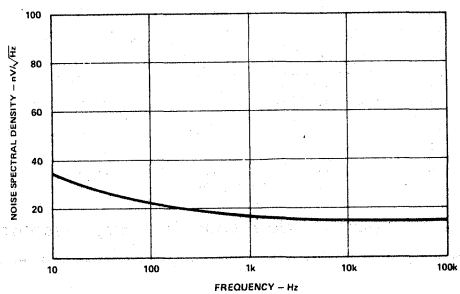


Figure 7. Input Noise Voltage Spectral Density

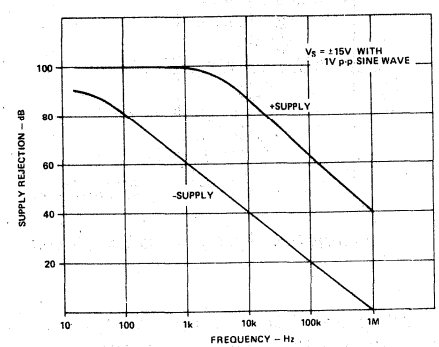


Figure 8. Power Supply Rejection

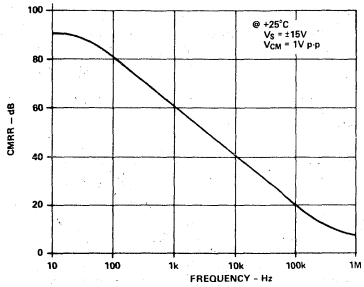


Figure 9. Common Mode Rejection

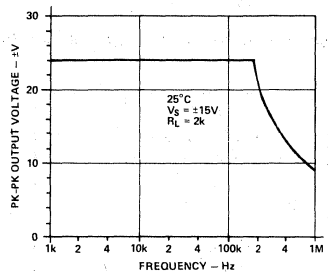


Figure 10. Large Signal Frequency Response

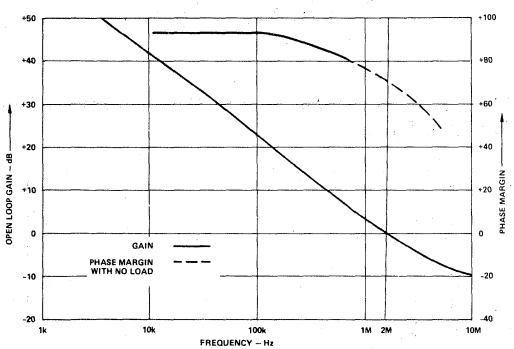


Figure 11. Open Loop Frequency Response

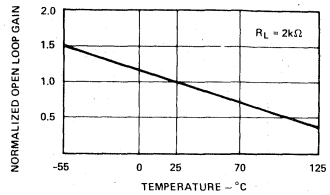


Figure 12. Open Loop Gain vs. Temperature

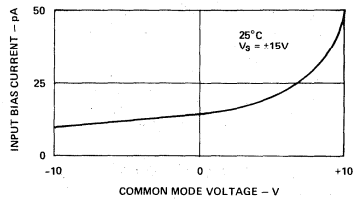


Figure 13. Input Bias Current vs. CMV

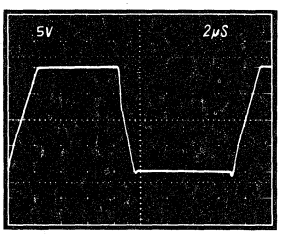


Figure 14a. Unity Gain Follower Pulse Response

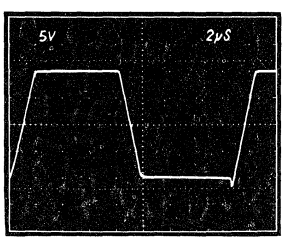


Figure 14b. Unity Gain Inverter Pulse Response

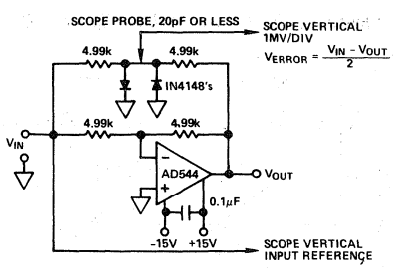


Figure 15a. Settling Time Test Circuit

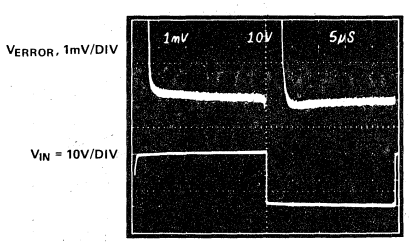


Figure 15b. Settling Characteristic Detail

The fast settling time (3.0μs to 0.01% for 20V p-p step) and low offset voltage make it an excellent choice as an output amplifier for current output D/A converters such as the AD565.

The upper trace of the oscilloscope photograph of Figure 15b shows the settling characteristic of the AD544. The lower trace represents the input to Figure 15a. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

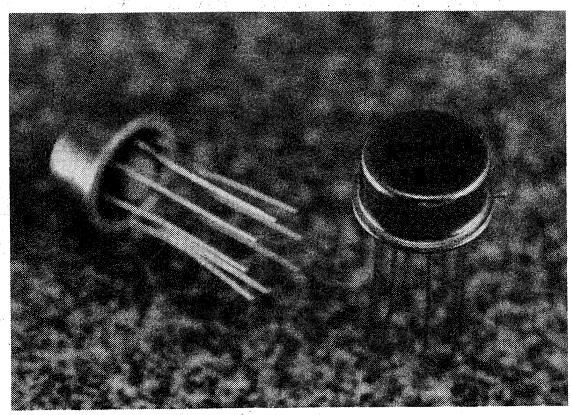
ANALOG DEVICES

Precision, Low Drift FET-Input Op Amp

AD545

FEATURES

Low Offset Voltage: 0.5mV max (AD545L), 0.25mV max (AD545M)
Low Offset Voltage Drift: 5μV/°C max (AD545L), 3μV/°C max (AD545M)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545K, L, M)
Low Noise: 3μV p-p, 0.1 to 10Hz
Low Cost



PRODUCT DESCRIPTION

The AD545 is a precision FET-input operational amplifier with overall performance far superior to the general purpose IC FET-input op amp. The device is fabricated using a low leakage FET paired with a low power op amp. Bias current is specified as 2pA max for the AD545J and 1pA max for the AD545K, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545L, 0.25mV max for the AD545M. All devices also feature low voltage noise and power consumption. The AD545 is internally compensated, short circuit protected and free of latch-up.

The AD545 series offers a broad combination of performance features previously unavailable from a single device. For precision applications the AD545M specifies a 0.25mV max offset voltage, 3μV/°C max drift and 1pA max bias current. The AD545J, with a 1mV max offset voltage, 25μV/°C max drift and 2pA max bias current, is the best price performance choice.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/plon sensitive electrodes, photo-current detectors, biological microprobes, long term precision integrators and vacuum iongauge measurements. The versatility of the AD545 is further enhanced by its excellent low frequency noise (3μV p-p, 0.1 to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD545 is available in four versions of bias current and offset voltage, the "J", "K", "L", and "M". All are specified from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The offset voltage on the AD545 is laser trimmed to a level typically less than 250μV. Offset voltage drift is significantly lower than previously available FET-input devices (3μV/°C max for the AD545M). If additional external nulling is desired, the effect on drift is minimal (approximately 3μV/°C per millivolt, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient.
3. The low quiescent current drain of 0.8mA typical, and 1.5mA max, is among the lowest of any IC op amp and keeps self heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristics.
5. Every AD545 receives a 24 hour stabilization bake at +150°C to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

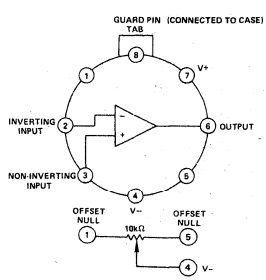
MODEL	AD545J	AD545K	AD545L	AD545M
OPEN LOOP GAIN[1]				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000V/V min	40,000V/V min	40,000V/V min	40,000V/V min
$R_L \geq 10k\Omega$	40,000V/V min	50,000V/V min	50,000V/V min	50,000V/V min
T_A = min to max $R_L \geq 2k\Omega$	15,000V/V min	25,000V/V min	40,000V/V min	40,000V/V min
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*	*
Load Capacitance[2]	500pF	*	*	*
Short Circuit Current	10mA min (25mA typ)	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	700kHz	*	*	*
Full Power Response	5kHz min (16kHz typ)	*	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (1.0V/μs typ)	*	*	*
Overload Recovery Inverting Unity Gain	100μs max (16μs typ)	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	1.0mV max	0.5mV max	0.25mV max
vs. Temperature, T_A = min to max	25μV/°C max	15μV/°C max	5μV/°C max	3μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	200μV/V max	200μV/V max	200μV/V max
INPUT BIAS CURRENT				
Either Input[4]	2pA max	1pA max	1pA max	1pA max
INPUT IMPEDANCE				
Differential	1.6pF‖$10^{13}\Omega$	*	*	*
Common Mode	0.8pF‖$10^{15}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	3.0μV (p-p)	*	*	5μV (p-p) max
f = 10Hz	55nV/$\sqrt{Hz}$	*	*	*
f = 100Hz	45nV/$\sqrt{Hz}$	*	*	*
f = 1kHz	35nV/$\sqrt{Hz}$	*	*	*
Current, 0.1 to 10Hz	0.01pA (p-p)	*	*	*
10Hz to 10kHz	0.03pA rms	*	*	*
INPUT VOLTAGE RANGE				
Differential	±20V min	*	*	
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*	
Common Mode Rejection, V_{IN} = ±10V	66dB min (80dB typ)	70dB min	76dB min	76dB min
Maximum Safe Input Voltages[5]	±V_S	*	*	*
POWER SUPPLY				
Rated Performance	±15V typ	*	*	*
Operating	±5V min (±18V max)	*	*	*
Quiescent Current	1.5mA max (0.8mA typ)	*	*	*
TEMPERATURE				
Operating, Rated Performance	0 to +70°C	*	*	*
Storage	-65°C to +150°C	*	*	*

*Specifications same as AD545J.

NOTES
[1] Open Loop Gain is specified with or without nulling of V_{OS}.
[2] A conservative design would not exceed 500pF of load capacitance.
[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
[5] If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage.

Specifications and prices subject to change without notice.

PIN CONFIGURATION



TOP VIEW

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves the additional function of reducing the effective capacitance to the input line. The case of the AD545 is brought out separately to pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.
3. Printed circuit board layout and construction is critical in achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545 but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

APPLICATION NOTES

The AD545 offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545 and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated; we recommend restricting the load impedance to be at least 10kΩ.

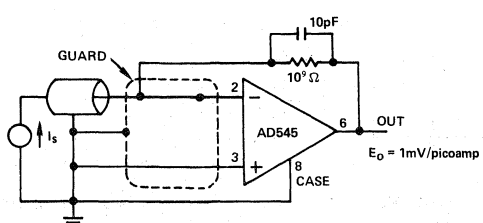


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

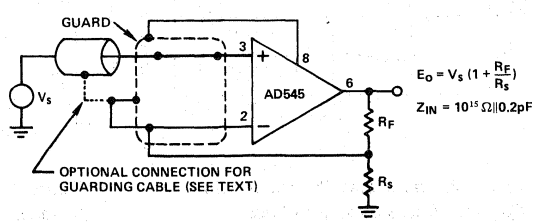


Figure 2. Very High Impedance Non-Inverting Amplifier

Typical Performance Curves

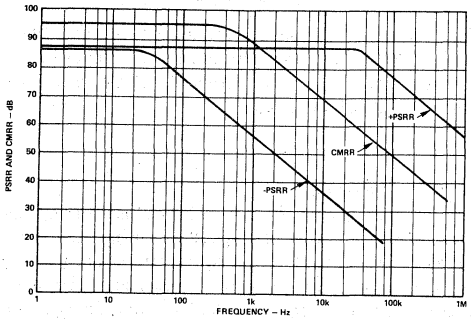


Figure 3. PSRR and CMRR Versus Frequency

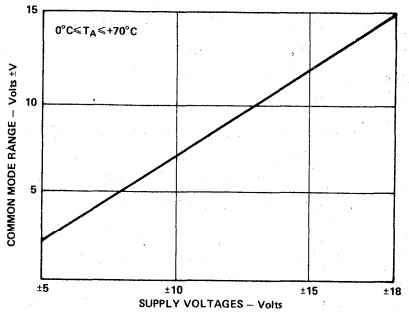


Figure 4. Input Common Mode Range Versus Supply Voltage

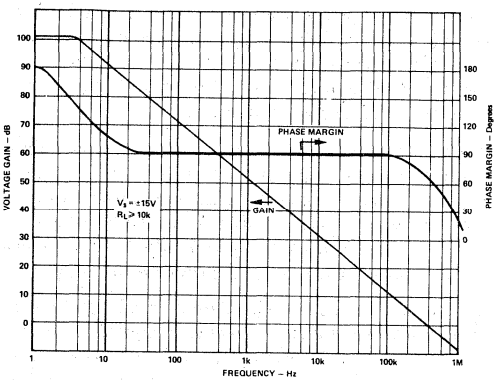


Figure 5. Open Loop Frequency Response

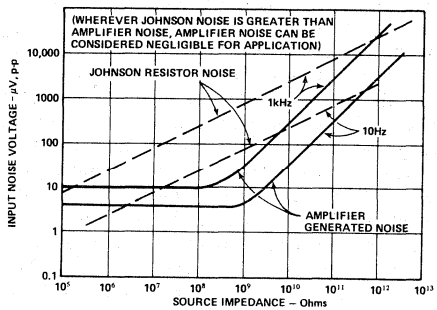


Figure 6. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

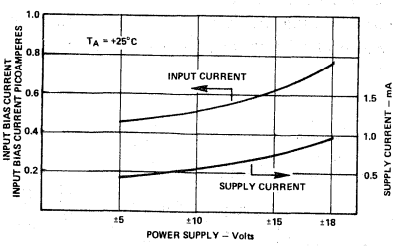


Figure 7. Input Bias Current and Supply Current Versus Supply Voltage

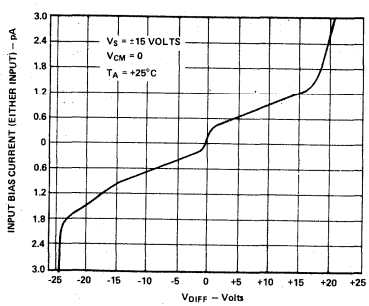


Figure 8. Input Bias Current Versus Differential Input Voltage

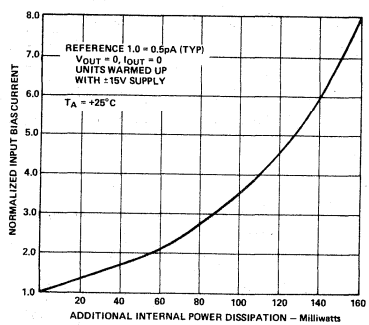


Figure 9. Input Bias Current Versus Addition Power Dissipation

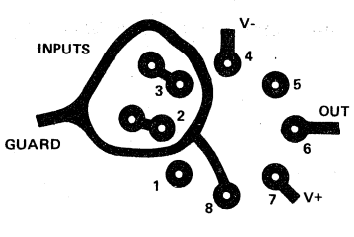
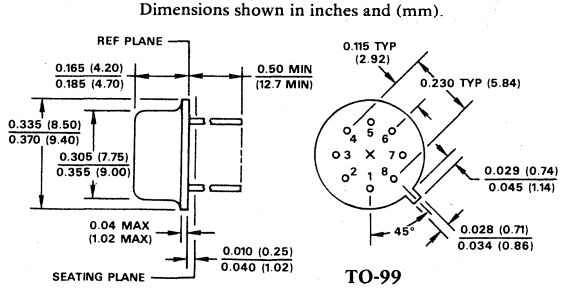


Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

ANALOG DEVICES

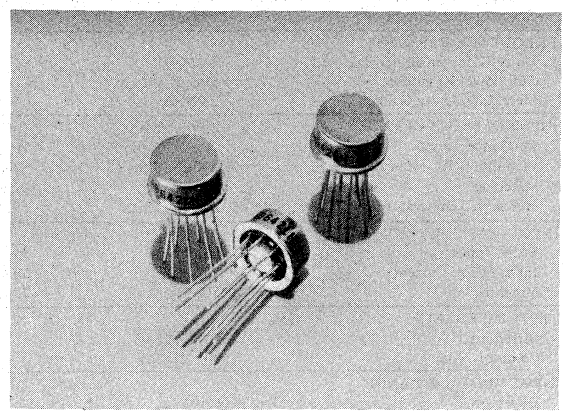
Precision Low Cost Dual TRI-FET Op Amp

AD642

ADVANCED TECHNICAL DATA

FEATURES

Low Bias Current: 35pA max, warmed-up (AD642K, L), 75pA max (AD642J)
Low Offset Voltage: 0.5mV max (AD642L), 1.0mV max (AD642K)
Low Offset Voltage Drift: 5μV/°C max (AD642L), 10μV/°C max (AD642K) 20μV/°C max (AD642J)
Excellent V_{OS} Matching: 0.25mV max (AD642L)
Low Quiescent Current: 3.0mA max
Standard Dual Amplifier Pin-Out



PRODUCT DESCRIPTION

The AD642 is a dual version of the popular AD542 precision TRI-FET operational amplifier. Produced with advanced ion-implantation and laser trimming technologies, the AD642 retains all the performance features of the AD542: low (35pA max) warmed-up bias current; low (0.5mV max) input offset voltage; low (5μV/°C) drift and high open-loop gain (300,000V/V). Additionally, the two amplifiers exhibit offset voltage matching within 0.25mV max (AD642L) and drifts matched to 5μV/°C max.

The key to the AD642 performance is the ion-implanted JFET. Analog Devices optimizes this process to produce bias currents lower than other popular monolithic FET-input op amps and specifies each device for the maximum value at either input under fully warmed-up conditions. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1 – 10Hz), and low quiescent current.

The AD642 is recommended for any operational amplifier application requiring excellent dc performance at low and moderate costs. Precision instrument front ends requiring accurate amplification of millivolt-level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" version) and high open-loop gain ensure better than "12-bit" linearity.

The AD642 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C military operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved processing on the AD642 results in the lowest bias current available in a precision dual monolithic FET-input op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD642L), thus eliminating the need for external nulling in many situations.
4. Low voltage noise (2μV, p-p) and low offset voltage drift enhance the AD642's performance as a precision op amp.
5. The matching specifications on offset voltage, bias current and drift ensure that the two amplifiers are closely matched.
6. The standard dual amplifier pin-out allows the AD642 to replace lower performance duals without redesign.

SPECIFICATIONS (typical for each section @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD642J	AD642K	AD642L	AD642S
OPEN LOOP GAIN				
V_{out} = ±10V, $R_L \geq 10k\Omega$	200,000 min	300,000 min	**	**
$R_L \geq 2k\Omega$	100,000 min	250,000 min	**	**
T_A = min to max, $R_L \geq 10k\Omega$	100,000 min	300,000 min	**	200,000 min
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.0MHz	*	*	*
Full Power Response	50kHz	*	*	*
Slew Rate, Unity Gain	3.0V/μs	*	*	*
INPUT OFFSET VOLTAGE[1]	2.0mV max	1.0mV max	0.5mV max	**
vs. Temperature	20μV/°C max	10μV/°C max	5μV/°C max	15μV/°C max
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**
Matching[2]	1.0mV max	0.5mV max	0.25mV max	**
Match vs. Temperature	20μV/°C max	10μV/°C max	5μV/°C max	15μV/°C max
INPUT BIAS CURRENT				
Either Input[3]	75pA max	35pA max	**	**
Input Offset Current	75pA	5pA	**	**
Matching[2]	50pA max	25pA max	15pA max	**
INPUT IMPEDANCE				
Differential	$10^{10}\Omega \| 2pF$	*	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[4]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{in} = ±10V	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	3.0mA max	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2μV p-p	*	*	*
10Hz	70nV/√Hz	*	*	*
100Hz	45nV/√Hz	*	*	*
1kHz	30nV/√Hz	*	*	*
10kHz	25nV/√Hz	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C[5]
Storage	−65°C to +150°C	*	*	*

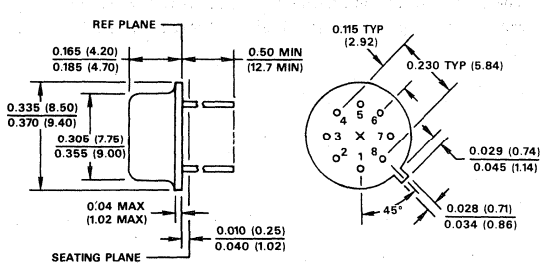
NOTES:
[1] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2] Matching is defined as the match between parameters of the two amplifiers.
[3] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[4] Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[5] The AD642S is available processed to the requirements of MIL-STD-883B. Order part number AD642SH/883B.

*Specifications same as AD642J.
**Specifications same as AD642K.

Specifications and prices subject to change without notice.

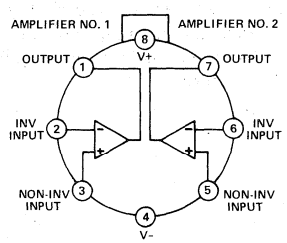
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TOP VIEW

ANALOG DEVICES

Lowest Cost High Accuracy IC Op Amps

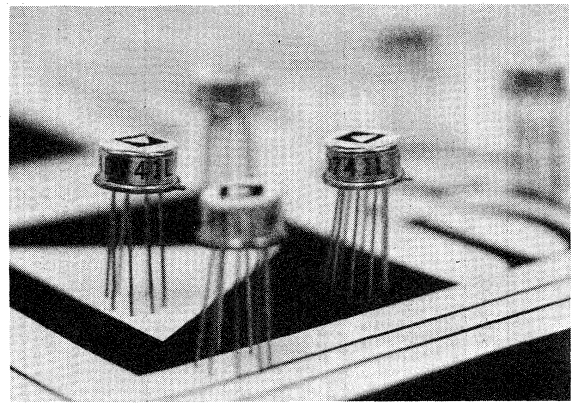
AD741 J,K,L,S

FEATURES

Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1kΩ load (J, S)
  T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

Low Cost



GENERAL DESCRIPTION

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the popular AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift, and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection (see Error Analysis). For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

GUARANTEED ACCURACY

The vastly improved performance of the AD741J, AD741K, AD741L and AD741S provides the user with an ideal choice when precision is needed and economy is a necessity. An error budget is calculated for all versions of the AD741 (see Table 1); it is obvious that these selected versions offer substantial improvements over the industry-standard AD741C and AD741. A typical circuit configuration (see Figure 1) is assumed, and the various errors are computed using maximum values over the full operating temperature range of the devices. *The results indicate a factor of 8 improvement in accuracy of the AD741L over the AD741C, a factor of 5 improvement using the AD741K, and a factor of 2.5 improvement using the AD741J. The AD741S, similarly, achieves a factor of 3.5 improvement over the standard AD741.* Note that the total error has been determined as a sum of component errors, while in actuality, the total error will be much less. Also, while the circuit used for the error analysis is only one of a multitude of possible applications, it effectively demonstrates the great improvement in overall 741 accuracy achievable at relatively low cost with the AD741J, K, L or S.

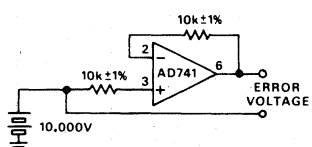


Figure 1. Error Budget Analysis Circuit

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

MODEL	AD741J	AD741K	AD741L	AD741S
OPEN LOOP GAIN				
R_L = 1kΩ, V_O = ±10V	50,000 min (200,000 typ)			*
R_L = 2kΩ, V_O = ±10V		50,000 min (200,000 typ)	50,000 min (200,000 typ)	
Over Temp Range, T_{min} to T_{max}, same loads as above	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 1kΩ, T_{min} to T_{max}	±10V min (±13V typ)			*
Voltage @ R_L = 2kΩ, T_{min} to T_{max}		±10V min (±13V typ)	±10V min (±13V typ)	
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1MHz	*	*	*
Full Power Response	10kHz	*	*	*
Slew Rate, Unity Gain	0.5V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial, $R_S \leq$ 10kΩ (adjustable to zero)	3mV max (1mV typ)	2mV max (0.5mV typ)	0.5mV max (0.2mV typ)	2mV max (1mV typ)
T_{min} to T_{max}	4mV max	3mV max	1mV max	*
Avg vs Temperature (untrimmed)	20μV/°C max	15μV/°C max (6μV/°C typ)	5μV/°C max (2μV/°C typ)	15μV/°C max (6μV/°C typ)
vs Supply, T_{min} to T_{max}	100μV/V max (30μV/V typ)	15μV/V max (5μV/V typ)	15μV/V max (5μV/V typ)	*
INPUT OFFSET CURRENT				
Initial	50nA max (5nA typ)	10nA max (2nA typ)	5nA max (2nA typ)	10nA max (2nA typ)
T_{min} to T_{max}	100nA max	15nA max	10nA max	25nA max
Avg vs Temperature	0.1nA/°C	0.2nA/°C max (0.02nA/°C typ)	0.1nA/°C max (0.02nA/°C typ)	0.25nA/°C max (0.1nA/°C typ)
INPUT BIAS CURRENT				
Initial	200nA max (40nA typ)	75nA max (30nA typ)	50nA max (30nA typ)	75nA max (30nA typ)
T_{min} to T_{max}	400nA max	120nA max	100nA max	250nA max
Avg vs Temperature	0.6nA/°C	1.5nA/°C max (0.6nA/°C typ)	1nA/°C max (0.6nA/°C typ)	2nA/°C max (0.6nA/°C typ)
INPUT IMPEDANCE				
Differential	1MΩ	2MΩ	2MΩ	2MΩ
INPUT VOLTAGE RANGE (Note 1)				
Differential, max safe	±30V	*	*	*
Common Mode, max safe	±15V	*	*	*
Common Mode Rejection, $R_S \leq$ 10kΩ, T_{min} to T_{max}, V_{in}= ±12V	80dB min (90dB typ)	90dB min (100dB typ)	90dB min (100dB typ)	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	±(5 to 22)V	±(5 to 22)V	±(5 to 22)V
Current, Quiescent	3.3mA max (2.0mA typ)	2.8mA max (1.7mA typ)	2.8mA max (1.7mA typ)	2.8mA max (2.0mA typ)
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

*Specifications same as AD741J.

Specifications subject to change without notice.

PARAMETER	AD741C SPEC (0 to +70°C)	AD741C ERROR	AD741J SPEC (0 to +70°C)	AD741J ERROR	AD741K SPEC (0 to +70°C)	AD741K ERROR	AD741L SPEC (0 to +70°C)	AD741L ERROR	AD741 SPEC (−55°C to +125°C)	AD741 ERROR	AD741S SPEC (−55°C to +125°C)	AD741S ERROR
Gain *(Error = 10V$_{in}$/G)*	15,000	660μV	25,000[1]	400μV	25,000	400μV	25,000	400μV	25,000	400μV	25,000[1]	400μV
I_b *(Error = I_b x resistor mismatch)*	800nA	160μV	400nA	80μV	120nA	24μV	100nA	20μV	1500nA	300μV	250nA	50μV
I_{os} *(Error = I_{os} x 10kΩ)*	300nA	3000μV	100nA	1000μV	15nA	150μV	10nA	100μV	500nA	5000μV	25nA	250μV
$\Delta V_{os}/\Delta T$ *(Error = $\Delta V_{os}/\Delta T$ x ΔT)*	25μV/°C[2]	1125μV	20μV/°C	900μV	15μV/°C	675μV	5μV/°C	225μV	25μV/°C[2]	2500μV	15μV/°C	1500μV
CMRR *(Error = 10V/CMRR)*	70dB	3300μV	80dB	1000μV	90dB	330μV	90dB	330μV	70dB	3300μV	80dB	1000μV
PSRR *(assume a ±5% power supply variation)*	150μV/V	450μV	100μV/V	300μV	15μV/V	45μV	15μV/V	45μV	150μV/V	450μV	100μV/V	300μV
TOTAL		8.7mV		3.7mV		1.6mV		1.1mV		12.0mV		3.5mV

[1] AD741J and AD741S...Open Loop Gain is guaranteed with a 1kΩ load.
[2] AD741C and AD741...$\Delta V_{os}/\Delta T$ is not guaranteed (for complete specifications, contact the factory for data sheet).

Table 1. Error Budget Analysis

INPUT CHARACTERISTICS

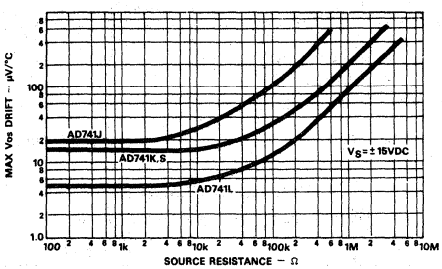


Figure 2. Max Equivalent Input Offset Drift vs. Source Resistance

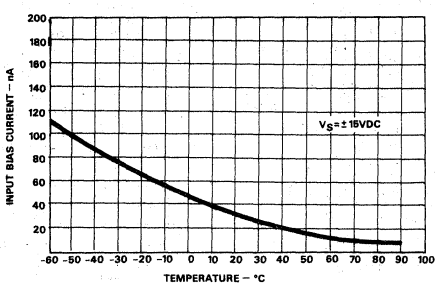


Figure 3. Input Bias Current vs. Temperature

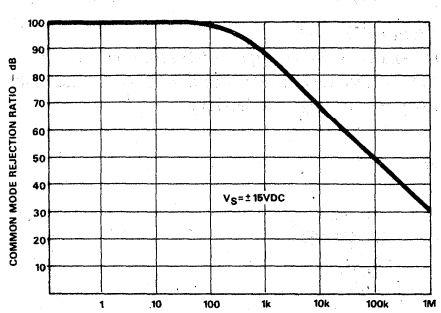


Figure 4. Common Mode Rejection vs. Frequency

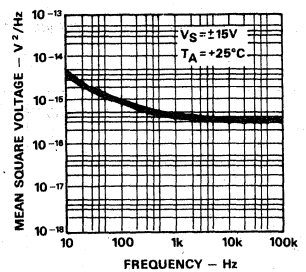


Figure 5. Input Noise Voltage vs. Frequency

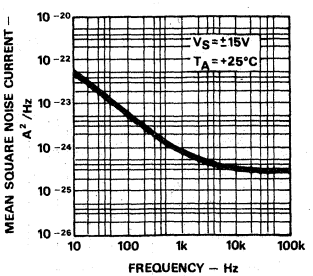


Figure 6. Input Noise Current vs. Frequency

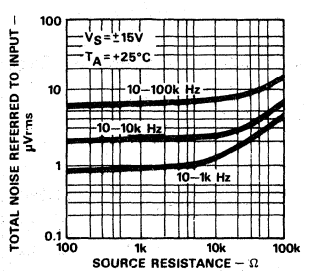


Figure 7. Broadband Noise vs. Source Resistance

OUTPUT CHARACTERISTICS

The AD741J and AD741S are specially selected for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C. The AD741K and AD741L are guaranteed with the standard 2kΩ load.

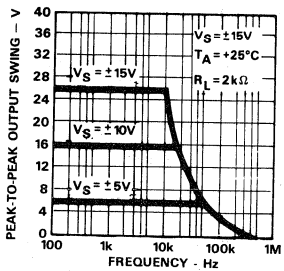


Figure 8. Output Voltage Swing vs. Frequency

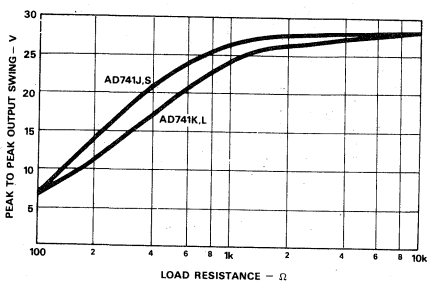


Figure 9. Output Voltage Swing vs. Load Resistance

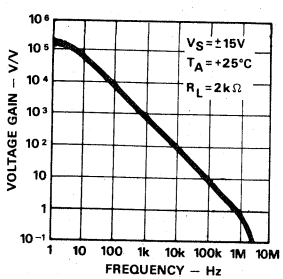
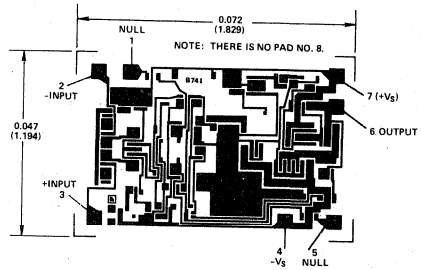


Figure 10. Open Loop Gain vs. Frequency

BONDING DIAGRAM

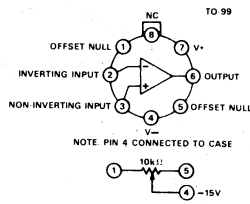
All versions of the AD741 are available in chip form. See the Analog Devices chip catalog for further information.



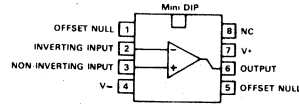
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

CONNECTION DIAGRAMS

(Top View)



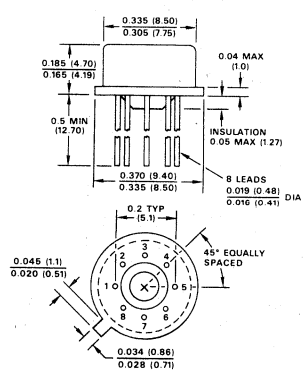
(H package)



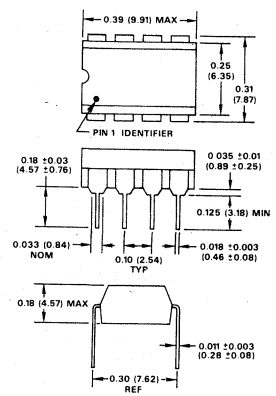
(N package)

PHYSICAL DIMENSIONS

Dimensions shown in inches and (mm).



TO-99 (H)



MINI-DIP (N)

MIL-STANDARD-883

The AD741S is available with 100% screening to MIL-STD-883, Method 5004, Class A, B, or C. Consult the factory for pricing and delivery.

ORDERING GUIDE

MODEL	TEMP. RANGE	ORDER NUMBER
AD741J	0°C to +70°C	AD741J*
AD741K	0°C to +70°C	AD741K*
AD741L	0°C to +70°C	AD741L*
AD741S	−55°C to +125°C	AD741SH

*Add Package Type Letter; H = TO-99, N = Mini-DIP.

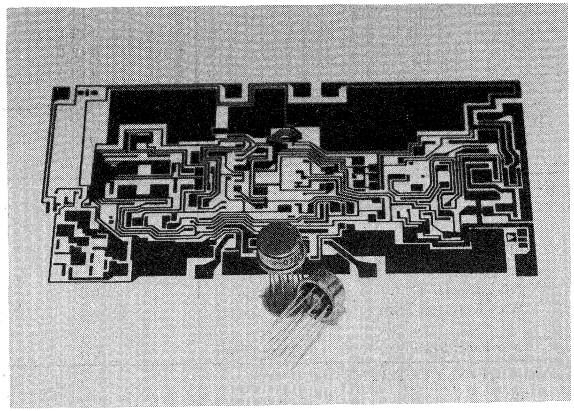
ANALOG DEVICES

Ultra-Low Offset Voltage Op Amp

AD OP-07

FEATURES

- Ten Times More Gain Than Other OP-07 Devices (3.0M min)
- Ultra-Low Offset Voltage: 10μV
- Ultra-Low Offset Voltage Drift: 0.2μV/°C
- Ultra-Stable vs. Time: 0.2μV/month
- Ultra-Low Noise: 0.35μV p-p
- No External Components Required
- Monolithic Construction
- High Common Mode Input Range: ±14.0V
- Wide Power Supply Voltage Range: ±3V to ±18V
- Fits 725, 108A/308A, 741 Sockets



PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed loop gain applications. Input offset voltages as low as 10μV, bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C and long-term stability of 0.2μV/month eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common mode input voltage range (±14V) high common mode rejection ratio (up to 126dB) and high differential input impedance (50MΩ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. Full processing to the requirements of MIL-STD-883, Class B, is available on the AD OP-07 and AD OP-07A. All devices are packaged in TO-99 hermetically-sealed metal cans.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultra-low offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultra-low input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-07EH			AD OP-07CH			AD OP-07DH		
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
OPEN LOOP GAIN	A_{VO}	2,000	5,000		1,200	4,000		1,200	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	±12.5	±13.0		±12.0	±13.0		±12.0	±13.0	
		±12.0	±12.8		±11.5	±12.8		±11.5	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	75		60	150		60	150
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift							(Note 3)			(Note 3)
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6 (Note 3)		0.7	2.5 (Note 3)
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	3.8		0.8	6.0		0.8	6.0
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8 (Note 3)	35		12 (Note 3)	50		12 (Note 3)	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	±4.0		±1.8	±7.0		±2.0	±12
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13 (Note 3)	35		18 (Note 3)	50		18 (Note 3)	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{IN} CM		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	±13.0	±14.0		±13.0	±14.0		±13.0	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common Mode Rejection Ratio	CMRR	106	123		100	120		94	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	4.0		3.5	5.0		3.5	5.0
Power Consumption	P_D		90	120		105	150		105	150
			6.0	8.4		6.0	8.4		6.0	8.4
Rejection Ratio	PSRR	94	107		90	104		90	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70

NOTES:

1) Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, AD OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.
2) Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — Parameter is not 100% tested; 90% of units meet this specification.
3) Parameter is not 100% tested; 90% of units meet this specification.
4) The AD OP-07A and AD OP-07 are available fully processed to MIL-STD-883, Class B. Order AD OP-07-AH-883B or AD OP-07-H-883B.

Specifications subject to change without notice.

AD OP-07AH (AD OP-07-AH-883B)[4]			AD OP-07H (AD OP-07-H-883B)[4]				
MIN	TYP	MAX	MIN	TYP	MAX	TEST CONDITIONS	UNITS
3,000	5,000		2,000	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		1,500	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		±12.5	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		±12.0	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		±10.5	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		±12.0	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	25		30	75	Note 1	μV
	25	60		60	200	Note 1, T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	0.6		0.3	1.3	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 2	μV/Month
	0.3	2.0		0.4	2.8		nA
	0.8	4.0		1.2	5.6	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	±2.0		±1.0	±3.0		nA
	±1.0	±4.0		±2.0	±6.0	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz, Note 3	μV p-p
	10.3	18.0		10.3	18.0	f_O = 10Hz, Note 3	nV/√Hz
	10.0	13.0		10.0	13.0	f_O = 100Hz, Note 3	nV/√Hz
	9.6	11.0		9.6	11.0	f_O = 1kHz, Note 3	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz, Note 3	pA p-p
	0.32	0.80		0.32	0.80	f_O = 10Hz, Note 3	pA/√Hz
	0.14	0.23		0.14	0.23	f_O = 100Hz, Note 3	pA/√Hz
	0.12	0.17		0.12	0.17	f_O = 1kHz, Note 3	pA/√Hz
±13.0	±14.0		±13.0	±14.0			V
±13.0	±13.5		±13.0	±13.5		T_{min} to T_{max}	V
110	126		110	126		V_{CM} = ±CMVR	dB
106	123		106	123		V_{CM} = ±CMVR, T_{min} to T_{max}	dB
	3.0	4.0		3.0	4.0	$V_S = \pm 15V$	mA
	90	120		90	120	$V_S = \pm 15V$	mW
	6.0	8.4		6.0	8.4	$V_S = \pm 3V$	mW
100	110		100	110		$V_S = \pm 3V$ to $\pm 18V$	dB
94	106		94	106		$V_S = \pm 3V$ to $\pm 18V$, T_{min} to T_{max}	dB
-55		+125	-55		+125		°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-07A, OP-07	-55°C to +125°C
OP-07E, OP-07C, OP-07D	0 to +70°C
Lead Temperature Range (Soldering, 60sec)	300°C

NOTES:

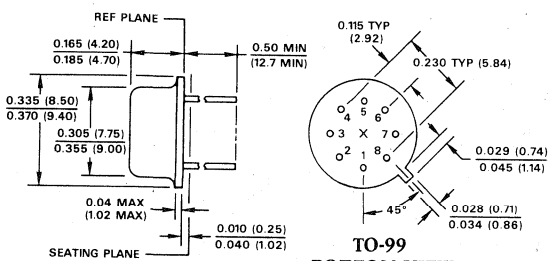
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

OUTLINE DIMENSIONS

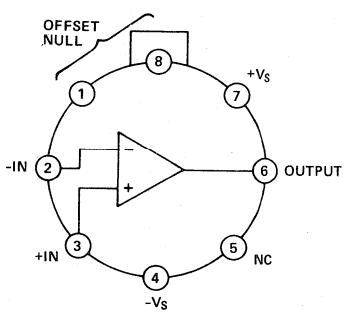
Dimensions shown in inches and (mm).

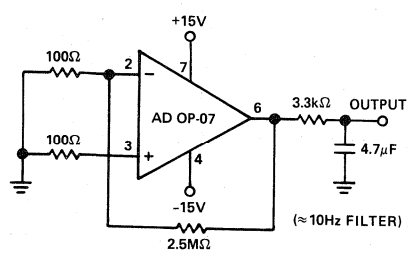


TO-99
BOTTOM VIEW

H-PACKAGE

PIN CONFIGURATION
TOP VIEW





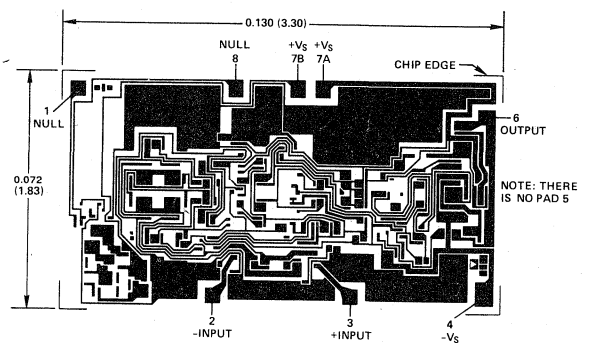
INPUT REFERRED NOISE = $\frac{V_O}{25{,}000} = \frac{5mV/cm}{25{,}000} = 200nV/cm$

SEE NOISE PHOTO-NEXT PAGE

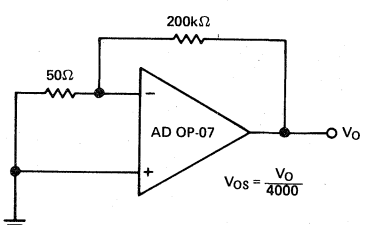
Low Frequency Noise Test Circuit

CHIP DIMENSIONS AND BONDING DIAGRAM

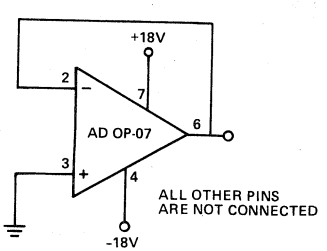
Dimensions shown in inches and (mm).



The AD OP-07 is available in wafer-trimmed chip form for precision hybrids. Consult the factory directly for details.



Offset Voltage Test Circuit



Burn-In Circuit

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/201A/301A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

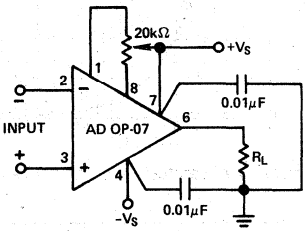


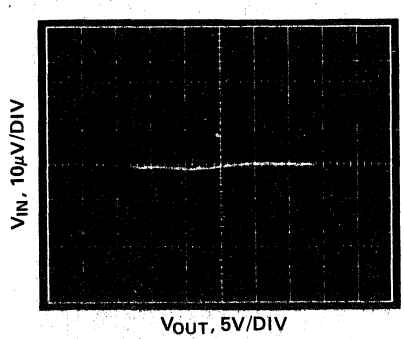
Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

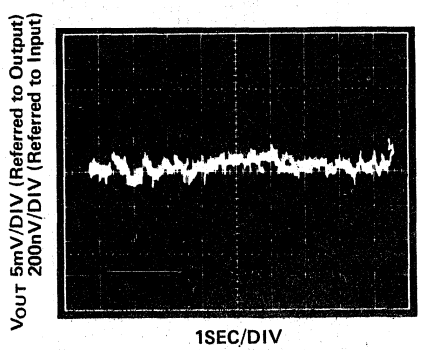
Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

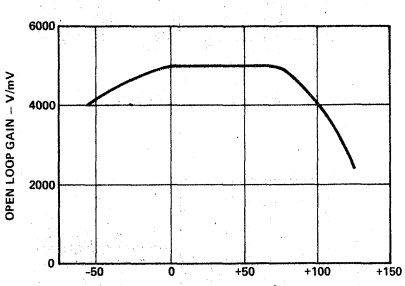
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



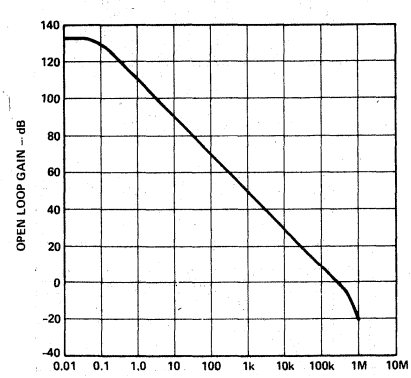
AD OP-07 Open Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

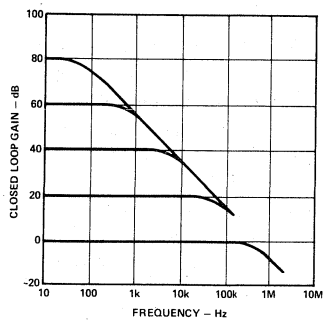


Open Loop Gain vs. Temperature

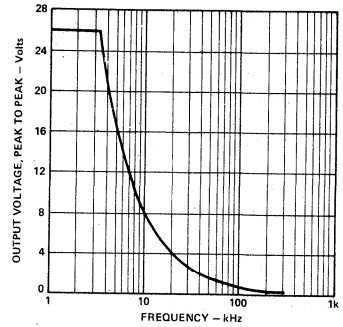


Open Loop Frequency Response

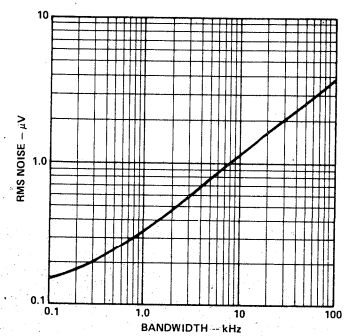
Typical Performance Curves



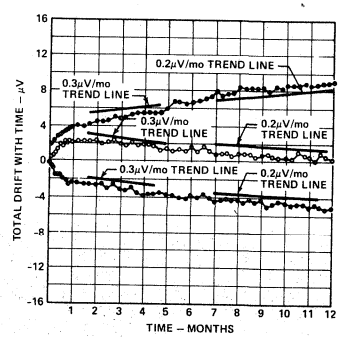
Closed Loop Response for Various Gain Configurations



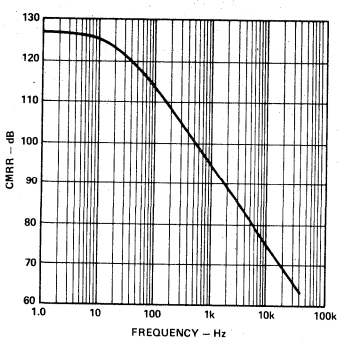
Maximum Undistorted Output vs. Frequency



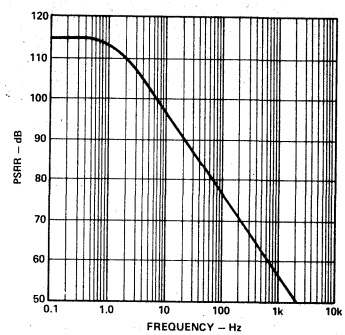
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



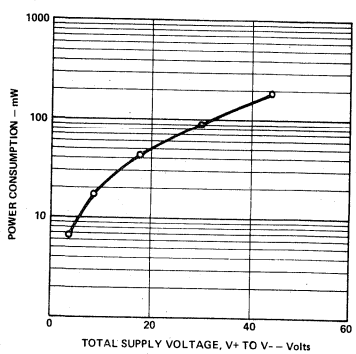
Offset Voltage Stability vs. Time



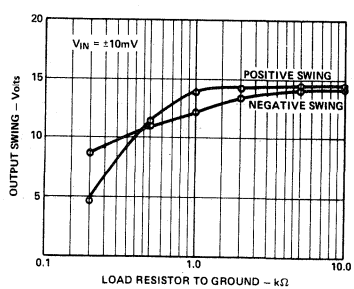
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



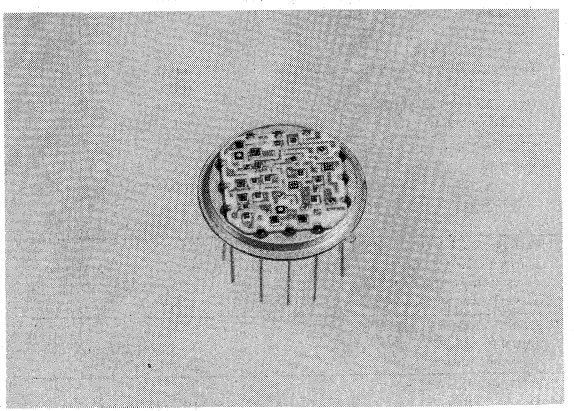
Output Voltage vs. Load Resistance

Fast Settling Video Operational Amplifier

HOS-050, 050A

FEATURES
- 80ns Settling to 0.1%; 200ns Settling Time to 0.01%
- 100MHz Gain Bandwidth Product
- 55MHz 3dB Bandwidth
- 100mA Output Capability @ ±10V
- Maximum Tempco of 35μV/°C (HOS-050A)

APPLICATIONS
- A to D Input Amplifier
- D to A Current Converter
- Video Pulse Amplifier
- CRT Deflection Amplifier
- Wideband Current Booster



GENERAL DESCRIPTION

The HOS-050 and HOS-050A op amps are very high speed wideband operational amplifiers specially designed to complement the Analog Devices' line of high speed data acquisition products. Both models feature a 100MHz gain bandwidth product, slew rate of 300μV/μs and settling time of 80ns to 0.1%.

Model HOS-050 has an input offset voltage of 25mV, typical; HOS-050A has an offset voltage of 10mV, typical. Both models have a rated output of ±100mA, min, and an exceptionally low input voltage noise of only 7μV rms, dc to 2MHz, making them ideally suited for a broad range of video applications.

D/A's AND FAST SETTLING

It used to be sufficient to specify op amps according to their slewing rates, bandwidth, and drive capability. Settling times were unimportant until the recent increase in the use of high speed video D/A converters. Since the conversion speed of D/A's can be limited by the settling time of the output amplifier, it has become essential to choose an op amp which will have a settling time which is compatible to the D/A.

Settling time is determined not only by the slew rate of an op amp, but also by the amount of overshoot and ringing experienced at the tail end of a step function change. This is largely due to the bandwidth limitations experienced in many op amps operating with closed loop gains greater than one. The HOS series avoids this problem since its 100MHz gain bandwidth product is more than large enough for most video applications.

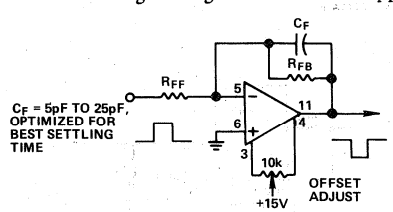


Figure 1. Settling Time Measurement

For additional information on fast amplifiers, see Analog Devices' model 48, 50, 51 data sheets.

For example, at a gain of 1 in the inverting mode, it has a bandwidth of 55MHz and a settling time of 80ns to 0.1% for a 5-volt input step voltage.

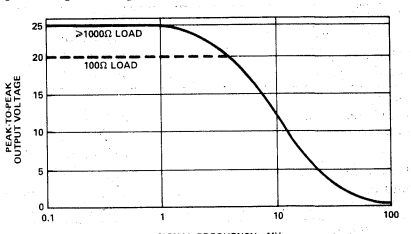


Figure 2. Output Voltage vs Signal Frequency

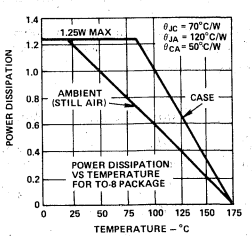


Figure 3. Power Dissipation vs Temperature

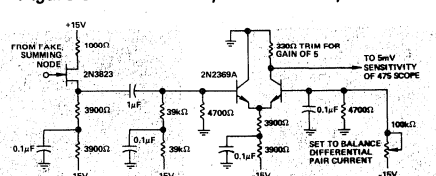


Figure 4. Settling Time Test Circuit for 0.01% Settling

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Model	HOS-050 (HOS-050A)
OPEN LOOP GAIN, DC	
Load = 100Ω	100dB min
RATED OUTPUT[1]	
Voltage, $R_L \geq 100\Omega$	±10V min
Current	±100mA min
FREQUENCY RESPONSE (Circuit of Figure 1)	
Gain Bandwidth Product, $R_{FF} = R_{FB} = 500\Omega$	100MHz
Small Signal Bandwidth, -3dB (See Table 1)	55MHz
Full Power (See Figure 2 for 3% distortion levels)	4MHz
Harmonic Distortion (See Table 2)	-60dB
Slew Rate	300V/μs
Overload Recovery (50% overdrive)	400ns
Rolloff Characteristic	6dB/Octave
SETTLING TIME to 0.1% Full Scale (See Table 3)	
Inverting A = 1, $R_{FF} = R_{FB} = 500\Omega$	
V_{OUT} = ±5V/±2.5V	100ns/80ns
Noninverting A = 2, $R_{FF} = 500\Omega$, $R_{FB} = 500\Omega$	
V_{OUT} = ±5V/±2.5V	200ns/135ns
INPUT OFFSET VOLTAGE	
Initial @ +25°C (adjustable to zero, see Figure 1)	35mV max (15mV max)
vs. Temperature μV/°C	150 max (35 max)
vs. Power Supply Voltage	±75μV/%
INPUT BIAS CURRENT	
Initial @ +25 °C	1nA typ, 2nA max
vs. Temperature	doubles/+10°C
INPUT IMPEDANCE	
Differential	$10^{10}\Omega \| 5pF$
Common Mode	$10^{10}\Omega \| 5pF$
INPUT NOISE ($R_{FF} = 100\Omega$, $R_{FB} = 1000\Omega$)	
dc to 100kHz	5μV rms
dc to 2MHz	7μV rms
INPUT VOLTAGE RANGE	
Common Mode Voltage	±10V min
Max Safe Differential Voltage	±Supply Voltage
Common Mode Rejection	70dB
POWER SUPPLY	
Voltage, Rated Performance	±15V dc
Voltage, Operating Range	±12V to ±18V (Absolute max)
Current, Quiescent max/typ	±25/±20mA
Power Consumption	0.6W (quiescent)
Allowable Power Dissipation (See Figure 3)	1.25W max
TEMPERATURE RANGE[2]	
Operating (See Figure 3 for derating)	-55°C to +125°C (case)
Storage	-65°C to +150°C

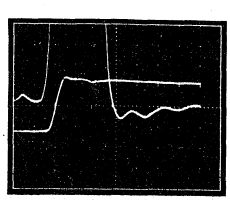
NOTE

[1] Output is short circuit protected for momentary shorts of 100ms or less.
[2] With case temperature of +125°C, max junction temperature is +175°C.

Specifications subject to change without notice.

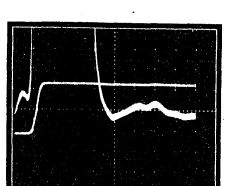
R_{FF}	R_{FB}	Gain	Bandwidth
500Ω	500Ω	1	55MHz
1000Ω	1000Ω	1	35MHz
500Ω	1000Ω	2	35MHz
250Ω	1000Ω	4	30MHz

Table 1.



5mV/DIV, 20ns/DIV

0.1% Settling, 5V Step



0.4mV/DIV, 50ns/DIV

0.01% Settling, 5V Step

HARMONIC DISTORTION — INVERTING MODE

The following data are useful for video applications where driving a 50Ω or a 75Ω coax cable is desirable. It is assumed that the cable is source and load terminated. Therefore, a 50Ω cable represents a 100Ω load to the amplifier, and a 75Ω cable represents a 150Ω load.

Case I DC load = 100Ω; Signal = 4MHz

Signal Output	Harmonics
2V p-p	60dB down
4V p-p	55dB down

Case II DC load = 150Ω; Signal = 4MHz

Signal Output	Harmonics
2V p-p	65dB down
4V p-p	60dB down

Case III DC load = 100Ω; Signal = 5MHz

Signal Output	Harmonics
2V p-p	60dB down
4V p-p	55dB down

Case IV DC load = 150Ω; Signal = 5MHz

Signal Output	Harmonics
2V p-p	60dB down
4V p-p	55dB down

Case V DC load = 1000Ω; Signal = 4MHz

Signal Output	Harmonics
2V p-p	70dB down
4V p-p	60dB down

Case VI DC load = 1000Ω; Signal = 5MHz

Signal Output	Harmonics
2V p-p	65dB down
4V p-p	55dB down

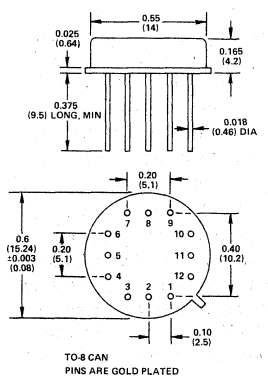
Table 2. Harmonic Distortion — Inverting Mode

P-P Output Voltage	to 1% FS	to 0.1% FS	to 0.05% FS	to 0.01% FS
10V	65ns	100ns	120ns	300ns
5V	50ns	80ns	90ns	200ns

Table 3. Settling Time — Inverting Mode (Measured with Gain of 1; $R_{FF}=R_{FB}=500\Omega$)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	-INPUT
6	+INPUT
7	NC
8	GROUND
9	-V
10	-V
11	OUTPUT
12	+V

*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. SEE FIGURE 1.

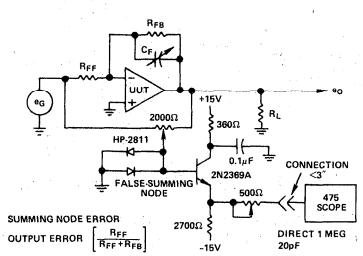


Figure 5. Settling Time Test Circuit for 0.1% Settling

ANALOG DEVICES

Fast Settling Differential FET Op Amp

MODEL 48

FEATURES
- Fast Settling: 500ns max
- Fast Slew Rate: 125V/μs
- Wide Bandwidth: 15MHz
- High Common Mode Rejection: 83dB min
- High Gain: A_0 = 100,000
- Low Drift: 15μV/°C (48K)

APPLICATIONS
- Stable Unity Gain Buffer to 15MHz
- Sample Hold Circuits
- Ultra Fast Current Source
- High Speed Integrator

GENERAL DESCRIPTION

The model 48 is an ultra fast, FET input differential op amp that should be considered where settling time, slew rate, bandwidth and good thermal stability are critical requirements. Characterized by a -6dB/octave rolloff to frequencies exceeding 15MHz, the model 48's dynamic response consists of a guaranteed slew rate of 110V/μs and settles to 0.01% in 500μs, max. For dc performance, the model 48 has open loop gain of 100,000 min, and common mode rejection at a full ±10V of 15,000 min (83dB). Maximum offset drifts of 50μV/°C (48J) and 15μV/°C (48K) complete the performance profile, proving this amplifier to be an excellent choice for both high speed analog and digital applications.

Packaged in a small 1 1/8" X 1 1/8" X 0.4" case, the model 48 requires little space, runs cool (9mA of quiescent current) and is competitively priced in unit quantities (48J).

FAST SETTLING APPLICATIONS

A/D and D/A converters, multiplexers and other sampling circuits require fast settling output amplifiers. Since system conversion speed is most often dictated by the settling time of the amplifier, model 48, with a guaranteed 500ns settling time to 0.01%, makes it an excellent choice.

D/A CURRENT TO VOLTAGE CONVERTER

Current to voltage converters for D/A applications place severe requirements on the op amp's slew rate, open loop gain and offset drift. Model 48 meets these requirements with smooth settling to 0.01% in 500ns, open loop gain of 100,000 and offset drift of 15μV/°C (48K).

SETTLING TIME VS SIGNAL LEVEL

Shown in Figure 1 is a graph of settling time for various step inputs and the test circuit used to obtain this data. Settling time varies in a nonlinear fashion with input level, error band, and polarity of input step. The worst case settling is that which is specified at ±10V.

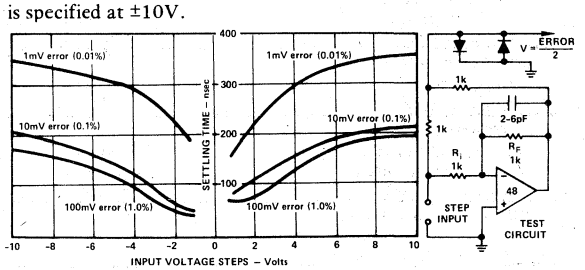


Figure 1. Settling Time for Various Input Steps

SETTLING TIME VS R_F AND C_L

Settling time of an amplifier is also influenced by the value of the gain resistors selected and the amount of capacitive loading. Model 48 is stable even when driving cap loads, C_L, up to 1000pF, but to obtain optimum settling time this value of capacitance should be held as low as possible. The effects of C_L and R_F on settling time are shown in Table 1.

TABLE 1. 0.1% SETTLING TIME VS R_F, C_L

$R_F = R_i$ (Ω)	t_s (ns)	Cap Load (pF)
1k	350	6
10k	420	6
50k	560	6
2k	320	100
2k	420	200
2k	1100	500

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	48J (K)
OPEN LOOP GAIN	
DC Load 500 ohms	100,000 min
RATED OUTPUT[1]	
Voltage, 500 ohm Load	±10V min
Current	±20mA min
Maximum Load Capacitance	1000pF
FREQUENCY RESPONSE	
Unity Gain	15MHz
Full Power	1.5MHz min
Slew Rate, Non-Inverting	90V/μs min
Slew Rate, Inverting	110V/μs min
Overload Recovery	0.5μs
SETTLING TIME, UNITY GAIN, 0.01%	
Non-Inverting	500ns max
Inverting, $R_f = R_i = 2k\Omega$	500ns max
SETTLING TIME, UNITY GAIN, 0.1%	
Inverting, $Z_f = 1k\Omega \| 3.3pF$	300ns max
Inverting, $Z_f = 1k\Omega \| 3.3pF$	250ns
Noninverting, $Z_f = 1k\Omega \| 3.3pF$	250ns
INPUT OFFSET VOLTAGE	
Initial @ +25°C	Adjust to Zero
Trim Potentiometer	1k ohm
With 499 ohm Fixed Trim Resistor	±2mV
vs. Temp (0 to +70°C)	±50μV/°C max (±15μV/°C max)
vs. Time	250μV/month
vs. Supply	±15μV/%
INPUT BIAS CURRENT	
Initial @ +25°C	-50pA max (-25pA max)
At +85°C	2nA (1nA)
INPUT IMPEDANCE	
Differential	$10^{11}\Omega \| 3.5pF$
Common Mode	$10^{11}\Omega \| 3.5pF$
INPUT NOISE	
Voltage, 0.01 to 1Hz	2μV p-p
5Hz to 50kHz	3μV rms
Current, 0.01 to 1Hz	0.1pA p-p
INPUT VOLTAGE RANGE	
Differential	±15V
Common Mode, 1% Error	±11V
COMMON MODE REJECTION	
±10V dc	15,000 min
±10V dc	30,000
POWER SUPPLY[2]	
Voltage, Rated Specifications	±15V
Operating	±(12 to 18)V
Current, Quiescent	9mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Weight	15 grams
Trimpot	1kΩ, ADI #79PR1k
Mating Socket	AC1010

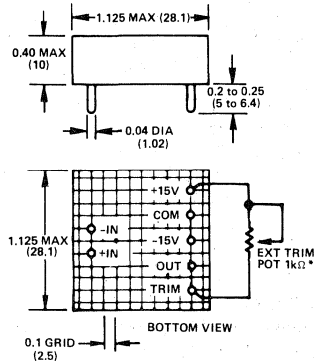
[1] Short circuit protected to ground.

[2] Recommend ADI model 904, ±15V @ 50mA.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

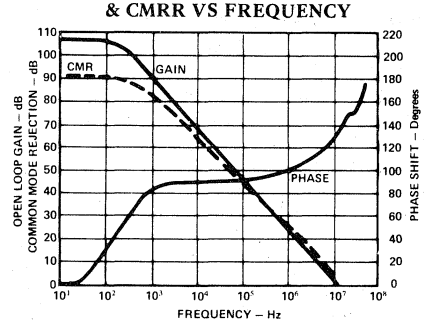
Dimensions shown in inches and (mm).



Mating Socket AC1010

*Analog Devices Model 79PR1k

OPEN LOOP GAIN, PHASE & CMRR VS FREQUENCY



KEY SPECS FOR ADI FAST SETTLING FET OP AMPS

Model	48J	46J	44J	45J	
Settling to 0.01% (max)	500	300	1000	1000	ns
Slew Rate	125	1000	75	75	V/μs
Bandwidth	15	40	10	10	MHz
Output @ 10V	20	100	20	20	mA
Drift	50	75	50	50	μV°C
CMR min @ 10V	83	72	80	74	dB
Gain (min)	100k	25k	100k	50k	

CONSIDERATIONS FOR HIGH SPEED APPLICATIONS

Components: Use gain resistors of 2kΩ or less to reduce effects of stray capacitance. Use metal film resistors for low capacitance and inductance.

Wiring: Run separate signal and power grounds terminating at a common point at the power supply common (preferably). Keep all leads as short as possible to reduce noise pickup and inductive effects.

Fast Settling, Wideband, 100mA Output, FET Amplifiers

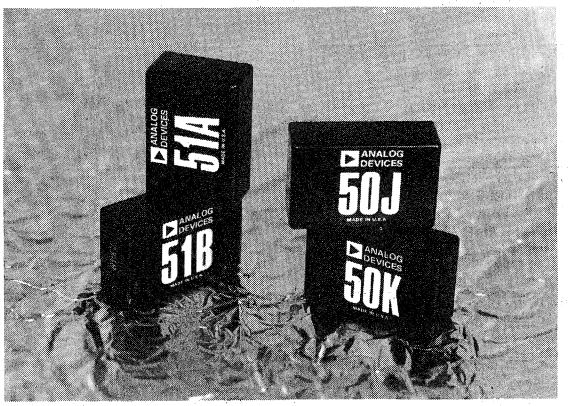
MODELS 50 & 51

FEATURES

Fast Settling: 200ns max, 0.05% (50J/K)
100ns max, 0.1% (50J/K)
100mA Output: dc to 8MHz (50J/K)
dc to 6MHz (51A/B)
All Hermetically Sealed Semiconductors (51A/B)
-55°C to +125°C Temperature Range (51A/B)
100MHz Gain Bandwidth (50J/K)

APPLICATIONS

A to D Input Amplifier
D to A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster



GENERAL DESCRIPTION

Models 50 and 51 are ultra fast, wideband differential FET amplifiers, designed for applications requiring fast settling time with high output current in closed loop gain configurations of 2 or greater. Model 50 offers guaranteed settling time of 100ns maximum to ±0.1% accuracy and 200ns maximum to ±0.05% accuracy. Model 51 features all hermetically sealed semiconductors for greater reliability and wide operating temperature range (-55°C to +125°C) with guaranteed settling times of 140ns maximum to ±0.1% and 250ns maximum to ±0.05%.

Model 50 is available in two input voltage drift selections, model 50J is ±50μV/°C max, model 50K is ±15μV/°C max. Other outstanding features of models 50J/K are 100MHz gain bandwidth product, slew rate of 500V/μs and output current of ±100mA from dc to 8MHz.

Model 51 is also available in two input voltage drift selections; model 51A is ±50μV/°C max, model 51B is ±20μV/°C max. Models 51A/B offer 80MHz gain bandwidth product, slew rate of 400V/μs and ±100mA output current from dc to 6MHz. Both models 50 and 51 offer significant improvement over previous designs with lower input voltage noise (6μV rms, 5Hz to 2MHz bandwidth), particularly important in display system D/A converter applications.

FAST SETTLING APPLICATIONS

D/A converters require fast settling output amplifiers since conversion speed is often dictated by the settling time of the amplifier. Models 50 and 51 offer fast settling time performance at closed loop gains from 2 to 6. This characteristic is extremely important for D/A applications requiring fast current to voltage conversion from less than ideal current sources.

The circuit shown in Figure 1 is that of a typical current to voltage converter. The output of the D/A converter is often considered an ideal current source ($R_{out} = \infty$) which is converted to a voltage by the amplifiers' feedback resistor. Although it may appear that in this application the amplifier is being operated in a closed loop gain of 1, a closer look at the D/A's specifications may show an output impedance of 800 to 2500 ohms. For this condition, the amplifier is operated in a closed loop gain of 2 to 6. This is then the range of gains over which settling time is important.

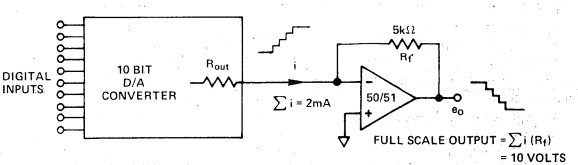


Figure 1. High Speed Current to Voltage Buffer

High speed amplifiers typically suffer significant degradation in settling time when operated in closed loop gains greater than unity. Model 50, with 100MHz gain bandwidth and model 51 with 80MHz gain bandwidth achieve fast settling time since they are far from the point of bandwidth limitations. For example, at a gain of 4, model 50 has a bandwidth of 20MHz, which represents a time constant of 8ns. For 0.1% settling, the bandwidth limitation is 6.9 time constants or approximately 55ns.

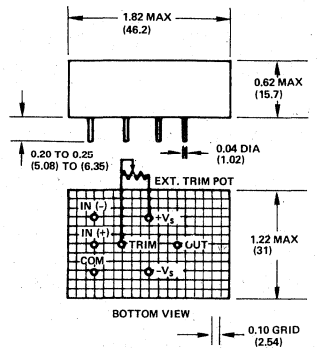
SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	50J	50K	51A	51B
OPEN LOOP GAIN				
DC, Load = 100 ohm	88dB min	*	94dB min	**
DC, Load = 2k ohm	94dB min	*	97dB min	**
RATED OUTPUT[1]				
Voltage, $R_L \geq 100\Omega$	±10V min	*	*	*
Current	±100mA min	*	*	*
Impedance, Open Loop dc	200Ω	*	*	*
Load Capacitance, max				
Inverting	100pF max	*	*	*
Noninverting	50pF max	*	*	*
FREQUENCY RESPONSE				
Small Signal, Unity Gain	70MHz	*	56MHz	**
Small Signal, -3dB, Unity Gain	100MHz	*	80MHz	**
Full Power	8MHz min	*	6MHz min	**
Slew Rate, Noninverting	400V/μs, min	*	300V/μs, min	**
Slew Rate, Inverting	500V/μs, min	*	400V/μs, min	**
Overload Recovery	200ns	*	*	*
SETTLING TIME				
Inverting, Gain = 2				
±0.1%, ±10 Volt Step	100ns max	*	140ns max	**
±0.05%, ±10 Volt Step	200ns max	*	250ns max	**
Noninverting, Gain = 2				
±0.1%, ±10 Volt Step	150ns max	*	200ns max	**
±0.05%, ±10 Volt Step	300ns max	*	400ns max	**
INPUT OFFSET VOLTAGE				
Initial, @ +25°C	Adjust to Zero	*	*	*
Trim Potentiometer[2]	1kΩ	*	*	*
With 499Ω Fixed Resistor	±3mV	*	*	*
vs. Temperature	±50μV/°C max	±15μV/°C max	±50μV/°C max	±20μV/°C max
vs. Supply Voltage	±15μV/%	*	*	*
vs. Time	±500μV/month	*	*	*
Warm up Drift, 20 Minutes	±2mV	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	0, 0-2nA max	*	*	*
vs. Temperature	Double/+10°C	*	*	*
vs. Supply Voltage	10pA/%	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±100pA	*	*	*
vs. Temperature	Double/+10°C	*	*	*
INPUT IMPEDANCE				
Differential	$10^{10}\Omega \| 3.5pF$	*	*	*
Common Mode	$10^{10}\Omega \| 3.5pF$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	5μV, p-p	*	*	*
5Hz to 2MHz	6μV, rms	*	*	*
Current, 0.1Hz to 10Hz	1pA, p-p	*	*	*
INPUT VOLTAGE RANGE				
Common Mode Voltage	±10V min	*	*	*
Max Safe Differential Voltage	$\pm V_S$	*	*	*
Common Mode Rejection, CMV = ±10V	60dB, min	*	*	*
Common Mode Rejection, CMV = ±5V	70dB, min	*	*	*
POWER SUPPLY				
Voltage, Rated Performance[3]	±15V dc	*	*	*
Voltage, Operating	±(12 to 18)V dc	*	*	*
Current, Quiescent	±40mA	*	*	*
TEMPERATURE RANGE				
Rated Specifications	0 to +70°C	*	-25°C to +85°C	**
Operating[4]	-25°C to +85°C	*	-55°C to +125°C	**
Storage	-55°C to +125°C	*	*	*
MECHANICAL				
Case Size, mm	1.8" x 1.2" x 0.6"	*	*	*
Weight, grams	31	*	*	*
Mating Socket	AC1034	*	*	*

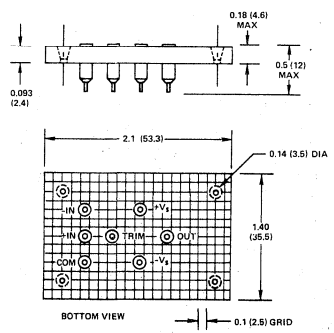
*Specifications same as Model 50J.
**Specifications same as Model 51A.
[1] Short circuit protected to ground.
[2] Analog Devices' part number 79PR1K.
[3] Recommended power supply ADI Model 920, ±15V @ 200mA.
[4] Models 51A and 51B have an operating temperature range of -55°C to +100°C when operating in the differential mode.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC1034



OTHER FAST AMPLIFIERS AVAILABLE

Models 44, 45 and 48, each available with two drift selections (J, K), offer fast settling of 1μs max (0.5μs, 48) to 0.01%. They provide ±10 volts output at 20mA with input drifts of 50μV/°C (J) and 15μV/°C (K) max. Unity gain response is 10MHz (15MHz, 48) with 1MHz (1.5MHz, 48) full power output.

ECONOMY – Select models 45J/K. Good performance for inverting or noninverting (±5V CMV) designs.

FOLLOWER – Select models 44J/K for guaranteed 80dB CMR (CMV ±10V). Excellent as buffer for A to D's, sample-hold multiplexer.

FAST SETTLING – Select models 48J & K for settling to 0.01% in 500ns - small package – 1" x 1".

Figure 2 illustrates 0.1% and 0.05% settling time performance achievable from models 50 and 51 over closed loop gains from 1 to 10. Both models offer dramatic improvement over previous designs.

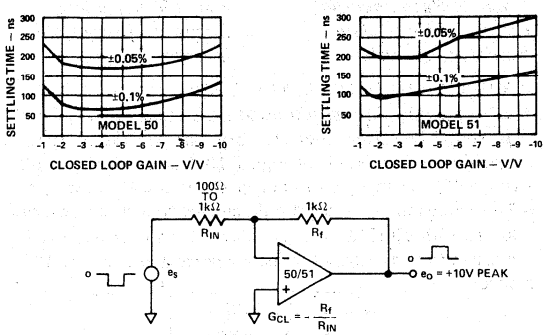


Figure 2. Settling Time versus Closed Loop Gain

SLEW RATE VS. CLOSED LOOP GAIN

Unlike most high speed amplifiers, models 50 and 51 do not require high input drive voltage to achieve fast slew rate and rise time. For small signals and closed loop gains of 2 or greater, models 50 and 51 can slew faster than amplifiers having slew rate specifications of 1000V/μs and greater. This is a consequence of the method used throughout industry to specify slew rate and the fact that slew rate is determined by the initial error signal at the summing junction and the transconductance of the amplifier. If either of these two factors is reduced, slew rate is reduced.

Figure 3 illustrates the higher slew rate sensitivity of models 50 and 51 by plotting slew rate versus initial error signal along with model 46, a popular 1000V/μs industry standard. These curves illustrate that for error signals of less than 2.5V, model 50 has a higher slew rate than model 46; for error signals less than 2V, model 51 has a higher slew rate compared to model 46.

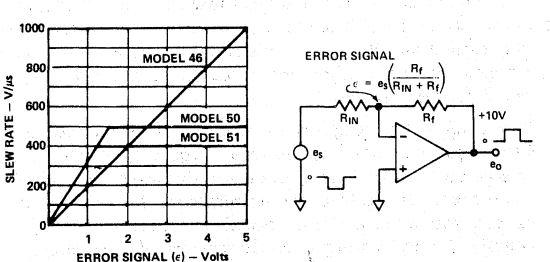


Figure 3. Slew Rate vs. Error Signal

As an example of the faster performance available from models 50/51, Figure 4 compares the response of model 50 and 46 to a 100ns pulse in an inverting, gain of 4 circuit. Model 50 is twice as fast as model 46 with a risetime (10%–90%) of 18ns compared to model 46's risetime of 38ns. Models 50 and 51 therefore, can be faster in many applications than model 46 and other fast amplifiers in the 1000V/μs category.

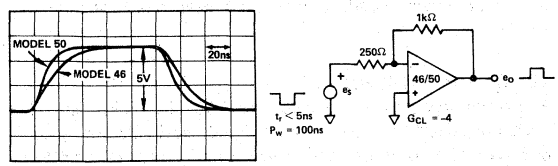


Figure 4. Pulse Response, Model 46/Model 50

SETTLING TIME VS. SIGNAL SWING

The curves in Figure 5 illustrate models 50/51 settling time error versus input signal level. These curves are useful as a design aid for bracketing settling time versus step input level. Settling time is defined as that time required for the output signal to settle within a specified error band about its final value in response to a perfect input step. During the settling time cycle, the output signal initially displays a propagation delay, a rise time, and a time period to settle into the specified error band.

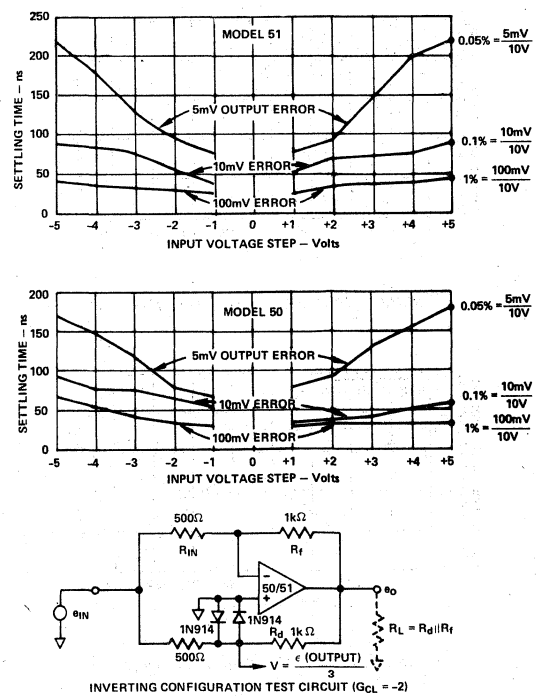


Figure 5. Settling Time Error vs. Input Level

Percentage settling time error is calculated by forming the ratio of output error to output voltage step. Shown in Figure 5 are 1%, 0.1% and 0.05% error points for a ±10V output step. The settling times for these errors are read off the vertical axis.

Because of nonlinear factors, extrapolation of settling times from one set of conditions to another becomes very difficult, if not impossible. This point becomes very apparent, in Figure 5, when reviewing settling time as a function of input signal swing.

FREQUENCY RESPONSE

The frequency performance of model 50, shown in Figure 6, is characterized by a useful small signal bandwidth of up to 80MHz and a common mode rejection of 70dB rolling off at 10kHz. The frequency performance of model 51, shown in Figure 7 is characterized by a useful small signal bandwidth of up to 60MHz and a common mode rejection of 70dB rolling off at 10kHz. Although the gain roll-off for both models 50 and 51 is running at -6dB per octave, implying a single pole response, the phase angle above 10MHz reveals the presence of higher order poles just beyond unity gain cross-over.

Whereas the design is developed to stagger these breaks for greater phase margin, it is not uncommon to encounter parasitic effects arising from stray capacitance and tight loop gain when designing in the amplifier. It is essential, therefore, to take certain precautions in selecting the value of gain resistors, load terminations and wiring techniques when applying wideband amplifiers.

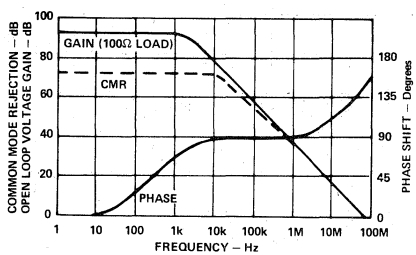


Figure 6. Model 50 Frequency Response

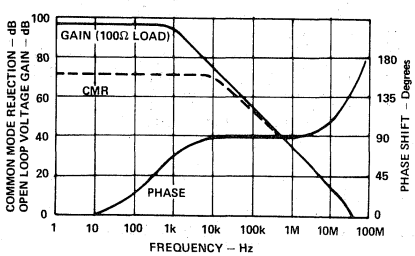


Figure 7. Model 51 Frequency Response

UNITY GAIN APPLICATIONS

Models 50 and 51 have been optimized for fast settling inverting applications, such as current to voltage conversion at the output of D/A converters. In these configurations the high speed amplifier is usually operating in a noise gain of about 5. (Noise Gain = 1 + R_f/R_{out} of D/A). They have also been designed as fast noninverting amplifiers and offer excellent performance at noise gains of 2 or higher. For unity gain applications the circuits shown in Figure 8 and Figure 9 are recommended.

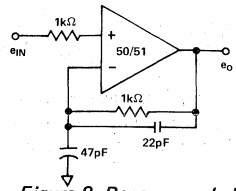


Figure 8. Recommended Circuit for Unity Gain Noninverting Buffer

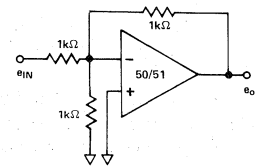


Figure 9. Recommended Circuit for Unity Gain Inverter

ADDITIONAL LOAD CAPACITANCE

If circuit applications require that load capacitances greater than 100pF be driven, then stability may be assured by using the load isolation circuit of Figure 10. The available output swing will be reduced by the drop across the 10Ω resistor. A 4.7pF feedback capacitor should suffice to insure stability for 1000 to 1500pF loads. Larger values of load capacitance will require increasing either the feedback capacitor or the 10Ω resistor.

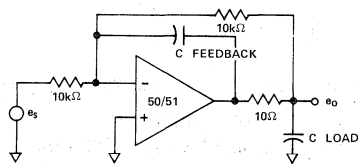


Figure 10. Isolation of Load Capacitance

COMPONENT SELECTION AND WIRING

As with all fast op amp designs, great care must be taken in designing and packaging these circuits to realize their ultimate capability. Unfortunately, what has been painstakingly gained in design can often be lost through misapplication. To assist the user, several elements of good design are presented for his consideration when applying these amplifiers.

CIRCUIT WIRING

It is of utmost importance that care be taken in laying out signal and power ground circuits to avoid extraneous voltage pick-up in the ground signal paths. Keep all leads short to minimize stray inductance and capacitance at the input terminals.

Stray effects at the input tend to cause excessive ringing while output strays destabilize the amplifier roll-off resulting in possible oscillations. Be sure to resistively decouple monitoring instruments such as oscilloscopes since their input capacitance can affect measurements also.

Power supply lead length is not as critical since models 50 and 51 use 1μF bypass supply capacitors internally. When mounting on a pc card, the designer should consider using a ground plane about the input and feedback terminals for line driving applications. Where the source or load signals are remote to the amplifier, consider using properly terminated coax cable. Don't overlook sockets or printed circuit mounting boards as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier.

COMPONENTS

Metal film resistors are preferred over wire-wounds because of their lower capacitance and inductance. Good selections are now available with excellent accuracies and temperature coefficients. Diodes are preferably hot carrier types for the fastest-settling applications. 1N914 types are suitable for more routine uses. Capacitors in critical locations should be polystyrene, teflon, or polycarbonate, to minimize dielectric absorption.

ANALOG DEVICES

Low Noise, Low Drift Precision FET Amplifier

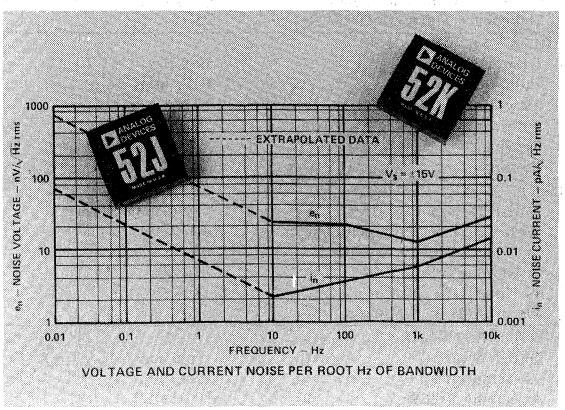
MODEL 52

FEATURES

Guaranteed Low Noise 1.5μV p-p max (0.01 to 1Hz)
Low Voltage Drift: 1μV/°C max (52K)
Low Bias Current: 3pA, max
High CMR: 100dB, min
High Voltage Gain: 120dB, min
Wide Power Supply Range: ±9V to ±18V
Excellent Long Term Stability: 5μV/month
Fast Thermal Response

APPLICATIONS

Low Level Instrumentation Preamp
High Impedance Precision Buffer
Long Term Integrator
Current to Voltage Converter
Precision Voltage Regulator
Preamp for 16-Bit Resolution V/F Converters



VOLTAGE AND CURRENT NOISE PER ROOT Hz OF BANDWIDTH

GENERAL DESCRIPTION

Model 52, a low noise, high accuracy FET input operational amplifier was designed for handling microvolt signals from high impedance (>100kΩ) sources. It features guaranteed low voltage noise (1.5μV p-p max, 0.01 to 1Hz bandwidth) with low input offset voltage drift (3μV/°C max, 52J; 1μV/°C max 52K). Unlike most available low drift amplifiers, model 52 voltage drift is unaffected by trimming the initial offset voltage (0.5mV max). The low input bias current (3pA max) is held constant over the entire ±10V common mode voltage range. High voltage gain (120dB, min) and high CMR (100dB, min) complete the performance profile. Model 52 is an excellent choice for high accuracy, high resolution linear signal processing applications.

By incorporating a new low noise N-channel monolithic FET input stage, thermal stability, voltage noise and differential signal performance are improved to a level previously obtainable only in the best bipolar amplifier designs. Model 52 is an excellent choice to replace chopper stabilized amplifiers where significant sources of error are introduced from zero beating, "chopper spikes" and ground loop currents.

The guaranteed accuracy performance of model 52 suggests critical applications such as low noise, low drift "front-end" preamplifiers for A to D converters and DVM's. For high impedance buffering applications, model 52 offers low input bias current, high linear common mode rejection, complete protection from input transients (offset voltage and bias current will not degrade due to reverse breakdown) and freedom from latch up when the common mode voltage range is exceeded. Model 52 is supplied in a reliable, compact epoxy module package. Output is protected from shorts to ground and/or supply voltage and is capable of driving up to 0.01μF load capacitance.

IMPROVED OFFSET VOLTAGE STABILITY

Model 52 has been designed for the lowest possible input voltage drift over the 0 to +70°C temperature range. In most operational amplifier designs, trimming is accomplished by unbalancing the current in the input stage. This trimming technique introduces an additional 2 to 12μV/°C for each millivolt of E_{OS} that is nulled. To provide performance consistent with low offset voltage drift, model 52 incorporates a three-point trim (see connection diagram) whereby a compensating voltage is introduced without unbalancing the input stage currents. By virtue of this trim scheme, there is no degradation in T.C. when E_{OS} is nulled and the specified performance is achieved.

IMPROVED NOISE PERFORMANCE

Input noise limits signal resolution in low level signal processing applications. The FET input stage of model 52 reduces noise current significantly from that of bipolar amplifiers, permitting high source impedance applications. Model 52 also offers voltage noise levels appreciably below that of other FET amplifiers. To illustrate the excellent low noise performance of model 52, Figure 1 shows typical input voltage noise in a 0.01 to 1Hz bandwidth. Noise is typically less than 1μV p-p and is free of noise spikes.

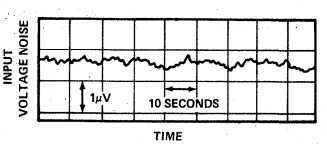


Figure 1. Voltage Noise 0.01 to 1Hz Bandwidth

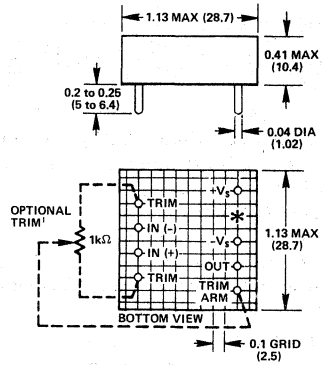
SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	52J	52K
OPEN LOOP GAIN		
DC 2kΩ Load	120dB Min (130dB Typ)	*
RATED OUTPUT[1]		
Voltage, 2kΩ Load	±10V min	*
Current	±5mA min	*
Maximum Load Capacitance	0.01μF	*
Impedance, Open Loop	75Ω	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	500kHz	*
Full Power	4kHz min	*
Slew Rate	0.25V/μs min	*
Overload Recovery	130μs	*
Settling Time, ±0.1%, ±10V Step	100μs	*
Settling Time, ±0.01%, ±10V Step	150μs	*
INPUT OFFSET VOLTAGE		
Initial[2], @ +25°C	±500μV max	*
With External Trim Potentiometer	Adjustable to Zero	*
vs. Temperature (0 to +70°C)	±3μV/°C max	±1μV/°C max
vs. Supply Voltage	±2μV/%	*
vs. Time	±5μV/Month	*
Warm-Up Drift, 5 Minutes	±5μV	*
INPUT BIAS CURRENT		
Initial, @ +25°C	-3pA max (-1pA Typ)	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
vs. Supply Voltage	±0.01pA/%	*
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±1pA	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
INPUT IMPEDANCE		
Differential	$10^{12}\Omega \| 3.5pF$	*
Common Mode	$10^{12}\Omega \| 3.5pF$	*
INPUT NOISE		
Voltage, 0.01Hz to 1Hz	1.5μV p-p max (1μV p-p Typ)	*
10Hz to 10kHz	3μV rms max (2μV rms Typ)	*
f = 1Hz	$70nV/\sqrt{Hz}$ rms	*
f = 10Hz	$25nV/\sqrt{Hz}$ rms	*
f = 100Hz	$20nV/\sqrt{Hz}$ rms	*
f = 1kHz	$13nV/\sqrt{Hz}$ rms	*
Current, 0.01Hz to 1Hz	0.1pA p-p	*
f = 1Hz	$7fA/\sqrt{Hz}$ rms	*
f = 10Hz	$2.5fA/\sqrt{Hz}$ rms	*
f = 100Hz	$3.5fA/\sqrt{Hz}$ rms	*
f = 1kHz	$6fA/\sqrt{Hz}$ rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±10V min	*
Common Mode Rejection, CMV = ±10V	100dB min (106dB Typ)	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY[3]		
Voltage, Rated Performance	±15V	*
Voltage, Operating	±(9 to 18)V	*
Current, Quiescent	±5mA	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.12" x 1.12" x 0.4"	*
Weight	16g	*
Mating Socket	AC1008	*

*Specifications same as model 52J.
[1] Protected for short circuit to ground.
[2] With no external trim potentiometer connected.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

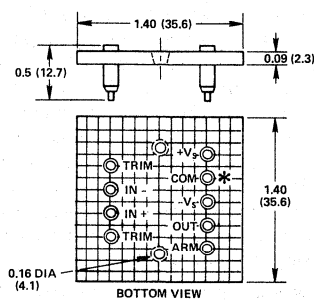
Dimensions shown in inches and (mm).



[1] Optional 1kΩ external trim pot, Analog Devices Model 79PR1K. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim pins left open, input offset voltage will be ±0.5mV, maximum.

*Common Supply connection not required.

MATING SOCKET AC1008



*No connection required on Model 52.

FREQUENCY RESPONSE

From the plot of Open Loop Voltage Gain and Phase Shift (see Figure 2) versus Frequency, it can be seen that model 52 is stable for all closed loop gains. Even at the crossover frequency of 500kHz, model 52 has a phase margin of 75°.

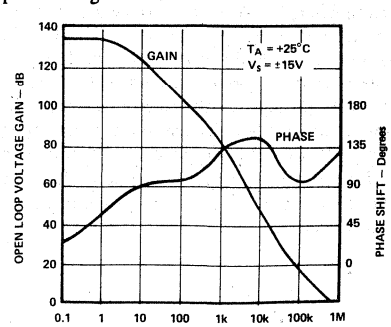


Figure 2. Open Loop Frequency Response

ANALOG DEVICES

High Voltage Differential FET Amplifier

MODEL 171

FEATURES
High Output Voltage: ±140V
High CMR: 100dB min
Operates With a Wide Range of Power Supplies
High CMV: ±(|V_S| - 10V)

APPLICATIONS
High Voltage Compliance Current Source
High Voltage Follower With Gain
High Voltage Integrator
Diff. Amp for High CMV Bridge Applications
Reference Power Supply

GENERAL DESCRIPTION
Model 171 is a high performance FET input op amp designed for operation over a wide range of supply voltages. This module features an output range of ±15V to ±140V at 10mA, a minimum CMRR of 100dB and a high common mode voltage rating of ±(V_S - 10V) min. DC offset is less than ±1mV, and maximum drift of either ±50 or ±15μV/°C is available in the J or K versions. Bias current is less than 50pA (171J) or 20pA (171K), doubling per +10°C increase of temperature. The model 171 also features small signal bandwidth of 3MHz for unity gain, full-power bandwidth of 15kHz, and slew rate of 10V/μs. These operating characteristics make model 171 an excellent choice for high voltage buffer applications, followers with gain, off-ground signal measurements and reference power supplies.

Excellent power supply rejection of 7μV/V enables model 171 to be powered by inexpensive, low regulation supplies, without sacrificing any of the 171's inherent high performance. The supplies also need not be symmetrical. Any combination of power supply voltages between the limits of 15 to +300V for the positive side and 15 to -300V for negative side is acceptable provided the total voltage across the amplifier is within the range of 30 to 300V.

Model 171's output is completely short circuit protected by the use of a current limit scheme. This type of protection provides a short circuit output that is only slightly greater than the rated output current for normal operation. With this design the module and external circuitry are protected, internal heat dissipation and the associated high temperature rise are limited, and added reliability is built in.

POWER SUPPLY VOLTAGES
Model 171 offers the flexibility of operating with an extensive range and combination of power supply voltages. Figure 1 shows a chart of permissible combinations of supply voltages for the 171. The model 171 maintains its normal operating characteristics when using asymmetrical power supply configurations.

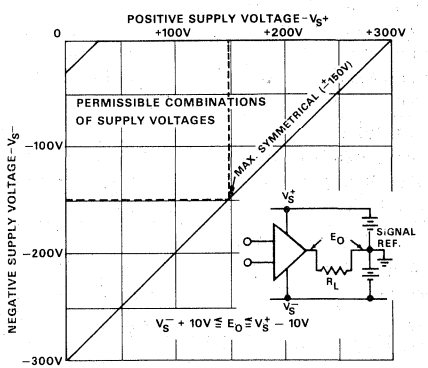


Figure 1. Power Supply Voltage Combinations

SPECIFICATIONS (typical @ +25°C and ±125V unless otherwise noted)

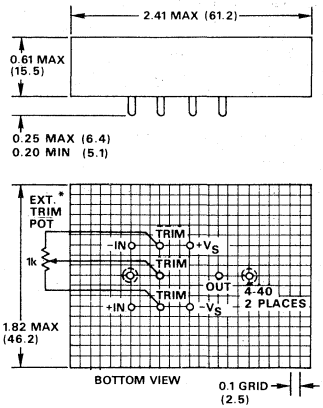
MODEL	171J	171K
OPEN LOOP GAIN	10^6 min	*
RATED OUTPUT		
Voltage	$\pm(\|V_S\|-10V)$ min	*
Current	±10mA min	*
Maximum Load Capacitance	1000pF	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	3MHz	*
Slewing Rate	10V/μs min	*
Full Power	15kHz min	*
Settling Time to ±0.1%, ±10V Step	25μs	*
Overload Recovery	5μs	*
INPUT OFFSET VOLTAGE		
Initial Offset, +25°C[1]	±1mV	*
Avg. vs. Temp (0 to +70°C)	±50μV/°C max	±15μV/°C max
vs. Supply Voltage	±7μV/V	*
vs. Time	±250μV/mo	*
INPUT BIAS CURRENT		
Initial Bias, +25°C	-50pA max	-20pA max
vs. Temp (0 to +70°C)	x 2/10°C	*
Difference Current	±10pA	±5pA
INPUT IMPEDANCE		
Differential	$10^{11}\Omega\|\|3.5$pF	*
Common Mode	$10^{11}\Omega\|\|3.5$pF	*
INPUT NOISE		
Voltage, 0.01 to 1.0Hz	4μV p-p	*
10Hz to 10kHz	2.5μV rms	*
5Hz to 50kHz	6μV rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	$\pm(\|V_S\|-10V)$ min	*
Common Mode Rejection	100dB min	*
Common Mode Rejection	114dB	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY		
Voltage, Rated Specification	±25 to ±150V dc	*
Voltage, Operating	±15 to ±150V dc	*
Current, Quiescent	±6mA	*
TEMPERATURE RANGE		
Rated Specification	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-40°C to +100°C	*
MECHANICAL		
Case Size	2.41" x 1.82" x 0.61"	*
Weight	80g	*
Mating Socket	AC1037	*

*Specifications same as 171J

[1] No external trim connection required.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

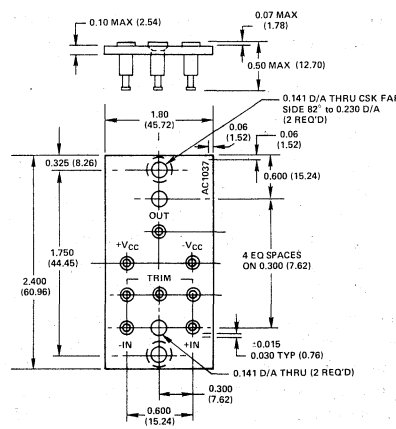
Dimensions shown in inches and (mm).



*Available from Analog Devices – #79PR1K

MATING SOCKET

Dimensions shown in inches and (mm).



MATING SOCKET AC1037

As shown in Figure 1, the model 171 requires at least ±15 volts applied across it in order to operate properly. The 171 may be operated from a single floating supply voltage by using the power supply offsetting scheme shown in Figure 2. When this configuration is used, the 171 is capable of operating over its specified input and output voltage range.

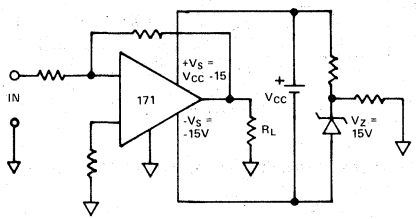


Figure 2. Single Supply Operation

FREQUENCY RESPONSE

Figure 3 shows a plot of open loop gain and phase shift as a function of frequency for model 171. It can be seen that the model 171 is stable for all closed loop gains. At the crossover frequency, model 171 typically displays a phase margin of 85°.

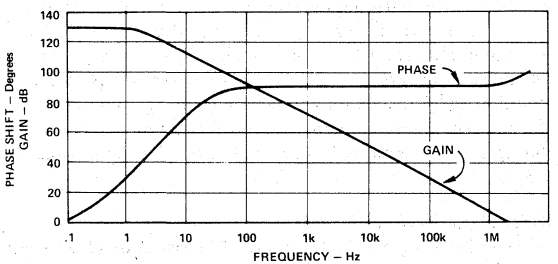


Figure 3. Gain and Phase Shift vs. Frequency

The open loop dc gain of the model 171 does not change appreciably as the power supply voltage is varied (see Figure 4). Open loop gain is typically greater than 106dB over the full power supply voltage range. Figures 3 and 4 show that excellent closed loop accuracy is assured over a great range of frequency and supply voltage when using the 171.

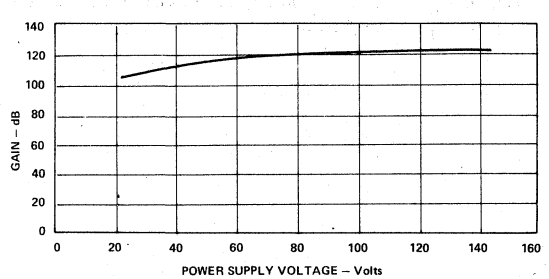


Figure 4. Open Loop dc Gain vs. Power Supply Voltage

COMMON MODE REJECTION RATIO

Common mode rejection is an important parameter in measurements requiring the amplification of small differential signals riding on high common-mode voltage levels. Model 171 is characterized by a minimum CMR of 100dB over its specified power supply voltage range. For the 171, CMR increases above this minimum value as the power supply voltage is raised. Figure 5 shows CMR as a function of supply voltage for model 171. The 171 also is capable of handling common-mode voltages up to 140 volts (with maximum supply voltages).

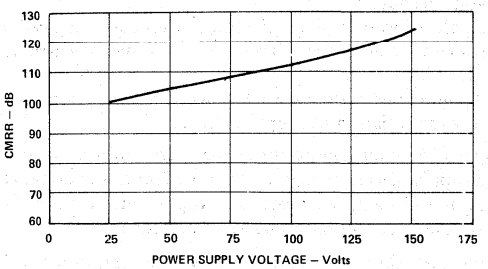


Figure 5. CMRR vs. Power Supply Voltage

OFFSET VOLTAGE

Model 171 provides excellent power supply rejection of 7μV/V and guaranteed input offset voltage drift of 15μV/°C (171K). The combination of these two characteristics, along with its gain and common mode performance, help make the model 171 an accurate and stable source of high voltage signals. Figure 6 shows input offset vs. power supply voltage for the 171. Supply rejection is fairly constant and is not dependent upon the power supply voltage level.

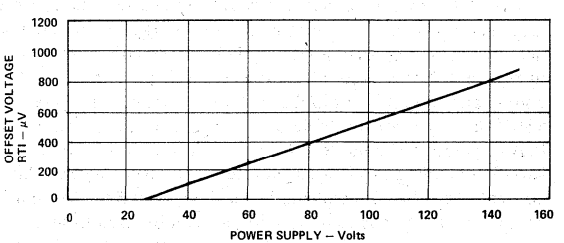


Figure 6. Input Offset Voltage vs. Power Supply Voltage

BIAS CURRENT

The input bias current for the model 171 is specified to be 50pA, max for the J version and 20pA, max for the K version. These specifications are guaranteed over the normal range of common mode voltage. Bias current is a function of CMV and decreases as the CMV approaches zero volts. Figure 7 shows bias current vs. CMV for model 171K. Notice that with zero CMV the bias current is typically less than 3pA.

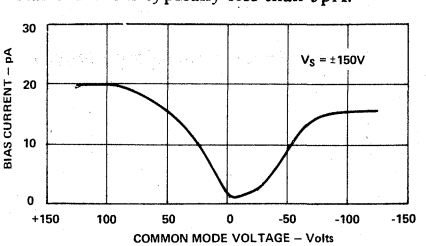


Figure 7. Bias Current vs. CMV for Model 171K

APPLICATIONS

There are many moderate-to-high voltage applications for which the model 171 FET-input op amp is useful. Typical classes of applications include:

1. Retrofit and auxiliary applications in existing analog computing systems utilizing a standard ±100V signal-voltage range.
2. Use as low-noise buffers and input amplifiers in differential or non-inverting applications with signals derived from high-voltage sources.
3. Applications for which high output voltage is needed, e.g., wide-range precision reference sources, piezoelectric crystal drivers, etc.
4. Applications with moderate signal levels in systems subject to wide variation of supply voltage.

Model 171's excellent performance characteristics, including high supply rejection, high input impedance, low noise, tolerance of capacitive load, and protection against output short circuits, make it ideal for all these classes of application.

In addition, there is one more class that is a bit unusual. For an amplifier to be safe against short-circuits, it must not only be self-protected, it must also protect the supply that feeds it. The 171 is programmed to draw a maximum short-circuit current slightly greater than the 10mA maximum load current plus its quiescent current. Therefore, model 171 is the ideal choice for applications where a fail-safe current load that is essentially independent of supply voltage is needed.

APPLICATIONS – PROGRAMMABLE REFERENCE VOLTAGE SOURCE

The operating specifications of the model 171 make it ideally suited for use as a low-cost, high voltage reference power supply. When coupled with an appropriate D/A converter, the 171 can also function as a 12-bit programmable voltage source. Such a network, utilizing Analog Devices DAC12QZ converter, is shown in Figure 8. This system offers the versatility of binary or BCD coding and unipolar or bipolar output. Programmable levels of ±50V or ±100V are available by setting the output level on the D/A converter. The model 171 supply voltages can also be varied depending on the desired reference output levels. Gain control and offset control can be used, as shown in Figure 8. This type of reference supply network can be used in such applications as generation of calibration voltages (circuit or instrument testing) and low current control signal levels. Trim resistors are used in this circuit to precisely adjust the full scale and zero levels of the reference output.

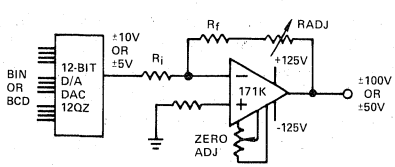


Figure 8. Programmable Power Supply

An expanded application for model 171 in a programmable voltage source for a mass spectrometer is shown in Figure 9.

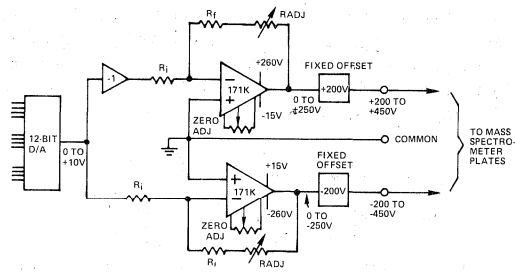


Figure 9. Programmable Mass Spectrometer Voltage Source

NONLINEAR CIRCUITS HANDBOOK

In addition to its linear devices, Analog Devices also offers a comprehensive line of nonlinear function modules (multipliers, dividers, rms to dc converters, etc.). These function modules provide essential building blocks in systems that process information in industrial applications. In order to further the understanding of function modules, Analog Devices has issued the Nonlinear Circuits Handbook. This handbook is an invaluable source of information on principles, circuitry, performance specifications, testing and application of the class of devices used in nonlinear applications. The handbook helps identify design situations for which nonlinear devices will offer the best solution and provides the fundamentals and guidelines necessary for the proper selection and use of function modules. The Nonlinear Circuits Handbook is available from Analog Devices for $5.95.

OTHER AMPLIFIERS

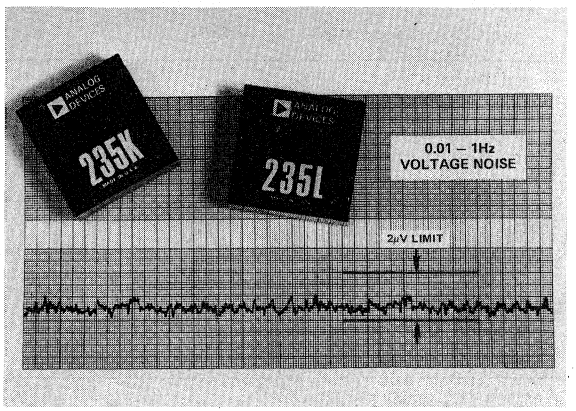
- High Performance FET – model 52: low noise (1.5μV p-p, 1Hz BW), low drift (1μV/°C, 52K) low bias (3pA max), CMRR = 80dB min
- Wideband – model 48: 15MHz (unity gain), low noise 2μV p-p, 1Hz BW, 300ns settling, 15μV/°C drift (max)
- Wideband, Fast Settling – model 50: 70MHz (unity gain), 100mA output, 15μV/°C drift (max, 50K)
- Chopper Stabilized – model 261: guaranteed low noise (1μV p-p max, 1Hz BW), ±0.1μV/°C drift (max, 261K)
- Economy Electrometer – model 42: lowest bias (75fA, 42K)
- High Output Current – model 50: 100mA output, wideband (10MHz, f_p), 80ns settling

Economy, Guaranteed Low-Noise Chopper Stabilized Amplifier

MODEL 235

FEATURES
Low Cost
Ultra-Low Noise: 0.5μV p-p, 1Hz BW (2μV, max)
Very Low Drift: 0.1μV/°C max, 0.5pA/°C max (235L)
Excellent Long Term Stability: 5μV/yr
Low Profile: 0.5" Height

APPLICATIONS
Precision Integrator
Picoamp Current Measurements
Microvolt Voltage Measurements
Bridge Amplifier
Balance Scales and Weighing Instruments



GENERAL DESCRIPTION

Analog Devices' model 235 is a chopper stabilized inverting op amp that delivers premium performance at economy prices. It is pin-compatible with existing, more expensive modules, allowing designers to upgrade systems while realizing significant cost savings.

Foremost among model 235's electrical specifications is its outstanding noise performance of 0.5μV p-p (f = 0.01 to 1Hz) with a guaranteed maximum limit of 2μV in a 1Hz BW. Low voltage noise combined with low current noise (10pA p-p, 1Hz BW) yields low input noise for source impedances up to several hundred-thousand ohms. The 235 also offers low voltage and current drift as a function of both temperature (0.1μV/°C max, 0.5pA/°C max, 235L) and time (5μV/yr). This combination of noise and drift performance makes model 235 ideally suited for demanding applications such as balance scales and weighing instruments requiring high accuracy and excellent long-term stability without the use of "front panel" balance pots or periodic internal adjustment.

Model 235 has been designed to virtually eliminate intermodulation problems caused by "beating" against power line frequencies. The chopper's ultra-stable oscillator is precisely set at the factory to a frequency that minimizes interactions with harmonics of 50, 60 and 400Hz power lines.

For new and upgraded designs, model 235 sets the benchmark for economy chopper performance.

APPLICATIONS

The model 235 inverting amplifier should be considered when long term stability must be maintained with time and temperature, and wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include amplification of microvolt signals, precision integration and analog computing. Low input noise and stable offset voltages make model 235 an ideal preamp for precision low frequency applications such as DVM's, 12- to 16-bit A to D converters, and error amplifiers in servo and null detector systems.

GUARANTEED NOISE PERFORMANCE

The excellent 1Hz voltage noise performance of model 235 (Figure 1) results from careful selection of critical design components during manufacturing. Selection permits 1Hz voltage noise to be maintained very near the typical specification (0.5μV p-p).

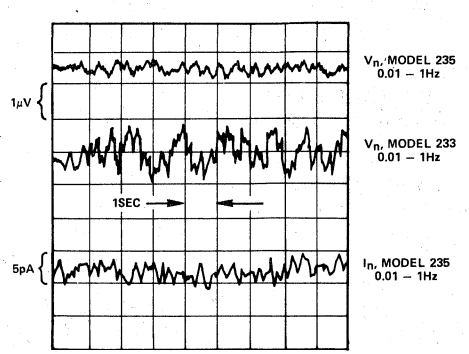


Figure 1. Model 235 Voltage and Current Noise. Model 233 Voltage Noise Shown for Comparison.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	235J	235K	235L
OPEN LOOP GAIN			
DC, 2k ohm load	5 x 10^7V/V min	*	*
RATED OUTPUT			
Voltage	±10V min	*	*
Current	±5mA min	*	*
Load Capacitance Range	0.01μF	*	*
FREQUENCY			
Unity Gain, Small Signal	1MHz	*	*
Full Power Response	5kHz min	*	*
Slew Rate	0.3V/μs min	*	*
Overload Recovery	10 sec	*	*
INPUT OFFSET VOLTAGE			
Initial Offset,[1] @ +25°C	±25μV max	±25μV max	±15μV max
vs. Temp, 0 to +70°C	±0.5μV/°C max	±0.25μV/°C max	±0.1μV/°C max
vs. Supply Voltage	±0.1μV/%	*	*
vs. Time	±5μV/year	*	*
vs. Turn On, 10 sec to 10 min	±3μV	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	±100pA max	±50pA max	±50pA max
vs. Temp, 0 to +70°C	±1pA/°C max	±0.5pA/°C max	±0.5pA/°C max
vs. Supply Voltage	0.2pA/%	*	*
INPUT IMPEDANCE			
Inverting Input to Signal Ground	300kΩ	*	*
INPUT NOISE			
0.01 to 1Hz, typ	0.5μV p-p		
0.01 to 1Hz, max	—	2μV p-p	2μV p-p
0.1 to 10Hz	3.5μV p-p	*	*
10Hz to 10kHz	5μV rms	*	*
Current, 0.01 to 1Hz	10pA p-p	*	*
0.1 to 10Hz	30pA p-p	*	*
INPUT VOLTAGE RANGE			
(-) Input to Signal Ground	±15V max	*	*
POWER SUPPLY (V dc)[2]			
Rated Performance	±15V @ 5mA	*	*
Operating	±(12 to 18)V	*	*
TEMPERATURE RANGE			
Rated Specifications	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +125°C	*	*

*Specifications same as model 235J.

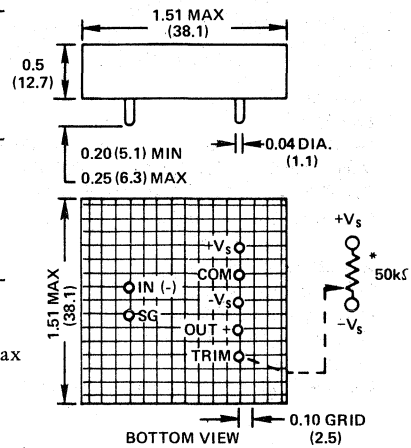
[1] Externally adjustable to zero.

[2] Recommended power supply, Analog Devices model 904, ±15V dc @ 50mA.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



NOTES:

*Optional Trim Pot Analog Devices Model 79PR50k
Connect Trim Terminal to Common if Trim Pot is not used.

1. SG Should Be Tied to Common.
2. Mating Socket AC1010
3. Weight: 27 grams.

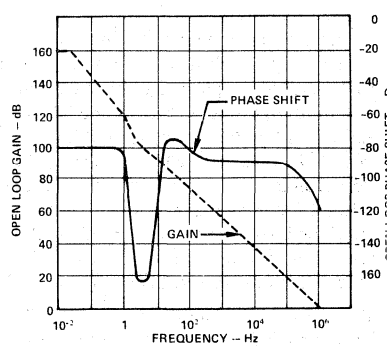


Figure 2. Open Loop Gain and Phase Shift vs. Frequency

Model 235's low frequency noise characteristics complement its very low drift performance to yield exemplary stability and accuracy for a chopper stabilized amplifier. A plot of noise as a function of bandwidth for model 235 is shown in Figure 3.

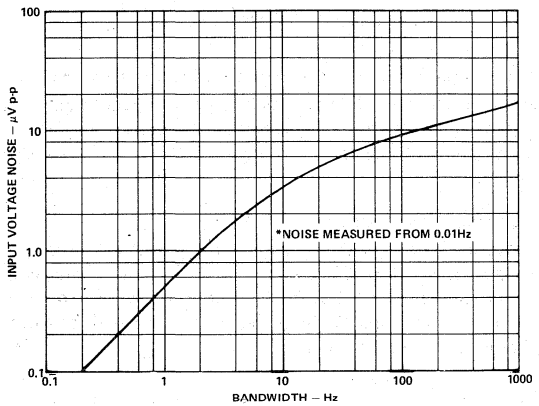


Figure 3. Input Voltage Noise vs. Bandwidth for Model 235

INPUT IMPEDANCE CONSIDERATIONS

Maximum input impedance for inverting amplifiers of all types is limited by bias current, bias current drift, and noise current. These currents flowing through the source impedance increase total error and noise as the input impedance increases. Figure 4 is a plot of total offset voltage, voltage drift and noise vs. input resistance for the model 235.

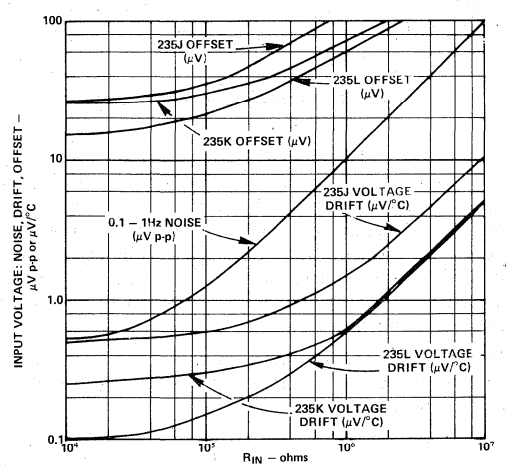


Figure 4. Uncompensated Offset, Drift and Noise vs. R_{IN}

INITIAL OFFSET ADJUSTMENT

Model 235 has low, untrimmed offset voltage specifications of 25μV max for the J and K versions, and 15μV max for the L version. In many applications there will be no need to further trim the offset. In such cases the trim terminal may either be left open, or grounded. If voltage offset adjustment is desired, it may be done with a potentiometer or selected fixed resistor network, as shown in the outline drawing. For circuits where the total input and source resistance remain relatively constant, the entire offset may be zeroed out with the voltage offset adjustment.

The circuit of Figure 5 should be used to compensate for bias current offset when using the model 235 as a current to voltage converter. The potentiometer-resistor network provides a compensating bias current to cancel the amplifier's own input bias current.

When the amplifier is used with a widely varying input resistance and minimum offset is desired, the voltage and current trim potentiometers should be used. The voltage offset should be zeroed with a low value (e.g. 1k ohm) resistor connected from the inverting input to ground. The offset current adjustment should be made with the maximum expected value of R_i connected between the input and ground.

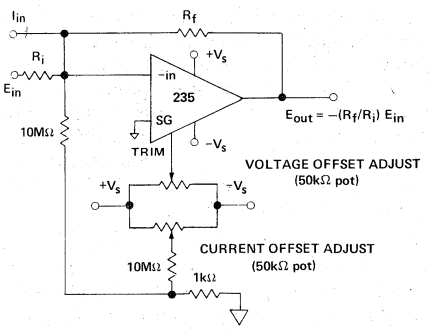


Figure 5. Offset Current Voltage Cancellation

INVERTING OPERATION

The model 235 is designed for use in the inverting mode. It is important that the SG (equivalent to +in) terminal be kept at the same potential as the amplifier's "common" terminal. Any voltage difference between these points is similar to a common mode voltage, and performance cannot be guaranteed under such conditions. The model 235 is also an excellent amplifier for measurement and conversion of low level current sources to proportionate voltages. With offset current externally zeroed, input currents of ten to twenty picoamperes can be amplified and converted to a voltage source for further processing.

SHIELDING, PICKUP AND GROUNDS

Model 235 has an internal electrostatic shield that prevents pickup of extraneous signals and radiation of chopper noise by the module. One precaution is to insure that noise sources are shielded from the inverting input. The user should also insure that ground loops do not occur which can add extraneous signals when amplifying from microvolt or millivolt sources. Ground loop errors most often occur when the power supply current is allowed to flow through the input (signal) ground connection. When this happens, a voltage drop is developed across the power supply leads which appears as a voltage generator in series with the signal source, and as error at the output. This is effectively eliminated by insuring that the signal return lead does not carry the power supply current. Figure 6 illustrates the proper connection.

Another source of error is the small voltages developed by the junction of dissimilar metals encountered in the external connections to the amplifier. Normally insignificant, these "therm-

ocouple" effects may approach the magnitude of the drift specifications of the 235. Careful attention to interconnection layout design will minimize these errors.

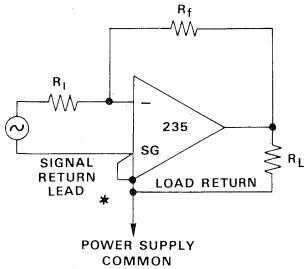


Figure 6. Ground Connection

INTERMODULATION CONSIDERATIONS

If noise at medium frequencies finds its way into the input circuits of carrier amplifiers (chopper amplifiers and the chopper-stabilizing portions of chopper-stabilized amplifiers), it may "beat" with the chopper frequency and produce sum and difference frequencies. The "sum" and noise are unimportant, because they are usually filtered out. But the difference frequencies (which can include dc) usually interfere directly with the low-level low-frequency signal information. These effects can be examined with an oscilloscope.

Model 235 employs specially designed internal shielding and a stable, factory-set oscillator frequency to drastically reduce problems caused by interference from 50, 60 and 400Hz power lines. The user can take further precautions to eliminate intermodulation problems by:

1. Properly shielding input and power supply leads.
2. Using shielded supplies with low ripple and source impedance at the line harmonic frequencies.
3. Avoiding ground loops and locating the amplifier far from interference sources.

THE "T" NETWORK

High gains and high input impedance to an inverting amplifier normally require excessively large feedback resistors. Such a resistor is relatively expensive, particularly for low tolerance units. Furthermore, any stray capacitance across this single resistor significantly reduces bandwidth. The "T" network in Figure 7 minimizes these problems. If R_f/R_i is at least 5:1, there will be no measurable change in other performance characteristics. If the ratio is lower, the effective drift and noise gain will be increased compared to the signal gain. As a general rule, make the ratio R_f/R_i approximately equal to R_2/R_1. This results in reasonable values of resistance for R_f, and a minimal

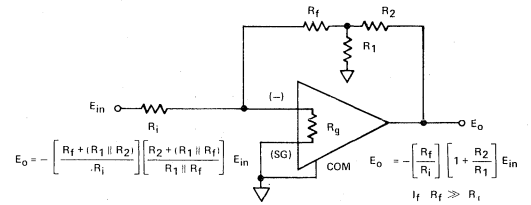


Figure 7. "T" Network

increase in noise and gain drift compared to the standard two resistor circuit. The "T" network also permits gain to be varied, by changing R_1, without the necessity of connecting a switch or potentiometer directly to the highly sensitive inverting input terminal.

OVERLOAD RECOVERY

The overload recovery circuit shown in Figure 8 will prevent the input circuitry from becoming saturated. This circuit, connected externally, will allow the amplifier to recover from overload in less than 0.5μs. Without this circuit overload recovery will require up to 10 seconds.

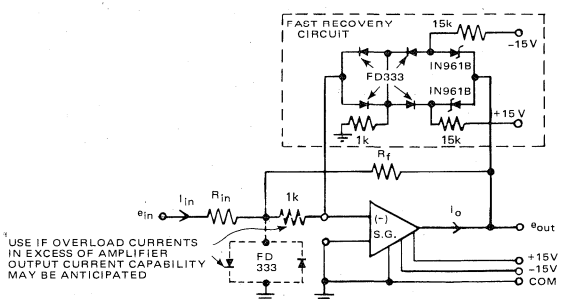


Figure 8. Overload Recovery Circuit

MODEL 234 WIDEBAND CHOPPER

The forte of model 235 is low frequency applications requiring high accuracy and highest stability. For wideband designs, the model 234 chopper is the recommended amplifier. The 234 has very good drift specifications coupled with outstanding bandwidth (2.5MHz unity gain, 500kHz full power) and wideband noise performance (1.5μV p-p, f = 0.1 to 10Hz and 2μV rms, f = 10 to 10kHz).

Model 234 is preferred for designs of wideband microvolt signal processors, low duty cycle pulse train integrators and fast analog computers.

ANALOG DEVICES

Low Noise Non-Inverting Chopper Amplifier

MODEL 261

FEATURES
- Non-Inverting Input
- $10^9\ \Omega$ Common Mode Impedance
- Protected MOSFET Chopper
- Ultra Low Drift $0.1\mu V/^{\circ}C$, Max (261K)
- Guaranteed Low Noise of $0.4\mu Vp\text{-}p$ (0.01 to 1Hz)
- Low Cost:

APPLICATIONS
- Microvolt & Millivolt Measurements
- Meter & Recorder Preamplifier
- Semiconductor Strain Gage Amplifier
- Biological Sensors
- Potentiometer Buffer

GENERAL DESCRIPTION

Model 261 is a low cost non-inverting chopper amplifier featuring ultra low drift of $0.1\mu V/^{\circ}C$, open loop gain of greater than 10 million V/V and guaranteed low noise performance of $0.4\mu V$ p-p max in a 0.01 to 1Hz bandwidth. It is ideally suited for low level pre-amplifier applications where high input impedance and low noise are essential.

Model 261 also offers a solution to beat frequency problems caused by a low frequency carrier mixing with harmonics of the ac line. Its carrier frequency of 3500Hz is nearly a decade higher than that of models previously available. The required harmonic of the ac line that could cause interference with a 3500Hz carrier has negligible energy content and beat frequencies are eliminated. As a further protection against interfering signals, model 261 has been completely shielded internally. This protective shield reduces interference due to RF signals, as well as carrier signals from adjacent chopper amplifiers.

Still another advantage of the 261 due to its higher chopper frequency and shielded design is an output signal that is free from both distortion and chopper spikes. The result is a design that can process low level signals while maintaining low distortion and high signal to noise ratios.

CHOPPER VS. CHOPPER-STABILIZED

Most conventional ultra-stable amplifiers are chopper-stabilized to achieve low drift. In these units, the higher frequency signal components are separated and directly amplified, while the low frequency and dc components are separately chopped, amplified, demodulated, and then summed with the high frequency components in an output stage. This method provides wide bandwidth and excellent performance at the expense of increased cost and complexity. Since many requirements for ultra-low drift amplification involve only dc and low frequency signals, the additional high frequency amplifier stage found in most chopper-stabilized amplifiers has been eliminated from the model 261. This design approach has made it possible to achieve a practical non-inverting configuration, which retains the advantages of low cost and small size. The input stage of the model 261 chops the signal at a 3500Hz rate, resulting in a maximum useful -3dB bandwidth of about 100Hz. For increased flexibility in meeting specific design requirements, terminals are provided for an external compensation capacitor, which determines the amplifier's gain-bandwidth product.

INPUT IMPEDANCE

One of the prime advantages of the non-inverting amplifier is the capability of bootstrapping the input impedance up to the level of the common mode impedance. For the model 261, this means that the $40k\Omega$ open loop input resistance will be multiplied by the open loop gain times the feedback factor. With a typical open loop gain of 40×10^6, closed loop gains of up to 1600 will allow the user to realize $10^9\ \Omega$ input resistance. Even at a gain of 10,000, the effective input resistance will be over 100 megohms. (i.e.) $(40k\Omega)\frac{40 \times 10^6}{10^4} = 160M\Omega$.

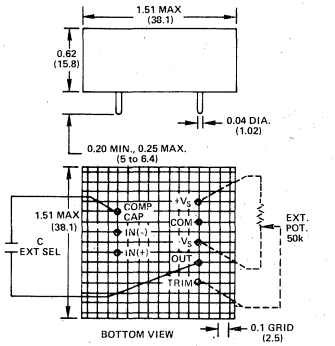
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

Model	261J	261K
OPEN LOOP GAIN		
DC rated load	10^7V/V min	*
RATED OUTPUT		
Voltage	±10V min	*
Current	±5mA min	*
Load Capacitance Range	0 to 0.001μF	*
FREQUENCY RESPONSE[1]		
Small Signal, -3dB	100Hz	*
Full Power Response	2-50Hz min	*
Slewing Rate	100V/sec min	*
Overload Recovery	300ms	*
INPUT OFFSET VOLTAGE		
External Trim Pot[2]	50kΩ	*
Initial Offset, +25°C	±25μV max	*
Avg vs Temp (0 to +70°C)	±0.3μV/°C max	±0.1μV/°C max
Supply Voltage	±0.1μV/%	*
Time	±½μV/month	*
Warm-Up Drift	<3μV in 20 minutes	*
INPUT BIAS CURRENT		
Initial Bias, +25°C, + Input	±300pA max	*
Avg vs Temp (0 to +70°C)	±10pA/°C max	*
Initial Bias, +25°C, - Input	±10nA max	*
Avg vs Supply Voltage	±3pA/%	*
INPUT IMPEDANCE		
Differential	40kΩ||0.01μF	*
Common Mode	10^9Ω||0.02μF	*
INPUT NOISE		
Voltage, 0.01 to 1Hz, p-p	0.4μV max	*
0.01 to 10Hz, p-p	1.0μV max	*
Current, 0.01 to 1Hz, p-p	8pA	*
0.01 to 10Hz, p-p	20pA	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±0.5V min	±1.0V min
Common Mode Rejection	300,000	*
Max Safe Differential Voltage	±20V	*
Max Safe Common Mode Voltage	±20V	*
POWER SUPPLY[3]		
Voltage, Rated Specification	±(14 to 16)V	*
Voltage, Operating	±(13 to 18)V	*
Current, Quiescent	±7mA	*
TEMPERATURE RANGE		
Rated Specifications	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1022	*
Weight	1.75 oz. (50g)	*

[1] See applications information.
[2] Ground trim terminal if trim potentiometer is not used.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output.
*Specifications same as for model 261J.
Specifications subject to change without notice.

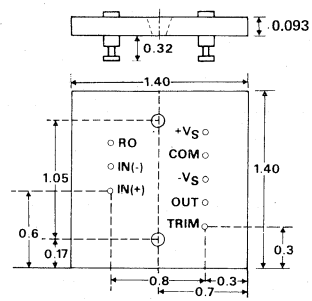
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



1. Trim terminal should be grounded if potentiometer is not used.
2. See Note 1 below for cap value. Use Polycarbonate, Mylar, Mica, Glass, or Polystyrene capacitor for best performance.

MATING SOCKET AC1022



Notes
1. R.O. is connection for compensation capacitor.
2. Bottom View Shown.
3. Mounting holes 0.141 Dia., countersunk 82° to 0.23" Dia.
4. All in line pins spaced 0.2".
5. Dimensions in inches.
6. Markings printed on socket.

OTHER ULTRA LOW DRIFT, LOW NOISE AMPLIFIERS

Model 43K: This ultra low noise differential FET amplifier has guaranteed noise performance of 2μV p-p max in a 10Hz B.W. and 3μV rms max in a 50kHz B.W. Drift is 5μV/°C max.

Model 235: Chopper stabilized amplifier has noise of less than 1μV p-p and drift is only 0.1μV/°C (235L).

Model 184: A chopperless differential input amplifier with 0.25μV/°C drift and 1MHz bandwidth. Noise is 1μV p-p in a 0.01 to 1Hz B.W. and 4μV rms in a 50kHz B.W.

Contact the factory or your local Sales Representative for data sheets on these units.

NON-INVERTING VS. INVERTING OPERATION

The major limitation of the standard inverting type chopper stabilized amplifier is due to the practical limit on input impedance resulting from input bias current characteristics. If one attempts to obtain 10^7 ohms input impedance by using a 10^7 ohm input resistor with an inverting amplifier, this resistor will convert input current drifts of 0.5pA/°C into equivalent voltage drifts of 5μV/°C. It will also add Johnson Noise of 2.5μV p-p/$\sqrt{Hz}$ to the amplifier's input. These results negate the advantage of selecting the chopper-stabilized amplifier in the first place. Noise current will similarly increase the input uncertainty: inverting amplifier input noise currents of 10pA become 100μV noise voltages (referred to input). Furthermore, uncompensated initial bias currents of 50pA cause additional offsets of 500μV. Due to the non-inverting configuration of the model 261, these limitations are avoided. The input bias current (with its drift and noise) flows only through the signal source impedance, effectively eliminating the multiplication of drift and noise and offset caused by the input resistor in the inverting configuration. These benefits of the model 261 are shown graphically in Figure 1. When required input impedance is more than 300,000 ohms, the model 261 gives increasingly superior performance. One additional advantage is that the gain-setting precision resistors can be low-cost low value resistors instead of the more costly high resistance values.

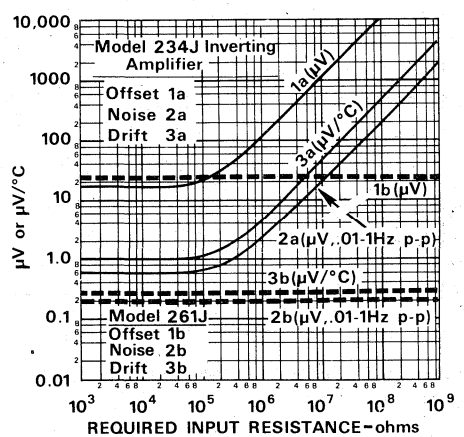


Figure 1. Offset, Drift, & Noise vs. Required Input Resistance

NON-INVERTING AMPLIFIER SELECTION CRITERIA

(Model 261 vs. chopperless amplifiers)

In selecting an amplifier for low drift, one of the major considerations is the effect of source resistance. For low values of source resistance, the total offset (or drift) for differential amplifiers is essentially equal to the amplifier's offset (or drift) voltage. At the value of source resistance equal to the ratio of offset voltage to difference current, or offset voltage drift to difference current drift, the respective current is contributing an error equal to its corresponding voltage error. For values of source resistance larger than this calculated value, the current error's contribution will be dominant. In this section, model 261's drift and offset are compared with two low drift chopperless differential amplifiers, one with FET input, the other with bipolar input.

Fixed Source Resistance. If source resistance is fixed, bipolar chopperless amplifiers not having internal bias current drift compensation can benefit by the use of a compensating resistor in series with the (-) input. Under these conditions, Figure 2 shows a comparison of total drift /°C vs. source resistance for the model 261K, the model 184L low drift bipolar amplifier, and the model 52K low drift FET amplifier. For source resistances up to 200,000 ohms, the model 261 gives the lowest temperature drift. Total drift (R.T.I.) is equal to:

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + R_S\,(\Delta I_{os}/\Delta T)\ \text{(Models 184, 52)}$$

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + R_S\,(\Delta I_b/\Delta T)\ \text{(Model 261)}$$

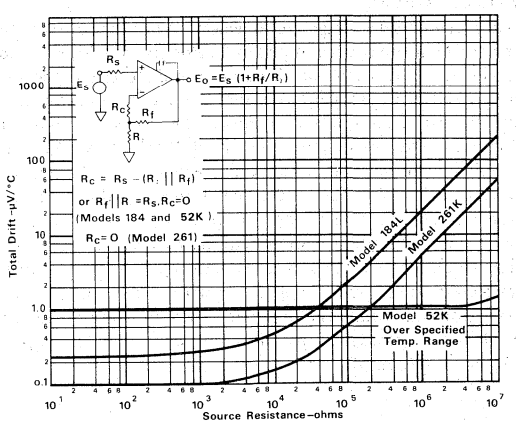


Figure 2. Offset Drift vs. Fixed Source Resistance

Variable Source Resistance. For situations where the source resistance can vary over a significant range, for instance when the amplifier's source is a multiturn potentiometer, a different set of conditions apply. The effective drift current to be considered for differential chopperless amplifiers is now the Input Bias Current/°C, rather than the Input Difference Current/°C (I_{os}/°C). A two to one improvement in drift for the model 184 can be obtained if the bias current balancing resistor (R_C in Figure 3) is made equal to the mean value of the source resistance. Under these conditions, drift will be approximately:

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + \tfrac{1}{2}\ (R_S\ \text{max} - R_S\ \text{min})\ (\Delta I_b/\Delta T) + R_C\ (\Delta I_{os}/\Delta T)\ \text{(Models 184, 52K)}$$

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + (R_S\ \text{max})\ (\Delta I_b/\Delta T)\ \text{(Model 261)}$$

Figure 3 shows the total drift for a source resistance varying from zero to the chosen value, for models 52K, 184L and 261K. For values up to 200,000 ohms the model 261 again gives the lowest total temperature drift.

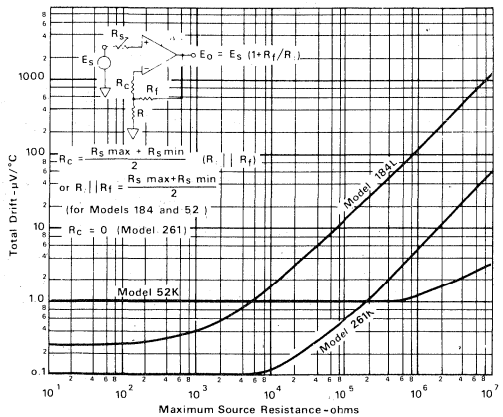


Figure 3. Offset Drift vs. Variable Source Resistance

INITIAL OFFSET

An initial offset voltage will develop due to bias current flowing through the source impedance. For fixed source impedances, this offset may be zeroed out in differential chopperless amplifiers not having internal bias current drift compensation by the use of the series compensating resistor, R_C shown in Figure 4. This offset should not be nulled out by adjusting the amplifier's offset trim because this will increase the offset voltage drift. With the model 261, however, all offsets may be zeroed out by means of the trim potentiometer. For variable source impedances, the offset should be zeroed out with the source impedance at its mean value. Figure 4 is a plot of the maximum offset which will occur with a given range of R_S variations, assuming the offsets are zeroed when operating with the mean value of R_S. Initial offset due to R_S is $I_b/2$ (R_S max - R_S min).

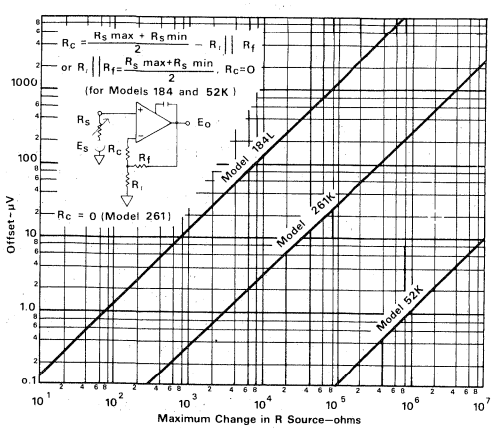


Figure 4. Offset vs. $\triangle R_S$

LONG TERM DRIFT

Offset voltage of any amplifier will show some change with time, due to normal component aging. It is important to realize that the published drift for amplifiers does not accumulate linearly with increasing time. For example, the voltage drift of the model 261 is specified as ±½μV/month (a calculated figure believed to be quite conservative). For calculation of random long term drift, a rule of thumb is that one should multiply drift by the square root of the time factor increase. For the model 261, this yields a conservative long term drift of less than 2μV per year.

NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. This is particularly important whenever high source impedances are encountered, since current noise through the source impedance will appear as an additional voltage noise, combining with the basic amplifier voltage noise and Johnson noise of the resistor. The sum of these noise sources will then be amplified along with the desired signal. For this reason, special care has been taken to reduce noise voltage and current to a level far below that of comparable chopper amplifiers. The one Hertz bandwidth noise voltage and current are 0.4μV p-p max and 8pA p-p respectively. For 10Hz bandwidth, corresponding values are 1μV p-p max and 20pA p-p. Figure 5A is a graph of noise vs. bandwidth for both current and voltage. Figure 5B is a spectral density plot for determining spot noise at any frequency. Figure 6 is a plot of peak to peak noise which will be encountered for these bandwidths, as a function of source resistance.

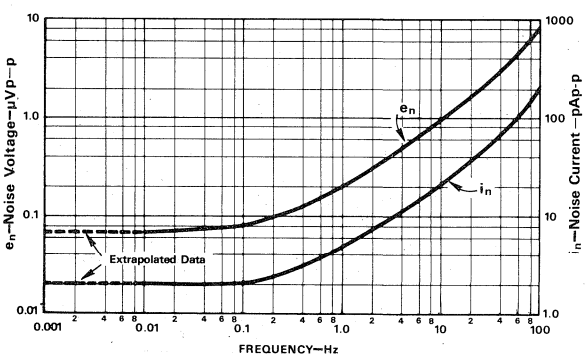


Figure 5A. Noise Current and Voltage vs. Bandwidth. Measured from 0.01Hz.

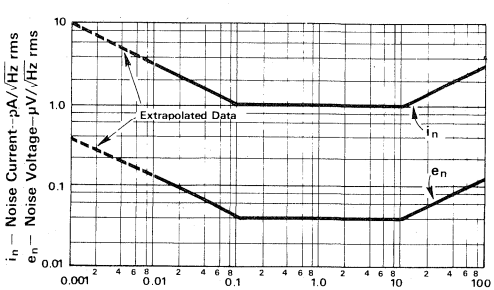


Figure 5B. Spectral Density of Current and Voltage

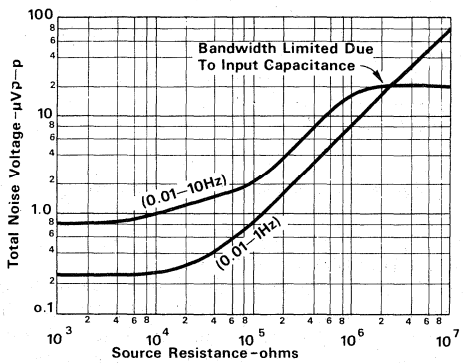


Figure 6. Total Noise vs. Source Resistance

preserving polarity information. The drift of the input stage is not present in the demodulated signal since it was not chopped by the input network. The demodulated signal is filtered and further amplified by the integrator connected output dc amplifier.

Using the system just described, the remaining drift and offset, referred to the amplifier input, is equal to the output dc amplifier stage input drift and offset divided by the ac-coupled amplifier's gain. If the output stage integrated circuit amplified had a 100μV/°C drift, and the ac-coupled amplifier gain is 1000, then the drift, referred to the input will be 0.1μV/°C (the specification for the model 261K). The same considerations apply for offset voltage, accounting for its low value and the excellent long term stability of this amplifier.

The chopping signal is generated by a standard multivibrator. The frequency is not critical, and the multivibrator circuit is protected against latch-up.

HOW THE MODEL 261 OPERATES

As shown in Figure 7, the model 261 consists of five specific circuit functions. The input signal is fed through a resistor to the MOSFET Chopper. When the MOSFET is off (high resistance), the error signal appears at the input to the ac-coupled amplifier. When the MOSFET transistor is on (low resistance), the input to this amplifier is reduced to near zero. The difference between the on and off voltages at the amplifier is a square wave of amplitude slightly less than the error voltage. The attenuating effect of the MOSFET Chopper's "on" resistance is negligible. For example, if the attenuation were as much as 10%, the only effect would be to lower the potential open loop gain of the amplifier by the same amount.

The ac-coupled amplifier, consisting primarily of a linear integrated circuit, amplifies the resulting chopper error signal. Its output is capacitively coupled into a synchronous demodulator which reconstructs the low frequency-dc input signal,

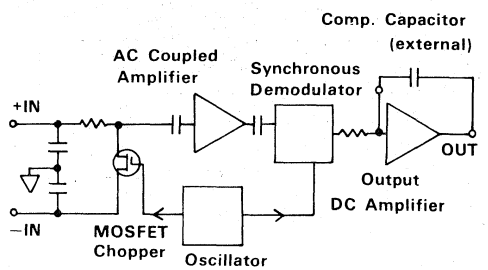


Figure 7. Model 261 Block Diagram

APPLICATION NOTES

Measurement of small signals or accurate handling of larger signals always requires care. Model 261 was specifically designed to minimize the problems raised by dc drift. To obtain best results, it is necessary to maintain good engineering practice and to observe a few requirements for optimizing performance of this precision instrument.

OFFSET VOLTAGE AND CURRENT TRIM

With the trim terminal connected to common, initial offset voltage of the model 261 is less than 25μV. An additional offset voltage is developed by the flow of the input bias current through the resistance of the signal source. With a 10,000 ohm source resistance and worst case bias current of 300pA, the maximum additional offset voltage would be only 3μV. For many applications, these offset voltages may be ignored, and the expense of a trim potentiometer and its adjustment is avoided. If the application requires lower offsets, an external 50,000 ohm trim potentiometer may be connected to zero the offset voltages, as shown previously. This trimming operation will not affect the drift or noise characteristics of the model 261.

INVERTING AND DIFFERENTIAL INPUT OPERATION

The input current to the amplifier's (–) terminal is less than ±10nA. Differential input operation of the amplifier is allowable, but the impedance from the inverting terminal to ground should not exceed 5000 ohms, and the common mode voltage range for best performance should not be exceeded. For purely inverting applications the user should select Analog Devices' models 234 or 235 chopper stabilized amplifiers, which are optimized for inverting operation.

SELECTABLE BANDWIDTH

For practical low-frequency applications, the model 261 uses an external compensation capacitor to determine the gain-bandwidth product. Its value may be chosen to allow the use of the maximum 100Hz -3dB bandwidth, at any given value of closed loop gain. By using a larger value of compensation capacitance, the bandwidth can be limited to any desired value below 100Hz, as required by the application. The minimum value of the required compensation capacitor, in μF, is 1000/GB, where G is the desired closed-loop dc gain, and B is the -3dB bandwidth. For example, the minimum value of recommended capacitance (for 100Hz bandwidth to -3dB) is

10/G. Shown in Figure 8 are curves of the amplifier's response for various closed loop gains while using values of capacitance appropriate for maintaining 100Hz (-3dB) bandwidth. Figure 9 illustrates the amplifier's open-loop response with various values of the compensation capacitor. It is recommended that the capacitor be polycarbonate, mylar, mica, glass or polystyrene for best performance.

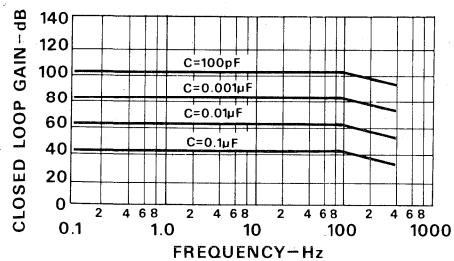


Figure 8. Compensation vs. Gain for 100Hz Bandwidth

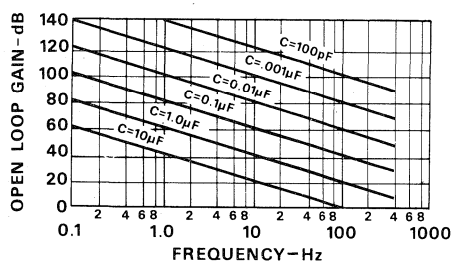


Figure 9. Open Loop Response vs. Compensation

FULL POWER RESPONSE

Full power output at any frequency can be obtained only with closed loop gains exceeding 10. This is due to the common mode voltage limitation described below.

The maximum full power output frequency is 50Hz, and will be obtained when using compensation capacitors of less than 0.013μF. For larger compensation capacitors, f_p is given by the formula:

$$f_p \text{ (Hz)} = 0.66/C \text{ (}\mu\text{F)}$$

When using a low gain, for instance 10, the maximum f_p will be 0.66Hz due to the 1.0μF required compensation capacitor for this closed loop gain. Under such conditions the user may wish to employ the compensation circuit of Figure 10. This will increase f_p to 5Hz (for a gain of 30). For higher gains, an increase in f_p will be obtained (with the same circuit), although the rise in f_p will not be proportionately as large.

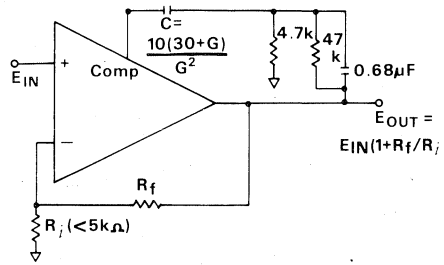


Figure 10. Compensation for Increased f_p

COMMON MODE CONSIDERATIONS

In the model 261, the maximum safe input voltage, both differential and common mode, exceeds ±20 volts. However, in order to maintain the specified Common Mode Rejection Ratio of 300,000 it is necessary that common mode voltage be limited to ±1.0 volts for the model 261K and ±0.5 volts for the model 261J. These values will not be exceeded by normal input signal swings if the amplifiers closed loop gain exceeds 10 and 20, respectively. Since most applications will use this amplifier at gains of 100 or more, the specified common mode range should prove entirely adequate.

COMMON MODE REJECTION

Model 261 is designed to provide high stability, high gain and low noise in non-inverting applications where the high input impedance minimizes input signal attenuation. Although operation as a differential amplifier is possible, it is not recommende

In the non-inverting mode, there is a source of error due to the common mode voltage; however this error term can be completely ignored since the error due to open loop gain will dominate.

INVERTING INPUT TERMINAL RESISTANCE (R_i)

An attempt should be made to maintain low resistance from the inverting input terminal to ground. This will prevent the negative input's bias current from degrading the offset performance of the amplifier. This restriction in no way relates to the source resistance seen by the positive (non-inverting) input terminal.

Instrumentation Amplifiers

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●New product since the 1979 *Data Acquisition Products Catalog Supplement.*

Selection Guide
Instrumentation Amplifiers

The abbreviated specifications listed here permit a choice on the basis of the key parameters of instrumentation amplifiers, depending on which parameters are critical for the application. Complete and detailed specifications can be found in the data-sheet section.

Descriptive information on instrumentation amplifiers and a guide to specifications are provided on the following pages. Devices that perform instrumentation-amplifier functions can also be found in sections 3 (Isolation Amplifiers), 8 (Signal Conditioners), 15 (Data-Acquisition Systems), and 16 (Computer Interfaces).

All specifications are typical at rated supply voltage and load, and $T_A = 25°C$, unless otherwise noted.

	AD522A/B/S **Hybrid IC** **Gain Programmed** **by External Resistor**	**610J/K/L** **Module** **Gain Programmed** **by External Resistor**	**612A/B/C/D/E●** **Hybrid IC** **Jumper-Programmable** **Gains in Binary** **Sequence 2^0 to 2^{10}**	**AD521J/K/L/S#** **Monolithic IC** **Gain Programmed** **by Ratio of** **External Resistor Pair**
Nominal Gain Range, V/V	1 to 1000	1 to 10,000	1 to 1,024	1 to 1000
Gain Tempco, ppm/°C	2 max, G = 1 50 max, G = 1000	±15 max	±10 max	±(3 ± 0.05G)(J, K, L) ±(15 ±0.4G)S
Nonlinearity, max (G = 100)	0.01%/0.005%/0.005%	0.01%	0.001% typ	0.2%/0.2%/0.1%/0.2% max
Offset Tempco RTI, µV/°C				
G = 1	50/25/100 max	200/150/150	200/150/100/150/100 max	400/150/75/150 max
G = 1000*	6/2/6 max	3/1/0.5 max	5/3/1/5/3 max	15/5/2/5 max
I_{BIAS}, nA max	±25/15/25	+60	+100	80/40/40/40
I_{BIAS} Tempco	±100/50/100pA/°C	−0.2nA/°C	0.5nA/°C	1/0.5/0.5/0.5nA/°C max
I_{OS}, nA	±20/10/20 max	±5	±0.5	20/10/10/10 max
I_{OS} Tempco, pA/°C	±100/50/100	±20	±25	250/125/125/125 max
Noise, RTI, 0.1Hz – 10Hz, µV p-p				
G = 1	15	50(0.01 – 10Hz)	20(0.01 – 10Hz)	225
G = 1000*	1.5	2.5/2/2 max (0.01 – 10Hz)	1(0.01 – 10Hz)	0.5
CMR at rated CMV				
1kΩ Unbalance, Frequency:		DC to 100Hz	DC to 60Hz	DC to 60Hz
G = 1, dB min	75/80/75 DC to 30Hz	60	74/84/90/74/84	70/74/74/74
G = 10, dB min	90/95/90 DC to 10Hz	80		90/94/94/94
G = 100, dB min	100 DC to 3Hz	86		100/104/104/104
G = 1000*, dB min	100/110/100 DC to 1Hz	90	90/100/106/90/100	100/110/110/110
Small Signal Frequency Range, kHz −3dB, typ				
G = 100‡	3	100	60/60/60/120/120	200
Settling Time to 0.1% ±10V output Step				
G = 100‡	5ms	30µs	100/100/100/25/25µs max	10µs
Temperature Range†	I/I/M	C	I	C/C/C/M
Page	2-13	*	2-17	2-7

*G = 1,024 for Model 612
†C: 0 to +70°C, I: −25°C to +85°C; M: −55°C to +125°C.
‡G = 128 for model 612, settling time to 0.05%
§A data sheet on the 610J/K/L is available upon request.
●New product since the 1979 *Data Acquisition Products Catalog Supplement.*
=Monolithic chips available with guaranteed performance for precision hybrids.
#Data sheet available upon request.

Orientation
Instrumentation Amplifiers

An instrumentation amplifier is a committed "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain – usually from 1V/V to 1000V/V or more – and causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 1,

$$V_S - V_R = G\,(V^+ - V^-)$$

An ideal instrumentation amplifier responds only to the *difference* between the input voltages. If the input voltages are equal ($V^+ = V^- = V_{CM}$, the *common-mode voltage*), the output of the ideal instrumentation amplifier will be zero.

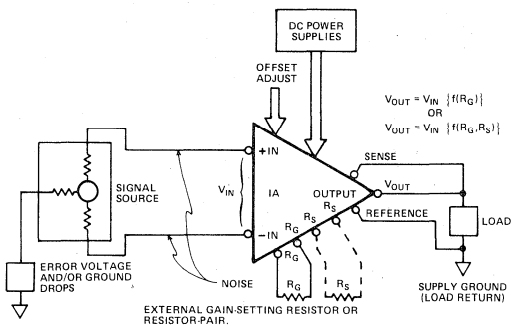


Figure 1. Basic Instrumentation Amplifier Functional Diagram

An amplifier circuit which is optimized for performance as an instrumentation-amplifier gain block has high input impedance, low offset and drift, low nonlinearity, stable gain, and low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples include: transducer amplification – for thermocouples, strain-gage bridges, current shunts, and biological probes, preamplification of small differential signals superimposed on high common-mode voltages, signal conditioning and (moderate) isolation for data acquisition, and signal translation for differential and single-ended signals wherever the common "ground" is noisy or of questionable integrity.

Instrumentation-amplifier modules and IC's are usually chosen in preference to user-assembled op-amp circuitry, because they offer optimized, specified performance in low-cost, easy-to-use, compact packages. If the application calls for high common-mode voltages (typically, voltages in excess of the amplifier supply voltage), or if isolation impedances must be very high (e.g., $10^{10}\,\Omega$, with galvanic isolation, as in medical and industrial applications), the designer should consult the *Isolator* section of this catalog (Section 3).

SPECIFYING INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier chosen for a given application will be the lowest-cost device that satisfies the performance and environmental requirements. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. It is essential that the designer have a firm understanding of the specifications of instrumentation amplifiers and of the contributions of the various sources of error to the total error. The data sheets provide much useful application data on these devices, as well as examples of basic error analyses.

Definitions of the key specifications follow a brief discussion of instrumentation-amplifier architectures. For more-complete information on the fundamentals and applications of instrumentation amplifiers, a number of publications are available from Analog Devices.[1,2,3]

INSTRUMENTATION-AMPLIFIER ARCHITECTURE

All Analog Devices instrumentation amplifiers have two high-impedance input terminals, a set of terminals for gain-programming, an "output" terminal, and a pair of feedback terminals, labeled *sense* and *reference*, as well as terminals for power supply and offset trim.*

Two basic circuit concepts are employed. The AD522 and 612 use variations of the well-known three-op-amp configuration (Figure 2), consisting of a differential input-output gain stage and a subtractor stage. Gain ($\geqslant$1V/V) is set by the choice of a single external gain-setting resistor, R_G. Its nominal value is $\frac{400{,}000}{G-1}\,\Omega$, for the 610, and $\frac{200{,}000}{G-1}\Omega$, for the AD522. When the *sense* (V_S) feedback terminal is connected to the output terminal, and the *reference* terminal (V_R) is connected to power common, the output voltage appears between the output terminal and power common.

The gain of model 612 is set by connecting a jumper between the appropriate terminals; the gain-setting resistors for a binary progression of gains from 1 to 1024 are included within the package. If desired, other values of gain can be set with external resistance (with some reduction in temperature stability); the required resistance total value is $80k\Omega/(G-1)$.

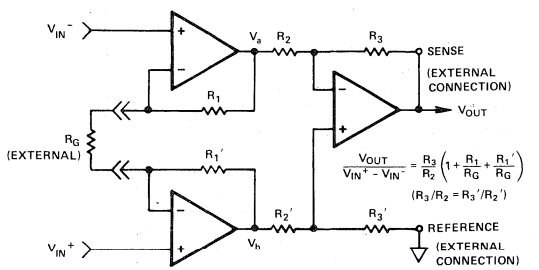


Figure 2. "Classic" 3 Op Amp Instrumentation Amplifier

The second circuit approach, employed in the case of the monolithic AD521 (Figure 3), employs two differential-input fol-

[1] *"Isolation and Instrumentation Amplifiers Designer's Guide*, 1978 edition, available upon request.
[2] "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, 1978, available upon request.
[3] *Transducer Interfacing Handbooks*, D.H. Sheingold, ed., 1980, $14.50, Analog Devices, Inc., P.O. Box 796, Norwood, MA 02062.
*In Model 612, *sense* is internally connected to the output terminal.

lower pairs to generate the currents, $\frac{V_1 - V_2}{R_G}$, and $\frac{V_S - V_R}{R_S}$

The current difference is applied to a control amplifier, and, with the feedback loop closed (for example, V_S to the output terminal and V_R to system ground or the supply midpoint), the currents are servoed to be equal, and the nominal gain is thus equal to the ratio, R_S/R_G, making possible a wide range of gain, including gains of less than unity.

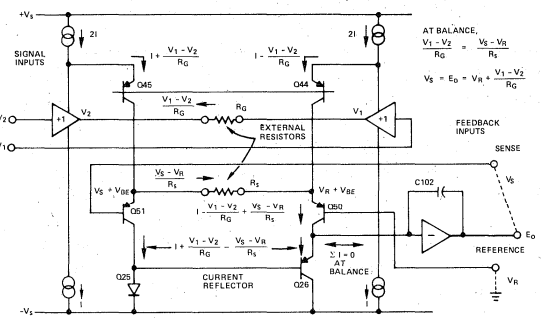


Figure 3. Simplified Schematic Diagram of the AD521 Instrumentation Amplifier

The V_S and V_R terminals may be used for remote sensing — to establish precise outputs in the presence of line drops; they may be used with an inside-the-loop booster follower to obtain power amplification without loss of accuracy; and they may be used to establish an output current that is precisely proportional to the difference signal. A voltage applied to the V_R terminal will bias the output by a predetermined amount. It is important always to maintain very low impedance (in relation to the specified V_S and V_R input impedances), when driving the V_S and V_R inputs, in order not to introduce common-mode, gain, and/or offset errors. In devices using the 3-amplifier configuration, the V_R terminal is sometimes used for "tweaking" common-mode rejection.

SPECIFICATIONS

Specification tables are generally headed by the legend: "specifications are typical at $V_S = \pm 15V$, $T_A = +25°C$, and rated load, unless otherwise noted." This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature), the significant effects are usually indicated within the specs. "Typical" means that the manufacturer's characterization process has shown this number to be "average," but individual devices vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Such specs are not uniquely applicable to instrumentation amps.

GAIN These specifications refer to the linear transfer function of the device; for example, the AD522 gain equation is: $G = 1 + \frac{200{,}000}{R_G}$ V/V. The value of R_G for a given gain value is: $R_G = \frac{200{,}000}{G - 1}\Omega$. For example, if G is to be 100 V/V, $R_G = 2020.2$ ohms.

Gain Range Specified at 1 to 1000, for example, the device may work at higher gains (1 V/V is minimum, except for the AD521), but the manufacturer does not specify performance outside the range. In practice, noise and drift may make higher gains impractical for a given device.

Equation Error (or "Gain Accuracy") The number given by this specification describes deviation from the gain equation when R_G is at its nominal value (or, in the case of model 612, when connected for a given gain). The user can trim the gain or compensate for gain error elsewhere in the overall system. Systems using microprocessors (or computers, or other digital "intelligence") can be made self-calibrating, to take into account the lumped gain errors of all the stages in the analog portion of the system, from transducer to a/d converter.

Nonlinearity (or Gain Nonlinearity) Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best straight line," with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

Gain vs. Temperature These numbers give the deviations from the gain equation as a function of temperature.

SETTLING TIME is defined as that length of time required for the output voltage to approach and remain within a certain (±) tolerance of its final value. It is usually specified for a fast step that will drive the output through its full-scale range and it includes slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%, nor is settling time necessarily proportional to gain. Principal contributing factors include slew-rate limiting, underdamping (ringing), and thermal gradients ("long tails").

VOLTAGE OFFSET Voltage offset and common-mode rejection (see below) specifications are often considered the key figures of merit for instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involve "intelligent" processors can correct for offset errors in the whole measurement chain, but such applications are still relatively infrequent; in most applications, the instrumentation amplifier's contribution to system offset error must be defined.

Voltage offset and offset drift in instrumentation amplifiers are functions of gain.[4] The offset, measured at the output, is equal to a constant plus a term proportional to gain. For an amplifier with specified performance over a gain range from 1 to 1000, the constant is essentially the offset at unity gain, and

[4] There is a good explanation of the specification of offset in instrumentation amplifiers in ANALOG DIALOGUE 6–2 (1972), p. 14

the proportionality term (or slope) is equal to the change in output offset between G = 1 and G = 1000, divided by 999. To refer offset to the input (RTI), divide the total output offset by the gain. Since offset at a gain of 1000 is dominated by the proportional term, the slope is often called the "RTI offset, G = 1000." At any value of gain, the offset is equal to the unity-gain offset plus the product of the gain and the "RTI offset, G = 1000".

The same considerations apply to the offset drift. For example, the maximum RTI drift of the AD522B is specified at 25μV/°C at G = 1, 2μV/°C at G = 1000, and $(\frac{25}{G} + 2)$ μV/°C at any arbitrary gain in the range. Thus, the output drift is (25 + 2G)μV/°C at any gain, G, in the range. The data sheets provide offset-vs.-gain plots, but the function is easily computed in the manner described above.

Voltage offset as a function of power supply level is also specified RTI at one or more gain settings.

INPUT BIAS AND OFFSET CURRENTS Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the junction-leakage of FET's. FET-input devices have lower bias currents than those using bipolar transistors, but FET leakage currents increase dramatically with temperature, approximately doubling every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

Important Note
Although instrumentation amplifiers have differential inputs, there *must* be a return path for the bias currents. If it is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of "floating" sources, such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to common, or to the *guard* terminal. If a dc return path is impracticable, an *isolator* must be used (see Section 3).

COMMON-MODE REJECTION (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full-range common-mode voltage change (CMV), at a given frequency, and a specified imbalance of source impedance (e.g. 1kΩ source unbalance, at 60Hz). CMR is a logarithmic expression of the *common-mode rejection ratio* (CMRR): CMR = 20 $\log_{10}$ (CMRR). The common-mode rejection ratio is defined as the ratio of the signal gain, G, to the ratio of common mode signal appearing at the output to the input CMV.

In most instrumentation amplifiers, the CMR increases with gain, because the front-end configuration does not amplify common-mode signals, and the amount of common-mode signal appearing at the output stays relatively constant as the signal gain (G) increases.

However, at higher gains, amplifier bandwidth decreases. Since differences in phase shift through the differential input stage will show up as common-mode errors, CMR becomes more frequency-dependent at high gains.

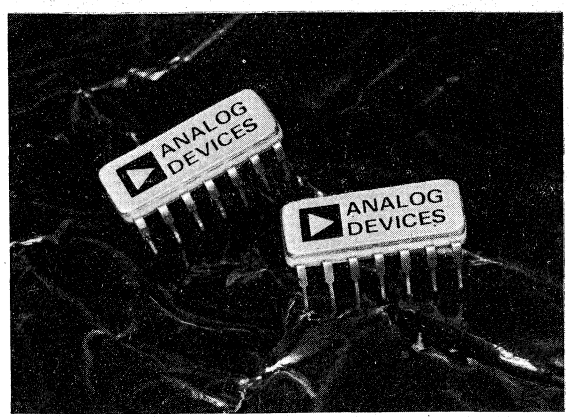
ANALOG DEVICES

Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Extremely Low Cost



PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9 \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the full MIL-temperature range: −55°C to +125°C. All versions are packaged in a hermetic 14-pin DIP.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
3. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
4. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
5. Offset nulling can be achieved with an optional trim pot.
6. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.
7. Every AD521 receives a 24 hour stabilization bake at +150°C to ensure high reliability and excellent long-term stability.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521J	AD521K	AD521L	AD521S
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	*	*	*
Equation	$G = R_S/R_G V/V$	*	*	*
Error from Equation	(±0.25–0.004G)%	*	*	*
Nonlinearity (Note 2)				
1≤G≤1000	0.2% max	*	0.1% max	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	*	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*	*
Impedance	0.1Ω	*	*	*
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>2MHz	*	*	*
G = 10	300kHz	*	*	*
G = 100	200kHz	*	*	*
G = 1000	40kHz	*	*	*
Small Signal, ±1.0% Flatness				
G = 1	75kHz	*	*	*
G = 10	26kHz	*	*	*
G = 100	24kHz	*	*	*
G = 1000	6kHz	*	*	*
Full Peak Response (Note 3)	100kHz	*	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*	*
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7μs	*	*	*
G = 10	5μs	*	*	*
G = 100	10μs	*	*	*
G = 1000	35μs	*	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	*	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	*	*	*
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	2μV/°C max	**
vs. Supply	3μV/%	*	*	*
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	**
vs. Supply (Note 6)	$0.005V_{OS_O}$/%	*	*	*
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs. Supply	2%/V	*	*	*
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	$3 \times 10^9 \Omega \| 1.8pF$	*	*	*
Common Mode Input Impedance (Note 8)	$6 \times 10^{10} \Omega \| 3.0pF$	*	*	*
Input Voltage Range for Specified Performance (with respect to ground)	±10V	*	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*	*
Voltage at either input (Note 9)	V_S ±15V	*	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\,\mu V$	*	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\,\mu V$	*	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*	*
REFERENCE TERMINAL				
Bias Current	3μA	*	*	*
Input Resistance	10MΩ	*	*	*
Voltage Range	±10V	*	*	*
Gain to Output	1	*	*	*
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	*	*	*
Quiescent Supply Current	5mA max	*	*	*
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	*	*	–55°C to +125°C
Operating	–25°C to +85°C	*	*	–55°C to +125°C
Storage	–65°C to +150°C	*	*	*

*Specification same as AD521J.
**Specification same as AD521K.

Specifications subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S −0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

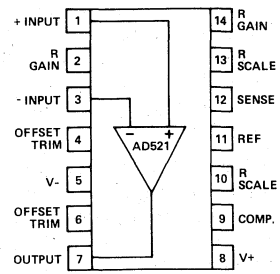
8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 10.

DESIGN PRINCIPLE

Figure 3 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.



TOP VIEW

Figure 1. AD521 Pin Configuration

TO-116

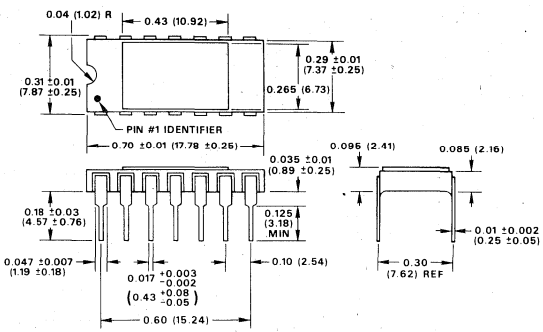


Figure 2. Physical Dimensions. Dimensions shown in inches and (mm).

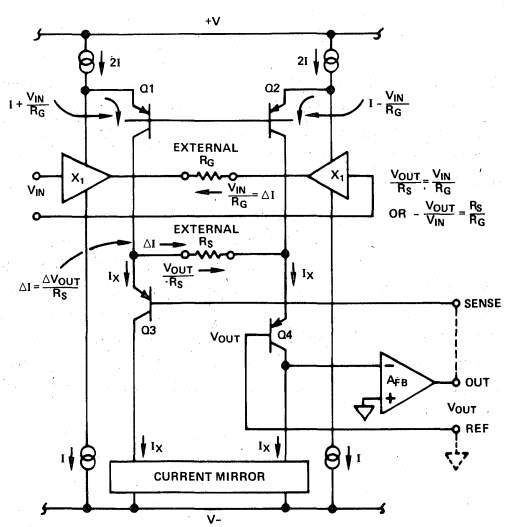


Figure 3. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 and above 1000 are realized by adjusting the gain setting resistors as shown in Figure 4 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V especially for gain equal to or less than 1.

2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 5. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

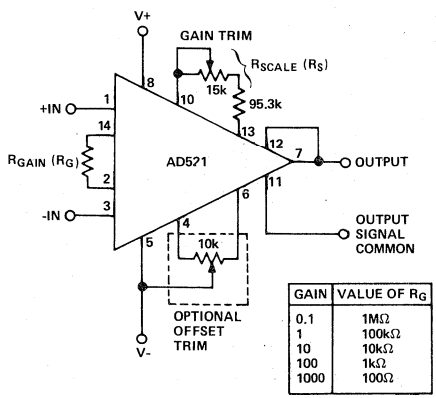
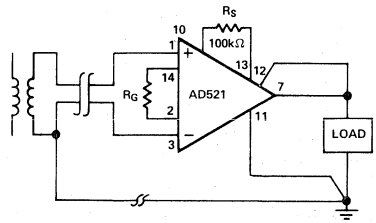


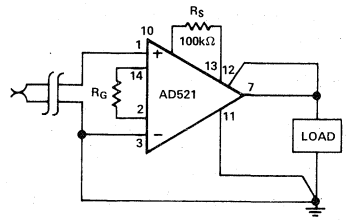
Figure 4. Operating Connections for AD521

3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 4). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.

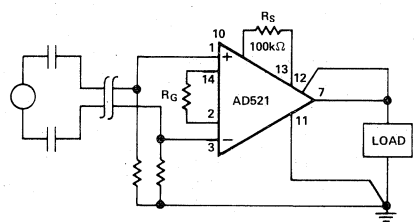
4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 6. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.



a). Transformer Coupled, Direct Return



b). Thermocouple, Direct Return



c). AC Coupled, Indirect Return

Figure 5. Ground Returns for "Floating" Transducers

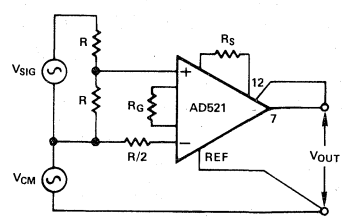


Figure 6. Operating Conditions for $V_{IN} \approx V_S = 10V$

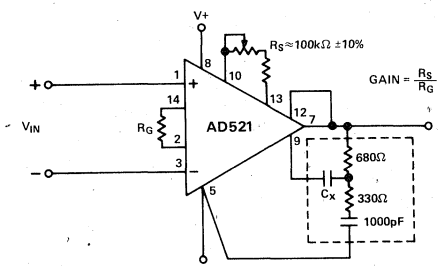
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 7. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V– to the output with little or no attenuation. Therefore, it is advisable to decouple the V– supply line to the output common or to pin 11.[1]



$$C_X = \frac{1}{100\pi f_t}$$ *when f_t is the desired bandwidth.*

(f_t in kHz, C_X in μF)

Figure 7. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 4) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 8, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_G). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.

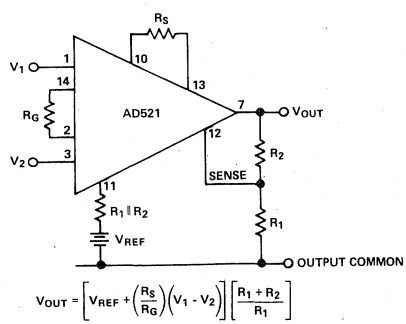


Figure 8. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R_1 and R_2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 8.

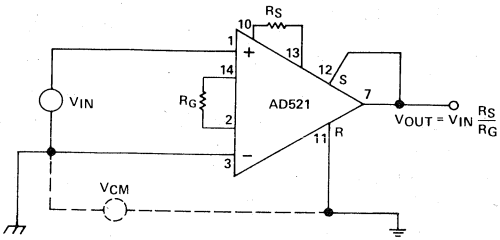


Figure 9. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

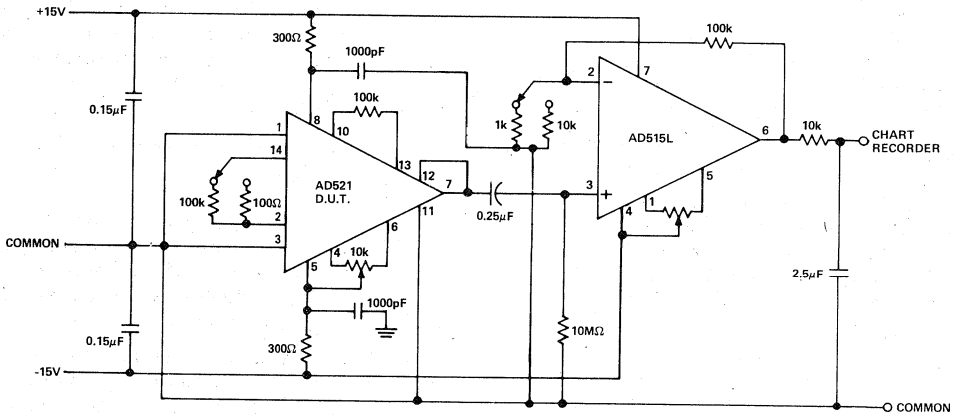


Figure 10. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

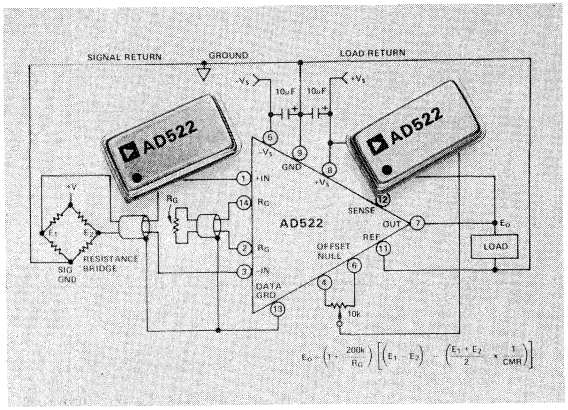
- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)
- Hermetically-Sealed, Electrostatically Shielded DIP

Versatility

- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR
- Low Cost



PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gauges, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

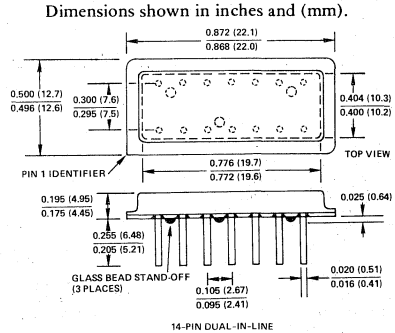
The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\,\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the military/aerospace temperature range of -55°C to +125°C. All versions are packaged in a hermetically-sealed, electrostatically shielded 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

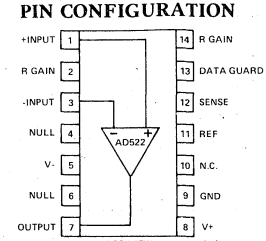
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



14-PIN DUAL-IN-LINE

PIN CONFIGURATION



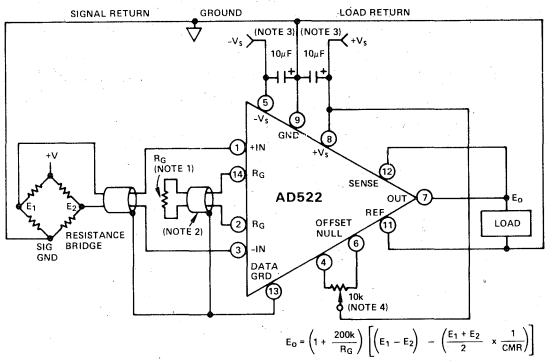
SPECIFICATIONS (typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25°C$ unless otherwise specified)

MODEL	AD522A	AD522B	AD522S
GAIN			
Gain Equation	$1 + \frac{2(10^5)}{R_g}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	**
G = 100	0.01%	0.005%	**
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	*	*
DYNAMIC RESPONSE (see Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/μs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
$1 < G < 1000$	$\pm(\frac{50}{G} + 6)\mu V/°C$	$\pm(\frac{25}{G} + 2)\mu V/°C$	$\pm(\frac{100}{G} + 6)\mu V/°C$
vs. Supply, max			
G = 1	±20μV/%	*	*
G = 1000	±0.2μV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	±15nA	±25nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
Input Offset Current			
Initial max, +25°C	±20nA	±10nA	±20nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
INPUT			
Input Impedance			
Differential	$10^9\Omega$	*	*
Common Mode	$10^9\Omega$	*	*
Input Voltage Range			
Maximum Differential Input, Linear	±10V	*	*
Maximum Differential Input, Safe	±20V	*	*
Maximum Common Mode, Linear	±10V	*	*
Maximum Common Mode Input, Safe	±15V	*	*
Common Mode Rejection Ration, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1.5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	±8mA

*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



NOTES:
1. GAIN RESISTOR R_G SHOULD BE <5ppm/°C (VISHAY TYPE RECOMMENDED).
2. SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS. WHEN NOT USED, THE DATA GUARD PIN CAN BE LEFT UNCONNECTED.
3. POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS.
4. NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202-Y-10k) IS RECOMMENDED.

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table 1)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table 1 lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocessor controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec. Sheet and Fig. 4)	±0.002	±0.002
Voltage Drift	$\frac{25\mu V/^\circ C}{\text{Gain}} + 2.0\mu V/^\circ C = 4.5\mu V/^\circ C$ R.T.I. = 0.00055%/°C (from Spec. Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs. F vs. G, typical curve)	±0.005	±0.005
Noise, R.T.O. (0.1 to 100Hz)	15μV (p-p) R.T.O. (from Spec. Sheet, Noise vs. G typical curve)	±0.0015	±0.0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec. Sheet) = ±50μV/°C = ±1.25μV R.T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table 1. Error Sources

these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

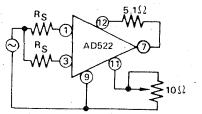


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in four drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

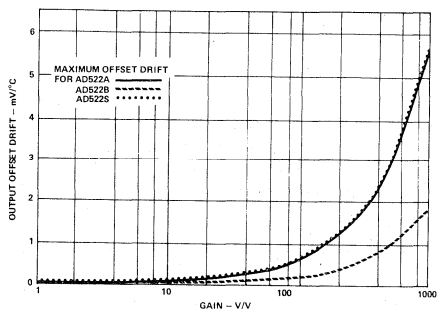


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

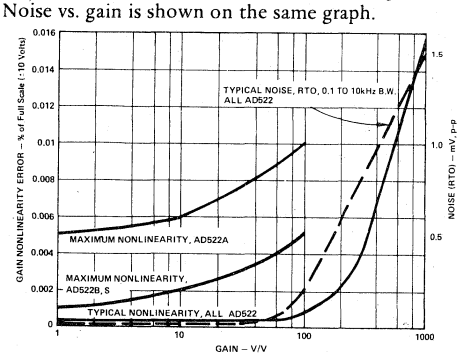


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

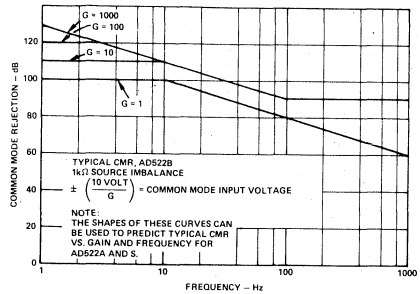


Figure 5. Common Mode Rejection vs. Frequency and Gain

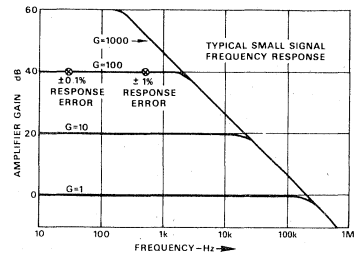


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

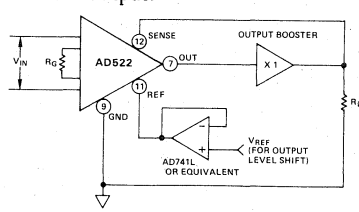


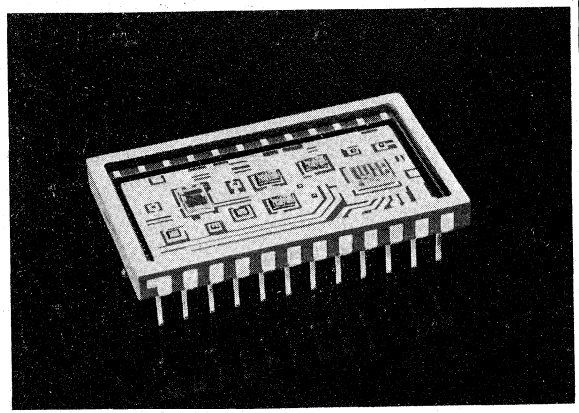
Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

Self-Contained High Performance Wide Band Instrumentation Amplifier

Model 612

PRELIMINARY TECHNICAL DATA



FEATURES

- Internal Gain Setting Resistors
- Wide Gain Range: 1 to 1024 in Binary Steps
- Settling Time: 30μs max to 0.01%, G = 128
- Low Gain Error: ±0.02% max
- Low Gain Drift: ±10ppm max
- Low Offset Voltage Drift: ±1.5μV/°C max, RTI, G = 1024V/V
- High CMR: 94dB min, G = 1024/V/V

APPLICATIONS

- Low Level High Speed Data Acquisition Systems
- Bridge Amplifiers for Resistance Transducers
- Precision Current Amplifiers
- Preamplifier for Recorder Instrumentation

PRODUCT DESCRIPTION

Model 612 is a self-contained, high accuracy, high speed hybrid instrumentation amplifier designed for data acquisition applications requiring speed and accuracy under worst-case operating conditions. Five selections of the model 612 are available: the A, B and C selections provide superior dc characteristics with good dynamic performance, while the D and E selections provide superior dynamic performance with good dc characteristics.

The model 612 contains a precision thin-film resistor network that allows the user to set the gain in binary steps from 1 to 1024V/V by strapping the appropriate gain pins. In addition the excellent tracking characteristics of the active laser-trimmed thin-film resistors provide maximum gain TC of ±10ppm/°C max.

The model 612 is designed to provide high speed and high accuracy signal conditioning. It provides input offset drift of 1.5μV/°C max, output offset drift of ±75μV/°C max, CMR of 74dB min at unity gain (94dB min at G = 1024) in the highest accuracy version (612C) or 120kHz small signal bandwidth and settling time to 0.01% of 30μs max in the high speed version (612D or E).

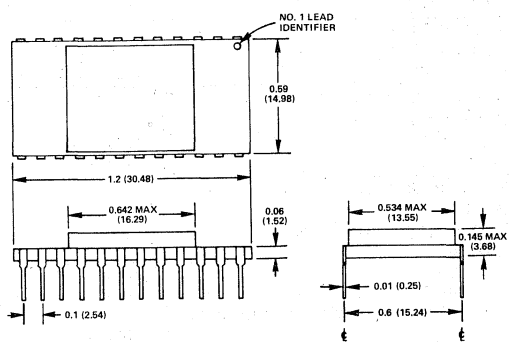
SETTING THE GAIN

The 612 operates at G = 1 if there is no pin strapping. For binary gains 2 thru 256, strap appropriate gain pin (3 thru 10) to the gain programming pin (1). For gain 512, strap both pins 10 and 11 to pin 1; for gain 1024, strap pins 10, 11 and 12 to pin 1. If a nonbinary gain is required, an external resistor (R_G) can be used to set the gain according to the formula G = 1 + 80k/R_G. R_G should be connected to pins 1 and 2.

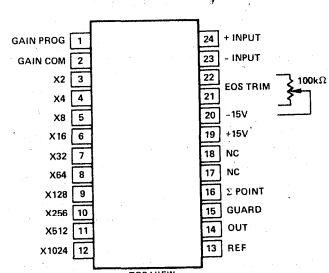
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-PIN DUAL-IN-LINE



PIN CONFIGURATION



SPECIFICATIONS (typical @ +25°C and V_S = ±15V, unless otherwise noted)

MODEL	612A	612B	612C	612D	612E
GAIN					
Gain Range, in Binary Steps	1 to 1024V/V	*	*	*	*
Gain Temperature Coefficient	±10ppm/°C max	*	*	*	*
Gain Accuracy, R_L = 10kΩ	±0.1% max	±0.05% max	±0.02% max	±0.1% max	±0.05% max
Gain Nonlinearity	±0.001%	*	*	*	*
RATED OUTPUT					
Voltage	±10V min	*	*	*	*
Current	±5mA min	*	*	*	*
Impedance	±0.15Ω	*	*	*	*
INPUT CHARACTERISTICS					
Absolute Max Voltage	±V_S	*	*	*	*
Common Mode Voltage	±10V min	*	*	*	*
Differential and Common Mode Impedance	10^9‖3Ω‖pF	*	*	*	*
OFFSET VOLTAGES					
Input Offset Voltage					
Initial @ +25°C (Adjustable to Zero)	±0.2mV	*	*	*	*
vs. Temperature (G = 1024)	±5μV/°C max	±3μV/°C max	±1.5μV°C max	±5μV/°C max	±3μV/°C max
vs. Supply (G = 1024)	±25μV/V	*	*	*	*
Output Offset Voltage G = 1					
vs. Temperature	±200μV/°C max	±150μV/°C max	±75μV/°C max	±150μV/°C max	±75μV/°C max
INPUT BIAS CURRENT					
Initial @ +25°C	+100nA max	*	*	*	*
vs. Temperature (–25°C to +85°C)	±0.5nA/°C	*	*	*	*
INPUT DIFFERENCE CURRENT					
Initial @ +25°C	±2nA	*	*	*	*
vs. Temperature (–25°C to +85°C)	±10pA/°C	*	*	*	*
INPUT VOLTAGE NOISE, G = 1024					
0.01Hz to 10Hz	1μV p-p	*	*	*	*
10Hz to 10kHz	2μV rms	*	*	*	*
OUTPUT VOLTAGE NOISE, (G = 1)					
0.01Hz to 10Hz	20μV p-p	*	*	*	*
10Hz to 10kHz	50μV rms	*	*	*	*
COMMON MODE REJECTION RATIO					
1kΩ Source Imbalance, dc to 60Hz					
G = 1024	94dB min	*	*	*	*
G = 1	74dB min	*	*	*	*
DYNAMIC RESPONSE					
Slew Rate	1V/μs	*	*	*	*
Small Signal Bandwidth (–3dB)					
G = 1	100kHz	*	*	*	*
G = 128	60kHz	*	*	200kHz	200kHz
G = 1024	10kHz	*	*	20kHz	20kHz
Settling Time to 0.01% 20V p-p Output Step					
G = 1	200μs max	*	*	100μs max	100μs max
G = 128	100μs max	*	*	30μs max	30μs max
Settling Time to 0.05% 20V p-p Output Step					
G = 1 to 128	60μs max	*	*	20μs max	20μs max
G = 1024	100μs max	*	*	60μs max	60μs max
POWER SUPPLY					
Voltage, Rated Performance	±15V	*	*	*	*
Voltage, Operating	±8V to ±18V	*	*	*	*
Current, Quiescent	±8mA	*	*	*	*
TEMPERATURE RANGE					
Rated Performance	–25°C to +85°C	*	*	*	*
Storage	–55°C to +125°C	*	*	*	*

*Specifications same as 612A.

Specifications subject to change without notice.

Contact factory for complete 6 page data sheet.

Isolation Amplifiers

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●New product since the 1979 *Data Acquisition Products Catalog Supplement.*

Selection Guide
Isolation Amplifiers

In this Selection Guide, isolation-amplifier families are divided into four categories:

1. Isolated Operational Amplifiers
2. Programmable-Gain Isolated Voltage Amplifiers
3. 4-to-20mA-Output Programmable-Gain V-to-I Converters
4. 4-Channel Multiplexed Signal Conditioners

Although (3) and (4) are not catalogued in this section, they are listed in this Selection Guide because they do perform the functions of isolation amplifiers and are likely to be relevant choices for many applications. Data sheets can be found at the listed pages.

The specifications and features are key for each device. Complete and detailed specifications, descriptions, and application information can be found on the data sheets. General information and definitions of important specifications can be found in the pages that follow.

All specifications are typical at rated supply voltage and load, and $T_A = 25°C$, unless noted otherwise.

1. ISOLATED OPERATIONAL AMPLIFIERS

Application	Primary Considerations	Features	Recommended Model	Page
Industrial Instrumentation and Control Systems	Highest Accuracy Functional Versatility High CMV/CMR Isolated Supply	0.025% max nonlinearity, 1μV/°C max input drift, Uncommitted High Performance Op Amp Front End 160dB min CMR @ dc; 3.5kV rms CMV (1 min) Floating Power Supply: ±15V dc @ ±15mA min	277J/K/A	3-7

2. PROGRAMMABLE-GAIN ISOLATED VOLTAGE AMPLIFIERS

Application	Primary Considerations	Features	Recommended Model	Page
Industrial Instrumentation and Control Systems	Highest Linearity True 3-port Synchronizable Widest Bandwidth	Stand-alone or multichannel operation; ±0.012% max nonlinearity (289L); Adjustable gain, 1 to 100V/V, ±0.005%/°C max gain drift; Bandwidth 20kHz small-signal, 5kHz full power; Floating auxiliary power available, ±5mA min at ±15V; Isolation ±2500V peak input-to-output-or-power supply, 120V rms continuous, output-to-power supply; CMR 104dB min at 60Hz, 1kΩ unbalance; Synchronizable either to external 100kHz source or to other 289s by consensus.	289J/K/L●	3-29
Industrial and Medical Instrumentation	Lowest Cost Self-Contained Wide Temperature Range	Nonlinearity ±0.1% (10V p-p output); Adjustable gain, 1 to 100V/V; Drift 10μV/°C (gain = 100V/V); Bandwidth 2.5kHz small-signal; Floating power available, ±13V at 5mA min. Isolation ±1500V peak max; CMR 100dB min, 1kΩ source unbalance.	290A●	3-35
Industrial and Medical Instrumentation	Single Channel Self-Contained Patient Safety High CMR, CMV	±0.05% Nonlinearity, ±75ppm/°C Gain Drift 2.0μA rms max leakage; Defibrillator Protection Floating Power Supply: ±8.5V dc @ ±5mA min 110dB min CMR @ 60Hz, ±5kV pk CMV (Pulse)	284J	3-11
Industrial and Medical Instrumentation	Lowest Cost Wide Temperature Range Multichannel	External drive, 100kHz oscillator, model 281; Nonlinearity ±0.1% (10V p-p output); Adjustable gain, 1 to 100V/V; Drift 10μV/°C (gain = 100V/V); Bandwidth 2.5kHz small-signal; Floating power supply ±13V at 15mA min; Isolation ±1500V peak max, CMR 100dB min, 1kΩ source unbalance	292A●	3-35
Industrial and Medical Instrumentation	Multichannel Reliability High CMR, CMR Isolated Supply	External drive; 100kHz Osc – model 281 Meets IEEE SWC Standard and UL 544 Leakage Std 5kV pk pulse differential and Input/Output CMV 110dB min CMR @ 60Hz; ±15V dc @ ±15mA Isolated Supply	286J 281 (Osc)	3-17 3-17

Industrial Instrumentation and Control Systems	Multichannel High Accuracy Low Cost Smallest Size	Externally carrier-powered; model 947 or 948 driver 0.05% max nonlinearity, 100ppm/°C max gain drift, 5μV/°C max input drift, Adjust. Gain, 1 to 1000V/V, 850V dc diff and in/out CMV, 1″ X 1″ X 0.56″	288J/K 947 (Driver) 948 (Driver)	3-23 3-23 3-23

3. 4-TO-20mA-OUTPUT PROGRAMMABLE-GAIN V-TO-I CONVERTERS

Application	Primary Considerations	Features	Recommended Model	Page
Industrial Instrumentation and Process Control Analog Transmitters and Controllers	High Performance Synchronizable Single Supply Local or Remote Loop Power	Resistor-programmable input range, 0 to +1V to 0 to +10V; Nonlinearity 0.05% max (L); Span drift 0.005%/°C max (L); Single supply, +14V to +32V; Meets IEEE Std. 472 (Transient Protection—SWC) and ISA Standard 50.1 (Isolated current-loop transmitters); Isolation voltage 1500V dc continuous; Stand-alone or multichannel.	2B22J/K/L	8-37

4. 4-CHANNEL MULTIPLEXED SIGNAL CONDITIONERS

Application	Primary Considerations	Features	Recommended Model	Page
Multichannel Transducer Measurements Industrial Measurement and Control Systems	Low-level measurements Multiplexing No Relays Normal-Mode Filtering Low Cost Per Channel	Resistor-programmable full-scale input span (±5mV to ±100mV) for ±5V output; Input offset drift ±1μV/°C max (B), gain drift 25ppm/°C max (B), nonlinearity ±0.02% max; Isolation ±1000V dc, channel-to-channel or channel-to-ground; CMR 156dB min at 60Hz; Inputs protected for up to 130V rms of differential voltage; Scanning rate up to 400 channels per second min; Thermocouple compensation available, see 2B56, Section 8.	2B54A/B●	8-49
Multichannel Transducer Measurements Industrial Measurement and Control Systems	High- or Low-Level Measurements Multiplexing No Relays Normal-Mode Filtering Low Cost Per Channel	Resistor-programmable full-scale input span (±50mV to ±5V) for ±5V output; Input offset drift ±5μV/°C max, gain drift ±25ppm/°C max, nonlinearity ±0.02% max (G = 1 to 100); Isolation ±1000V dc channel-to-channel or channel-to-ground; CMR 156dB min at 60Hz; inputs protected for up to 130V rms of differential range; Scanning rate up to 400 channels per second min.	2B55●	8-49

●New product since 1979 *Data-Acquisition Products Catalog Supplement*

Orientation
Isolation Amplifiers

The *isolation amplifier* (or *isolator*) has an input circuit that is galvanically isolated from the power supply and the output circuit. Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process-control systems.

Analog Devices Isolators described in this catalog use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input circuit.

CHOOSING AN ISOLATOR

The choice of an isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning), and the availability of isolated power for additional external front-end circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, a designers' guide[1], available upon request, provides information useful to the circuit designer.

The devices described in this section are all isolation amplifiers, useful in general-purpose circuit applications for instrumentation amplifiers or op amps where isolation is a necessity. In addition to these devices, there are a growing number of isolators available from Analog Devices that perform dedicated functions, for use where isolation is necessary or desirable. Data sheets for them can be found in other sections of this catalog, and some of their applications can be seen in the *Transducer Interfacing Handbook*[2]. Here is a brief list:

2B54 Thermocouple/mV 4-Channel Multiplexer-Amplifier: Section 8

2B55 Low- or HIgh-Level 4-Channel Multiplexer-Amplifier: Section 8

2B22 Voltage or Current to 4-to-20mA Converter: Section 8

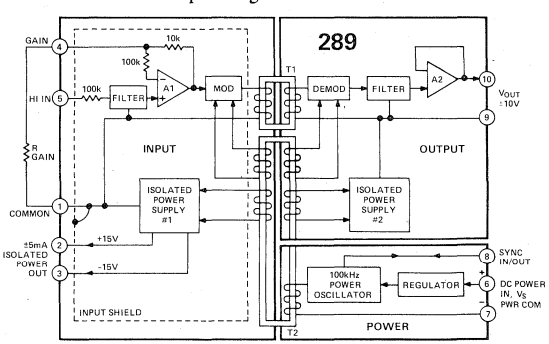
DAC1423 10-Bit Digital to 4-to-20mA Converter: Section 9

AD2036, AD2037, AD2038 Scanning Panel Instruments: Section 8

Isolation is also inherent in transformer-coupled synchro-digital conversion products (Section 12).

Functional Characteristics The figure shows the circuit architecture of a self-contained isolator, Model 289. The various models differ, but their properties can be discussed in terms of the device shown. An isolator of this type requires power from a two-terminal dc supply. An internal oscillator converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output. The ac carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and amplified, using isolated dc power, derived from the carrier.

The amplifier in this example is a resistor-protected op amp (actually, the protection works both ways – it protects the amplifier against differential overloads (120V rms continuous) and it protects sensitive input sources from supply voltage if the amplifier malfunctions), connected for a programmable gain from 1 to 100V/V, as determined by a single external resistor. Since both input terminals are floating, the amplifier functions effectively as an instrumentation amplifier. All but one of the amplifiers in this series function in the instrumentation-amplifier mode, but with various gain ranges. The 277 is an exception; its input stage is an uncommitted high-gain low-drift, low-noise op amp, and the output terminal of the input stage is available for feedback connections to perform a wide range of single-ended or differential operations. Because of the transformer coupling, the outputs of all these devices are isolated from their input stages.



In the figure, it can be seen that the demodulator drive is magnetically coupled from the oscillator to the output stage. This permits the output to operate at a dc common-mode potential with respect to power common. An isolator of this type is said to provide *three-port* isolation, because there are three isolated ports: input, power supply, and output. The 275, the 284, the 285, and the 286 also have this property,

*Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.

[1] *Analog Devices Isolation and Instrumentation Amplifiers Designer's Guide"* (1978)

[2] Sheingold, D.H., ed. *Transducer Interfacing Handbook—A guide to analog signal conditioning.* Norwood MA 02062 (P.O. Box 796): Analog Devices, Inc., 1980, $14.50.

but the demodulator coupling is capacitive. The data sheets carry block diagrams, which show the architecture of each device; 3-port devices, in general, have an output common-mode-voltage spec in the "Rated Output" section. Two-port devices are those in which there is a dc connection between the power supply and the output stage. An example of where a 3-port device might be used: if the isolator power supply is at some distance from the destination (say, a data-acquisition system), line drops could result in common-mode errors if the output were tied to the power supply.

The 289, as can be seen, is a completely self-contained device. There are applications for which a degree of "unbundling" can lead to economy and improved performance. For example, if there are many input channels to be isolated, economies can be realized by the use of a common oscillator. In addition, the common oscillator makes it possible to avoid the possibility of small errors due to beat frequencies developed by small amounts of crosstalk.

Several synchronized multichannel devices are available. Model 292A is essentially a 290A with a power amplifier instead of an oscillator. It requires a dc power input and a pair of leads for a low-power oscillator input, which can be furnished by a 281 synchronizable oscillator. The 281 will drive from one to 16 292As, and it will also synchronize additional 281s for increments of up to 16 292s per 281. The 288 isolator does not require dc power inputs. Instead, the ac input is furnished from 947/948 matching dc-ac high-frequency drivers. The 947, for example, has eight (isolated) output windings, which provide the carrier signal and input power for as many as eight 288Js. Isolated front-end power is provided by rectification and filtering of the 947 "MOD DRIVE" signal. The result is a very inexpensive high-accuracy multichannel system.

SPECIFICATIONS

The illustration on the next page shows a typical specification block and defines the specifications of key interest.

NONLINEARITY – This is the peak deviation from a best straight line, expressed as a % of peak-to-peak output. Should be considered when signal fidelity is of prime importance.

MAX SAFE DIFFERENTIAL INPUT – Max voltage that can be safely applied across input terminals. Important to consider for fail-safe designs in the presence of high voltages.

CMR, INPUT TO GUARD – Indicates ability to reject differential voltage between signal low and guard. Should be considered in applications where guard cannot be connected directly to signal low.

INPUT NOISE – Total noise, referred to the input. Facilitates comparison with expected signal input levels.

ISOLATED SUPPLY – Dual supply voltages, completely isolated from the input power supply terminals; provide the capability to excite floating input signal conditioners, front-end amplifiers, as well as remote transducers.

MODEL	284J
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 10V/V
Formula (R_i in kΩ)	$G = 1 + \frac{100k\Omega}{10.7k\Omega + R_i}$
Deviation from Formula	±3%
vs. Temperature (0 to +70°C)	±0.0075%/°C
vs. Time	±0.001%/1000 hours
Nonlinearity, ±5V Output (G = 1 to 10V/V)	±0.05%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±5V
Max Safe Differential Input	
Continuous	240V rms
Pulse, 10ms Duration, 1 Pulse/10 sec	±6500V pk max
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 minute Duration	2500V rms
Pulse, 10ms Duration, 1 Pulse/10 sec	±2500V pk max
With 510kΩ in series with guard	±5000V pk max
Continuous, ac or dc	±2500V pk
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Pwr Com @ 115V ac, 60Hz	2.0μA rms max
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C	±(5 + 20/G)mV
vs. Temperature (0 to +70°C)	
At Gain = 10V/V	±15μV/°C
At Other Gains	±(1 + 150/G)μV/°C
vs. Supply Voltage	±1mV/%
INPUT IMPEDANCE	
Differential	10^8 Ω‖150pF
Overload	320kΩ
Common Mode	5×10^{10} Ω‖20pF
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C	±0.1nA/°C
INPUT NOISE	
Voltage, Gain = 10V/V	
0.01Hz to 100Hz	8μV pk-pk
10Hz to 1kHz	10μV rms
Current	
0.01Hz to 100Hz	5pA pk-pk
FREQUENCY RESPONSE, GAIN = 1 to 10V/V	
Small Signal Bandwidth, -3dB	1kHz
Slew Rate	25mV/μs
Full Power, Gain = 1V/V	700Hz
Full Power, Gain = 10V/V	200Hz
ISOLATED POWER SUPPLY	
Voltage/Current	±8.5V dc/±5mA
Accuracy	±5%
Regulation, No Load to Full Load	+0, -15%
CMV, Outputs to Pwr. Com.	±50V pk max
RATED OUTPUT	
Voltage, 50kΩ Load	±5V min
Output Impedance	1kΩ
Output Ripple Noise, 1MHz Bandwidth	5mV pk-pk
POWER SUPPLY, SINGLE POLARITY	
Voltage, Rated Performance	+15V dc
Voltage, Operating	+(8V dc to 15.5V dc)
Current, Quiescent	+10mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

CMV, INPUTS TO OUTPUTS – Voltage that may be safely applied to *both* inputs with respect to outputs or power common. Necessary consideration in applications with high CMV input or when high voltage transients may occur at the input.

CMR, INPUTS TO OUTPUTS – Indicates ability to reject common mode voltages between inputs and outputs. Important when processing small signals riding on high common mode voltages.

LEAKAGE CURRENT – Maximum input leakage current when power-line voltage is impressed on inputs. Vital consideration for patient safety in medical applications.

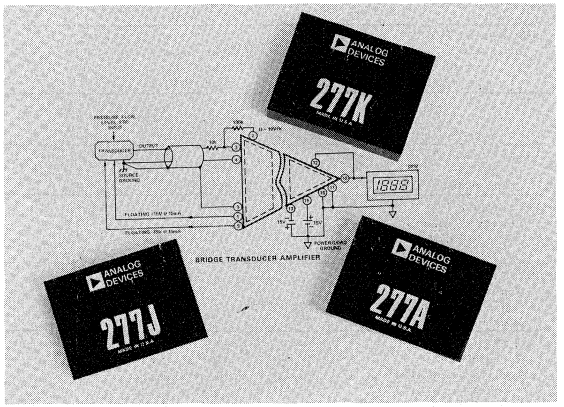
OFFSET VOLTAGE REFERRED TO INPUT – Total input drift is composed of two sources (input and output stage drifts) and is gain (G) dependent. Referring offsets to the input allows them to be compared to signal levels.

OVERLOAD RESISTANCE – This is the apparent input impedance under conditions of amplifier saturation. It limits differential fault currents.

Precision Isolation Amplifier
High CMV/CMR, ±15V Floating Power
MODEL 277

FEATURES
Versatile Op Amp Front End: Inverting, Non-Inverting, Differential Applications
Low Nonlinearity: 0.025% max, Model 277K
Low Input Offset Voltage Drift: 1μV/°C max, Model 277K
Floating Power Supply: ±15V dc @ ±15mA
High CMR: 160dB min @ dc
High CMV: 3500V_{rms}

APPLICATIONS
Programmable Gain Isolated Amplifier
Isolated Power Source and Amplifier for Bridge Measurements
Instrumentation Amplifier
Instrumentation Grade Process Signal Isolator
Current Shunt Measurements



GENERAL DESCRIPTION
Model 277 is a versatile isolation amplifier which combines a high-performance, uncommitted operational amplifier front end with a precision, isolated output stage and a floating power supply section. This configuration, shown in Figure 1, makes the 277 ideally suited to instrumentation applications where the need for various forms of signal conditioning, high CMV protection and isolated transducer power requirements are encountered.

The input stage is a low drift (±1μV/°C max, model 277K) differential op amp that may be connected for use in inverting, non-inverting and differential configurations. The circuitry employed around the operational amplifier input stage can be designed by the user to suit each application's particular signal processing needs. A full ±10V signal range is available at the output of the front end amplifier.

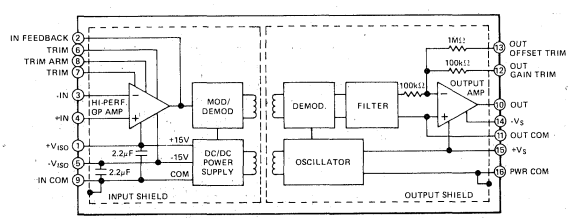


Figure 1. Model 277 Functional Block Diagram

The isolated output stage includes a special modulator/demodulator technique which provides the 277 with 160dB minimum dc common mode rejection between input and output common and an input-to-output CMV rating of 3500V_{rms}. When combined with the output stage's low nonlinearity (0.05%, models 277J/A and 0.025% model 277K), these high CMR and CMV ratings facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays. In addition, model 277A offers a -25°C to +85°C rated operating temperature range. All versions of model 277 have a ±10 volt output range.

The floating power supply section provides isolated ±15 volt outputs capable of delivering currents up to ±15mA. This feature permits model 277 to power transducers and auxiliary isolated circuitry, thereby eliminating the need for a separate isolated dc/dc converter.

All of the features of the model 277 isolation amplifier are packaged in a compact (3" x 2.2" x 0.59") module. As an assurance of high performance reliability, every model 277 is factory tested for CMV rating by application of 3500V_{rms} (±4900V peak) between input and output common terminals for one minute (meets NEMA and CSA requirements for 660V_{rms} service.) In addition, the 277 has a calculated MTBF of 133,000 hours.

SPECIFICATIONS (typical at +25°C and ±15V unless otherwise noted)

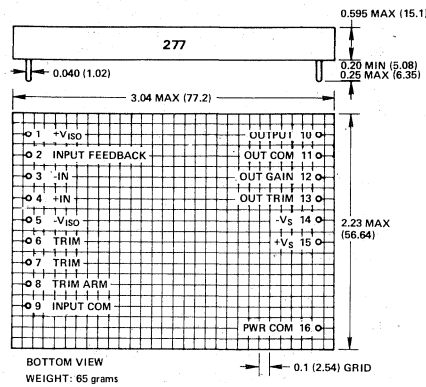
MODEL	277J	277K	277A
INPUT STAGE PERFORMANCE[1,2]			
OPEN LOOP GAIN	106dB min	*	*
INPUT OFFSET VOLTAGE			
Initial, @ +25°C (Adjustable to Zero)	±1.5mV max	*	*
vs. Temperature			
Offset Untrimmed	±5μV/°C max	*	±5μV/°C
Offset Trimmed to Zero	±3μV/°C max	±1μV/°C max	*
vs. Supply Voltage	±30μV/V	*	*
vs. Time	±3.5μV/mo	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	±20nA max	*	*
vs. Temperature	±50pA/°C	*	*
vs. Supply Voltage	±100pA/V	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	±6nA	*	*
vs. Supply Voltage	±50pA/V	*	*
INPUT IMPEDANCE			
Differential	4MΩ	*	*
Common Mode[3]	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.01Hz to 10Hz	1μV p-p	*	*
10Hz to 1kHz	3μV rms	*	*
Current, 0.01Hz to 10Hz	35pA p-p	*	*
INPUT VOLTAGE RANGE			
Common Mode Voltage[3]	±10V min	*	*
Common Mode Rejection[3], CMV = ±10V, 60Hz	100dB	*	*
Max Safe Differential Voltage	±13V	*	*
ISOLATED POWER SUPPLY[4]			
Voltage/Current[2]	±15V @ ±15mA max	*	*
Load Regulation (No Load – Full Load)	+0, -6%	*	*
Line Regulation	1V/V	*	*
Ripple, Full Load	30mV p-p @ 70kHz	*	*
OUTPUT STAGE PERFORMANCE			
GAIN	1V/V	*	*
Gain Error	±0.5% max	*	*
vs. Temperature	±50ppm/°C max	*	*
Nonlinearity, ±10V Output	±0.05% max	±0.025% max	*
VOLTAGE RATINGS[5]			
Max CMV, Output Com/Input Com			
ac, 60Hz, 1 Minute	$3500V_{rms}$ max	*	*
Nonrecurring Spike (<1 Second)	±5000V pk max	*	*
Peak ac or dc, Continuous	±2500V max	*	*
CMR, Output Com/Input Com[5]			
dc	160dB min	*	*
60Hz	120dB min	*	*
Leak. Cur., Input/output $115V_{rms}$, 60Hz	1μA rms max	*	*
ISOLATION IMPEDANCE[5]			
Input Com/Output Com	$10^{12}Ω‖16pF$	*	*
OUTPUT OFFSET VOLTAGE			
Initial, @ +25°C (Adjustable to Zero)	±10mV max	*	*
vs. Temperature	±100μV/°C max	±50μV/°C max	±100μV/° C max
vs. Supply Voltage	±1mV/V	*	*
vs. Time	±100μV/mo	*	*
FREQUENCY RESPONSE			
Small Signal, -3dB	2.5kHz	*	*
Full Power, 20V p-p Output	1.5kHz	*	*
Settling Time ±10V Step to 0.1%	1ms	*	*
RATED OUTPUT			
Voltage/Current	±10V min @ ±5mA min	*	*
OUTPUT NOISE			
Voltage, 0.01Hz to 10Hz	7μV p-p	*	*
10Hz to 1kHz	25μV rms	*	*
POWER SUPPLY[6]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(14 to 16)V dc	*	*
Current, Quiescent	+35, -5mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-25°C to +85°C
Operating	-25°C to +85°C	*	*
Storage	-55°C to +85°C	*	*
CASE SIZE	3.0" x 2.2" x 0.59"	*	*

NOTES:
[1] Current drawn from INPUT FEEDBACK terminal must be ≤5mA.
[2] Total current drawn from IN FEEDBACK and either $+V_{ISO}$ or $-V_{ISO}$ must be ≤15mA.
[3] Input common mode specifications are measured at +IN and -IN terminals with respect to INPUT COM.
[4] Protected for momentary shorts to IN COM.
[5] Isolation specifications are measured at INPUT COM with respect to OUT COM and PWR COM.
[6] Recommended power supply, ADI model 904, ±15V @ ±50mA.
*Specifications same as model 277J.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



MATING SOCKET – AC1053

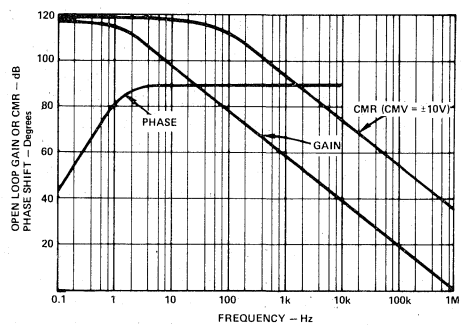


Figure 2. Input Stage Gain, CMR and Phase vs. Frequency

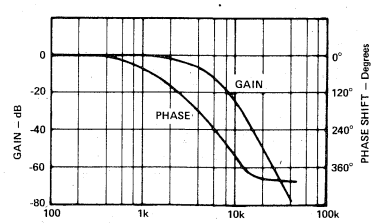


Figure 3. Output Stage Gain and Phase vs. Frequency

PERFORMANCE CHARACTERISTICS

Gain Nonlinearity: Nonlinearity error is expressed as a % of peak-to-peak output voltage span; e.g. ±0.05% @ 10V p-p output = ±5mV max RTO nonlinearity error. Model 277 is available in two maximum nonlinearity grades — ±0.05% (277J/A), ±0.025% (277K).

The nonlinearity of model 277 is virtually independent of output voltage swing. Therefore, the 277 can be used at any level of gain and output signal range up to ±10V while maintaining its excellent linearity characteristics.

Output Voltage Noise: Peak-to-peak output voltage noise is dependent on bandwidth, as shown in Figure 4. The graph shows RTO noise, that is, output noise for a gain of 1V/V through the isolator. For lowest noise performance, a low pass filter at the output can be used to roll-off noise and undesired signal frequencies beyond the bandwidth of interest. As gain increases, voltage noise referred-to-input decreases, resulting in higher input signal to noise ratios. The next section demonstrates how voltage noise, referred-to-input, can be calculated.

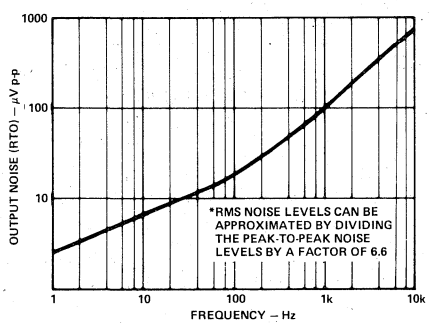


Figure 4. Output Voltage Noise vs. Bandwidth

RTI Offset Voltage, Drift and Noise: Offset voltage, referred to input (RTI) for model 277 may be computed by treating the isolator as two cascaded amplifier stages. The input stage has variable gain G_1 while the output isolation stage has a fixed gain of 1. RTI offset is given by:

$$E_{OS}\ (RTI) = E_{OS_1} + E_{OS_2}/G_1$$

where: E_{OS_1} = total input stage offset voltage
E_{OS_2} = output stage offset voltage
G_1 = input stage gain

Offset voltage drift, RTI, may be calculated in the same manner.

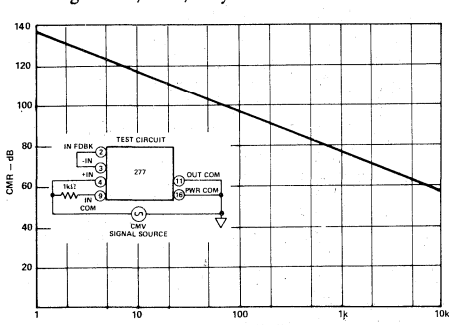


Figure 5. Input-to-Output CMR vs. Frequency with 1kΩ Source Imbalance

RTI noise, in a given bandwidth, (for Figure 8a) may be calculated as follows:

$$E_N\ (rms, RTI) = \sqrt{E_{N_1}^2 + (E_{N_2}/G_1)^2}$$

where: E_{N_1} = total rms input stage voltage noise
E_{N_2} = rms output voltage noise (RTO)

Common Mode Rejection: A 160dB rejection of potential differences between input and output common is achieved in model 277 by maintaining low coupling capacitance between the input and output stages. Input-to-output rejection is a function of frequency as shown in Figure 5 under the adverse condition of 1kΩ in series with IN COM. CMR versus frequency for the input stage is shown in Figure 2.

The section on GUARDING TECHNIQUES & INTERCONNECTION demonstrates how to calculate total CMR error for the isolator and indicates the precautions to be taken to preserve the model 277's inherently excellent CMR performance.

GUARDING TECHNIQUES & INTERCONNECTION

Model 277 CMR performance is best preserved by using shielded signal cable with the shield connected as close as possible to signal low and IN COM to reduce pickup (see Figure 6).

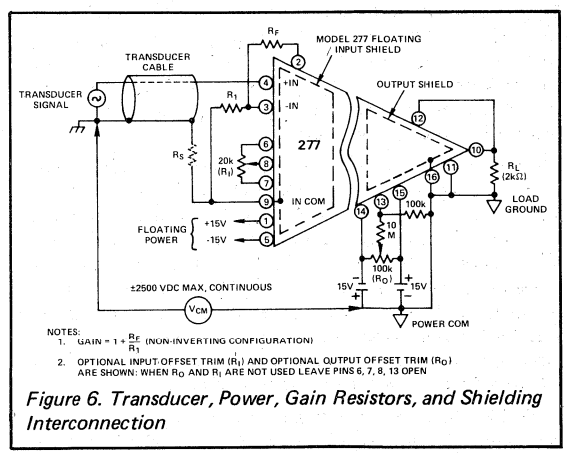


Figure 6. Transducer, Power, Gain Resistors, and Shielding Interconnection

Overall CMR error at the output (e_{err}) is due to the CMR of the input amplifier and the CMR between input and output stages and is given by:

$$e_{err} = \frac{e_{cm}}{CMR_{IN}}(G_1) + \frac{e_{IO}}{CMR_{IO}}$$

where: e_{cm} = input amp CMV with respect to IN COM
e_{IO} = CMV between OUT COM and signal ground
CMR_{IN} = CMR of the input op amp
CMR_{IO} = CMR from input IN COM to OUT COM
G_1 = input stage gain

To preserve CMR_{IN}, amplifier source impedances should be balanced with respect to IN COM. Components connected to the input should be enclosed by a shield tied to IN COM to reduce CMR_{IO} degradation due to unguarded capacitance to ground.

High CMR_{IO} is maintained with low capacitance between IN COM and OUT COM. For best CMR performance, printed circuit layouts should minimize stray capacitance between input and output stages. *Do not run a ground plane under the isolator since this increases input-output coupling.* CMR_{IO} also degrades

at high frequencies by resistance (R_S) between IN COM and signal ground. Voltage between OUT COM and source ground divides between this resistance (generally wire resistance) and the input-to-output capacitance resulting in an input error signal. If R_S becomes excessive, a capacitor from +IN to OUT COM will help compensate for its effect on CMR. The capacitor must withstand the isolation voltages encountered.

ADJUSTMENT PROCEDURE

The input and output offset voltage of model 277 can be trimmed as shown below with the isolator set up in the desired circuit configuration.

(1) Refer to Figure 6 for terminal and component designations.
(2) Connect IN COM to OUT COM and set input signal to zero.
(3) Place floating DVM across IN FDBK and OUTPUT terminals.
(4) Null DVM reading using output offset trim potentiometer R_O.
(5) Disconnect IN COM from OUT COM.
(6) Place DVM across IN FDBK and IN COM terminals.
(7) Adjust input offset trim potentiometer, R_I, until DVM reads zero volts.

The overall gain of the isolator may be increased over a limited range (5%) with a 5kΩ potentiometer connected between pins 10 and 12.

APPLICATIONS

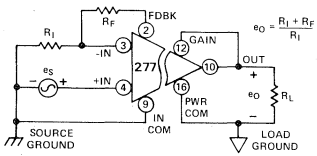
Programmable Gain Bridge Transducer Amplifier: The versatility of model 277 is shown by the programmable gain bridge transducer amplifier application of Figure 7. In this circuit the 277's uncommitted front end and floating voltage output permit both bridge excitation and signal gain conditioning to be provided by the isolation amplifier.

Control switches are driven by TTL inputs which are isolated from source ground by the opto-isolators in the control switch. Control signals operate the CMOS switch network to establish the gains shown in the table in Figure 7. The CMOS switch network is operated in a manner that causes the resistance of the switches only to be in series with the negative input of the isolator and not in series with the gain setting resistors. With this arrangement the switch resistance does not affect gain accuracy. A resistor, R_B, should be in series with -IN to reduce errors due to bias current drift.

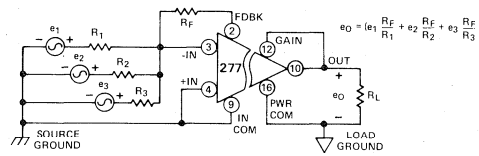
With this circuit the isolator gain can be remotely set at a value that optimizes input signal-to-noise ratio and eliminates the need for high quality post-amplifiers at the isolator output. This network is extremely useful in wide dynamic range measurements such as flow, level or pressure where auto-gain ranging would be a desirable system instrumentation feature.

INPUT CONFIGURATION

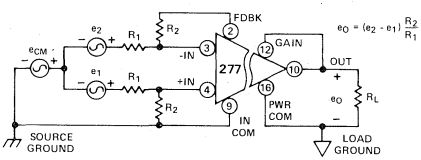
Model 277's input stage is an isolated, uncommitted operational amplifier that may be configured to suit a variety of applications. Model 277 may be used in the same way as any op amp except that the feedback is taken from the FDBK terminal rather than the OUTPUT pin. Figure 8 shows four typical input configurations for interfacing with a wide range of signal sources.



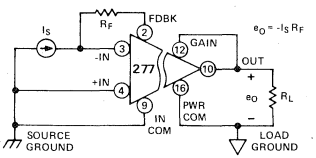
(a) Non-Inverting Configuration



(b) Summing Configuration



(c) Isolated Differential Configuration



(d) Current Source Amplifier Configuration

Figure 8. Model 277 Input Amplifier Configurations

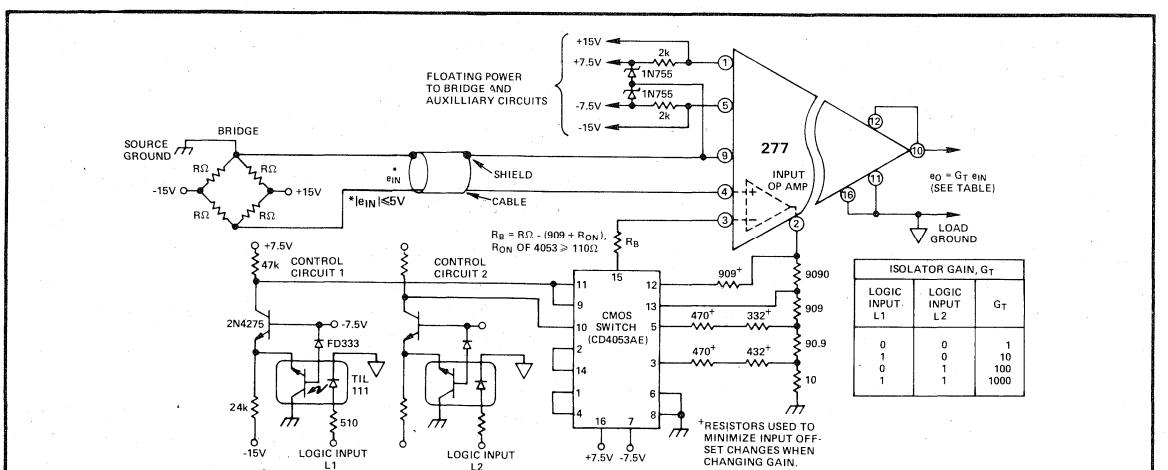


Figure 7. Programmable Gain Bridge Transducer Amplifier

Economy, High Performance, Self-Contained, Isolation Amplifier

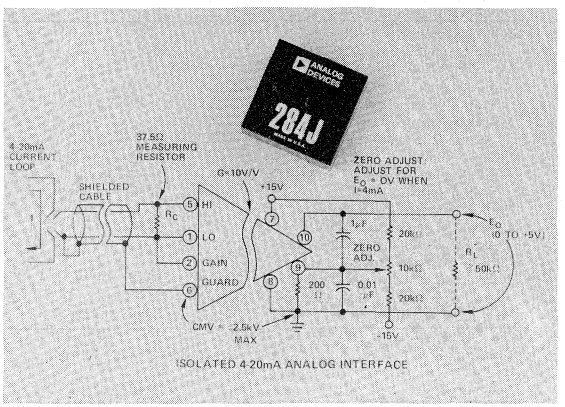
MODEL 284J

FEATURES

- Low Cost
- Low Nonlinearity: ±0.05% @ 10V pk-pk Output
- High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
- Isolated Power Supply: ±8.5V dc @ ±5mA
- High CMR: 110dB min with 5kΩ Imbalance
- High CMV: ±5000V_{pk}; 10ms Pulse; ±2500V dc continuous
- Small Size: 1.5″ x 1.5″ x 0.6″
- Adjustable Gain: 1 to 10V/V; Single Resistor Adjust
- Meets IEEE Std 472: Transient Protection (SWC)
- Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz

APPLICATIONS

- Biomedical and Patient Monitoring Instrumentation
- Ground Loop Elimination in Industrial Control
- Off-Ground Signal Measurements
- 4-20mA Isolated Current Loop Receiver



GENERAL DESCRIPTION

Model 284J is a low cost isolation amplifier featuring isolated power, ±8.5V dc @ ±5mA loads, ±2500V dc off-ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5″ x 1.5″ x 0.6″ epoxy encapsulated package. This improved design achieves low nonlinearity of ±0.05% @ 10V pk-pk output, gain stability of ±0.0075%/°C and input offset drift of ±30μV/°C at G = 10V/V. Using modulation techniques with reliable transformer isolation, model 284J will interrupt ground loops, leakage paths and high voltage transients to ±5kV_{pk} (10ms pulse) providing dc to 1kHz (-3dB) response over an adjustable gain range of 1V/V to 10V/V. Model 284J's fully floating guarded input stage and floating isolated power for external input circuitry, offers versatility for both medical and industrial OEM applications.

WHERE TO USE MODEL 284J

Medical Applications: In all biomedical and patient monitoring equipment such as multi-lead ECG recorders and portable diagnostic designs, model 284J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 284J's low input noise (8μV p-p) and high CMR (110dB, min).

Industrial Applications: In computer interface systems, process signal isolators and high CMV instrumentation, model 284J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface is afforded with model 284J's 10V pk-pk input signal capability at a gain of 1V/V operation. In portable field designs, model 284J's single supply, low power drain of 85mW @ +12V operation offers long battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±8.5V dc @ ±5mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Model 284J's adjustable gain combined with its 10V pk-pk output signal dynamic range offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 10V/V providing the flexibility of applying model 284J in both high level transducer interfacing as well as low level sensor measurements.

Floating, Guarded Front-End: The input stage of model 284J can directly accept floating differential signals, such as ECG biomedical signals, or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Model 284J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 284J has a calculated MTBF of over 400,000 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 284J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

SPECIFICATIONS (typical @ 25°C and V_S = +15V dc unless otherwise noted)

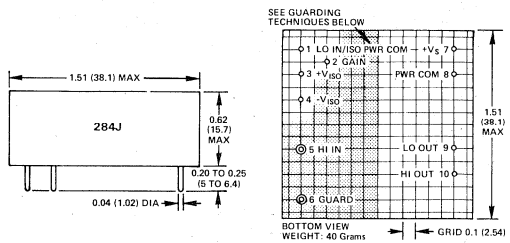
MODEL	284J
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 10V/V
Formula	Gain = $[1 + \frac{100k\Omega}{10.7k\Omega + R_j(k\Omega)}]$
Deviation from Formula	±3%
vs. Time	±0.001%/1000 Hours
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
Nonlinearity, G = 1V/V to 10V/V[2]	±0.05%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±5V min
Max Safe Differential Input	
Continuous	$240V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 6500V_{pk}$ max
Max CMV, Inputs to Outputs	
AC, 60Hz, 1 minute duration	$2500V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 2500V_{pk}$ max
With 510kΩ in series with Guard	$\pm 5000V_{pk}$ max
Continuous, ac or dc	$\pm 2500V_{pk}$ max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common @ 115V ac, 60Hz	2.0μA rms max
INPUT IMPEDANCE	
Differential	$10^8\Omega \| 70pF$
Overload	300kΩ
Common Mode	$5x10^{10}\Omega \| 20pF$
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE	
Voltage, G = 10V/V	
0.05Hz to 100Hz	8μV p-p
10Hz to 1kHz	10μV rms
Current	
0.05Hz to 100Hz	5pA p-p
FREQUENCY RESPONSE	
Small Signal, -3dB, G = 1V/V to 10V/V	1kHz
Slew Rate	25mV/μs
Full Power, 10V p-p Output	
Gain = 1V/V	700Hz
Gain = 10V/V	200Hz
Recovery Time, to ±100μV after Application of $\pm 6500V_{pk}$ Differential Input Pulse	200ms
OFFSET VOLTAGE REFERRED TO INPUT	
Initial, @ +25°C, Adjustable to Zero	±(5 + 20/G)mV
vs. Temperature (0 to +70°C)	±(1 + 150/G)μV/°C
vs. Supply Voltage	±1mV/%
RATED OUTPUT	
Voltage, 50kΩ Load	±5V min
Output Impedance	1kΩ
Output Ripple, 1MHz Bandwidth	5mV pk-pk
ISOLATED POWER OUTPUTS	
Voltage, ±5mA Load	±8.5V dc
Accuracy	±5%
Current	±5mA min
Regulation, No Load to Full Load	+0, -15%
Ripple, 100kHz Bandwidth	100mV p-p
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage Operating	+(8 to 15.5)V dc
Current, Quiescent	+10mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

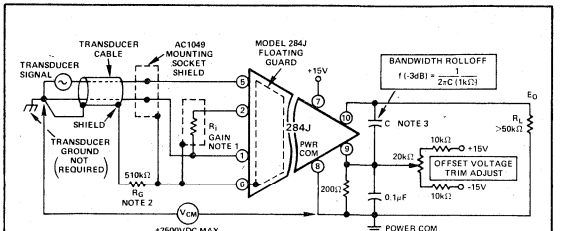


SHIELDED MOUNTING SOCKET AC1049

INTERCONNECTION AND GUARDING TECHNIQUES

Model 284J can be applied directly to achieve rated performance as shown in Figure 1 below. To preserve the high CMR performance of model 284J, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 284J as illustrated in the outline drawing above (screened area). The GUARD (Pin 6) should be connected to this shield. This guard-shield is provided with the mounting socket, model AC1049. A recommended guarding technique using model AC1049 is illustrated in Figure 1. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low.

Offset Voltage Trim Adjust: The trim adjust circuit shown in Figure 1 can be used to zero the output offset voltage over the gain range from 1 to 10V/V. The output terminals, HI OUT and LO OUT, can be floated with respect to PWR COM up to $\pm 50V_{pk}$ max, offering three-port isolation. A 0.1μF capacitor is required from LO OUT to PWR COM whenever the output terminals are floated with respect to PWR COM. LO OUT can be connected directly to PWR COM when output offset trimming is not required.



NOTE 1. GAIN RESISTOR, R_I, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 10V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$GAIN = 1 + \frac{100k\Omega}{10.7k\Omega + R_I(k\Omega)}$$

NOTE 2. GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > $\pm 2500V_{PK}$ ($\pm 5kV_{PK}$ MAX).
R_G MAY BE MOUNTED ON AC1049 MOUNTING SOCKET USING STANDOFF PROVIDED.
(USE ¼ WATT, 5%, CARBON COMPOSITION TYPE; ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR, C, SELECT TO ROLLOFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C = 1.5μF FOR dc TO 100Hz BANDWIDTH).

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 284J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 284J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 35μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 10V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 284J at a gain of 10V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 20pF leakage capacitance between the floating guarded input section and the rest of the circuitry keeps the CMR from being infinite.

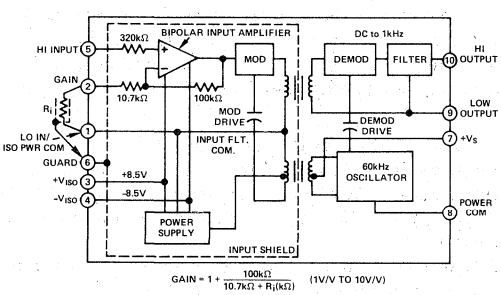


Figure 2. Block Diagram – Model 284J

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 3 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

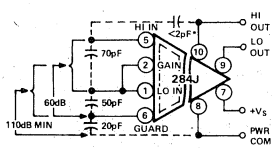


Figure 3. Model 284J Terminal Capacitance and CMR Ratings

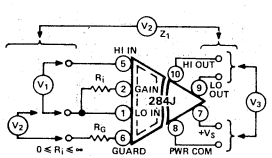


Figure 4. Model 284J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 and Table 1 illustrate model 284J's ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont.)	±2500V_{PK}	Isolation, Steady State
V3 (cont.)	±50V_{PK}	Isolation, DC
Z1	50kMΩ‖20pF	Isolation Impedance

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.0μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 5, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 60kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 284J.

For medical applications, model 284J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies. (e.g. model 284J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 284J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

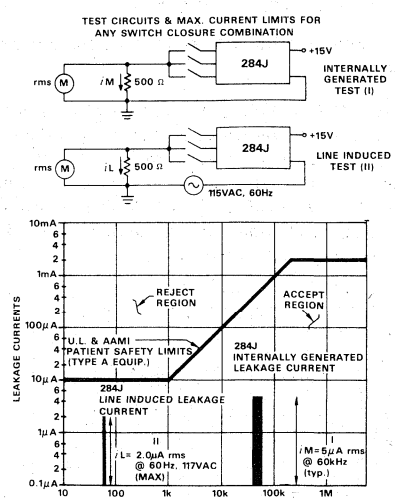


Figure 5. Model 284J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 10V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 146dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 10V/V.

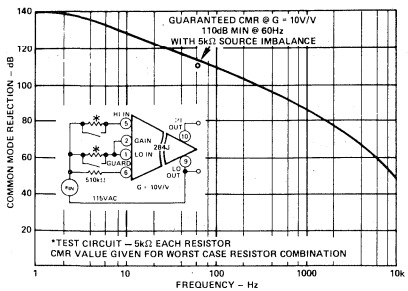


Figure 6. Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 10V/V. CMR is typically 120dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

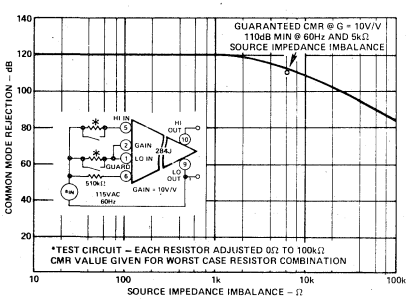


Figure 7. Common Mode Rejection vs. Source Impedance Imbalance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 10V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 8 (1.2μV rms) by 6.6.

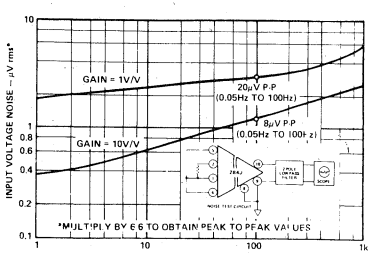


Figure 8. Input Voltage Noise vs. Bandwidth

For lowest noise performance, a low pass filter at the output should be used to selectively roll-off noise, output ripple and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1).

Input Offset Voltage Drift: Total input voltage drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 9 illustrates the total input voltage drift over the gain range of 1 to 10V/V.

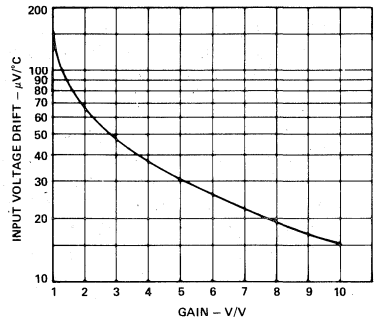
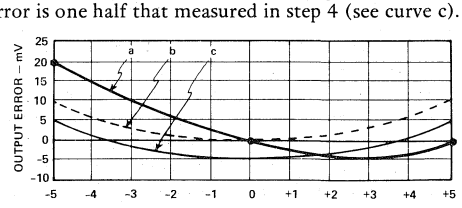


Figure 9. Input Offset Voltage Drift vs. Gain

Gain Nonlinearity: Linearity error is defined as the peak deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g. nonlinearity of model 284J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. In applying model 284J, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error over the operating output voltage span. A calibration technique illustrating how to minimize output error is shown below. In this example, model 284J is operating over an output span of +5V to −5V and a gain of 5V/V.

GAIN AND OFFSET TRIM PROCEDURE

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +1.000V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = −1.000V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply e_{IN} = +1.000V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).



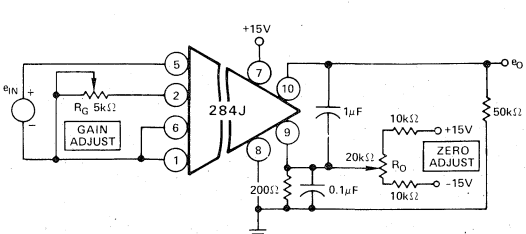


Figure 10. Gain and Offset Adjustment

GROUNDING PRACTICES

The more common sources of electrical noise arise from ground loops, electrostatic coupling and electromagnetic pickup. The guidelines listed below pertain to guarding low level, millivolt signals in hostile environments such as current shunt signals in "heavy industrial" plants.

Guidelines:

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 11 below. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 284J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- To avoid ground loops and excessive hum, signal low, B, or the transducer cable shield, S, should never be grounded at more than one point.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

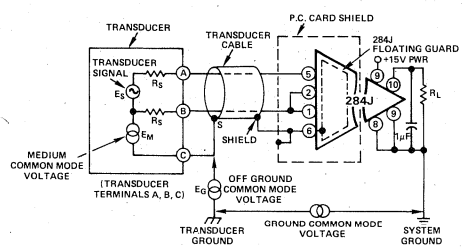


Figure 11. Transducer- Amplifier Interconnection

Isolated Power and Output Voltage Swing: Model 284J offers a floating power supply providing ±8.5V dc outputs with ±5mA output current rating. As shown in Figure 12, the minimum voltage output for $\pm V_{ISO}$, as well as the maximum load capability, is dependent on the input power supply, $+V_S$. Figure 12 also illustrates the typical output voltage range as both input supply, $+V_S$, and the isolated supply loads, $\pm I_L$, are varied. At ±5mA isolated load and V_S = +15V dc, model 284J can provide an output voltage swing of ±7.5V.

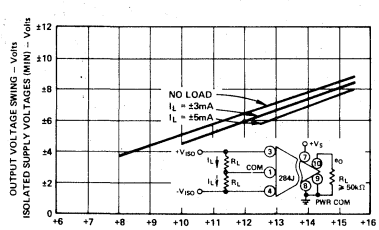


Figure 12. Isolated Power ($\pm V_{ISO}$) and Output Voltage Swing ($\pm E_O$) Versus Power Supply Input (V_S)

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 284J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems of on-line process measurement systems such as pollution monitoring, model 284J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 13 illustrates how model 284J can be combined with a low drift, 1µV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Model 284J's isolated ±8.5V dc power and front-end guard eliminate ground loops and preserve high CMR (114dB @ 60Hz).

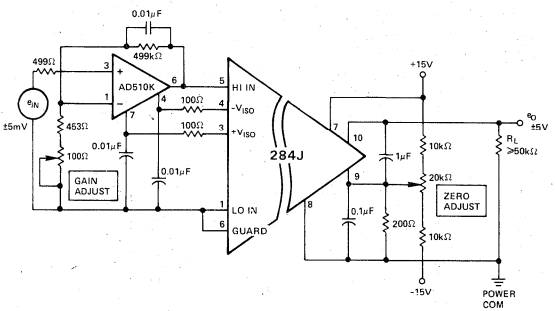


Figure 13. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Model 284J provides a floating guarded input stage capable of directly accepting isolated differential signals. The non-inverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, model 284J can be connected as shown in Figure 14. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 14.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum e_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum e_O.
4) Repeat steps 2 and 3 for best CMR performance.

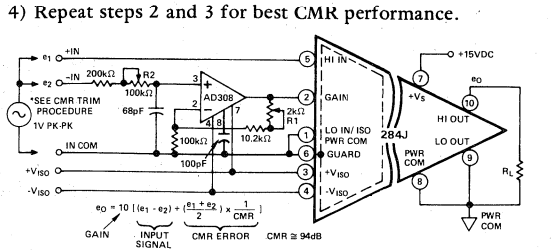


Figure 14. Application of 284J as Instrumentation Amplifier

APPLICATIONS IN BIOMEDICAL DESIGNS

Cardiac Monitoring: Heart signals can be masked by muscle noise, electrochemical noise, residual electrode voltages and 60Hz power line pickup. To achieve high performance in cardiac monitoring, model 284J's design provides high CMR in the dc to 100Hz bandwidth and substantial source impedance — to 5kΩ. An especially demanding ECG requirement is that of fetal heart monitoring as illustrated in Figure 15. The low input noise of model 284J and the dual CMR ratings are exploited in this application to extract the fetal ECG signals. The separation between the mother's and the fetal heartbeat is enhanced by the 78dB of CMR between the input electrodes and guard, while the 110dB of CMR from input to output ground screens out 60Hz pickup and other external interference.

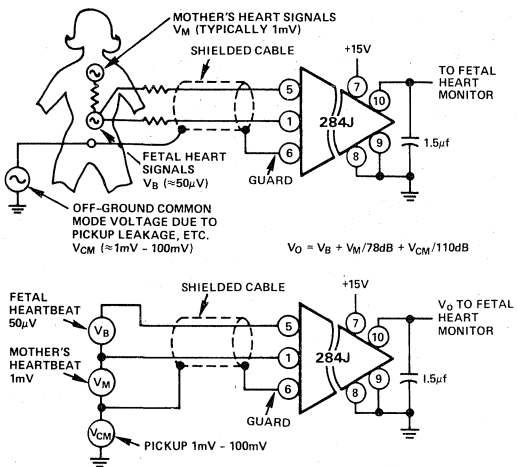


Figure 15. Fetal Heartbeat Monitoring

Single Lead ECG Recorder with Leads Off Indicator: In single lead applications model 284J offers simple two-wire hook-up to the ECG signal as illustrated in Figure 16. The floating signal can be connected directly to the HI IN and LO IN terminals using the GUARD tied to the patients' right leg for best CMR performance. Using the isolated power from model 284J an inexpensive calibration signal is easily provided. In ECG applications, model 284J provides a simple means to determine whenever a "Leads-Off" condition exists at the input. A "Leads-Off" condition ($R_S = \infty$) will cause the HI OUT terminal to be at a negative output saturation level; i.e. e_O = -8.5V to -9.5V @ V_S = +15V.

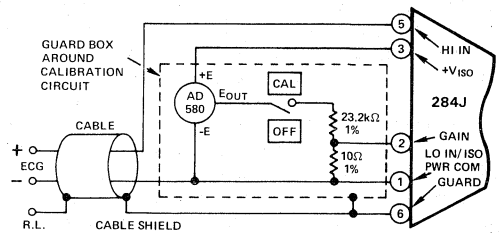


Figure 16. Single Lead ECG Recorder with 1mV Calibration Circuit and Leads Off Indicator

Multi-Lead ECG Recorder with Right Leg Drive: The small size, economy and isolated power makes model 284J an ideal isolation amplifier for application in clinical ECG recorders. Figure 17 illustrates how this new isolator can be applied in a high performance, portable multi-lead ECG recorder. In this application, model 284J's input is configured as an instrumentation amplifier with high CMR to the floating input common. The right leg drive offers improved CMR between input and isolated common by driving to zero any CMV existing between these points. The isolated power, $\pm V_{ISO}$, is used to drive the lead buffer amplifiers and the front-end, 1mV calibration signal.

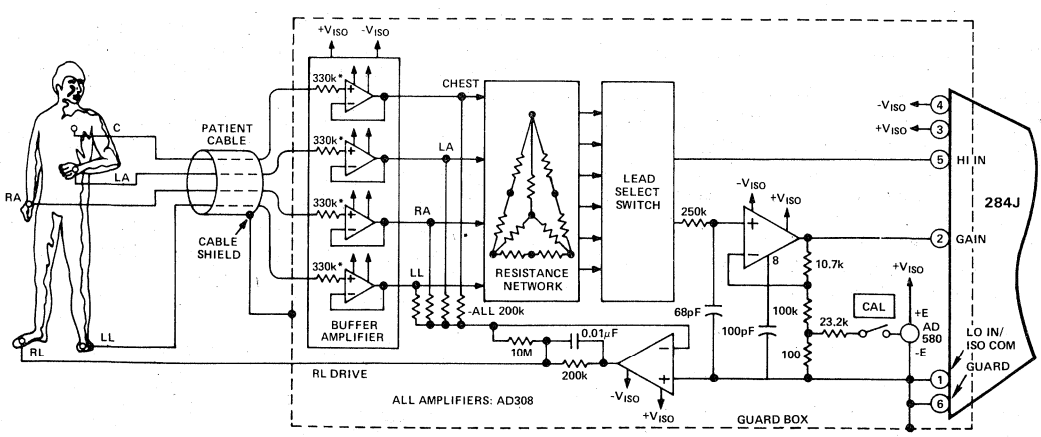


Figure 17. Multi-Lead ECG Recorder Application Using Model 284J with Right Leg Drive Output

High CMV, High Performance, Synchronized Isolation Amplifier

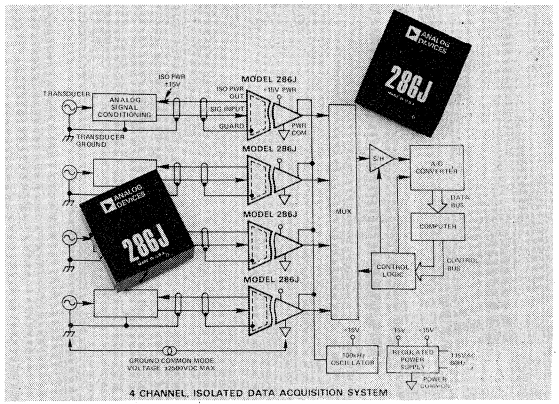
MODEL 286J, 281

FEATURES

Low Cost
Single or Multi-Channel Capability Using External Oscillator
Isolated Power Supply: ±15V dc @ ±15mA
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.0075%/°C
Small Size: 1.5″ x 1.5″ x 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 2500V dc Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Biomedical and Patient Monitoring Instrumentation
Off-Ground Signal Measurements



4 CHANNEL ISOLATED DATA ACQUISITION SYSTEM

GENERAL DESCRIPTION

Model 286J is a low cost, compact, isolation amplifier that is optimized for single or multi-channel use in data acquisition systems for industrial and medical applications. A single external synchronizing oscillator can drive from 1 to 16 model 286J's, or a virtually limitless number of model 286's can be configured using multiple ganged oscillators. The oscillator drive circuit can be supplied by the user of specified in a compact, low cost, epoxy encapsulated module, model 281, which also includes a voltage regulator for operation over a wide single voltage range of +8V to +28V.

In addition to providing multi-channel operation, this new design features adjustable gain, 1 to 100V/V, dual isolated power, ±15V dc @ ±15mA, ±2500V dc off ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5″ x 1.5″ x 0.6″ epoxy encapsulated package. Model 286J achieves a low input noise of 8μV pk-pk (100Hz bandwidth, G = 100V/V), nonlinearity of ±0.05% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, model 286J will interrupt ground loops, leakage paths, and high voltage transients to ±5kV pk (10ms pulse), providing dc to 1kHz (-3dB) response.

WHERE TO USE MODEL 286J

Industrial Applications: In multi-channel data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, model 286J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with model 286J's 20V pk-pk input signal range at a gain of 1V/V operation. In portable multi-channel designs, model 286J's single supply, wide range operation (+8V to +16V) offers simple battery operation.

Medical Applications: In biomedical and patient monitoring equipment such as multi-channel VCG, ECG, and polygraph recorders, model 286J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 286J's low input noise (8μV pk-pk @ G = 100V/V) and high CMR (110dB, min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 286J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 286J has a calculated MTBF of 392,125 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 286J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

Isolated Power Supply: Dual ±15V dc @ ±15mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers as well as remote transducers such as thermistors or bridges.

Adjustable Gain: A single external resistor enables gain adjustment from 1V/V to 100V/V providing the flexibility of applying model 286J in both high-level transducer interfacing as well as low-level sensor measurements.

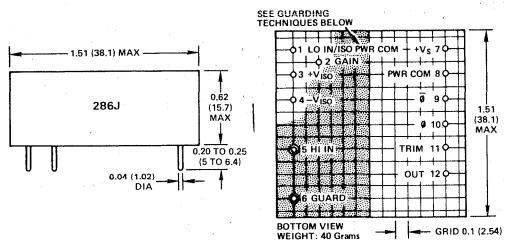
SPECIFICATIONS (typical @ +25°C and V_S = +15V dc unless otherwise noted)

MODEL	286J*
GAIN (NONINVERTING)	
Range (50kΩ Load)	1 to 100V/V
Formula	Gain = 1+ [100kΩ/(1kΩ+R_i(kΩ))]
Deviation from Formula	±4%
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
vs. Time	±0.001%/1000 hours
Nonlinearity,[2] ±5V Output (G = 1 to 100V/V)	±0.05%
Nonlinearity,[2] ±10V Output (G = 1 to 100V/V)	±0.2%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±10V min
Max Safe Differntial Input	
Continuous	240V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±6500V pk max
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 Minute Duration	2500V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±2500V pk max
With 510kΩ in series with Guard	±5000V pk max
Continuous, ac or dc	±2500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common	
@ 115V ac 60Hz	2.5μA rms max
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C (Adjustable to zero)	±(5 + 45/G) mV
vs. Temperature (0 to +70°C)	
At Gain = 100V/V	±10μV/°C
At Other Gains (1 to 100V/V)	±(7 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%
INPUT IMPEDANCE	
Differential	10^8 Ω||150pF
Overload	300kΩ
Common Mode	5 x 10^{10} Ω||20pF
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE (Gain = 100V/V)	
Voltage	
0.05Hz to 100Hz	8μV pk-pk
10Hz to 1kHz	3.0μV rms
Current	
0.05Hz to 100Hz	5pA pk-pk
FREQUENCY RESPONSE (Gain: 1V/V to 100V/V)	
Small Signal Bandwidth, -3dB	1.0kHz
Slew Rate	25mV/μs
Full Power, 10V pk-pk Output	900Hz
Full Power, 20V pk-pk Output	400Hz
Recovery Time, to ±100μV	200ms
RATED OUTPUT	
Voltage, 50kΩ Load	±10V min
Output Impedance	1kΩ
Output Ripple, 1mHz Bandwidth	20mV pk-pk
OSCILLATOR DRIVE INPUT*	
Input Voltage	(8 to 16)V pk-pk
Input Frequency	100kHz ±5%, max
ISOLATED POWER SUPPLY	
Voltage	±15V dc
Accuracy	0, -6%
Current	±15mA min
Regulation, No Load to Full Load	+0, -10%
Ripple, 100kHz Bandwidth	200mV pk-pk
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage, Operating	+(8V dc to 16V dc)
Current, Quiescent	+13mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

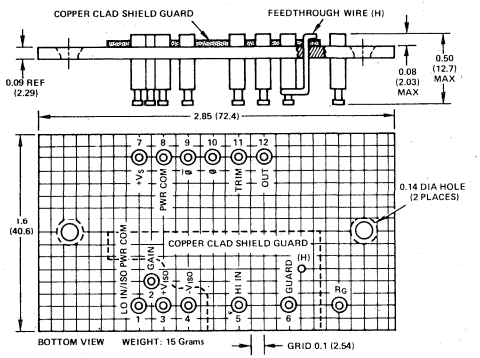
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of output signal span.
[3] Recommended power supply, ADI model 904, ±15V @ ±50mA output.
*Specifications are for model 286J when driven by ADI model 281 oscillator circuit (see Figure 12). Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



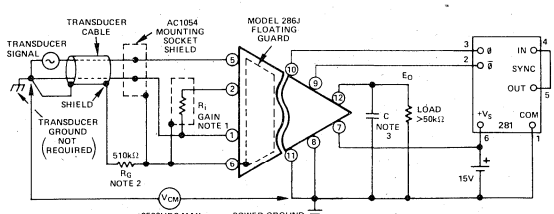
SHIELDED MOUNTING SOCKET AC1054



GUARDING TECHNIQUES

To preserve the high CMR performance of model 286, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 286 as illustrated in the outline drawing above (screened area). The GUARD (pin 6) must be connected to this shield. This shield is provided with the mounting socket, model AC1054 (solder feedthrough wire to the socket guard pin and copper foil surface.) A recommended guarding technique using model AC1054 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable to reduce inductive and capacitive pickup. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to signal low as shown in Figure 1.



NOTE 1. GAIN RESISTOR, R_i, USE 50ppm/°C, METAL FILM TYPE.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1
FOR GAINS FROM 1V/V TO 100V/V:

$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i\ (k\Omega)}$$

NOTE 2. OPTIONAL GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > ±2500V_{PK}
R_G MAY BE CONVENIENTLY MOUNTED ON AC1054 MOUNTING SOCKET USING THE STANDOFF PROVIDED (R_G). USE 1/4 WATT, 5% CARBON COMPOSITION TYPE; (ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR C, SELECT TO ROLL-OFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C=1.5μF FOR dc TO 100Hz BANDWIDTH)

$$F\ (-3dB) = \frac{1}{2 \pi C\ (1k\Omega)}$$

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 286J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 286J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 50μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 286J at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry.

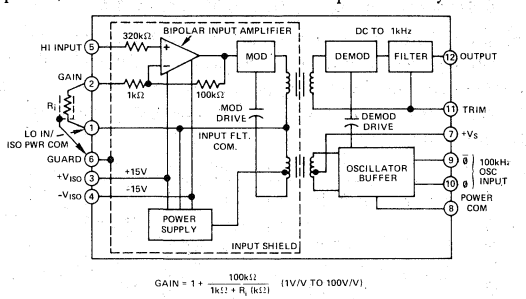


Figure 2. Block Diagram — Model 286J

OPTIONAL TRIM ADJUSTMENTS

Model 286J can be applied directly to achieve rated performance as shown in Figure 1, on previous page. Additional trim adjustment capability for bandwidth, output offset voltage and gain (for gains greater than 100V/V) is easily provided as shown in Figure 3 (below). The OUT and TRIM terminals can be floated with respect to PWR COM up to ±50V pk, max offering three-port isolation.

The TRIM terminal (pin 11) must be connected to the PWR COM terminal (pin 8) when not used to adjust the output offset voltage. A 0.1μF capacitor from pin 11 to PWR COM is recommended whenever the TRIM terminal is used.

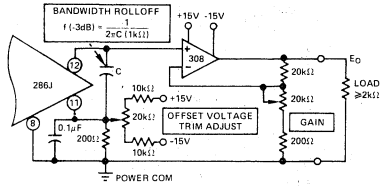


Figure 3. Optional Connections: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Gain Adjust (G>100V/V)

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 4 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

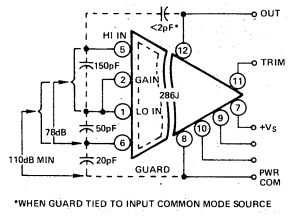


Figure 4. Model 286J Terminal Capacitance and CMR Ratings

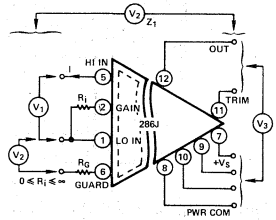


Figure 5. Model 286J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 5 and Table 1 illustrate model 286J ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont.)	±2500V_{PK}	Isolation, Steady State
V3 (cont.)	±50V_{PK}	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I	50μA rms	Input Fault Limit, dc to 200kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.5μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 6, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 100kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 286J.

For medical applications, model 286J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies (e.g., model 286J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment — reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 286J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

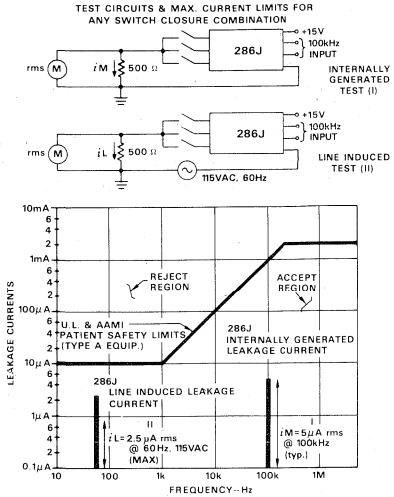


Figure 6. Model 286J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 100V/V. Figure 7 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V CMR is typically 6dB lower than at gain of 100V/V.

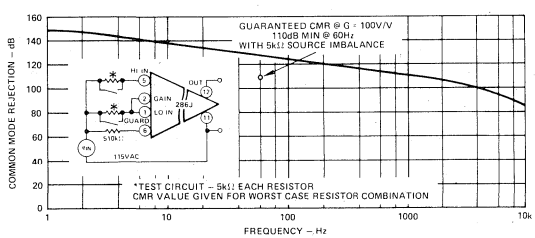


Figure 7. Common Mode Rejection vs. Frequency

Figure 8 illustrates the effect of source imbalance on CMR performance at 60Hz at gains of 1V/V, 10V/V, and 100V/V. CMR is typically 140dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

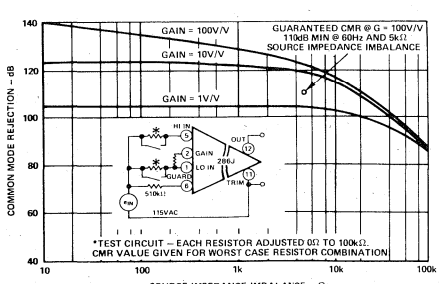


Figure 8. Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of model 286J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

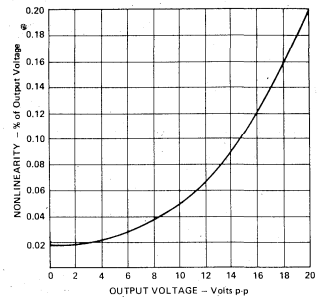


Figure 9. Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 10. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 10 (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1). Increasing gain will also reduce the input noise.

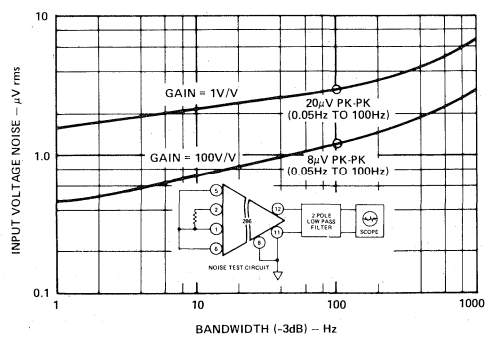


Figure 10. Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 11 illustrates total input drift over the gain range of 1 to 100V/V.

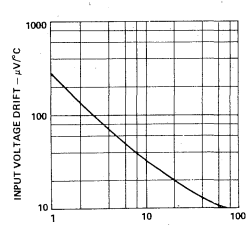


Figure 11. Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR

When applying model 286J, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 12, or purchasing a module from Analog Devices – model 281.

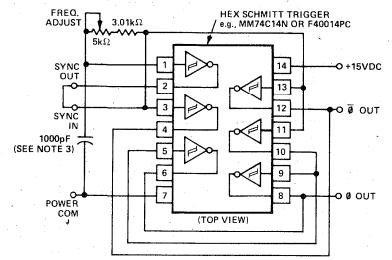


Figure 12. Model 281 100kHz Oscillator – Logic and Interconnection Diagram

The block diagram of model 281 is shown in Figure 13. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.

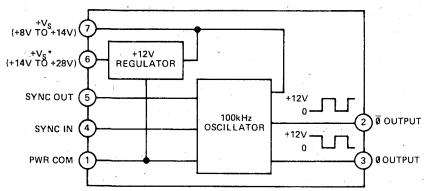


Figure 13. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 286J's as shown in Figure 14. An additional model 281 may be driven in a slave-mode, as shown in Figure 15, to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

EXTERNAL OSCILLATOR INTERCONNECTION

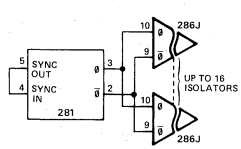


Figure 14. Model 281/286 Connection for Driving from 1 to 16 Isolators

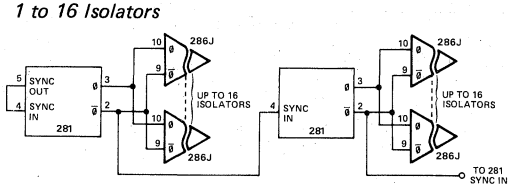


Figure 15. Model 281/286 Connection for Driving > 16 Isolators

SPECIFICATIONS

(typical @ +25°C and V_S = +15V dc unless otherwise noted)

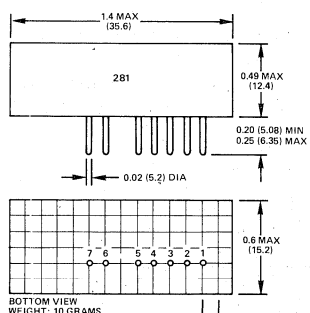
MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	−55°C to +85°C
MECHANICAL	
Case Size	1.4" x 0.6" x 0.49"
Weight	10 grams

[1] Model 286J oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 286J's, additional 281's may be used in a master/slave mode. Refer to Figure 15.
[3] Full load consists of 16 model 286J's and 281 oscillator slave.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

MODEL 281



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	$\bar{\phi}$ OUTPUT	6	$+V_S$: HIGH RANGE +(14 to 28)V_{dc}
3	ϕ OUTPUT	7	$+V_S$: LOW RANGE +(8 to 14)V_{dc}
4	SYNC INPUT		

MATING SOCKET: CINCH #16 DIP OR EQUIVALENT

GUIDELINES ON EFFECTIVE SHIELDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 16. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 286J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

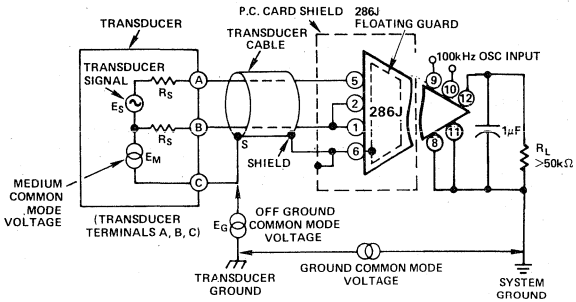
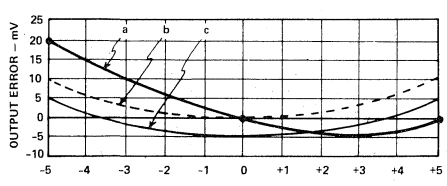


Figure 16. Transducer – Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +0.500V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = -0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).



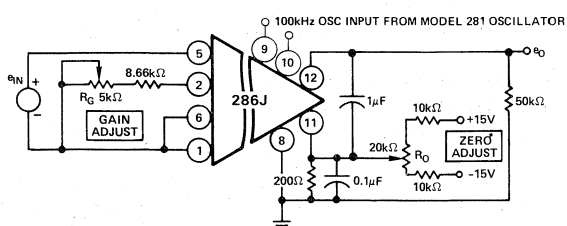


Figure 17. Gain and Offset Adjustment

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 286J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, model 286J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 18 illustrates how model 286J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Model 286J's isolated ±15V dc power and front-end guard eliminate ground loops and preserve high CMR (110dB min @ 60Hz).

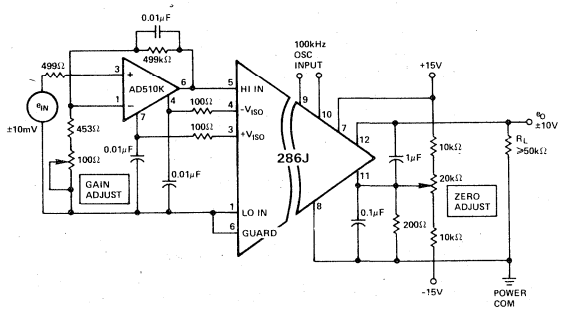


Figure 18. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Current Loop Receiver: Model 286J can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 19 shows an application of model 286J as a current loop receiver. A 25Ω resistor converts the 4–20mA current input from a remote loop to a 100–500mV differential voltage input, which the 286J amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the 286J in this kind of measurement are the high common-mode rejection (110dB minimum at 60Hz with 5kΩ source unbalance) and the high common-mode rating (±2500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

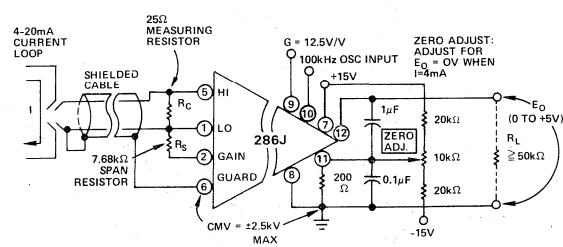


Figure 19. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±2500V of Isolation

Low-Cost, High Accuracy, Synchronized Isolation Amplifier

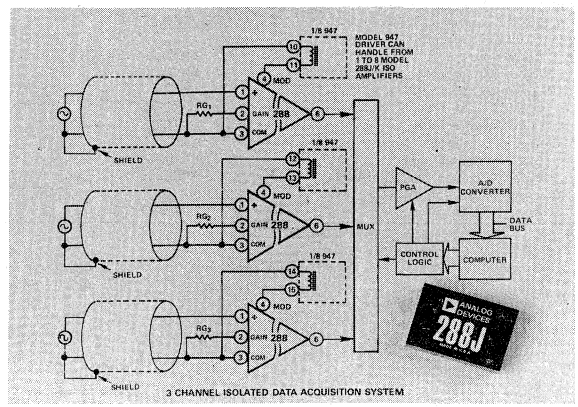
MODELS 288, 947, 948

FEATURES

Low Cost
Versatility: 3-Port Isolation
Multichannel
Adjustable Gain: 1 to 1,000V/V
Accuracy: Nonlinearity: 0.05% max (288K)
Low Gain Drift: 0.01%/°C max (288K)
Low Input Drift: 5μV/°C max (288K)
Single Supply Operation: +13.5V dc to +26V dc
High CMV Isolation: 850V dc

APPLICATIONS

Transient Voltage Protection: Data Acquisition Systems
Isolated 10-Bit D/A Converters
Ground Loop Elimination: Industrial Process Control
Process Signal Isolator
Off-Ground Measurements



3 CHANNEL ISOLATED DATA ACQUISITION SYSTEM

GENERAL DESCRIPTION

Model 288 is an economy isolation amplifier offering both high accuracy, 0.05% (model 288K), and a unique transformer isolated, multichannel design with separate signal and modulator/demodulator modules. Designed for low level, multichannel industrial instrumentation and control applications, this new design can be applied to achieve 4-channel, 3-port isolated systems, or low cost 8-, 16- or 32-channel systems with complete input/output isolation and channel/channel isolation.

Available in two high accuracy selections, this design features guaranteed low nonlinearity, 0.05% max (model 288K), 0.1% max (model 288J) and guaranteed low gain drift, 100ppm/°C max (model 288K), 300ppm/°C max (model 288J). The low drift bipolar input stage, 5μV/°C max (288K), 10μV/°C max (288J), provides gain adjustment from 1 to 1,000V/V with a single external resistor. Front-end differential protection (850V dc, continuous) combined with high CMV (850V dc, continuous) and high CMR (92dB min @ 60Hz) facilitates low level precision measurements in the presence of harsh RFI. Model 288J/K will interrupt ground loops, leakage paths and high voltage transients to ±850V pk, providing dc to 3.5kHz (−3dB @ G = 1V/V) response.

WHERE TO USE MODELS 288, 947, 948

Model 288 has been designed for multichannel data acquisition systems that have to handle dc sensor inputs such as thermocouples, strain gages and other low level signals in harsh industrial environments. Providing complete galvanic isolation and protection from line transients and fault voltages, model 288's low noise, high accuracy performance suggests applications such as process controllers, isolated 10-bit DAC's, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

DRIVER MODEL SELECTION

Model 288 requires external modulator and demodulator drive signals. Model 947 and 948 are available for driving up to 8 model 288J/K isolation amplifiers.

Model 947 offers 8 separate isolated modulator drive outputs for applications where complete input-to-input isolation as well as input-to-output isolation is required. For example, a single model 947 could be combined with four model 288J/K to configure a 4-channel 3-port isolated system.

Model 948 affords the same 850V dc input-to-output isolation for 1 to 8 model 288J/K isolation amplifiers with a common ground input reference as illustrated in Figure 1.

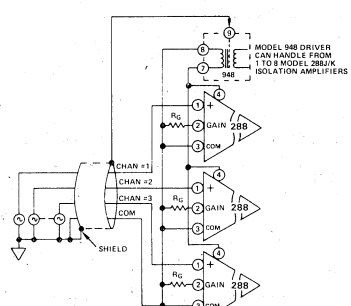


Figure 1. Application of Models 288/948 in Multichannel Data Isolation – (Note Common Signal Data Reference at Input)

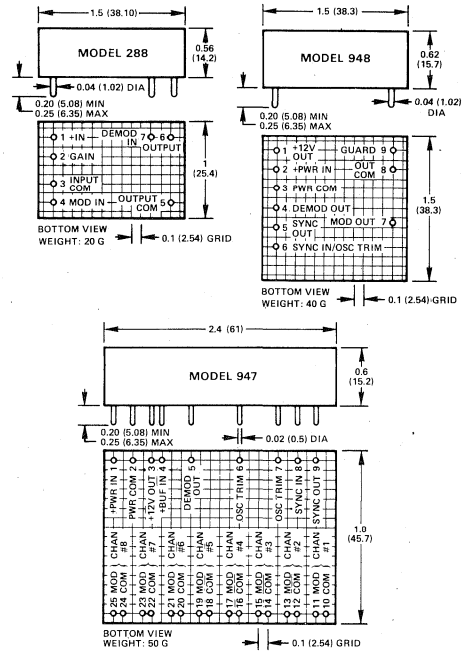
SPECIFICATIONS (typical @ +25°C over full range of power supply input unless otherwise noted, see note 1)

Model	288J	288K
GAIN (NON-INVERTING)		
Range (50kΩ Load)	1 to 1000V/V	
Gain Formula	Gain = 1 + 100kΩ/R_i(kΩ)	
Deviation from Formula	±4%	
vs. Temperature (0 to +70°C)[2]	±0.01%/°C typ, ±0.03%/°C max	±0.0035%/°C typ, ±0.01%/°C max
vs. Time	±0.001%/1000 hours	
Nonlinearity,[3] ±5V Output (G = 1 to 1000V/V)	±0.05% typ, ±0.1% max	±0.01% typ, ±0.05% max
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V	±5V min	
Safe Differential Input Voltage		
Continuous	240V rms max	
Pulse, 10ms Duration, 1 Pulse/sec	±400V pk max	
CMV, Inputs to Outputs		
ac, 60Hz, One Minute Duration	750V rms	
Continuous, ac or dc	±850V pk max	
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k$		
Balanced Source Impedance	100dB	
1kΩ Source Impedance Imbalance	92dB min	
Leakage Current, Inputs to Outputs @ 115V ac, 60Hz	5.0μA rms max	
OFFSET VOLTAGE, REFERRED TO INPUT		
Initial, @ +25°C (Adjustable to zero)		
Gain = 500V/V	±0.5mV typ, ±1mV max	±0.1mV typ, ±0.5mV max
Gain = 1 to 1000V/V	±(1.0 + 50/G)mV max	±(0.5 + 30/G)mV max
vs. Temperature (0 to +70°C)		
Gain = 500V/V	±5μV/°C typ, ±10μV/°C max	±2μV/°C typ, ±5μV/°C max
Gain = 1V/V	±250μV/°C typ, ±500μV/°C max	±100μV/°C typ, ±300μV/°C max
Gain = 1 to 1000V/V	±(10 + 500/G)μV/°C max	±(5 + 300/G)μV/°C max
vs. Supply Voltage	$\pm\left(20 + \frac{500}{G}\right)$ μV/V	
INPUT BIAS CURRENT		
Initial, @ +25°C	±25nA max	
vs. Temperature (0 to +70°C)	±0.1nA/°C	
INPUT IMPEDANCE		
Differential	10^8Ω‖70pF	
Overload	200kΩ	
Common Mode	10^8Ω‖30pF	
INPUT NOISE		
Voltage, Gain = 500V/V		
0.01Hz to 10Hz	1.5μV p-p	
10Hz to 1kHz	0.8μV rms	
Current		
0.01Hz to 10Hz	5pA pk-pk	
FREQUENCY RESPONSE		
Small Signal Bandwidth, -3dB		
Gain = 500V/V	400Hz	
Gain = 1V/V	3.5kHz	
Full Power Response, 10V pk-pk Output		
Gain = 500V/V	400Hz	
Gain = 1V/V	2.0kHz	
RATED OUTPUT		
Voltage, 50kΩ Load	±5V min	
Output Impedance	1kΩ	
Output Ripple, 1MHz Bandwidth	2mV pk-pk	
POWER SUPPLY[4]		
Voltage Range, Rated Performance	+13.5V dc to +26V dc	
Current, Quiescent, Model 947	+23mA @ V_S = +15V dc	
Current, Quiescent, Model 948	+15mA @ V_S = +15V dc	
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	
Operating	-25°C to +85°C	
Storage	-55°C to +85°C	
PACKAGE SIZE	1.0" X 1.5" X 0.56"	

NOTES:
[1] Specifications apply using either model 947 or model 948 mod/demod drive.
[2] Gain temperature drift is specified as a percentage of output signal level.
[3] Gain nonlinearity is specified as a percentage of output signal span.
[4] Power supply voltage ratings refer to models 947 or 948 mod/demod modules.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SPECIFICATIONS (typical @ +25°C over full range of power supply input unless otherwise stated)

Model	947(948)
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage	
Mod Drive	22V p-p (18V p-p)
Demod Drive	22V p-p (18V p-p)
Fan-Out[1,2]	8
POWER SUPPLY	
Voltage, Rated Performance	+13.5V dc to +26V dc
Current, Quiescent @ +15V dc	
No Load	+23 (+15)mA
Full Load[3]	+40 (+32)mA
TEMPERATURE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
CASE SIZE	2.4" X 1.8" X 0.6" (1.5" X 1.5" X 0.62")

NOTES
[1] Model 288J/K Mod Input and Demod Input represent unity load.
[2] For applications requiring more than eight 288's, additional 947's or 948's may be used in a master/slave mode. Refer to Figure 5.
[3] Full load consists of eight model 288's and a driver module (either 947 or 948).

Specifications subject to change without notice.

ORDERING GUIDE

Model	Type	Socket
288J	Iso Amp	AC-1055
288K	Iso Amp	AC-1055
947	Driver	AC-1056
948	Driver	AC-1057

GUIDELINES ON INTERCONNECTION TECHNIQUES

To preserve the high CMR performance of model 288, care must be taken to keep the capacitance balanced about the input terminals. Best CMR performance will be achieved by using twisted shielded cable to reduce inductive and capacitive pickup. To reduce the effective cable capacitance, the cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low. To reduce capacitive coupling from input to output, dress all leads from the driver modules, models 947 or 948, short at the connection terminals and reduce the area formed by these leads. Input and output signal leads should be dressed away from the driver signals, demod and mod. Input leads should not be twisted together to reduce crosstalk noise.

BASIC INTERCONNECTION – MODELS 288, 947 AND 948

4-CHANNEL 3-PORT ISOLATED SYSTEM

Figure 2 illustrates the basic interconnection between model 288J/K and 947 to provide a 4-channel system with 3-port isolation. Total isolation exists between the input signal commons, the output signal commons and the power supply common. The model 947 provides two separate isolated drive signals for each 288 signal channel. Independent gain setting of each channel, from 1V/V to 1,000V/V, is available. To achieve the highest CMR performance, the input/output driver leads must be dressed to minimize capacitive cross-talk.

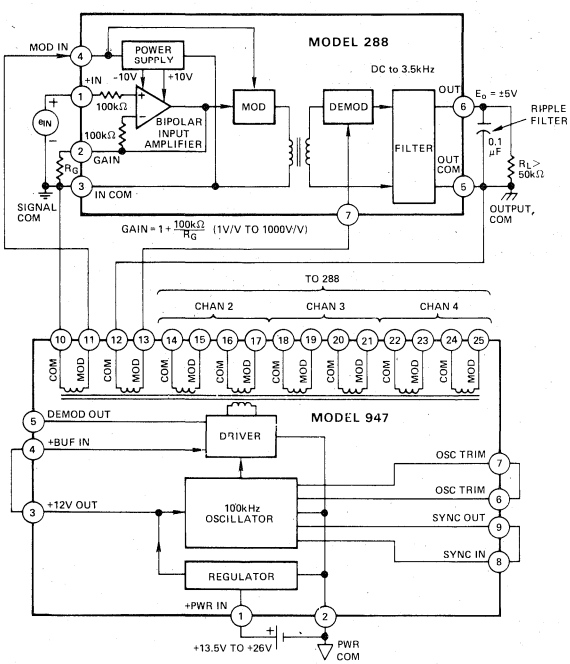
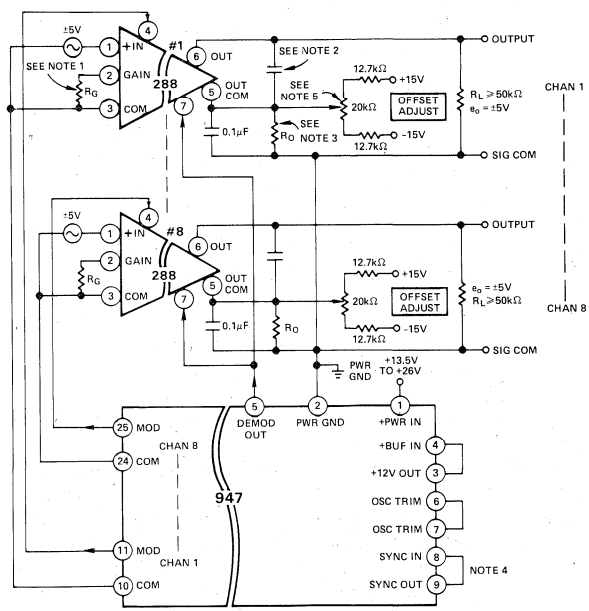


Figure 2. 4-Channel, 3-Port Isolated System

8-CHANNEL SYSTEM – MODELS 288 AND 947

Figure 3 illustrates the basic interconnection between a single model 947 and up to eight model 288 isolation amplifiers to provide complete input-to-output isolation as well as channel-to-channel isolation at the input. Each channel output is referenced to a common power supply ground. Offset voltage trimming is also provided for each channel. When offset voltage trimming is not required, the output common, pin 5, should be connected to the power common.



NOTES:
1. GAIN FORMULA = 1 + 100kΩ/R_G (kΩ).
2. TO ROLL OFF NOISE AND OUTPUT RIPPLE, USE BANDWIDTH FORMULA f(-3dB) = 1/2πC(1kΩ),
3. FOR GAINS = 1 TO 100V/V, R_O = 200Ω; FOR GAINS = 100 TO 1000V/V, R_O = 1kΩ.
4. SEE DRIVER SYNCHRONIZATION, ON NEXT PAGE FOR SYSTEMS WITH MORE THAN 8 CHANNELS.
5. OFFSET ADJUSTMENT POT SHOULD BE 10 OR 20 TURN CERMET TYPE.

Figure 3. 8-Channel System

GAIN AND OFFSET TRIM PROCEDURE

In applying model 288, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak output error over the operating output voltage span. A calibration technique illustrating how to minimize the output error is shown below. In this example, model 288K is operating over an output span of +5V to −5V and a gain of 100V/V.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.05V dc and adjust R_t for E_O = +5.000V dc.
3. Apply E_{IN} = −0.05V dc and measure the output error (see curve a).
4. Adjust R_t until the output error is one half that measured in step 3 (see curve b).
5. Apply E_{IN} = +0.05V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).

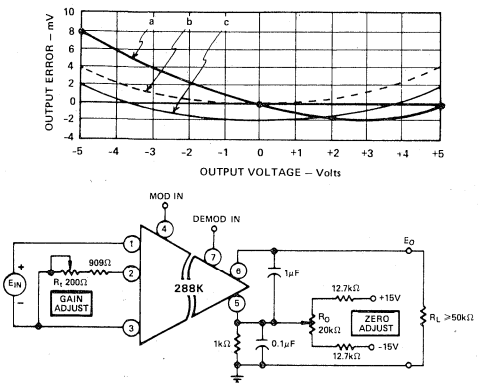


Figure 4. Gain and Offset Adjustment

APPLICATION IN DATA ACQUISITION SYSTEMS HAVING MORE THAN 8 CHANNELS

Driver Synchronization: A single model 947 or model 948 driver can be applied in systems having from 1 to 8 data channels, as shown in Figures 3 and 10. Additional model 947's and 948's may be driven in a slave-mode, as shown in Figure 5, to expand the total system channels from 8 to virtually any number of channels.

Optional Oscillator Adjustment: Models 947 and 948 provide the user with a method to trim the internal 100kHz oscillator over a range of ±5% (95kHz to 105kHz). This feature may be used when an external noise is "beating" with the 100kHz oscillator and a small trim adjustment of the oscillator frequency will eliminate the resulting noise frequency. As shown in Figure 5, a trim adjust, R_t, is installed between the OSC TRIM terminals. No specification changes occur when this trim adjustment is employed.

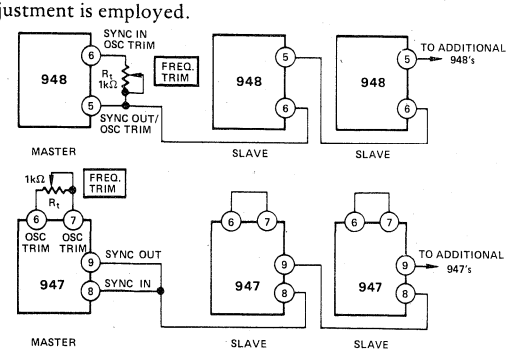


Figure 5. Model 948 and 947 Connections for Systems with Greater than 8 Channels

Selecting Bandwidth: In low frequency signal measurements, such as thermocouple temperature measurements, strain gage measurements and geophysical instrumentation, an external filter is used to select bandwidth and minimize output noise. As shown in Figure 6a, a capacitor connected between the OUT and OUT COM terminals will result in model 288's bandwidth set according to the following: $f(-3dB) = \frac{1}{2\pi C(1k\Omega)}$. For lowest noise performance, the filter capacitor should be located as close to the actual load as possible.

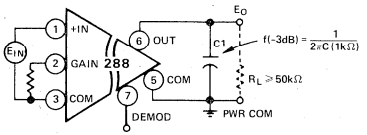


Figure 6a. Selecting Bandwidth with External Capacitor (C)

When used with a buffer amplifier as shown in Figure 6b below, a series resistor (R_S) is used to lower the effective value of the filter capacitor required to achieve very low frequency (under 200Hz) noise filtering.

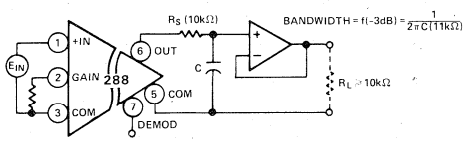


Figure 6b. Selecting Bandwidth with External Capacitor and Buffer

An active filter, as illustrated in Figure 6c will significantly improve 60Hz noise reduction at the output by providing a sharp rolloff characteristic. The 5Hz 3-pole active filter design illustrated in Figure 6c, will increase the 60Hz noise reduction by 50dB. Overall CMR performance of model 288 and the 5Hz active filter approaches 140dB @ 60Hz and 1kΩ imbalance.

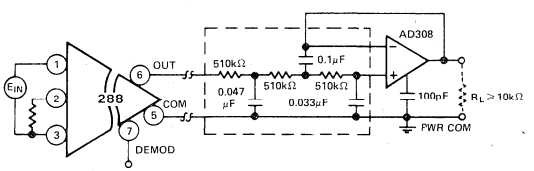


Figure 6c. Selecting Bandwidth with a 3-Pole 5Hz Active Filter

Noise Reduction in Data Acquisition Systems: In multichannel data acquisition systems using a multiplexer to select sequentially the channel for A/D conversion, a filter can be easily applied to reduce the input noise and select the channel bandwidth. As illustrated in Figure 7, a single 3-pole active filter is inserted at the mux output.

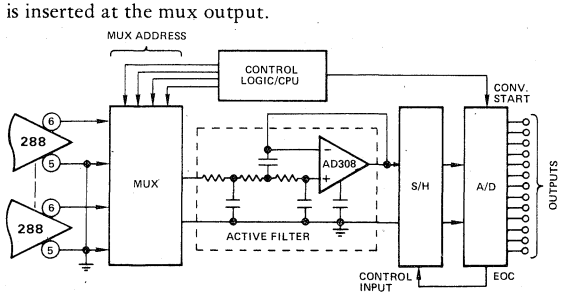


Figure 7. Applying Active Filter in Isolated Data Acquisition System to Select Bandwidth, Reduce Input Noise to A/D Converter and Increase CMR to 140dB @ 60Hz

ISOLATED 10-BIT D/A CONVERTER WITH 4/20mA CURRENT LOOP OUTPUT

The versatility of models 288/947 for industrial process control applications is illustrated in Figure 8. A low cost 10-bit CMOS D/A converter, model AD7533, is combined with models 288K/947 to provide an isolated 4/20mA current loop D/A converter to drive remote actuators. The 850V dc isolation provided by model 288K protects the microprocessor interface from power-line switching spikes and other voltage transients introduced in the remote cabling to the process control actuators.

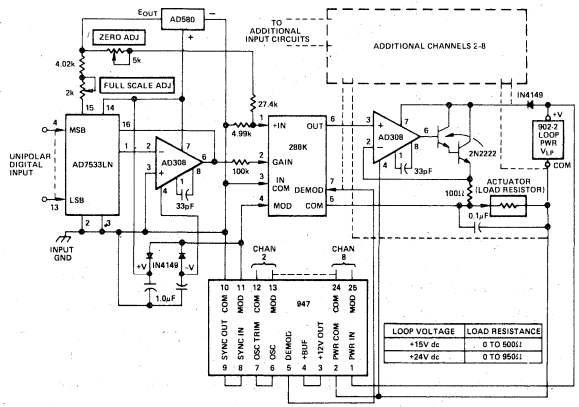


Figure 8. 10-Bit DAC with 4/20mA Output

The 947 driver module provides drive signals for both the 288K isolator as well as a power supply rectifier/filter circuit. Sufficient power is available to handle the D/A converter, voltage reference and the D/A converter output amplifier. The 947 and 288K isolated outputs are referenced to a floating loop power source (V_{LP}) which can be set from +15V dc to +24V dc. With a loop power of +24V dc the load range is 0 to 950 ohms. A series diode protects the model 288K output current stage in the event loop power polarity is accidently reversed. The 947 driver module has internal protection for accidental power reversal.

A total of 8 isolated channels can be configured using a single loop power source, 8 model 288K channels and a single model 947. Each 4/20mA current loop will add an additional 20mA to a single 288K channel—thus the maximum loop power required for eight channels is 200mA. Each input will be isolated from the loop power common as well as from each input common. In this manner, a total of eight isolated 10-bit D/A converters, with 4/20mA output drive capability and a single loop power source of +15V dc to +24V dc, is easily configured.

FRONT-END SIGNAL CONDITIONING USING ISOLATED POWER

To provide the capability to interface source impedances greater than 10k, a high impedance buffer amplifier, as illustrated in Figure 9 can be used. The modulator drive signal is applied to a rectifier/filter circuit to generate isolated dual voltages for powering the front-end buffer. In applications where additional isolated power is required, a separate modulator drive signal can be used to provide dual 12V dc @ ±2.5mA output capability. This approach eliminates the need for a separate isolated dc/dc converter for powering front-end signal conditioning circuits.

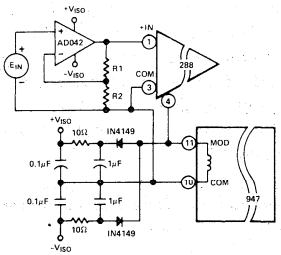


Figure 9. Developing Isolated Dual 12V dc for Powering Front-End Signal Conditioning Circuitry

ISOLATED INSTRUMENTATION AMPLIFIER

To interface low level, differential signals from bridge type sensors, two model 288 units can be connected as shown in Figure 10 to provide a true differential, high accuracy isolated instrumentation amplifier. Gain is set using a single resistor, R_G, as shown. Using a single 947 driver, up to four isolated channels can be configured. The output 47k resistors are contained in a single thin-film network chip, reducing cost and circuit density. Gain is programmable from 1 to 1,000V/V.

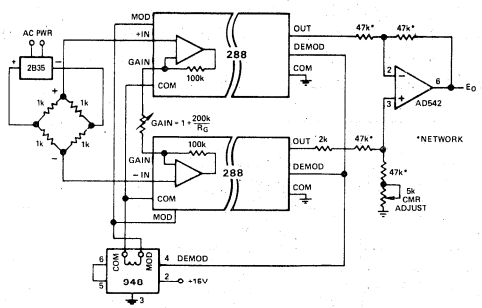


Figure 10. Floating Instumentation Amplifier

ISOLATED TEMPERATURE MEASUREMENTS

Industrial temperature measurements are often performed in harsh environments where accidental line voltages can be impressed on the temperature sensor. To provide protection for the delicate recording instrumentation, model 288 can be applied as shown in Figure 11. The AD590 is a temperature sensor whose output is a current directly proportional to absolute temperature. The 288/947 provides the isolated power (+12V dc) as well as the input/output isolation. Zero calibration is performed by placing the AD590 probe at a zero temperature bath and adjusting R_O for E_O to 0 Volts. Full scale output is performed by placing the AD590 probe in boiling water (100°C) and adjusting R_S for 1.000V output.

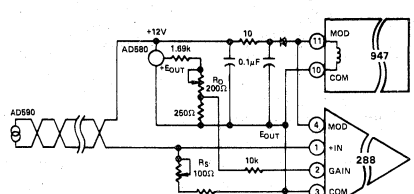


Figure 11. Isolated Temperature Measurements

PERFORMANCE CHARACTERISTICS

Gain Nonlinearity: Linearity error is defined as the peak deviation of the output voltage from the best straight line and is specified as a % of the peak-to-peak output voltage span; e.g., ±0.05% @ 10V p-p output = ±5mV max RTO linearity error. Model 288 is available in two nonlinearity selections; ±0.05% (288K) and ±0.1% (288J)—max over the 10V p-p output span. The curves of Figure 12 illustrate typical linearity error over the 10V p-p (±5V) output span. At output levels less than 5V p-p (±2.5V), linearity error is typically less than ±0.025% for both models 288J and 288K.

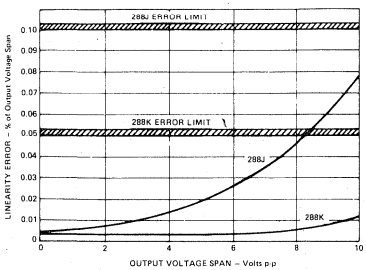


Figure 12. Gain Linearity Error vs. Output Voltage

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ imbalance at a gain of 1V/V. Figure 13 illustrates CMR performance as a function of signal frequency and gain. CMR approaches 130dB at dc with source imbalances as high as 1kΩ in the INPUT COMMON lead (worst case condition).

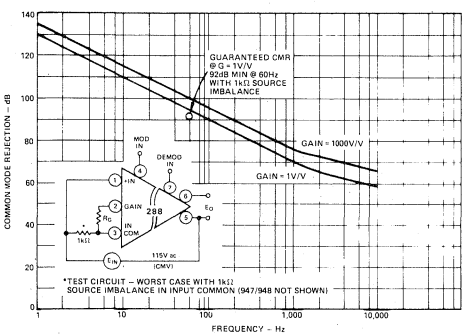


Figure 13. Common Mode Rejection vs. Frequency

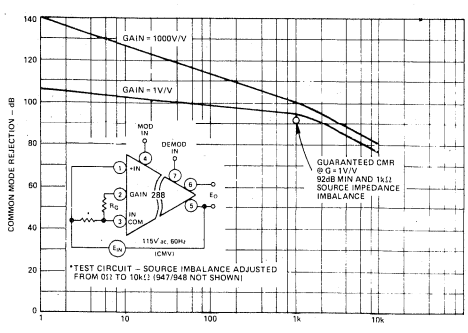


Figure 14. CMR vs. Source Impedance Imbalance

Figure 14 illustrates the effect of source imbalance on CMR performance at 60Hz and gains of 1V/V and 1,000V/V. CMR is typically 140dB at 60Hz, gain of 1,000V/V and a balanced source. CMR is maintained greater than 70dB for source imbalances up to 10k ohms.

Input Offset Voltage Drift: Model 288 is available in two drift selections: 5μV/°C (288K) and 10μV/°C (288J)—max, RTI, G=500V/V. Total input voltage drift is composed of two sources (input and output stage drifts) and is gain dependent. The curves of Figure 15 illustrate the worst case total input drift (RTI) over the gain range of 1 to 1,000V/V.

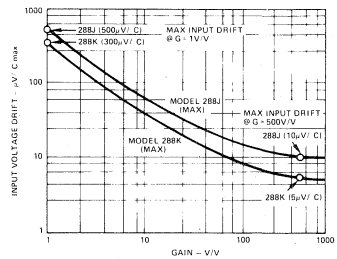


Figure 15. Max Input Offset Voltage Drift vs. Gain

Input Voltage Noise: Voltage noise, referred to input (RTI), is dependent on gain and bandwidth as illustrated in Figure 16. Rms voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.01Hz to 10Hz is 1.5μV p-p at a gain of 500V/V. This value is derived by multiplying the rms value at f = 10Hz shown in Figure 16 (0.22μV rms) by 6.6.

For lowest noise performance, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see Figure 6).

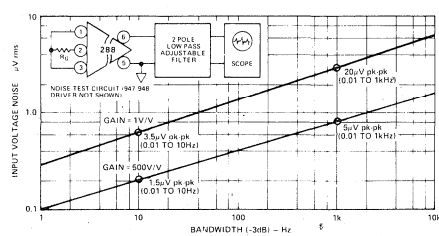


Figure 16. Input Voltage Noise vs. Bandwidth

Frequency Response: Small signal bandwidth and full power bandwidth versus gain are shown in Figure 17. For gains greater than 100V/V, both bandwidths are identical and approach 200Hz at G = 1000V/V. Full power response is measured with the output set at 10V p-p; small signal bandwidth (-3dB) is measured with the output set at 100mV p-p.

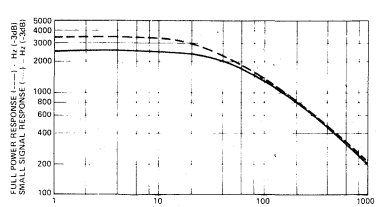


Figure 17. Full Power and Small Signal Bandwidth vs. Gain

Precision, Wide Bandwidth, Synchronized Isolation Amplifier

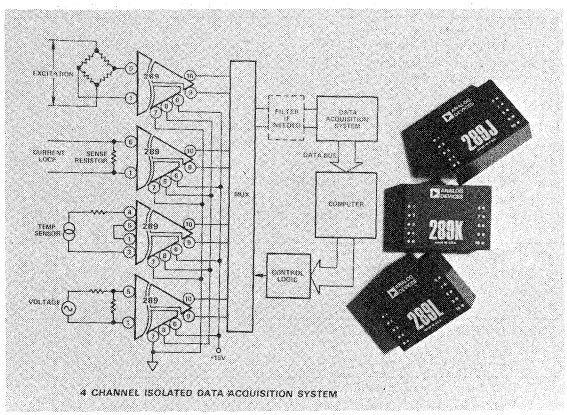
MODEL 289

FEATURES

- Low Nonlinearity: ±0.012% max (289L)
- Frequency Response: (-3dB) dc to 20kHz
  (Full Power) dc to 5kHz
- Gain Adjustable 1 to 100V/V, Single Resistor
- 3-Port Isolation: ±2500V CMV Isolation Input/Output
- Low Gain Drift: ±0.005%/°C max
- Floating Power Output: ±15V @ ±5mA
- 120dB CMR at 60Hz: Fully Shielded Input Stage
- Low Cost

APPLICATIONS

- Multi-Channel Data Acquisition Systems
- Current Shunt Measurements
- Process Signal Isolator
- High Voltage Instrumentation Amplifier
- SCR Motor Control



4 CHANNEL ISOLATED DATA ACQUISITION SYSTEM

GENERAL DESCRIPTION

Model 289 is a wide-band, accurate, low cost isolation amplifier designed for instrumentation and industrial applications. Three accuracy selections are available offering guaranteed gain nonlinearity error at 10V p-p output: ±0.012% max (289L), ±0.025% max (289K), ±0.05% max (289J). All versions of the 289 provide a small signal frequency response from dc to 20kHz (-3dB) and a large signal response from dc to 5kHz (full power) at a gain of 1V/V. This new design offers true 3-port isolation, ±2500V dc between inputs and outputs (or power inputs), as well as 240V rms between power supply inputs and signal outputs. Using carrier modulation techniques with transformer isolation, model 289 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. It provides 120dB Common Mode Rejection between input and output common. The high CMV and CMR ratings of the model 289 facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays.

WHERE TO USE THE MODEL 289

The model 289 is designed to interface single and multichannel data acquisition systems with dc sensors such as thermocouples, strain gauges and other low level signals in harsh industrial environments. Providing high accuracy with complete galvanic isolation, and protection from line transients of fault voltages, model 289's performance is suitable for applications such as process controllers, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

Use the model 289 when data must be acquired from floating transducers in computerized process control systems. The photograph above shows a typical multichannel application allowing potential differences or interrupting ground loops, among transducers, or between transducers and local ground.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: The floating power supply section provides isolated ±15V outputs @ ±5mA. Isolated power is regulated to within ±5%. This feature permits model 289 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers such as thermistors or bridges, eliminating the need for a separate isolated dc/dc converter.

Adjustable Gain: A single external resistor adjusts the model 289's gain from 1V/V to 100V/V for applications in high and low level transducer interfacing.

Synchronized: The model 289 provides a synchronization terminal for use in multichannel applications. Connecting the synchronization terminals of model 289s synchronizes their internal oscillators, thereby eliminating the problem of oscillator "beat frequency" interference that sometimes occurs when isolation amplifiers are closely mounted.

Internal Voltage Regulator: Improves power supply rejection and helps prevent carrier oscillator spikes from being broadcast via the isolator power terminal to the rest of the system.

Buffered Output: Prevents gain errors when an isolation amplifier is followed by a resistive load of low impedance. Model 289 can drive a 2kΩ load.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates need for power supply and output ports being returned through a common terminal.

Reliability: Model 289 is conservatively designed to be capable of reliable operation in harsh environments. Model 289 has a calculated MTBF of 2,298,851 hours.

SPECIFICATIONS (typical @ +25°C and V_S = +14.4V to +25V dc unless otherwise noted.)

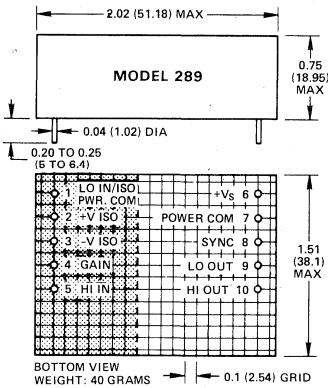
Model	289J	289K	289L
GAIN (NONINVERTING)			
Range		1 to 100V/V	
Formula		$G = 1 + \frac{10k\Omega}{R_G(k\Omega)}$	
Deviation from Formula		±1.5% max	
vs. Temperature (0 to +70°C)[1]		15ppm/°C typ (50ppm/°C max)	
Nonlinearity, (±5V Swing)[2,3]	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range (G = 1V/V)		±10V min	
Max Safe Differential Input			
Continuous		120V rms	
1 Minute		240V rms	
Max CMV (Inputs to Outputs)			
Continuous ac or dc		±2500V peak max	
ac, 60Hz, 1 Minute Duration		2500V rms	
CMR, Inputs to Outputs 60Hz			
$R_S \leq 1k\Omega$, Balanced Source Impedance		120dB	
$R_S \leq 1k\Omega$, HI IN Lead Only		104dB min	
Max Leakage Current, Input to Output @			
115V rms, 60Hz ac		2μA rms max	
INPUT IMPEDANCE			
Differential		$33pF \| 10^8 \Omega$	
Overload		100kΩ	
Common Mode		$20pF \| 5 \times 10^{10} \Omega$	
INPUT DIFFERENCE CURRENT			
Initial @ +25°C		10nA (75nA max)	
vs. Temperature (0 to 70°C)		0.15nA/°C	
INPUT NOISE (GAIN = 100V/V)			
Voltage			
0.05Hz to 100Hz		8μV p-p	
10Hz to 1kHz		3μV rms	
Current			
0.05Hz to 100Hz		3pA rms	
FREQUENCY RESPONSE			
Small Signal -3dB			
G = 1V/V		20kHz	
G = 100V/V		5kHz	
Full Power, 10V p-p Output			
G = 1V/V		5kHz	
G = 100V/V		3.5kHz	
Full Power, 20V p-p Output			
G = 1V/V		2.3kHz	
G = 100V/V		2.3kHz	
Slew Rate		0.14V/μs	
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial, @ +25°C		$\pm 5 \pm \frac{10}{G}$ mV max	
vs. Temperature (0 to +70°C)	$\pm 20 \pm \frac{200}{G}$ max	$\pm 15 \pm \frac{100}{G}$ max	$\pm 10 \pm \frac{50}{G}$ μV/°C max
vs. Supply Voltage (+15V to +20V change)		$\pm 2 \pm \frac{10}{G}$ μV/V	
RATED OUTPUT			
Voltage, 2kΩ Load		±10V min	
Output Impedance		<1Ω(dc to 100Hz)	
Output Ripple, 0.1MHz Bandwidth			
No Signal IN		5mV p-p	
$+10V_{IN}$		50mV p-p	
ISOLATED POWER SUPPLY			
Voltage		±15V dc	
Accuracy		±10%	
Current		±5mA, min	
Regulation No Load to Full Load		±5%	
Ripple, 0.1MHz Bandwidth, No Load		25mV p-p	
Full Load		75mV p-p	
POWER SUPPLY, SINGLE POLARITY[4]			
Voltage, Rated Performance		+14.4V to +25V	
Voltage, Operating		+8.5V to +25V	
Current, Quiescent (@ V_S = +15V)		+25mA	
TEMPERATURE RANGE			
Rated Performance		0 to +70°C	
Operating		-15°C to +75°C	
Storage		-55°C to +85°C	
CASE DIMENSIONS		1.5" X 2.0" X 0.75"	

NOTES:
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn.
[4] Recommended power supply, ADI model 904, ±15V @ 50mA output.

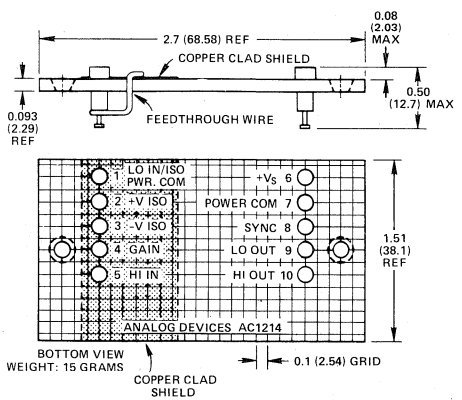
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



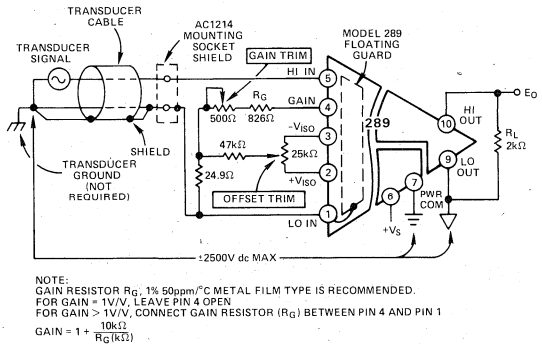
SHIELDED MATING SOCKET AC1214



INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of model 289, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 289 as illustrated in the outline drawing above (screened area). The LO IN/ISO PWR COM (pin 1) must be connected to this shield. This shield is provided with the mounting socket, model AC1214 (solder feedthrough wire to the socket pin 1 and copper foil surface). A recommended shielding technique using model AC1214 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable for the input signal to reduce inductive and capacitive pickup. To further reduce effective cable capacitance, the cable shield should be connected to the common mode signal source as close to signal low as possible (see Figure 1).



NOTE:
GAIN RESISTOR R_G, 1% 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE PIN 4 OPEN
FOR GAIN > 1V/V, CONNECT GAIN RESISTOR (R_G) BETWEEN PIN 4 AND PIN 1

$$\text{GAIN} = 1 + \frac{10k\Omega}{R_G(k\Omega)}$$

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of the model 289 is derived from the carrier isolation technique used to transfer both signal and power between the amplifier's input stage and the rest of the circuitry. A block diagram is shown in Figure 2.

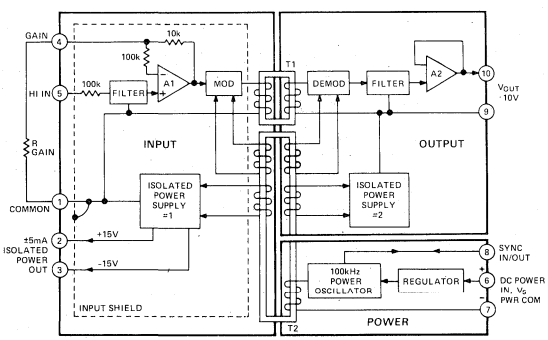


Figure 2. Model 289 Block Diagram

The input signal is filtered and appears at the input of the non-inverting amplifier, A1. This signal is amplified by A1, with its gain determined by the value of resistance connected externally between the gain terminal and the input common terminal. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulated voltage is filtered, amplified and buffered by amplifier A2, and applied to the output terminal. The voltage applied to the V_S terminal is set by the regulator to +12V which powers the 100kHz symmetrical square wave power oscillator. The oscillator drives the primary winding of transformer T2. The secondary windings of T2 energize both input and output power supplies, and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance, arising from stray coupling capacitance effects between the input terminals and the signal output terminals, are each shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates model 289's capacitance, between terminals.

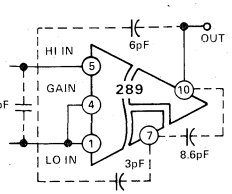


Figure 3. Model 289 Terminal Capacitance

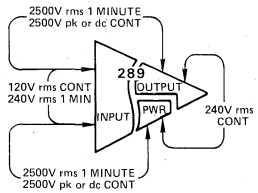


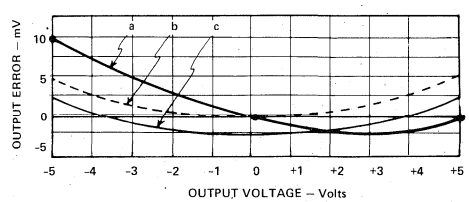
Figure 4. Model 289 Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 illustrates model 289 ratings between terminals.

GAIN AND OFFSET TRIM PROCEDURE

The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to −5V and Gain = 10V/V.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.500V dc and adjust R_G for E_O = +5.000V dc.
3. Apply E_{IN} = −0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one-half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one-half that measured in step 4 (see curve c).



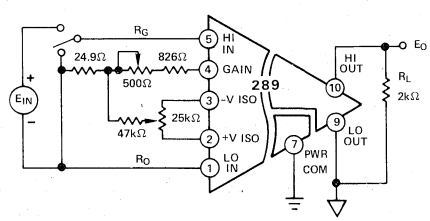


Figure 5a. Recommended Offset and Gain Adjustment for Gains > 1

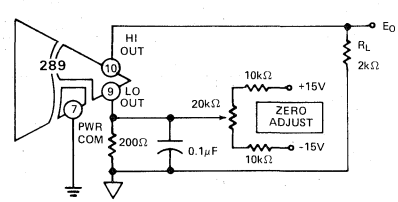


Figure 5b. Recommended Offset Adjustment for G = 1V/V

PERFORMANCE CHARACTERISTICS

Figure 6 shows the phase shift vs. frequency. The low phase shift and wide bandwidth of the model 289 make it suitable for use in SCR Motor Controller and other high frequency applications.

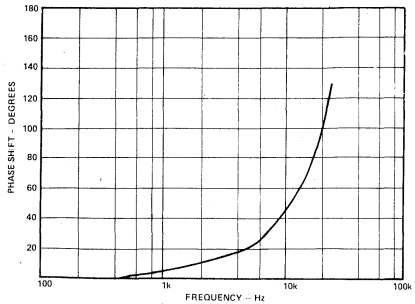


Figure 6. Typical 289 Phase vs. Frequency

Figure 7 illustrates the effect of source impedance imbalance on CMR performance at 60Hz for gains of 1V/V, 10V/V, and 100V/V. CMR is typically 120dB at 60Hz and a balanced source impedance. CMR is >60dB for source impedance imbalances up to 100kΩ.

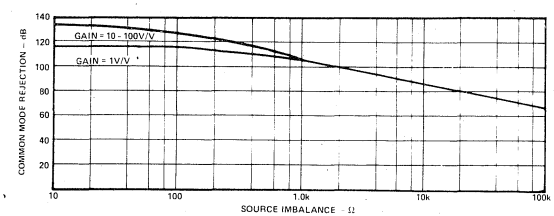


Figure 7. Typical 289 Common Rejection vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth. Figure 8 shows rms voltage noise in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. The peak-to-peak value is derived by multiplying the rms value at F = 100Hz (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the noise, referred to input.

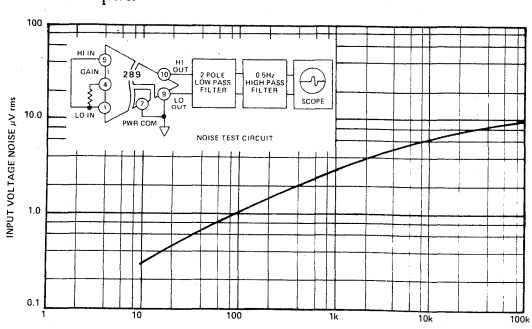


Figure 8. Typical Input Voltage Noise vs. Bandwidth

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % peak-to-peak output voltage span; e.g., nonlinearity of model 289J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V). Figure 10 shows the effect of gain vs. gain nonlinearity.

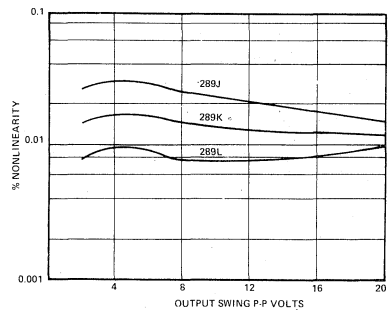


Figure 9. Typical Gain Nonlinearity vs. Output Swing

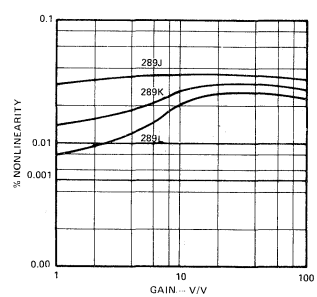


Figure 10. Typical Gain Nonlinearity vs. Gain

Common Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ imbalance at a gain of 100V/V. Figure 11 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalance as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 100V/V.

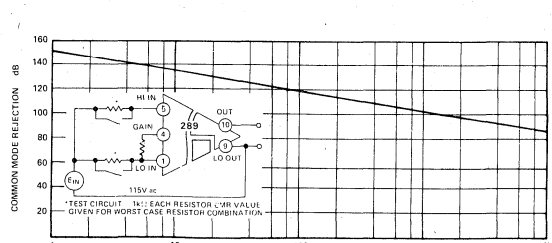


Figure 11. Typical Common Mode Rejection vs. Frequency

MULTICHANNEL APPLICATIONS

Isolation amplifiers containing internal oscillators may exhibit a slowly varying offset voltage at the output when used in multichannel applications. This offset voltage is the result of adjacent internal oscillators beating together. For example, if two adjacent isolation amplifiers have oscillator frequencies of 100.0kHz and 100.1kHz respectively, a portion of the difference frequency may appear as a slowly varying output offset voltage error. Model 289 eliminates this problem by offering a synchronization terminal (pin 8). When this terminal is interconnected with other model 289 synchronization terminals, the units are synchronized. Alternately, one or more units may be synchronized to an external 100kHz ±2% square-wave generator by the connection of synchronization termial(s) to that generator. The generator output should be 2.5V–5.0V p-p with 1kΩ source impedance to each unit. Use an external oscillator when you need to sync to an external 100kHz source, such as a sub-multiple of a microprocessor clock. A differential line driver, such as SN75158, can be used to drive large clusters of model 289. When using the synchronization pin, keep leads as short as possible and do not use shielded wire. These precautions are necessary to avoid capacitance from the synchronization terminal to other points. It should be noted that units synchronized must share the same power common to ensure a return path.

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Isolated DAS: In data acquisition systems where multiple transducers are powered by a single supply and the magnitude of that supply is low enough for a multiplexer to handle the voltages on all the transducers, it is economical to multiplex ahead of an isolator. The fast settling time of the model 289 makes this configuration practical where slower isolators would not be usable.

Figure 12 shows an application where the difference in voltage between any two terminals of any of the transducers does not exceed 30 volts. Though the input of the model 289 is protected against line voltage, its power terminals are not; neither is the multiplexer so protected. This circuit will not, therefore, withstand the differential application of line voltage.

Multiplexer addressing is binary, an enable providing selection of the circuit shown as a signal source. Optical isolation is provided for digital signals. When several of these circuits are used for several groups of transducers, the model 289's should be synchronized.

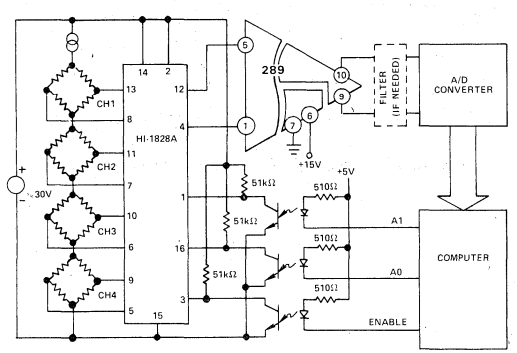


Figure 12. DAS with MUX Ahead of Isolator

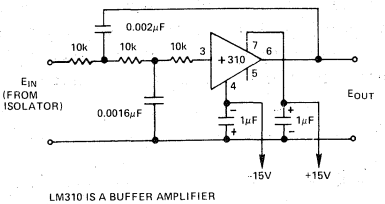


Figure 13. 2-Pole, 5kHz Active Filter

Noise Reduction in Data Acquisition Systems: Transformer coupled isolators must have a carrier to pass dc signals through their signal transformers. Inevitably some carrier frequency ripple passes through to the isolator output. As the bandwidth of an isolator becomes a larger fraction of its carrier frequency, this ripple becomes more difficult to control. Despite this difficulty, the model 289 produces very low ripple; therefore, additional filtration will usually be unnecessary. However, in some applications, particularly where a fast analog-to-digital converter is used following the isolator, it may be desirable to add filtration; otherwise, ripple may cause inaccurate conversions. The 2-pole low-pass shown in Figure 13 limits isolator bandwidth to 5kHz, which is the full power bandwidth of the model 289. Carrier ripple is much reduced. Another beneficial effect of an output filter is smoothing of discontinuous high frequency waveforms.

Motor Control and AC Load Control: Phase shift and bandwidth are important considerations for motor control and ac load control applications. The model 289 possesses sufficient bandwidth and acceptable phase shift for such tasks.

Figure 14 shows two model 289's sensing the armature voltage and current of a motor. Faithful replicas of the waveforms of these variables are applied to the motor control. A1 operates at unity gain from divided R1–R3 to deliver an output that is 1/100 of the armature voltage of the motor. A2 operates at a gain of 100V/V to deliver a voltage 100 times that developed across the current sensing shunt.

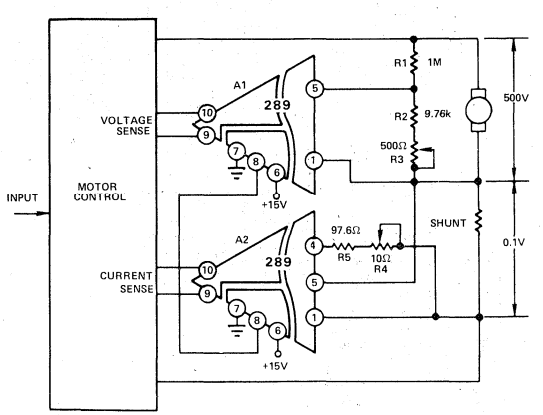


Figure 14. Isolating a Motor Controller

Figure 15 shows three model 289's sensing the voltages on the three phases of an ac load. The Y network shown divides the voltages of the three phases and creates a neutral for the input commons of the isolators. The output of each isolator is a faithful replica of the phase of the waveform it senses. The isolator outputs provide the feedback necessary for the trigger control to correctly fire the triacs. In other applications, the outputs of the isolators might have been fed to rms-to-dc converters.

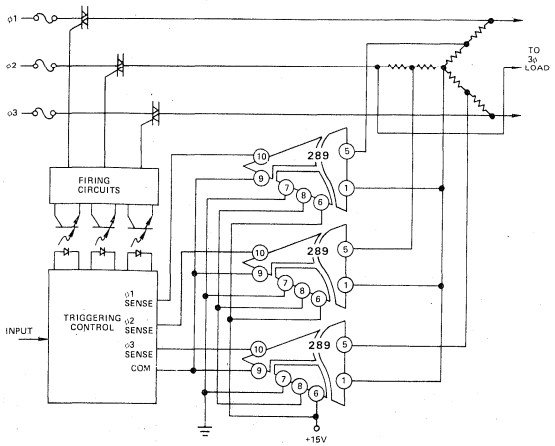


Figure 15. Isolating a 3 Phase Load Controller

Isolated DACs: Figure 16 shows a 12-bit DAC with ±5V isolated output. A buffered -5V reference voltage is provided to the DAC by A1a, A1b and associated circuitry. The digital input causes a proportion of DAC current to flow into OUT1 of the DAC. The remaining DAC current flows into OUT2. Current flowing into OUT1 causes positive voltage at the output of A1c. Current flowing into OUT2 causes a positive voltage at the output of A1d, which in turn causes a negative voltage at the output of A1c. Voltage appearing at the output of A1c is reproduced at the output of the model 289. R5 and R8 must be adjusted to produce less than 0.5mV at OUT1 and OUT2 of the DAC respectively. R15 may be used to adjust gain and R11 to adjust offset with the binary code 1000 0000 0000 to zero.

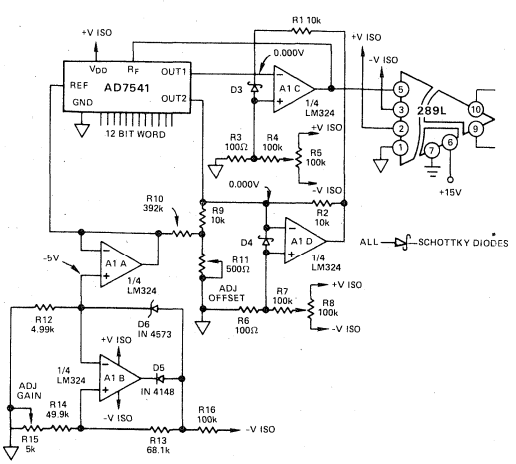


Figure 16. 12-Bit Isolated Voltage DAC

Figure 17 shows the model 289 providing an isolated 4-to-20mA output from a 12-bit DAC. A1a provides a -4V reference to the DAC. The digital input causes a portion of DAC current to flow into OUT1, causing a positive voltage at the output of A1d. A1b produces a voltage across R4 proportional to DAC current. A1c and associated circuitry sink a current which is one-fourth of the full scale current of the DAC, causing a positive voltage of 1 volt at the output of A1d. With the code 1111 1111 1111, +5 volts appears at the output of A1d. Operation is unipolar with a positive offset. The output voltage of A1d is reproduced at the output of the isolator, where the circuitry shown converts it into a 4-to-20mA current which may be applied to the load R_L.

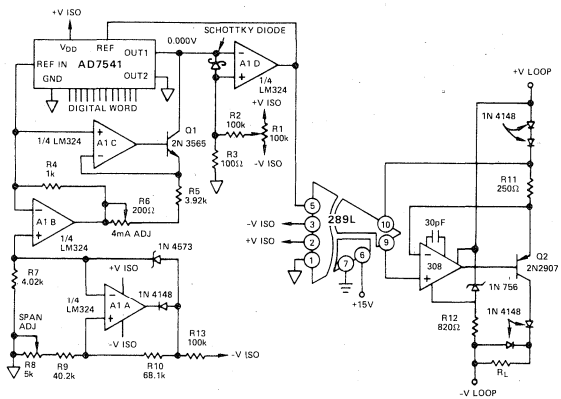


Figure 17. 12-Bit Isolated Process Current DAC

Temperature Measurement: Figure 18 shows the model 289 providing a ground-referred output in an application measuring the temperature of an object floating at a high common mode voltage. The AD590 temperature sensor sinks a current of -1μA/K. This current flows into the gain terminal of the model 289, developing +10mV/K across the internal feedback resistor. This voltage also appears at the output of the model 289.

The circuitry shown connected by a dotted line may be useful if an output of 10mV/°C is desired. A current of +273μA is sourced through the 8.66k resistor and the potentiometer cancelling the AD590 current at 0°C (273K), resulting in 0mV at the output at 0°C.

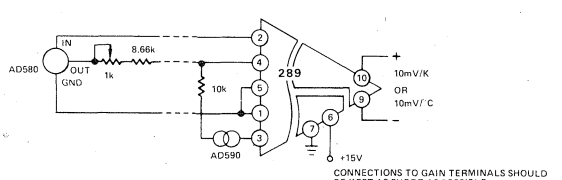


Figure 18. Isolated Temperature Measurement

Low Cost, Single and Multichannel Isolation Amplifier

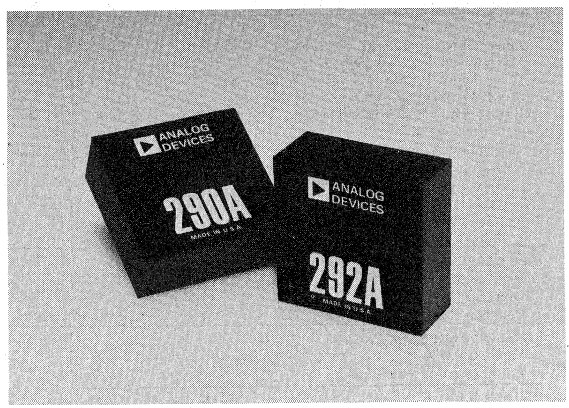
MODELS 290A, 292A

FEATURES

Low Cost
Multichannel Capability Using External Oscillator (292A)
Isolated Power Supply: ±13V dc @ ±5mA (290A) or ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ × 1.5″ × 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Fetal Heart Biomedical and Monitoring Instrumentation
Off-Ground Signal Measurements



GENERAL DESCRIPTION

Models 290A and 292A are low cost, compact, isolation amplifiers that are optimized for single and multichannel industrial applications, respectively. The model 290A has a self-contained oscillator and is intended for single channel applications. A single external synchronizing oscillator can drive up to 16 model 292A's or, a virtually limitless number of model 292A's can be configured using multiple oscillators. The user can supply the external oscillator circuit or specify model 281 oscillator module, which includes a voltage regulator for operation over a wide single supply voltage range of +8V to +28V.

Models 290A and 292A design features include: adjustable gain, from 1 to 100V/V, dual isoalted power, ±13V dc, ±1500V dc off ground isolation, 100dB minimum CMR at 60Hz, 1kΩ source imbalance, in a compact 1.5″ × 1.5″ × 0.6″ epoxy encapsulated module. Models 290A and 292A achieve low input noise of 1μV pk-pk (10Hz bandwidth, G = 100V/V), nonlinearity of ±0.1% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, models 290A and 292A will interrupt ground loops, leakage paths, and voltage transients, while providing dc to 2kHz (–3dB) response.

WHERE TO USE MODELS 290A AND 292A

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 290A and 292A offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with 20V pk-pk input signal range at a gain of 1V/V operation. In portable single or multichannel designs, single power supply operation (+8V to +16V) enables battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±13V dc output, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Models 290A and 292A adjustable gain offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 100V/V providing flexibility in both high level transducer interfacing as well as low level sensor measurement applications.

Floating, Guarded Front-End: The input stage of models 290A and 292A can directly accept floating differential signals or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Models 290A and 292A are conservatively designed, compact modules, capable of reliable operation in harsh environments. They have a calculated MTBF of over 400,000 hours and are designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

SPECIFICATIONS (typical @ +25°C; G = 100V/V and V_S = +15V dc, unless otherwise noted)

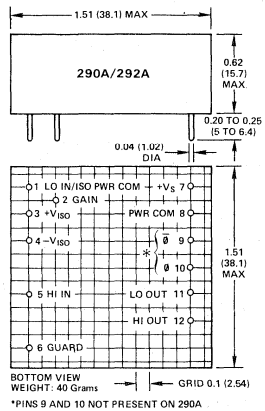
MODEL	290A	292A
GAIN (NONINVERTING)		
Range (50kΩ Load)	1 to 100V/V	
Formula	$\text{Gain} = \left[1 + \frac{100k\Omega}{1k\Omega + R_i\,(k\Omega)}\right]$	
Deviation from Formula	±3%	
vs. Time	±0.001%/1000 Hours	
vs. Temperature (−25°C to +85°C)[1]	±0.0075%/°C	
Nonlinearity, G = 1V/V to 100V/V[2]	±0.1% (±0.25%)[3]	
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V	±5V min (±10V min)[3]	
Max Safe Differential Input		
Continuous, 1 min	110V rms	
Max CMV, Inputs to Outputs		
ac, 60Hz, 1 Minute Duration	1500V rms max	
Continuous, ac	±1000V pk max	
Continuous, dc	±1500V pk max	
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k\Omega$		
Balanced Source Impedance	106dB	
1kΩ Hi In Lead Only	100dB min	
Max Leakage Current, Inputs to Power Common		
@ 115V ac, 60Hz	10μA rms max	
INPUT IMPEDANCE		
Differential	$10^8\,\Omega \| 70pF$	
Overload	100kΩ	
Common Mode	$5 \times 10^{10}\,\Omega \| 100pF$	
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	+3nA	
vs. Temperature (−25°C to +85°C)	±0.1nA/°C	
INPUT NOISE		
Voltage, G = 100V/V		
0.01Hz to 10Hz	1μV p-p	
10Hz to 1kHz	1.5μV rms	
Current		
0.05Hz to 100Hz	5pA p-p	
FREQUENCY RESPONSE		
Small Signal, −3dB, G = 1V/V	2.5kHz	
Slew Rate	50mV/μs	
Full Power, 10V p-p Output		
Gain - 1V/V thru 100V/V	2.0kHz(1.0kHz)[3]	3.0kHz(1.0kHz)[3]
OFFSET VOLTAGE REFERRED TO INPUT		
Initial, @ +25°C, Adjustable to Zero	±(5 + 50/G)mV	
vs. Temperature (−25°C to +85°C)	±(10 + 150/G)μV/°C	±(8 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%	
RATED OUTPUT		
Voltage, 50k Load	±5V min (±10V min)[3]	
Output Impedance	1kΩ	
Output Ripple, 1MHz Bandwidth	10mV pk-pk	
OSCILLATOR DRIVE INPUT		
Input Voltage	N/A	8 to 16V pk-pk
Input Frequency	N/A	100kHz ±5%, max
ISOLATED POWER OUTPUTS		
Voltage Full Load	±13V dc	
Accuracy	±5%	
Current[4]	±5mA min	±15mA min
Regulation, No Load to Full Load	+0, −15%	
Ripple, 100kHz Bandwidth	200mV p-p	250mV p-p
POWER SUPPLY, SINGLE POLARITY		
Voltage, Rated Performance	+15V dc	
Voltage, Operating	+8V dc to +15.5V dc	
Current, Quiescent	+20mA	
TEMPERATURE RANGE		
Rated Performance	−25°C to +85°C	
Storage	−55°C to +85°C	
CASE DIMENSIONS	1.5″ X 1.5″ X 0.62″	

[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] These specs apply for a 20V pk-pk output span.
[4] Do not load V_{ISO} when operating at output spans greater than 10V pk-pk.

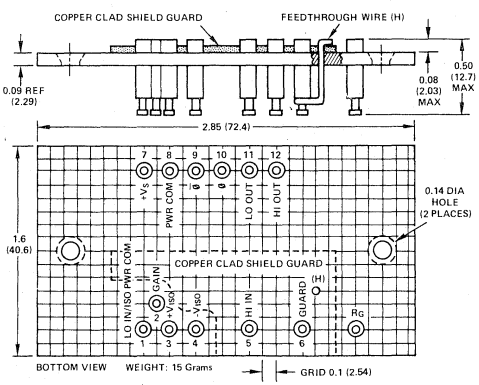
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MOUNTING SOCKET AC1054



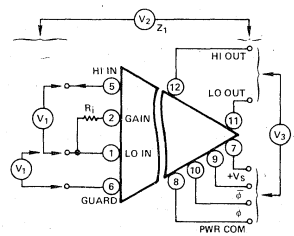


Figure 1. Model 290A and 292A Terminal Ratings

Symbol	Rating	Remarks
V_1	±110V rms (cont.)	Withstand Voltage, Steady State
V_2	±1000V pk (cont.)	Isolation, Steady State, ac
V_2	±1500V pk (cont.)	Isolation, Steady State, dc
V_2	±1500V rms (1 min)	Isolation, ac, 60Hz
V_3	±50V pk (cont.)	Isolation, dc
Z_1	$50G\Omega \| 20pF$	Isolation Impedance

Table 1. Isolation Ratings Between Terminals

THEORY OF OPERATION

The remarkable performance of models 290A and 292A are derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for both models is shown in Figure 2 below.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating the isolator at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 10pF leakage capacitance between the floating input section and the rest of the circuitry keeps the CMR from being infinite.

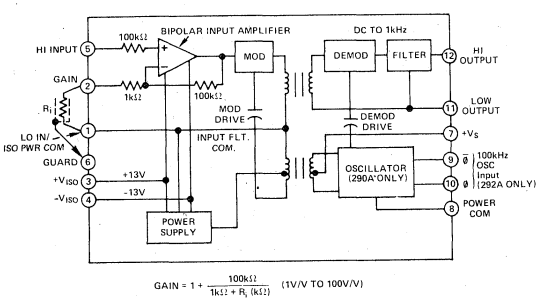


Figure 2. Block Diagram – Models 290A and 292A

GUIDELINES ON EFFECTIVE SHEILDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 3. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 86dB CMR capability of both models between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

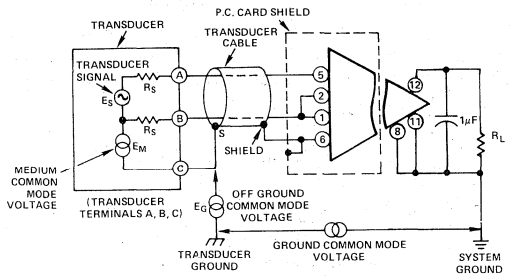
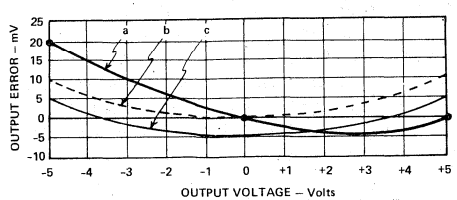


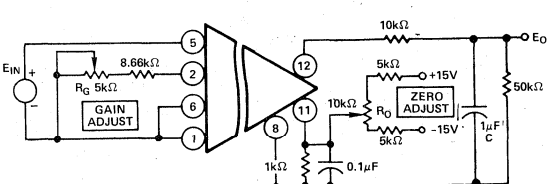
Figure 3. Transducer – Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.5V dc and adjust R_G for E_O = +5.0V dc.
3. Apply E_{IN} = -0.5V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.5V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).





GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i(k\Omega)}$$

OUTPUT FILTER, 10kΩ RESISTOR AND CAPACITOR, C.
SELECT C TO ROLL-OFF NOISE AND OUTPUT RIPPLE:

$$f = (-3dB) = \frac{1}{2\pi C\,(11k\Omega)}$$

Figure 4. Gain and Offset Adjustment

SELECTING BANDWIDTH

In low frequency signal measurements, such as thermocouple temperature measurements, strain gage measurements and geophysical instrumentation, an external filter is used to select bandwidth and minimize output noise.

When used with a buffer amplifier as shown in Figure 5a below, a series resistor (R_S) is used to lower the effective value of the filter capacitor required to achieve very low frequency (under 200Hz) noise filtering.

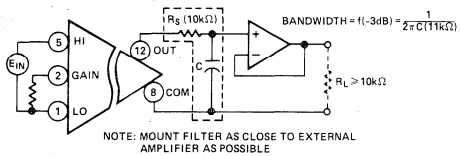


Figure 5a. Selecting Bandwidth with External Capacitor and Buffer

An active filter, as illustrated in Figure 5b will significantly improve 60Hz noise reduction at the output by providing a sharp roll-off characteristic. The 5Hz 3-pole active filter design illustrated in Figure 5b, will increase the 60Hz noise reduction by 50dB. Overall CMR performance of models 290 and 292 and the 5Hz active filter approaches 150dB @ 60Hz and 1kΩ imbalance.

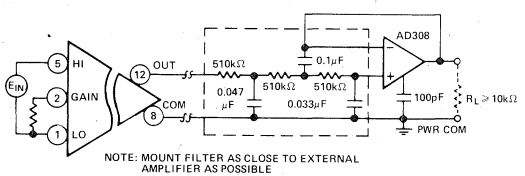


Figure 5b. Selecting Bandwidth with a 3-Pole 5Hz Active Filter

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ imbalance at a gain of 100V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 130dB at dc with source imbalances as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 12dB lower than at a gain of 100V/V.

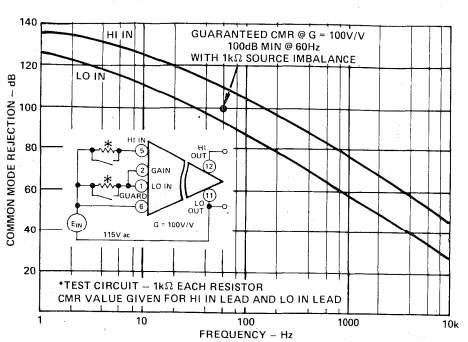


Figure 6. Typical Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 100V/V. CMR is typically 110dB at 60Hz and a balanced source. CMR is maintained greater than 70dB for source imbalances up to 100kΩ.

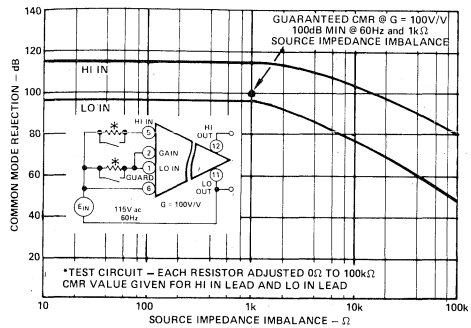


Figure 7. Typical Common Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of models 290A and 292A operating at an output span of 10V pk-pk (±5V) is ±0.1% or ±10mV. Figure 8 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

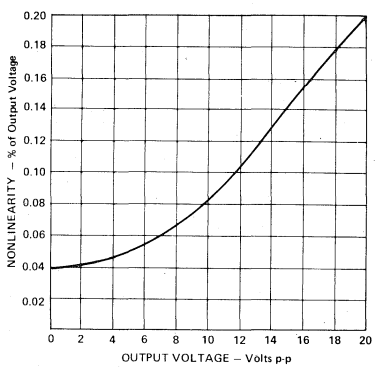


Figure 8. Typical Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 9. RMS voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.01Hz to 10Hz is 1μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 10Hz shown in Figure 9 by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the input noise.

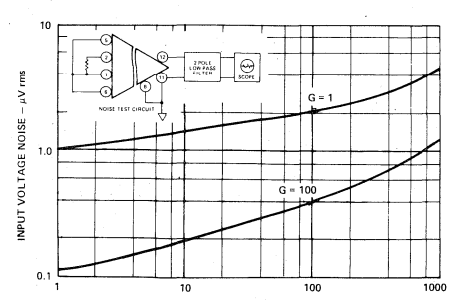


Figure 9. Typical Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 10 illustrates total input drift over the gain range of 1 to 100V/V.

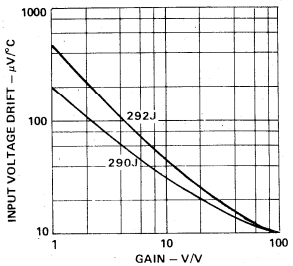
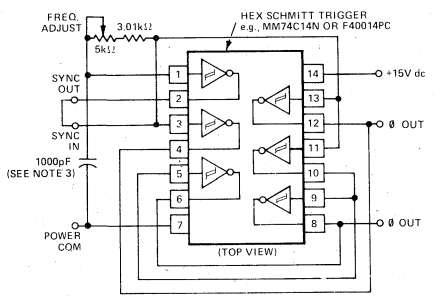


Figure 10. Typical Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR, MODEL 281

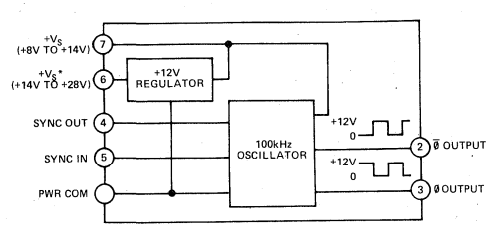
When applying model 292A, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 11, or purchasing a module from Analog Devices—model 281.



NOTES:
1. FREQ. ADJUST: ADJUST TRIM POT FOR OUTPUT FREQUENCY OF 100kHz ±5%.
2. FOR SLAVE OPERATION, REMOVE JUMPER FROM SYNC OUT AND SYNC IN PINS.
3. USE CERAMIC CAPACITOR, "COG" OR "NPO" CHARACTERISTIC.

Figure 11. 100kHz Oscillator Interconnection Diagram

The block diagram of model 281 is shown in Figure 12. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7.

Figure 12. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 292A's. As shown in Figure 13, an additional model 281 may be driven in a slave-mode to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

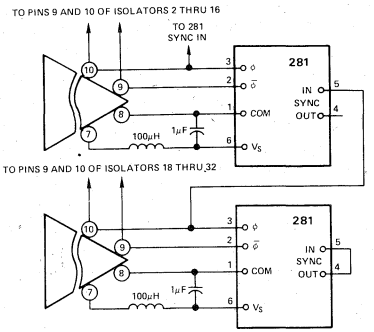


Figure 13. External Oscillator Interconnection

SPECIFICATIONS

(typical @ +25°C and V_S = +15V dc unless otherwise noted)

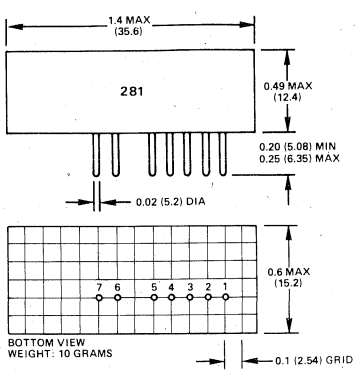
MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	1ϕ max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C

[1] Model 292A oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 292A's, additional 281's may be used in a master/slave mode. Refer to Figure 13.
[3] Full load consists of 16 model 292A's and 281 oscillator slave.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC INPUT
2	$\bar{\phi}$ OUTPUT	6	+V_S: HIGH RANGE +(14 to 28)V dc
3	ϕ OUTPUT	7	+V_S: LOW RANGE +(8 to 14)V dc
4	SYNC OUTPUT		

MATING SOCKET:
CINCH #16 DIP OR EQUIVALENT

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, models 290A and 292A can be applied to measure and control off-ground millivolt signals in the presence ±1500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, models 290A and 292A offer complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of these models.

Figure 14 illustrates how model 290A or 292A can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Both products provide isolated ±13V dc power and front-end guard in addition to eliminating ground loops and preserving high CMR (100dB @ 60Hz).

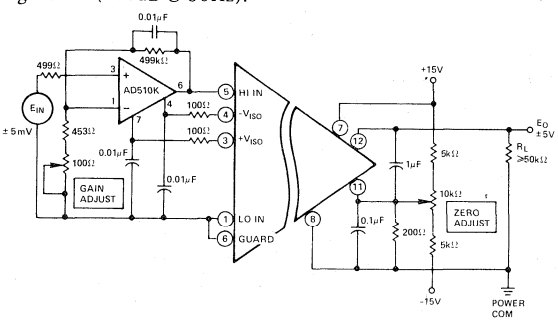


Figure 14. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Models 290A and 292A provide a floating guarded input stage capable of directly accepting isolated differential signals. The noninverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, models 290A and 292A can be connected as shown in Figure 15. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 15.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum E_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum E_O.
4) Repeat steps 2 and 3 for best CMR performance.

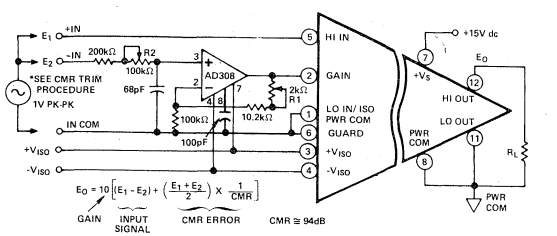


Figure 15. Application of 290A as Instrumentation Amplifier

Isolated Temperature Measurements: Industrial temperature measurements are often performed in harsh environments where line voltages or transients can sometimes be impressed on the temperature sensor. To provide protection for the delicate recording instrumentation, models 290A and 292A can be applied as shown in Figure 16. The Analog Devices' AC2626 probe is a temperature sensor whose output is a current directly proportional to absolute temperature. The isolation amplifier provides the isolated power (+13V dc) as well as the input/output isolation. Zero calibration is performed by placing the AC2626 probe in a zero temperature bath and adjusting R_O for E_O to 0 volts. Full scale output adjustment is performed by placing the AC2626 probe in boiling water (100°C) and adjusting R_S for 1.000V output.

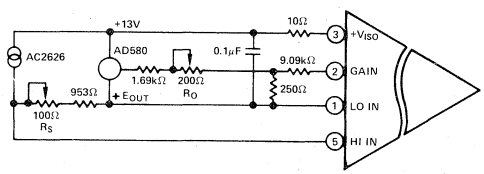


Figure 16. Isolated Temperature Measurements

Current Loop Receiver: Model 290A and 292A can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 17 shows an application of model 290A or 292A as a current loop receiver. A 25Ω resistor converts the 4-20mA current input from a remote loop to a 100–500mV differential voltage input, which the isolator amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the isolator in this kind of measurement are the high common-mode rejection (100dB minimum at 60Hz with 1kΩ source unbalance) and the high common-mode rating (±1500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

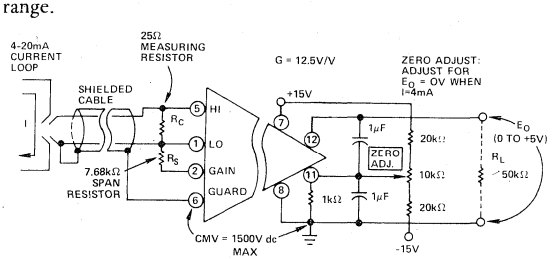


Figure 17. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±1500V of Isolation

Multipliers & Dividers

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Selection Guide
Multipliers & Dividers

In this Selection Guide, multiplier/divider products are partitioned into four categories:

1. General-purpose devices capable of optimization as multipliers or dividers
2. Internally trimmed devices optimized as multipliers
3. Internally trimmed devices optimized as dividers
4. Multifunction devices

Complete and detailed specifications, descriptions, and application information can be found in the data sheets. General information and definitions of important specifications can be found in the following pages.† Specifications are typical at rated supply voltage and load, and $T_A = +25^\circ C$, unless noted otherwise.

1. GENERAL-PURPOSE EXTERNALLY TRIMMED DEVICES

Type	Characteristics	Page
AD533J/K/L/S	Lowest cost general-purpose 4-quadrant IC, external trim to 0.5% max total error (L)	4–13

2. INTERNALLY TRIMMED MULTIPLIERS

Type	Characteristics	Page
AD532J/K/S#	General-purpose 4-quadrant IC, differential inputs, standard pinouts, internally trimmed to 1.0% max total error (K), 0.04%/°C max (S)	4–7
Model 435J/K	Highest-accuracy 4-quadrant, module, pretrimmed to 0.1% max total error (K), 0.01%/°C max (K)	*
Model 429A/B	Widest-bandwidth 4-quadrant, module, full-power response to 2MHz min, slewing rate 120V/μs min, –3dB bandwidth 10MHz, small-signal, 1% settling-time 500ns; pretrimmed to 0.5% max error (B)	4–31
AD534J/K/L/S/T#	High-accuracy internally trimmed 4-quadrant IC multiplier featuring 0.25% max total error (L), low noise (90μV rms, 10Hz – 10kHz), and versatile differential input configuration.	4–7

3. INTERNALLY TRIMMED DIVIDERS

Type	Characteristics	Page
Model 436A/B	High-accuracy 2-quadrant divider-only module, pretrimmed to 0.25% max error (B, denominator [V_X] range from +0.1V to +10V [$\|V_Z\| \leq \|V_X\|$]), 2% max error over temperature (B), 1% max error 0 to +70°C.	
AD535J/K#	IC 2-quadrant divider, pretrimmed for 0.5% max total error (K version) for 10:1 denominator range. Differential inputs permit choice of denominator range. Differential inputs permit choice of denominator polarity.	4–25

4. MULTIFUNCTION DEVICES

Type	Characteristics	Page
Model 433J/B	Programmable multifunction module, $Y(Z/X)^m$ ($10V/E_{REF}$), one-quadrant, m adjustable from 0.2 to 5, max division error 25mV (B, V_Z from 0.01V to 10V, V_X from 0.1V to 10V, $V_Z \leq V_X$), 1% max over temperature.	4–35

†Letter suffixes denote temperature range and performance grade. J/K/L are specified for 0 to +70°C; A/B are specified for –25°C to +85°C; S/T are specified for –55°C to +125°C.
#Monolithic chips available with guaranteed performance for precision hybrids. Chip catalog available upon request.
*Data sheet available upon request.

Orientation
Multipliers & Dividers

The devices catalogued in this section accept analog voltages and multiply, divide, square, and/or square-root them, depending on device properties and connections.

Multiplication For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_x V_y / E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If E_{ref} = 10V, E_{out} = 10V when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement, and mathematical operations in analog computing, curve fitting, and linearizing.

If the inputs may be of either positive or negative polarity, and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the 4 quadrants of the X-Y plane.

Squaring If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2 / E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive, whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads, and mathematical operations.

Division For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If E_{ref} = 10V, E_{out} will be 10V or less for $V_z \leqslant V_x$. V_x is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios—such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements, and for mathematical operations in analog computing.

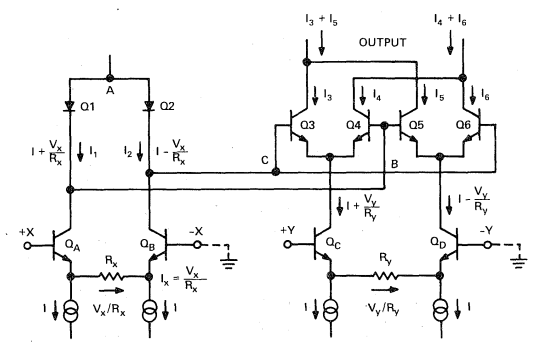
Square rooting For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref} V_{in}}$. A square-rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, etc.

A number of devices are listed here, differing in internal architecture, external functional configuration, device technology, and performance specifications. Some have essentially fixed references; others have an actively variable or programmable reference as a third input (*multifunction devices*), and one type (model 433) performs the one-quadrant operation, $E_o = V_z(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5. With one exception (model 436 precision 2-quadrant divider), all of the devices listed here can be used for any of the functions defined above.

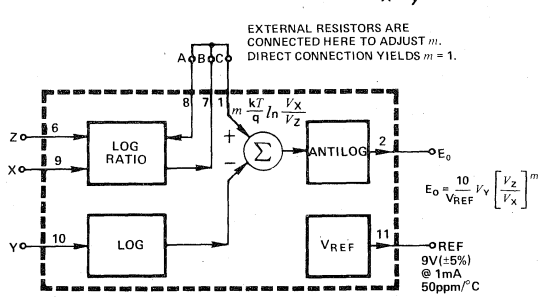
Considerable information on these functions, the nature of devices to perform them, and extensive discussions of their applications can be found in two publications available from Analog Devices.[1,2] A wealth of information is also to be found in the data sheets for the individual devices, published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture All of the devices in this selection rely on the logarithmic properties of silicon P-N junctions. With the exception of models 433 and 436, the circuit employed is basically like that of the "Gilbert cell" (its 4-quadrant-multiplying circuitry and performance are described in (1) and (2), with further references to original sources). The input voltages are converted to currents, the currents are multiplied together and divided by a reference, and the net output current, $I_x I_y / I_{ref}$, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division. In the AD531[3], the I_{ref} terminals are available for external programming or variation; thus, the AD531 is a 3-variable "multifunction" IC which can divide without external feedback. This versatile feature offers greater bandwidth as a divider.



Basic 4-quadrant variable-transconductance multiplier circuit

$$I_o = (I_3 + I_5) - (I_4 + I_6) = \frac{2 V_X V_Y}{I R_X R_Y}$$



Functional Block Diagram of Model 433.

In multifunction devices like Model 433, the feedback currents of the input op amps are used to develop logarithmic

[1] *Multiplier Application Guide*, available upon request

[2] *Nonlinear Circuits Handbook*, D. H. Sheingold, ed., 1976, 536pp., $5.95, P.O. Box 796, Norwood MA 02062

[3] Data sheet available upon request.

voltages across transistor base-emitter junctions; these voltages are summed and differenced and produce an exponential current proportional to V_yV_z/V_x via another transistor junction in the input path of the output amplifier. Thus, the output voltage is proportional to V_yV_z/V_x; an internally generated reference voltage is available as a fixed reference for the odd input in two-variable operations. In the 433, the internal emitter-voltage difference proportional to log (V_z/V_x) can be amplified or attenuated by the appropriate connection of a resistive attenuator with an attenuation ratio, m; since the antilog of m(log V_z/V_x) is $(V_z/V_x)^m$, the output of the 433 is proportional to $V_y(V_z/V_x)^m$. In the model 436 divider, the inputs are scaled and linearly combined, before the log-antilog computation takes place; the result is that the numerator (of V_z/V_x) may have positive or negative values. The 436 circuit is optimized and trimmed for performance as a dedicated divider; it has a fixed reference. Its circuit principles are discussed in some detail on the data sheet.

External functional configuration As noted earlier, with the exception of the model 436 dedicated divider, all of the devices listed here can be used for multiplication, division, squaring, and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. As an example, the AD534 is shown connected for multiplication, and the AD535, which has similar architecture but is optimized for division, is shown connected for division and square-rooting. Performance of pretrimmed devices is optimized in specified modes of operation, usually multiplication. The data sheets show how devices are connected for the various modes of operation; where appropriate, the trim circuits and procedures for optimizing performance are provided.

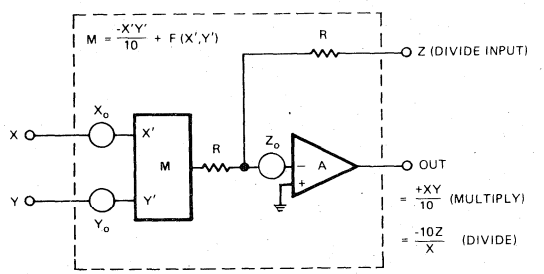
Some devices have differential inputs, which provide a great deal of flexibility. They permit polarity changes without external inversion, direct subtraction of inputs, insertion of bias voltages for additive constants, and direct multiplication of the results of differential measurements.

Technologies The devices described here are either monolithic integrated circuits or high-performance modules. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The modules provide the highest performance: speed (model 429), accuracy as a divider (436), and accuracy in multifunction applications (433). On the other hand, the IC's provide economy of cost and space, and the availability of "mil-temp" range (-55°C to +125°C) versions. The pretrimmed IC's (AD534, AD535 and AD532) use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors to 0.25%, and linearities as yet unmatched in the industry.

Performance Multiplier performance, specifications and test circuitry are described in great detail in the NONLINEAR CIRCUITS HANDBOOK. Here is a brief digest of the factors relating to low-frequency performance.

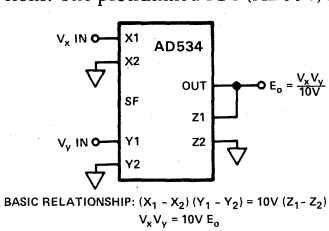
In theory, a multiplier has an output which is ideally the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities, which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practice (see the figure), the multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is the gain-conditioning op amp, A.

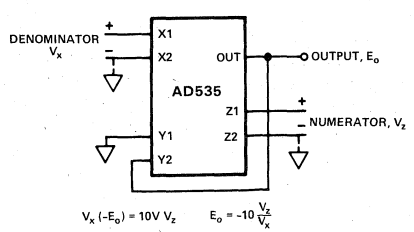


Functional Block Diagram of Typical Multiplier/Divider

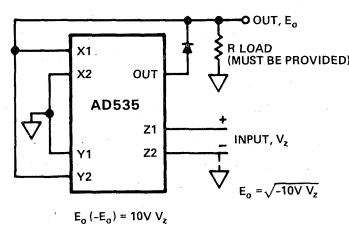
Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model used for considering errors. X_0 and Y_0 are input offset voltages, Z_0 is the offset-referred-to-the-input of the output amplifier, and $F(X', Y')$ is the nonlinearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form



Multiplier



Divider



Square Rooter

$$E_o = \frac{XY}{10B} \pm \left[\underbrace{\frac{X_o Y}{10B}}_{\substack{X_{offset} \\ \text{Linear} \\ \text{“Y”}}} \pm \underbrace{\frac{XY_o}{10B}}_{\substack{Y_{offset} \\ \text{Feedthrough} \\ \text{“X”}}} \pm \underbrace{Z_o}_{\substack{\text{Output} \\ \text{offset}}} + \underbrace{f(X,Y)}_{\substack{\text{Nonlinearity} \\ \text{and feedthrough}}} \right]$$

Product

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by applying external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_X| \epsilon_X + |V_Y| \epsilon_Y$$

were ϵ_X and ϵ_Y are the specified fractional linearity errors (%/100) and V_X and V_Y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_X$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (e.g., 10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of X.

DEFINITIONS OF SPECIFICATIONS*

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Scale Factor The *scale-factor error* (or *gain* error) is the difference between the average scale factor and the ideal scale factor (e.g., $(10V)^{-1}$). It is expressed in percent of the output signal. *Temperature dependence* is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the multiplier may improve small-signal resolution significantly.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error,* and *settling time.*

Small-signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

Full-power response is the maximum frequency at which the multiplier can produce full-scale voltage into its rated load without noticeable distortion.

Slew(ing) rate is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

Small-signal amplitude error is defined in relation to the frequency at which the amplitude response, or scale factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling time, for the product of a ±10V step and 10Vdc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Vector error is the most-sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.

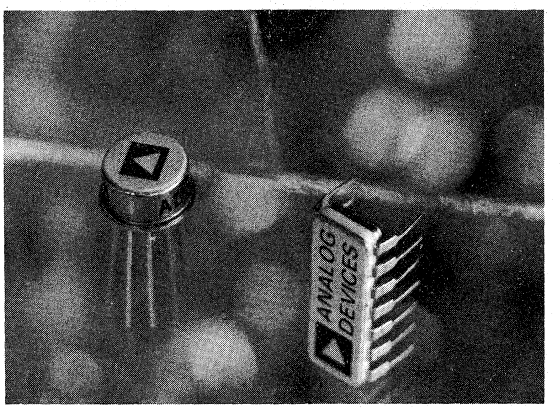
*These are general definitions. Further definitions are provided as footnotes to the specification tables; they should be read carefully.

Internally Trimmed Integrated Circuit Multiplier

AD532

FEATURES
- Pretrimmed To ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs For $(X_1-X_2)(Y_1-Y_2)/10$ Transfer Function
- Monolithic Construction, Low Cost

APPLICATIONS
- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications



PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10$, divides in two quadrants with a $10Z/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10Z}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as $XY/10$, $(X^2-Y^2)/10$, $\pm X^2/10$, and $10Z/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of -55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP packages.

ADVANTAGES OF ON-THE-CHIP TRIMMING OF THE MONOLITHIC AD532

1. True ratiometric trim for improved power supply rejection.
2. Reduced power requirements since no networks across supplies are required.
3. More reliable since standard monolithic assembly techniques can be used rather than more complex hybrid approaches.
4. High impedance X and Y inputs with negligible circuit loading.
5. Differential X and Y inputs for noise rejection and additional computational flexibility.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, V_{OS} grounded, unless otherwise specified)

PARAMETER	CONDITIONS	AD532J	AD532K	AD532S
ABSOLUTE MAX RATINGS				
Supply Voltage		±18V	*	±22V
Internal Power Dissipation		500mW	*	*
Input Voltage (Note 1)				
X, Y, V_{OS}, Z		$\pm V_S$	*	*
Rated Operating Temp Range		0 to +70°C	*	−55°C to +125°C
Storage Temp Range		−65°C to +150°C	*	*
Lead Temperature	60 Sec Soldering	+300°C	*	*
Output Short Circuit	To Ground	Indefinite	*	*
MULTIPLIER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)(Y_1-Y_2)/10$	*	*
Total Error (% F.S.)	V_X = 0/±10V, V_Y = 0/±10V	±2.0% max [±1.5% typ]	±1.0% max [±0.7% typ]	±1.0% max [±0.5% typ]
	T_A = min to max	±2.5%	±1.5%	±4.0% max
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.04%/°C max [±0.01%/°C typ]
Nonlinearity				
X Input	V_X = 20V(p-p), V_Y = ±10V	±0.8%	±0.5%	**
Y Input	V_Y = 20V(p-p), V_X = ±10V	±0.3%	±0.2%	**
Feedthrough				
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	200mV(p-p) max [50mV(p-p) typ]	100mV(p-p) max [30mV(p-p) typ]	**
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	150mV(p-p) max [30mV(p-p) typ]	80mV(p-p) max [25mV(p-p) typ]	**
vs. Temperature	T_A = min to max	2.0mV(p-p)/°C	1.0mV(p-p)/°C	**
DIVIDER SPECIFICATIONS				
Transfer Function		$10Z/(X_1-X_2)$	*	*
Total Error (Note 2)	V_X = −10V, V_Z = ±10V	±2%	±1%	**
	V_X = −1V, V_Z = ±10V	±4%	±3%	**
SQUARER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)^2/10$	*	*
Total Error		±0.8%	±0.4%	**
SQUARE ROOTER SPECIFICATIONS				
Transfer Function		$-\sqrt{10Z}$	*	*
Total Error (Note 2)	V_Z = 0/+10V	±1.5%	±1.0%	**
INPUT SPECIFICATIONS				
Input Resistance				
X, Y Inputs		10MΩ	*	*
Z Input		36kΩ	*	*
Input Bias Current				
X, Y Inputs		3μA	4μA max [1.5μA typ]	**
Z Input		±10μA	±15μA max [±5μA typ]	**
X, Y Inputs	T_A = min to max	10μA	8μA	**
Z Input	T_A = min to max	±30μA	±25μA	**
Input Offset Current				
X, Y Inputs		±0.3μA	±0.1μA	**
Input Voltage Diff/CM	T_A = min to max			
X, Y, Z Inputs	For Rated Accuracy	±10V	*	*
CMRR (X or Y Inputs)	X or Y = ±10V	40dB min	50dB min	**
DYNAMIC SPECIFICATIONS				
Small Signal, Unity Gain		1.0MHz	*	*
Full Power Bandwidth		750kHz	*	*
Slew Rate		45V/μs	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*
Small Signal 1% Vector Error	0.5° phase shift	5kHz	*	*
Settling Time	±10V step	1μs to 2%	*	*
Overload Recovery		2μs to 2%	*	*
OUTPUT AMPLIFIER SPECIFICATIONS				
Output Impedance	Closed Loop	1Ω	*	*
Output Voltage Swing	T_A = min to max			
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min [±13V typ]	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*
Output Offset Voltage				
Initial Offset	Trimmable To Zero	±40mV	±30mV max	**
vs. Temperature	T_A = min to max	0.7mV/°C	*	2.0mV/°C max
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	*	*
	Operating	±10V to ±18V	*	±10V to ±22V
Supply Current	Quiescent	±6mA max [±4mA typ]	*	*
Power Supply Variation				
Multiplier Accuracy		±0.05%/%	*	*
Output Offset		±2.5mV/%	*	*
Scale Factor		−0.03%/%	*	*
Feedthrough		±0.25mV/%	*	*

NOTE: 1. Max input voltage is zero when supplies are turned off. 2. With recommended external trim (see Applications).

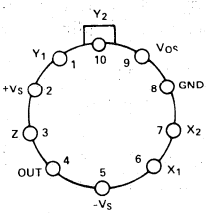
*Specifications same as AD532J. Specifications subject to change without notice.

**Specifications same as AD532K.

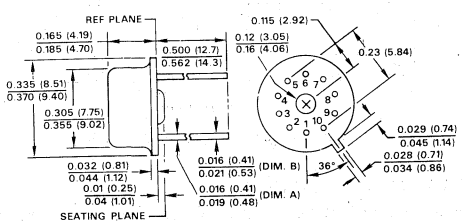
PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

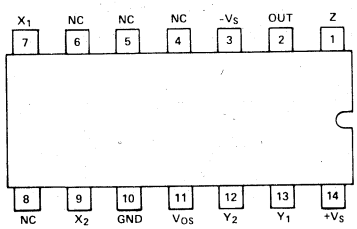
AD532H



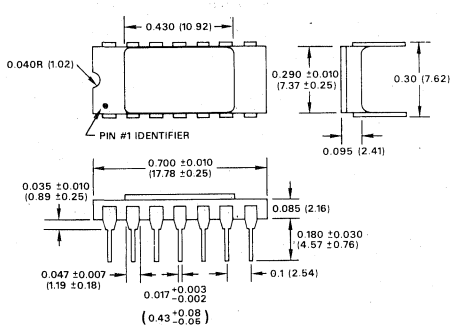
TO-100



AD532D



TO-116



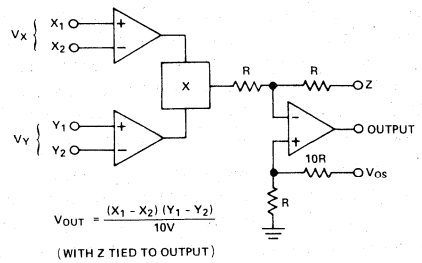


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1, and the complete schematic in Figure 2. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{OUT} = (X_1 - X_2)(Y_1 - Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{OS} in critical applications . . . . otherwise the V_{OS} pin should be grounded.

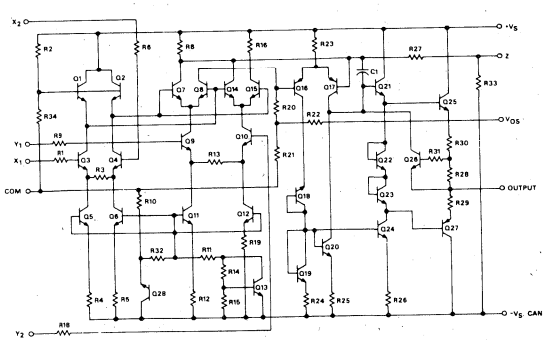


Figure 2. AD532 Schematic Diagram

ORDERING GUIDE

MODEL*	MAX MULT ERROR	TEMPERATURE RANGE
AD532JH/D	±2.0%	0 to +70°C
AD532KH/D	±1.0%	0 to +70°C
AD532SH/D	±1.0%	-55°C to +125°C
AD532SH/883	±1.0%	-55°C to +125°C
AD532SD/883	±1.0%	-55°C to +125°C

*Add suffix.....H for TO-100 package; D for TO-116 package.

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 13. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwidth and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10/X_1 - X_2)$ where ϵ_m represents multiplier full scale error and drift, and $(X_1 - X_2)$ is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 3 and 4 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 4 the sine wave amplitude is 20V(p-p).

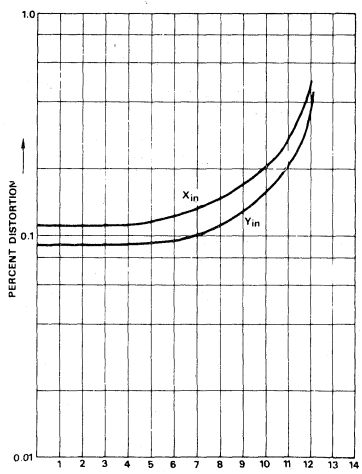


Figure 3. Percent Distortion vs. Input Signal

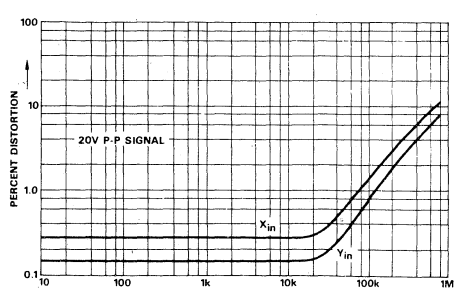


Figure 4. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 5. It is measured for the condition $V_X = 0$, $V_y = 20V(p\text{-}p)$ and $V_y = 0$, $V_X = 20V(p\text{-}p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

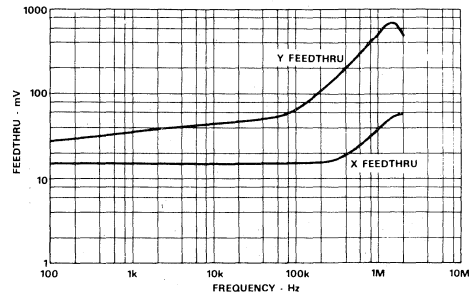


Figure 5. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 6. It is measured with $X_1 = X_2 = 20V(p\text{-}p)$, $(Y_1 - Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p\text{-}p)$, $(X_1 - X_2) = \pm 10V$ dc.

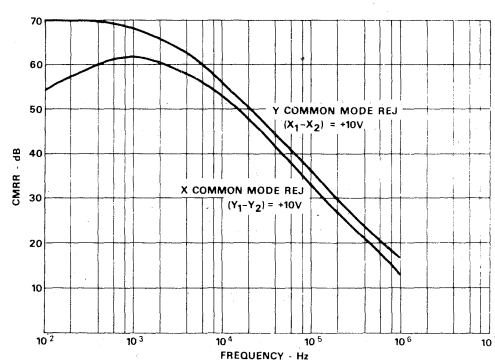


Figure 6. CMRR vs. Frequency

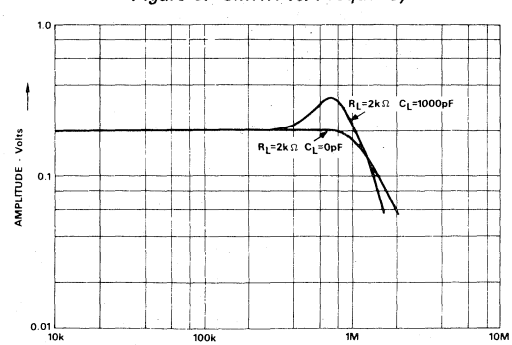


Figure 7. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 7. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 8.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

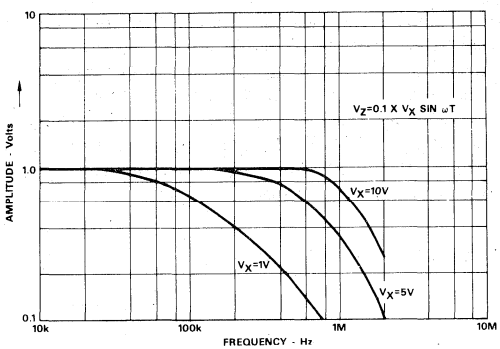


Figure 8. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 9. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

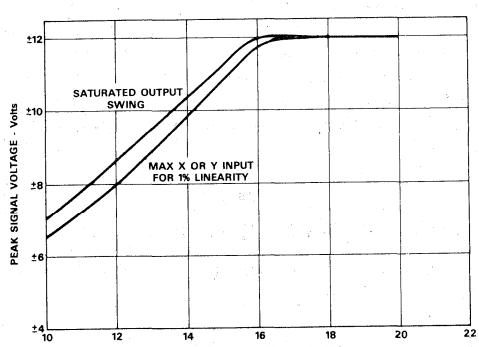


Figure 9. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532's are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 10.

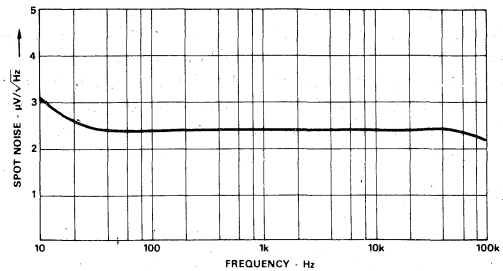


Figure 10. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

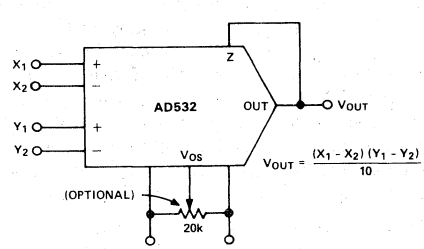


Figure 11. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 11. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

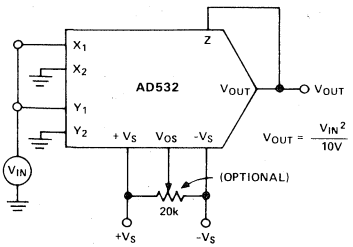


Figure 12. Squarer Connection

The squaring circuit in Figure 12 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

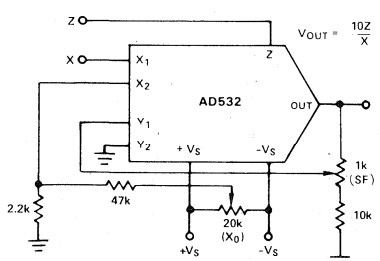


Figure 13. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 13. It should be noted, however, that the output error is given approximately by $10\epsilon_m/(X_1 - X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1 - X_2)/10$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to −10V), connect the input to X_1 and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_O) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $500mV \leq |(X_1 - X_2)| \leq 10V$. The voltage offset adjust (V_{OS}), if used, is trimmed with Z at zero and $(X_1 - X_2)$ at full scale.

SQUARE ROOT

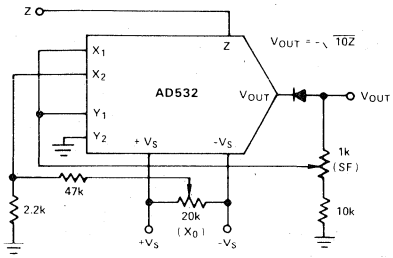


Figure 14. Square Rooter Connection

The connections for square root mode are shown in Figure 14. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{os} to obtain −1.0V dc in the output, $V_{out} = -\sqrt{10Z}$. For optimum performance, gain (S.F.) and offset (X_O) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

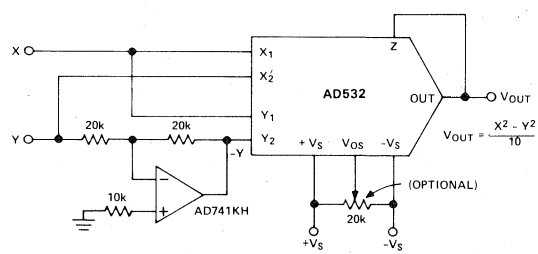


Figure 15. Difference of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2 - Y^2/10$. As shown in Figure 15, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	±10V	±10V	±10V	−10V
X_o (Offset)	−1V	±1V	±10V	±0.1V	−1V

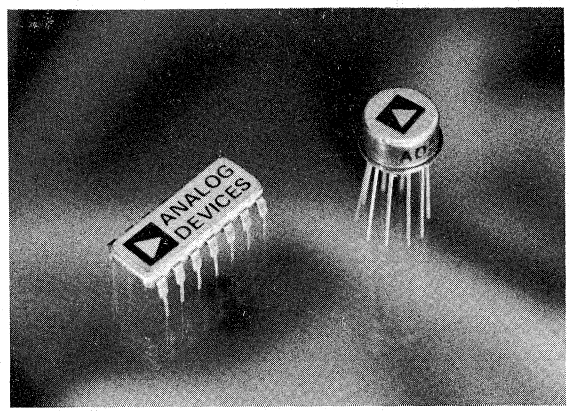
Repeat if required.

ANALOG DEVICES

Low Cost IC Multiplier,Divider,Squarer,Square Rooter

AD533

FEATURES
Low Cost
Simplicity of Operation: Only Four External Adjustments
Max 4-Quadrant Error Below 0.5% (AD533L)
Low Temperature Drift: 0.01%/°C (AD533L)
Multiplies, Divides, Squares, Square Roots



PRODUCT DESCRIPTION

The Analog Devices AD533 is a low cost integrated circuit multiplier comprised of a transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. Specified accuracy is easily achieved by the straight-forward adjustment of feedthrough, output zero, and gain trim pots. The AD533 multiplies in four quadrants with a transfer function of XY/10, divides in two quadrants with a 10Z/X transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10Z}$. Several levels of accuracy are provided: the AD533J, AD533K, and AD533L, for 0 to +70°C operation, are specified for maximum multiplying errors of 2%, 1%, and 0.5% respectively at +25°C. The AD533S, for operation from -55°C to +125°C, is guaranteed for a maximum 1% multiplying error at +25°C. The maximum error specification is a true measure of overall accuracy since it includes the effects of offset voltage, feedthrough, scale factor, and nonlinearity in all four quadrants.

The low drift design of the AD533 insures that high accuracy is maintained with variations in temperature. The op amp output provides ±10 volts at 5mA, and is fully protected against short circuits to ground or either supply voltage: all inputs are fully protected against over-voltage transients with internal series resistors. The devices provide excellent ac performance, with typical small signal bandwidth of 1.0MHz, full power bandwidth of 750kHz, and slew rate of 45V/μs.

The low cost and simplicity of operation of the AD533 make it especially well suited for use in such widespread applications as modulation and demodulation, automatic gain control and phase detection. Other applications include frequency discrimination, rms computation, peak detection, voltage controlled oscillators and filters, function generation, and power measurements.

All models are available in the hermetically-sealed TO-100 metal can and TO-116 ceramic DIP packages.

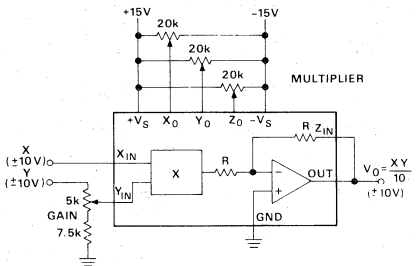
SPECIFICATIONS (typical @ +25°C, externally trimmed and V_S = ±15V dc unless otherwise specified)

PARAMETER	CONDITIONS	AD533J	AD533K	AD533L	AD533S
ABSOLUTE MAX RATINGS					
Internal Power Dissipation		500mW	*	*	*
Input Voltage (Note 1)					
X_{in}, Y_{in}, Z_{in}, X_O, Y_O, Z_O		$\pm V_S$	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	-55°C to +125°C
Storage Temp Range		-65°C to +150°C	*	*	*
Output Short Circuit	To Ground	Indefinite	*	*	*
MULTIPLIER SPECIFICATIONS					
Transfer Function		XY/10	*	*	*
	Untrimmed	XY/6 max [XY/10 min]	*	*	*
Total Error (of full scale)		±2.0% max	±1.0% max	±0.5% max	±1.0% max
	T_A = min to max	±3.0%	±2.0%	±1.0%	±1.5%
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.01%/°C
Nonlinearity					
X Input	$V_X = V_O$ = 20V(p-p)	±0.8%	±0.5%	**	**
Y Input	$V_Y = V_O$ = 20V(p-p)	±0.3%	±0.2%	**	**
Feedthrough					
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	150mV(p-p) max	200mV(p-p) max	50mV(p-p) max	100mV (p-p) max
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	200mV(p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
DIVIDER SPECIFICATIONS					
Transfer Function		10Z/X	*	*	*
	Untrimmed	10Z/X max [6Z/X min]	*	*	*
Total Error (of full scale)	V_X = -10V dc, V_Z = ±10V dc	±1.0%	±0.5%	±0.2%	±0.5%
	V_X = -1V dc, V_Z = ±10V dc	±3.0%	±2.0%	±1.5%	±2.0%
SQUARER SPECIFICATIONS					
Transfer Function		$X^2/10$	*	*	*
	Untrimmed	$X^2/6$ max [$X^2/10$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
SQUARE ROOTER SPECIFICATIONS					
Transfer Function		$-\sqrt{10Z}$	*	*	*
	Untrimmed	$-\sqrt{10Z}$ max [$-\sqrt{6Z}$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
INPUT SPECIFICATIONS					
Input Resistance					
X Input		10MΩ	*	*	*
Y Input		6MΩ	*	*	*
Z Input		36kΩ	*	*	*
Input Bias Current					
X, Y Inputs		3μA	7.5μA max	5μA max	7.5μA max
Z Input		±25μA	*	*	*
X, Y Inputs	T_A = min to max	12μA	10μA	7μA	7μA
Z Input	T_A = min to max	±35μA	*	*	*
Input Voltage	T_A = min to max				
V_X, V_Y, V_Z	For Rated Accuracy	±10V	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μs	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Sm Sig 1% Vector Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μs to 2%	*	*	*
Overload Recovery		2μs to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance		100Ω	*	*	*
Output Voltage Swing	T_A = min to max				
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		Trimmable To Zero	*	*	*
vs. Temperature	T_A = min to max	0.7mV/°C	*	*	*
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	Rated Performance	±15V	*	*	*
	Operating	±15V to ±18V	±10V to ±18V	±10V to ±18V	±10V to ±22V
Supply Current	Quiescent	±6mA max	*	*	*
Power Supply Variation	*Includes* Effects of Recommended Null Pots				
Multiplier Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor		±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

Note 1: Max input voltage is zero when supplies are turned off.
*Specifications same as AD533J
**Specifications same as AD533K
Specifications subject to change without notice.

MULTIPLIER

Multiplier operation is accomplished by closing the loop around the internal op amp with the Z input connected to the output. The X_O null pot balances the X input channel to minimize Y feedthrough and similarly the Y_O pot minimizes the X feedthrough. The Z_O pot nulls the output op amp offset voltage and the gain pot sets the full scale output level.



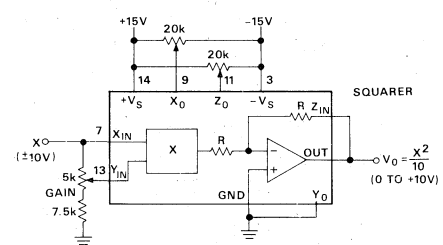
TRIM PROCEDURES

1. With X = Y = 0 volts, adjust Z_O for 0V dc output.
2. With Y = 20 volts p-p (at f = 50Hz) and X = 0V, adjust X_O for minimum ac output.
3. With X = 20 volts p-p (at f = 50Hz) and Y = 0V, adjust Y_O for minimum ac output.
4. Readjust Z_O for 0V dc output.
5. With X = +10V dc and Y = 20 volts p-p (at f = 50Hz), adjust gain for output = Y_{in}.

NOTE: For best accuracy over limited voltage ranges (e.g., ±5V), gain and feedthrough adjustments should be optimized with the inputs in the desired range, as linearity is considerably better over smaller ranges of input.

SQUARER

Squarer operation is a special case of multiplier operation where the X and Y inputs are connected together and two quadrant operation results since the output is always positive. When the X and Y inputs are connected together, a composite offset results which is the algebraic sum of the individual offsets which can be nulled using the X_O pot alone.

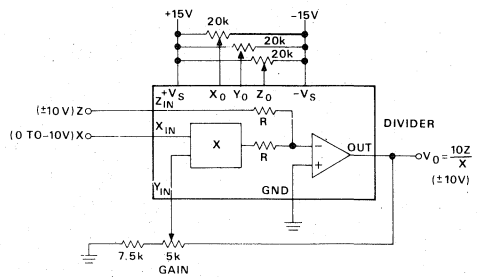


TRIM PROCEDURES

1. With X = 0 volts, adjust Z_O for 0V dc output.
2. With X = +10V dc, adjust gain for +10V dc output.
3. Reverse polarity of X input and adjust X_O to reduce the output error to ½ its original value, readjust the gain to take out the remaining error.
4. Check the output offset with input grounded. If nonzero, repeat the above procedure until no errors remain.

DIVIDER

The divide mode utilizes the multiplier in a fed-back configuration where the Y input now controls the feedback factor. With X = full scale, the gain (V_O/Z) becomes unity after trimming. Reducing the X input reduces the feedback around the op amp by a like amount, thereby increasing the gain. This reciprocal relationship forms the basis of the divide mode. Accuracy and bandwidth decrease as the denominator decreases.

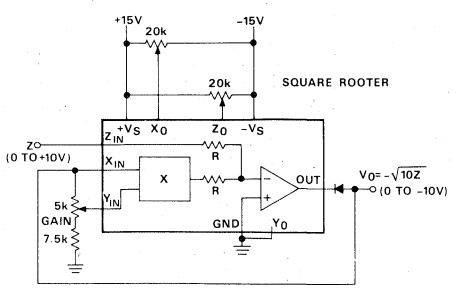


TRIM PROCEDURES

1. Set all pots at mid-scale.
2. With Z = 0V, trim Z_O to hold the output constant, as X is varied from -10V dc through -1V dc.
3. With Z = 0V, X = -10V dc, trim Y_O for 0V dc.
4. With Z = X or -X, trim X_O for the minimum worst-case variations as X is varied from -10V dc to -1V dc.
5. Repeat steps 2 and 3 if step 4 required a large initial adjustment.
6. With Z = X or -X, trim the gain for the closest average approach to ±10V dc output as X is varied from -10V dc to -3V dc.

SQUARE ROOTER

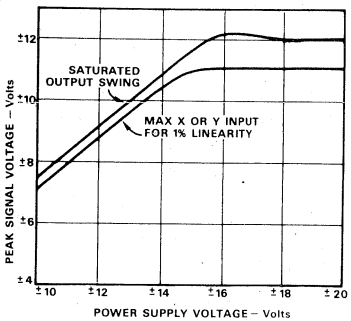
This mode is also a fed-back configuration with both the X and Y inputs tied to the op amp output through an external diode to prevent latchup. Accuracy, noise and frequency response are proportional to $\sqrt{Z}$, which implies a wider usable dynamic range than the divide mode.



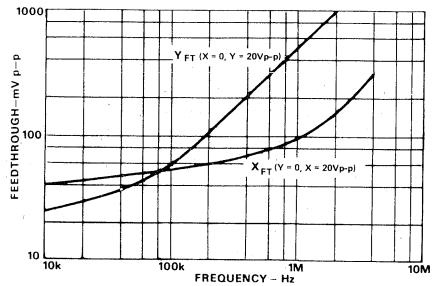
TRIM PROCEDURES

1. With Z = +0.1V dc, adjust Z_O for Output = -1.0V dc.
2. With Z = +10.0V dc, adjust gain for Output = -10.0V dc.
3. With Z = +2.0V dc, adjust X_O for Output = -4.47 ±0.1V dc.
4. Repeat steps 2 and 3, if necessary. Repeat step 1.

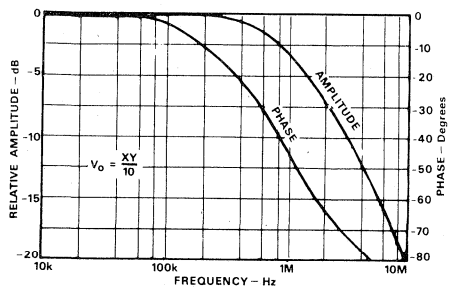
TYPICAL PERFORMANCE CHARACTERISTICS



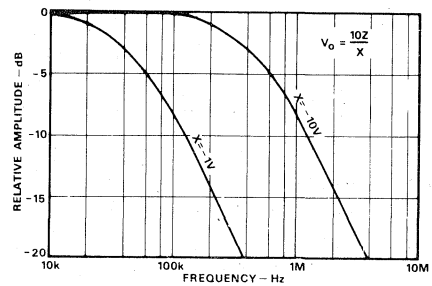
Allowable Signal Swing vs. Supply Voltage



Feedthrough vs. Frequency



Closed Loop Frequency and Phase Response

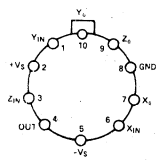


Divide Mode Frequency Response

PIN CONFIGURATION & DIMENSIONS

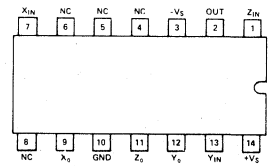
Dimensions shown in inches and (mm).

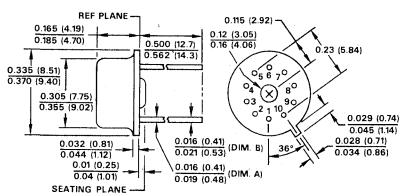
AD533H
TO-100

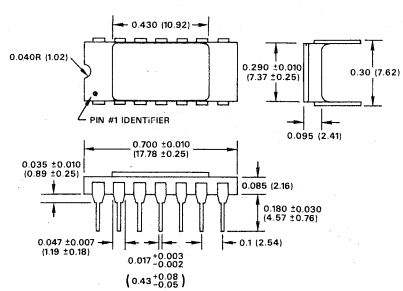


TOP VIEW

AD533D
TO-116







ORDERING GUIDE

MODEL	MULT. ERROR (Max @ +25°C)	TEMP. RANGE	ORDER NUMBER
AD533J	±2.0%	0 to +70°C	AD533JH*
			AD533JD†
AD533K	±1.0%	0 to +70°C	AD533KH
			AD533KD
AD533L	±0.5%	0 to +70°C	AD533LH
			AD533LD
AD533S	±1.0%	-55°C to +125°C	AD533SH
			AD533SD

*TO-100 metal can package
†TO-116 ceramic DIP package

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

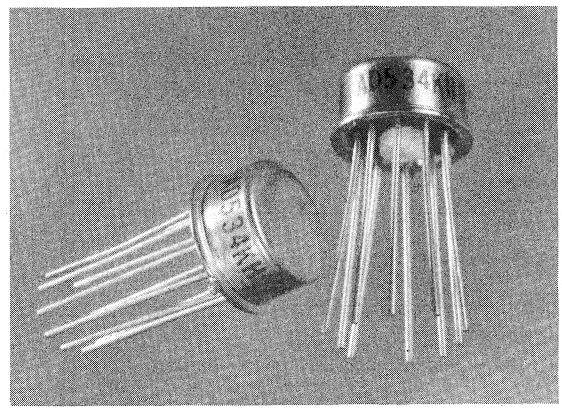
AD534

FEATURES

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters



PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced to values as low as 3, with corresponding reductions in bias current and noise level.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, -55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS (typical at +25°C, with $\pm V_S$ = 15V, $R_L \geq 2k$, unless otherwise stated)

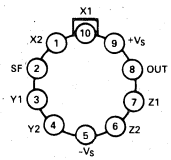
PARAMETER	CONDITIONS	AD534J	AD534K	AD534L	AD534S	AD534T
MULTIPLIER PERFORMANCE						
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	*	*	*	*
Total Error[1]	$-10V \leq X, Y \leq +10V$	±1.0% max	±0.5% max	±0.25% max	*	**
	T_A = min to max					
	V_S = ±14V to ±16V	±1.5%	±1.0%	±0.5%	±2.0% max	±1.0% max
vs. Temperature		±0.022%/°C	±0.015%/°C	±0.008%/°C	±0.02%/°C max	±0.01%/°C max
Scale Factor Error	SF = 10.00 nominal[2]	±0.25%	±0.1%	**	*	**
Temperature-Coefficient of						
Scaling-Voltage	T_A = min to max	±0.02%/°C	±0.01%/°C	±0.005%/°C	*	±0.005%/°C max
Supply Rejection	$\pm V_S$ = (15V) ±1V	±0.01%	*	*	*	*
Nonlinearity, X	X = 20V pk-pk					
	Y = ±10V	+0.4%	±0.2% (0.3% max)	±0.1% (0.12% max)	*	**
Nonlinearity, Y	Y = 20V pk-pk					
	X = ±10V	±0.01%	±0.01% (±0.1% max)	±0.005% (±0.1% max)	*	**
Feedthrough[3], X	Y nulled					
	X = 20V pk-pk 50Hz	±0.3%	±0.15% (0.3% max)	±0.05% (0.12% max)	*	**
Feedthrough[3], Y	X nulled					
	Y = 20V pk-pk 50Hz	±0.01%	±0.01% (±0.1% max)	±0.003% (±0.1% max)	*	**
Output Offset Voltage		±5mV (±30mV max)	±2mV (±15mV max)	±2mV (±10mV max)	*	**
Drift	T_A = min to max	200μV/°C	100μV/°C	**	500μV/°C max	300μV/°C max
DYNAMICS						
Small-Signal BW	V_{OUT} = 0.1V rms	1MHz	*	*	*	*
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz	*	*	*	*
Slew Rate	V_{OUT} 20V pk-pk	20V/μs	*	*	*	*
Settling Time to ±1%	ΔV_{OUT} = 20V	2μs	*	*	*	*
NOISE						
Noise Spectral-Density	SF = 10	$0.8\mu V/\sqrt{Hz}$	*	*	*	*
	SF = 3 (Note 4)	$0.4\mu V/\sqrt{Hz}$	*	*	*	*
Wideband Noise	f = 10Hz to 5MHz	1mV rms	*	*	*	*
	f = 10Hz to 10kHz	90μV rms	*	*	*	*
	f = 10Hz to 10kHz,					
	SF = 3 (Note 4)	60μV rms	*	*	*	*
OUTPUT						
Output Voltage Swing	T_A = min to max	±11V min	*	*	*	*
Output Impedance	Unity-Gain, f ≤ 1kHz	0.1Ω	*	*	*	*
Maximum Output Current	R_L = 0, T_A = min to max	30mA	*	*	*	*
Amplifier Open-Loop Gain	f = 50Hz	70dB	*	*	*	*
INPUT AMPLIFIERS (X, Y and Z)[5]						
Signal Voltage Range	Rated Accuracy					
	(Diff. or CM)	±10V	*	*	*	*
	Operating (Diff.)	±12V	*	*	*	*
Offset Voltage, X, Y		±5mV (±20mV max)	±2mV (±10mV max)	**	*	**
Drift	T_A = min to max	100μV/°C	50μV/°C	**	*	150μV/°C
Offset Voltage, Z		±5mV (±30mV max)	±2mV (±15mV max)	±2mV (±10mV max)	*	**
Drift	T_A = min to max	200μV/°C	100μV/°C	**	500μV/°C max	300μV/°C max
CMRR (X, Y, Z)	50Hz, 20V pk-pk	80dB (60dB min)	90dB (70dB min)	**	*	**
Bias Current	Diff. Input = 0	0.8μA (2μA max)	*	*	*	*
Offset Current	Diff. Input = 0	0.1μA	*	0.05μA (0.2μA max)	*	*
Differential Resistance		10MΩ	*	*	*	*
DIVIDER PERFORMANCE[6]						
Transfer Function	$X_1 > X_2$	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*	*	*	*
Total Error[1]	X = 10V					
	$-10V \leq Z \leq +10V$	±0.75%	±0.35%	±0.2%	*	**
	X = 1V					
	$-1V \leq Z \leq +1V$	±2.0%	±1.0%	±0.8%	*	**
	$0.1V \leq X \leq 10V$					
(Note 7)	$-10V \leq Z \leq +10V$	±2.5%	±1.0%	±0.8%	*	**
SQUARER PERFORMANCE						
Transfer Function		$\frac{(X_1 - X_2)^2}{10} + Z_2$	*	*	*	*
Total Error[1]	$-10V \leq X \leq +10V$	±0.6%	±0.3%	±0.2%	*	**
SQUARE-ROOTER PERFORMANCE[6]						
Transfer Function	$Z_1 \leq Z_2$	$\sqrt{10(Z_2 - Z_1)} + X_2$	*	*	*	*
Total Error[1]	$1V \leq Z \leq 10V$	±1.0%	±0.5%	±0.25%	*	**
POWER SUPPLY SPECIFICATIONS						
Supply Voltage	Rated Performance	±15V	*	*	*	*
	Operating	±8V to ±18V	*	*	±8V to ±22V	±8V to ±22V
Supply Current	Quiescent	4mA (6mA max)	*	*	*	*

NOTES
*Specifications same as AD534J.
**Specifications same as AD534K.
[1] Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).
[2] May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3] Irreducible component due to nonlinearity; excludes effect of offsets.
[4] Using external resistor adjusted to give SF = 3.
[5] See Functional Block Diagram, Figure 1, for definition of sections.
[6] The AD535 is a functional equivalent to the AD534, has guaranteed performance in the divider and square rooter modes and is recommended for such applications.
[7] With external Z-offset adjustment, $Z \leq \pm X$.

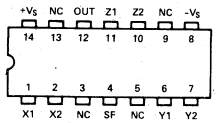
Specifications subject to change without notice.

PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

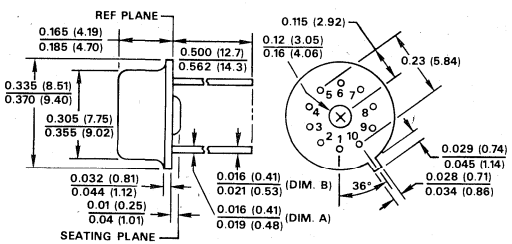


H-PACKAGE
TO-100
(TOP VIEW)

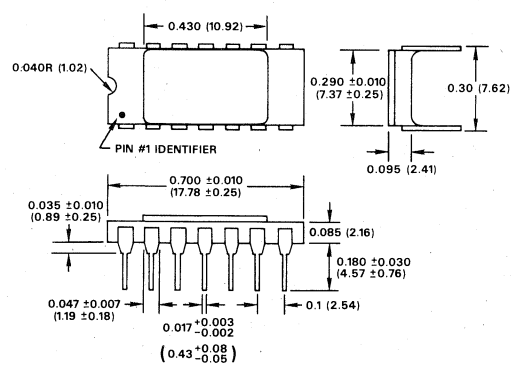


D-PACKAGE
TO-116
(TOP VIEW)

TO-100

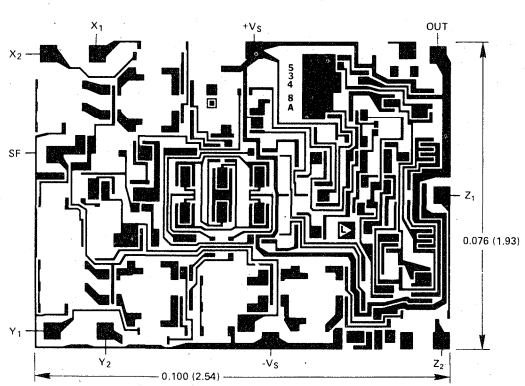


TO-116



CHIP DIMENSIONS & PAD LAYOUT

Dimensions shown in inches and (mm).



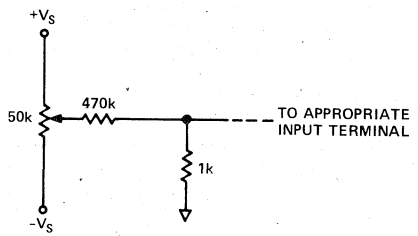
THE AD534 IS AVAILABLE IN LASER-TRIMMED CHIP FORM; CONSULT THE CHIP CATALOG FOR DETAILS.

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10.000V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.025% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

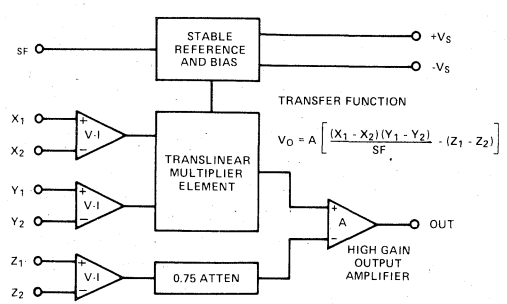


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00 but adjustable by the user down to 3.

In most cases the open loop gain can be regarded as infinite, and SF will be 10. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00 and 3 by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

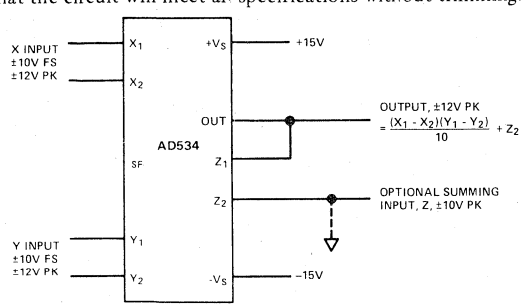


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input (see Optional Trimming Configuration, previous page). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

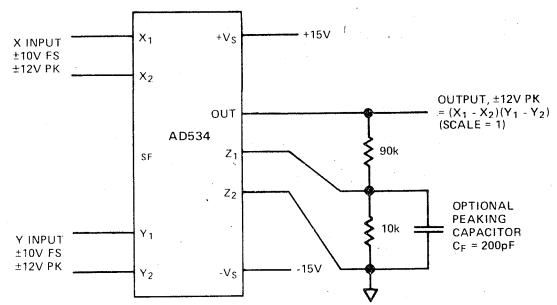


Figure 3. Connections for Scale-Factor of Unity

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

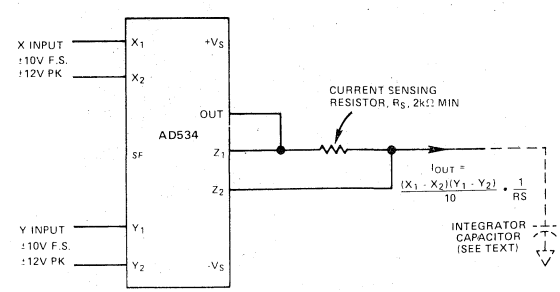


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

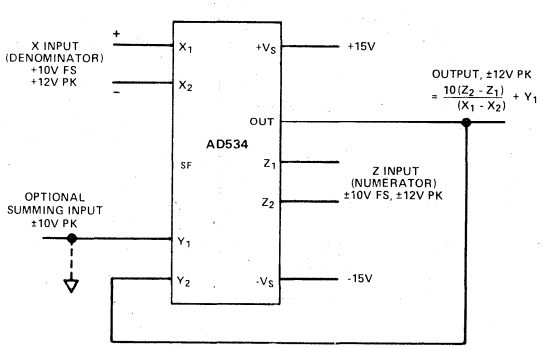


Figure 5. Basic Divider Connection

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input (see Optional Trimming Configuration, page 4-19). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

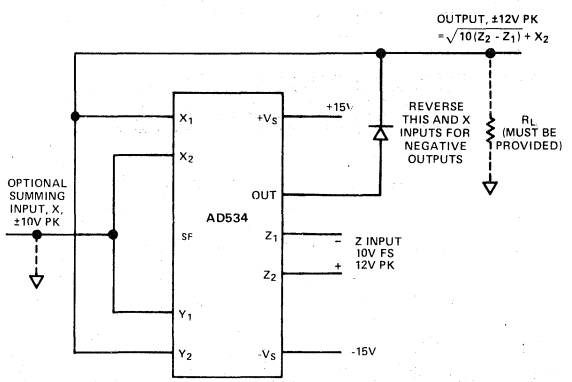


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration, page 4-19) will improve accuracy for inputs below 1V.

*See the AD535 Data Sheet for more details.

Applications Section

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few. These applications along with many other such "idea stimulators" are described in detail in the *Multiplier Application Guide*, available upon request from Analog Devices.

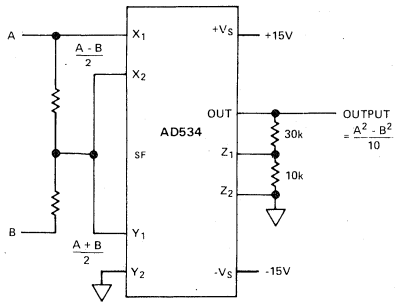
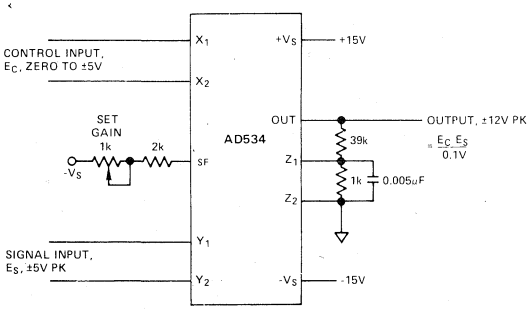
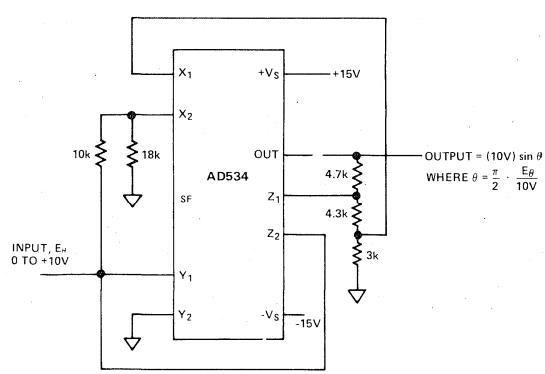


Figure 7. Difference-of-Squares



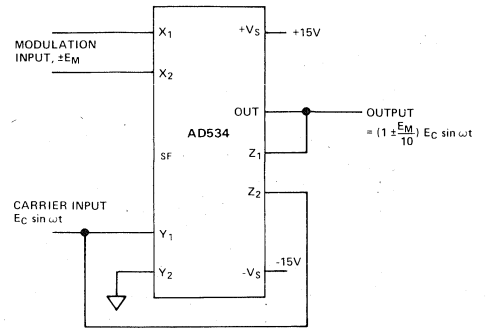
NOTES:
1) GAIN IS X10 PER VOLT OF E_C, ZERO TO X50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F.S. S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60μV RMS, TYP
4) BANDWIDTH IS DC TO 20kHz, -3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



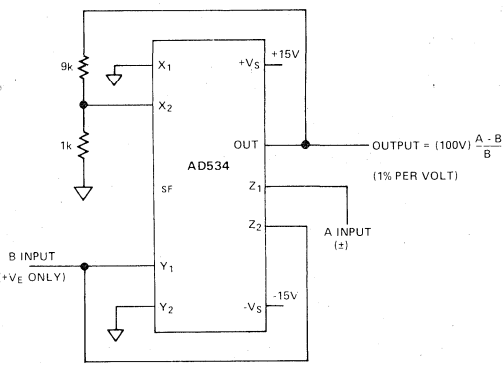
USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator



THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION. OPERATION FROM A SINGLE SUPPLY IS POSSIBLE; BIAS Y_2 TO $V_S/2$.

Figure 10. Linear AM Modulator



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 11. Percentage Computer

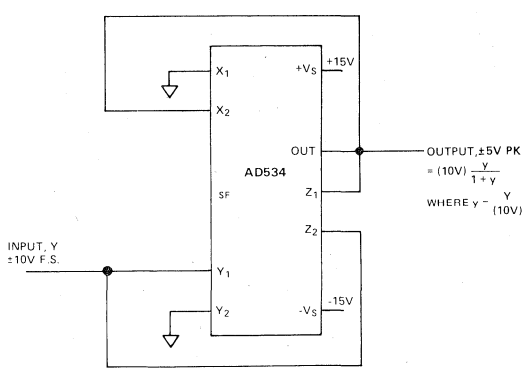
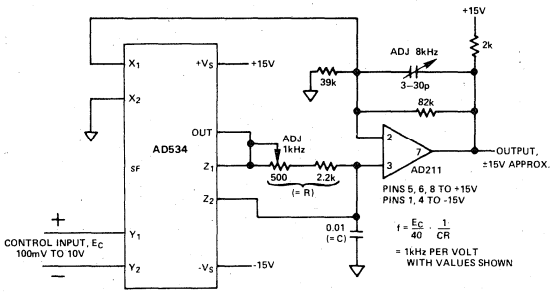


Figure 12. Bridge-Linearization Function



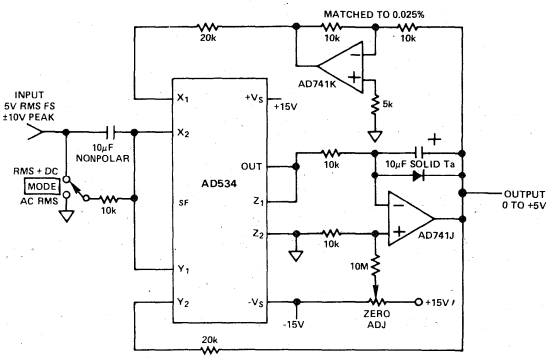
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V, ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ±0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE TO FREQUENCY CONVERTER IS RECOMMENDED.

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01μF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED FROM 60Hz to 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE).

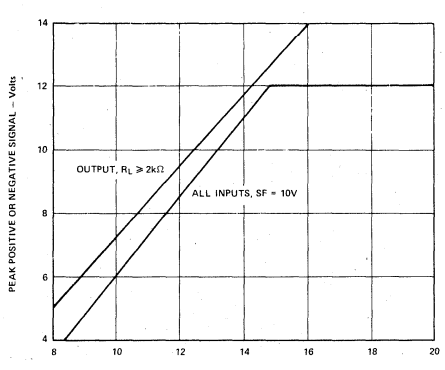
PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

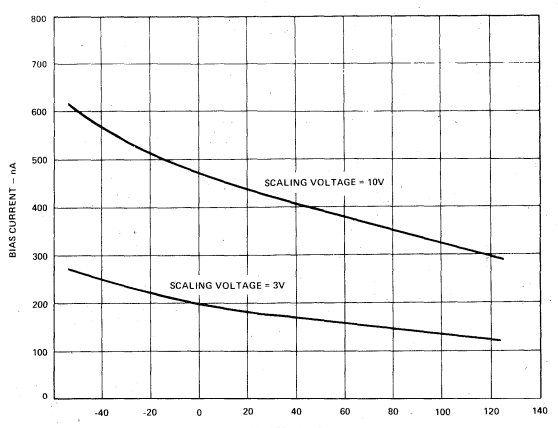
FOR GUARANTEED SPECIFICATIONS THE AD536A IS OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER.

Figure 14. Wideband, High-Crest Factor, RMS-to-DC Converter

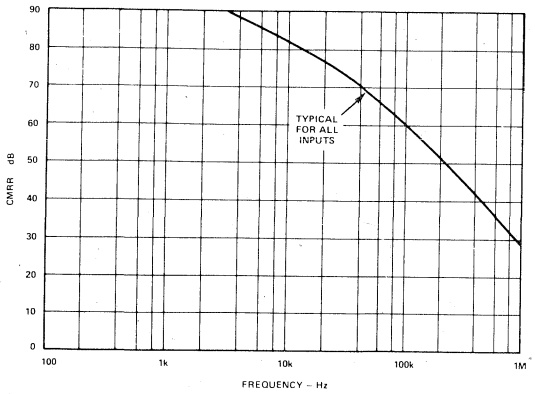
Typical Performance Curves (typical at +25°C, with V_S = ±15V dc, unless otherwise stated)



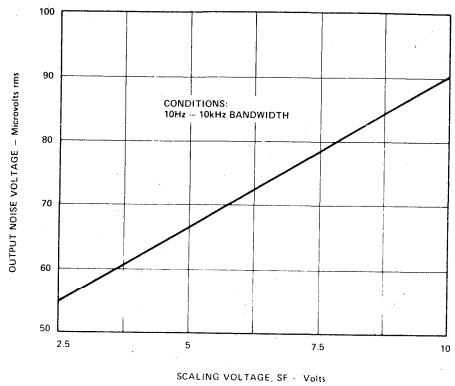
Curve 1. Input/Output Signal Range Vs. Supply Voltages



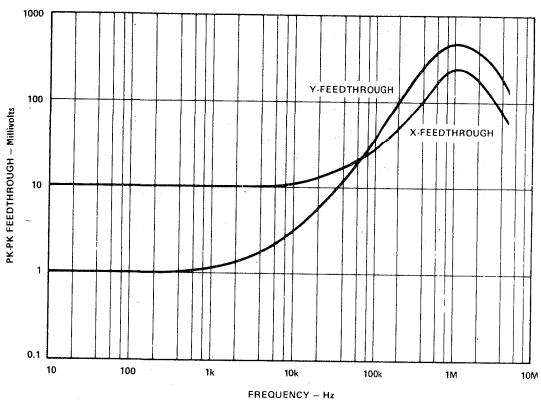
Curve 2. Bias Currents Vs. Temperature (X, Y or Z inputs)



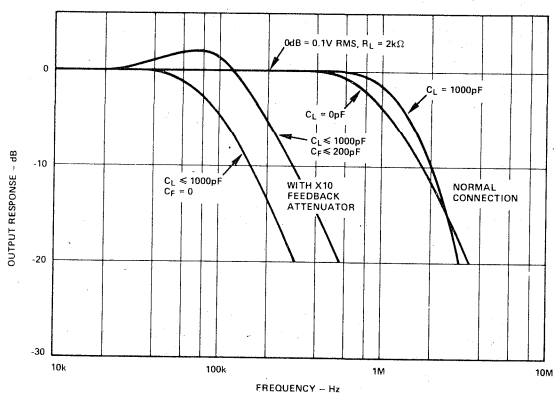
Curve 3. Common-Mode-Rejection-Ratio Vs. Frequency



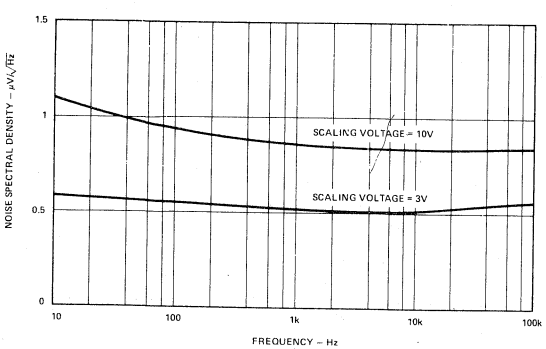
Curve 6. Wideband Noise Vs. Scaling Voltage



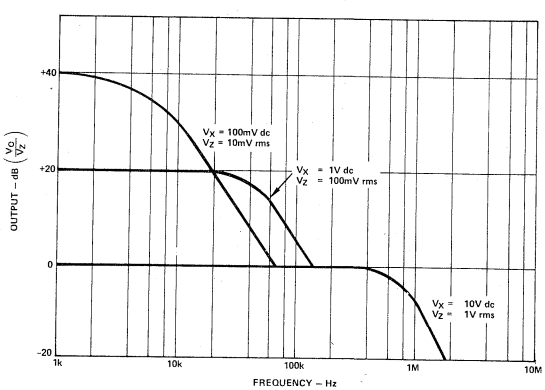
Curve 4. AC Feedthrough Vs. Frequency



Curve 7. Frequency Response as a Multiplier



Curve 5. Noise Spectral Density Vs. Frequency



Curve 8. Frequency Response Vs. Divider Denominator Input Voltage

ANALOG DEVICES

Internally Trimmed Integrated Circuit Divider

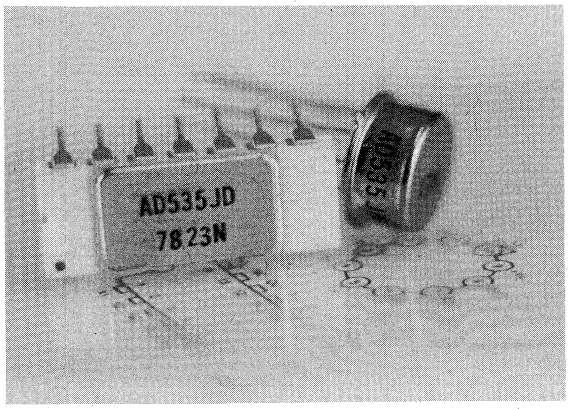
AD535

FEATURES

Pretrimmed to ±0.5% max Error, 10:1 Denominator Range (AD535K)
±2.0% max Error, 50:1 Denominator Range (AD535K)
All Inputs (X, Y and Z) Differential
Low Cost, Monolithic Construction

APPLICATIONS

General Analog Signal Processing
Differential Ratio and Percentage Computations
Precision AGC Loops
Square-Rooting



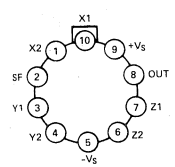
PRODUCT DESCRIPTION

The AD535 is a monolithic laser-trimmed two-quadrant divider having performance specifications previously found only in expensive hybrid or modular products. A maximum divider error of ±0.5% is guaranteed for the AD535K without any external trimming over a denominator range of 10:1; ±2.0% max error over a range of 50:1. A maximum error of ±1% over the 50:1 denominator range is guaranteed with the addition of two external trims. The AD535 is the first divider to offer fully differential, high impedance operation on all inputs, including the z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced by any amount down to 3.

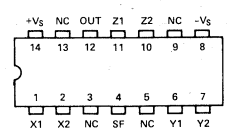
The extraordinary versatility and performance of the AD535 recommend it as the first choice in many divider and computational applications. Typical uses include square-rooting, ratio computation, "pin-cushion" correction and AGC loops. The device is packaged in a hermetically sealed, 10-pin TO-100 can or 14-pin TO-116 DIP and made available in a ±1% max error version (J) and a ±0.5% max error version (K). Both versions are specified for operation over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. Laser trimming at the wafer stage enables the AD535 to provide high accuracies without the addition of external trims (±0.5% max error over a 10:1 denominator range for the AD535K).
2. Improved accuracies over a wider denominator range are possible with only two external trims (±0.5% max error over a 20:1 denominator range for the AD535K).
3. Differential inputs on the X, Y and Z input terminals enhance the AD535's versatility as a generalized analog computational circuit.
4. Monolithic construction permits low cost and, at the same time, increased reliability.



TO-100
(TOP VIEW)



TO-116
(TOP VIEW)

SPECIFICATIONS (V_S = ±15V, $R_L \geq 2k\Omega$, T_A = +25°C unless otherwise stated)

PARAMETER	CONDITIONS	AD535J	AD535K
TRANSFER FUNCTION	Figure 2	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*
TOTAL ERROR[1]	No External Trims, Figure 2		
	1V≤X≤10V, Z≤|X|	1.0% max	0.5% max
	0.2V≤X≤10V, Z≤|X|	5.0% max	2.0% max
	With External Trims, Figure 5		
	0.5V≤X≤10V, Z≤|X|	1.0% max	0.5% max
	0.2V≤X≤10V, Z≤|X|	2.0% max	1.0% max
TEMPERATURE COEFFICIENT	1V≤X≤10V, Z≤|X|	0.01%/°C typ	*
	0.5V≤X≤10V, Z≤|X|	0.02%/°C typ	*
	0.2V≤X≤10V, Z≤|X|	0.05%/°C typ	*
SUPPLY RELATED	1V≤X≤10V	0.1%/V typ	*
Error	0.5V≤X≤10V	0.2%/V typ	*
V_S = ±14V to ±16V	0.2V≤X≤10V	0.5%/V typ	*
SQUARE ROOTER	No External Trims, Figure 11		
TOTAL ERROR[1]	1V≤Z≤10V	0.4% typ	*
	0.2V≤Z≤10V	0.7% typ	*
NOISE[2]	X = 0.2V, f = 10Hz to 10kHz	4.5mV rms typ	*
BANDWIDTH	X = 0.2V	20kHz typ	*
INPUT AMPLIFIERS[3]			
CMRR	f = 50Hz, 20V p-p	60dB min	*
Bias Current		2.0μA max	*
Offset Current		0.1μA typ	*
Differential Resistance		10MΩ typ	*
OUTPUT AMPLIFIER[3]			
Open-Loop Gain	f = 50Hz	70dB typ	*
Small Signal Gain-Bandwidth	V_{OUT} = 0.1V rms	1MHz typ	*
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz typ	*
Output Voltage Swing	T_{min} to T_{max}	±11V min	*
Slew Rate	V_{OUT} = 20V p-p	20V/μs typ	*
Settling Time	V_{OUT} = 20V ±1%	2μs typ	*
Output Impedance	Unity Gain, f≤1kHz	0.1Ω typ	*
Wide-band Noise	f = 10Hz to 5MHz	1mV rms typ	*
	f = 10Hz to 10kHz	90μV rms typ	*
OUTPUT CURRENT	T_{min} to T_{max}, R_1 = 0	30mA max	*
POWER SUPPLIES			
Rated Performance		±15V	*
Operating		±8V min, ±18V max	*
Supply Current	Quiescent	6mA max	*

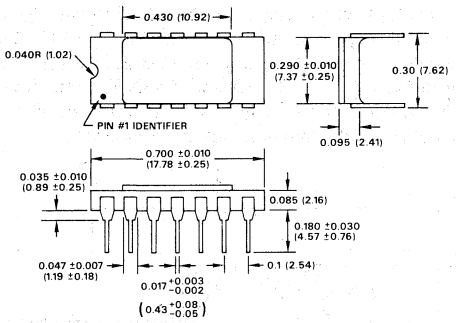
NOTES:
*Specifications same as AD535J.
[1] Figures are given as a percent of full scale (i.e. 1.0% = 100mV).
[2] Noise may be reduced as shown in Figure 14.
[3] See Figure 1 for definition of section.

Specifications subject to change without notice.

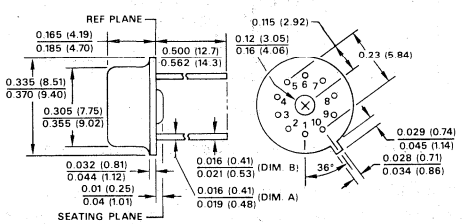
PHYSICAL DIMENSIONS

Dimensions shown in inches and (mm).

TO-116



TO-100



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltages, X_1, X_2, Y_1, Y_2, Z_1, Z_2	$\pm V_S$
Rated Operating Temp Range	0 to +70°C
Storage Temp Range	−65°C to +150°C
Lead Temp, 60s soldering	+300°C

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD535. Inputs are converted to differential currents by three identical voltage to current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique with an internal scaling voltage.

The difference between XY/SF and Z is applied to the high gain output amplifier. The transfer function can then be expressed...

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - V_{OUT})}{SF} - (Z_1 - Z_2)\right]$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite and SF will be 10V. Dividing both sides of the equation by A and solving the V_{OUT}, we get...

$$V_{OUT} = 10V\,\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$$

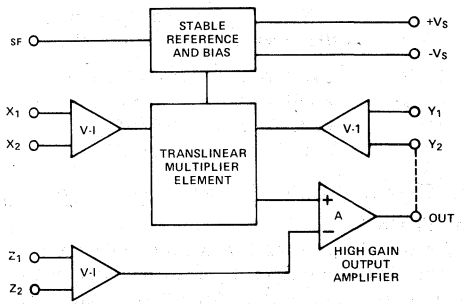


Figure 1. AD535 Functional Block Diagram

SOURCES OF ERROR

Divider error is specified as a percent of full scale (i.e. 10.00V) and consists primarily of the effects of X, Y and Z offsets and scale factor (which are trimmable) as shown in the generalized equation....

$$V_{OUT} = (SF + \Delta SF)\left[\frac{(Z_2 - Z_1) + Z_{OS}}{(X_1 - X_2) + X_{OS}}\right] + Y_1 + Y_{OS}$$

Note especially that divider error is inversely proportional to X, that is, the error increases rapidly with decreasing denominator values. Hence, the AD535 divider error is specified over several denominator ranges on previous page. (See also Figure 12, AD535 Total Error as a function of denominator values.)

Overall accuracy of the AD535 can be significantly improved by nulling out X and Z offset as described in the applications sections. Figure 13 illustrates a factor of 2 improvement in accuracy with the addition of these external trims. The remaining errors stem primarily from scale factor error and Y offsets which can be trimmed out as shown in Figure 6.

Figure 14 illustrates the bandwidth and noise relationships versus denominator voltage. Whereas noise increases with decreasing denominator, bandwidth decreases, the net result given by the expression...

$$En_{OUT}\ (\text{wideband}) = \frac{1.26}{\sqrt{\left(\frac{X}{10}\right)}}\ \text{mV rms}$$

External filtering can be added to limit output voltage noise even further. In this case...

$$En_{OUT}\ (B.W.\ externally\ limited) = \frac{0.9\sqrt{f}}{\left(\frac{X}{10}\right)}\ mV\ rms$$

where f = bandwidth in MHz of an external filter whose bandwidth is less than the noise bandwidth of the AD535. Table 1 provides calculated values of the typical output voltage noise, both filtered and unfiltered for several denominator values.

X	Noise 10Hz to 5MHz	Noise Limited by External Filtering 10Hz to 10kHz
0.2V	8.9mV rms	4.5mV rms
0.5V	5.6mV rms	1.8mV rms
1V	4.0mV rms	0.9mV rms
10V	1.3mV rms	0.09mV rms

Table 1. AD535 Calculated Voltage Noise

APPLICATIONS

Figure 2 shows the standard divider connection without external trims. The denominator X, is restricted to positive values in this configuration. X, Y and Z inputs are differential with high (80dB typical) CMRR permitting the application of differential signals on X and Z (see Figure 3).

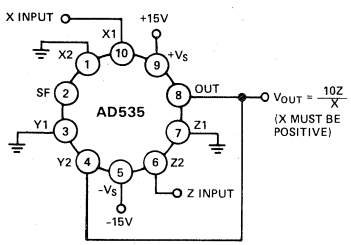


Figure 2. Divider Without External Trims

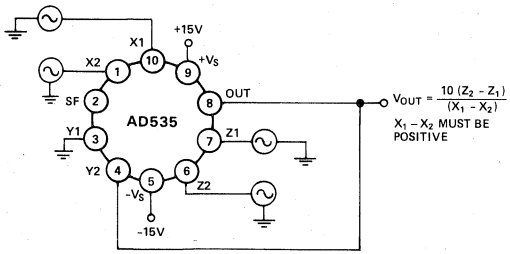


Figure 3. Differential Divider Connection

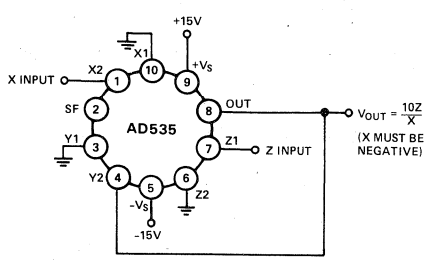


Figure 4. Divider Connection for Negative X Inputs

Negative denominator inputs are handled as shown in Figure 4. Note that in either configuration, operation is limited to two quadrants (i.e. Z is bipolar, X is unipolar).

A factor of two improvements in accuracy is possible by trimming the X and Z offsets as illustrated in Figure 5. To trim, set X to the smallest denominator value for which accurate computation is required (i.e., X = 0.2V). With Z = 0, adjust the Z_O trim for V_{OUT} = 0. Next, adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V). Finally, readjust Z_O for the best compromise at Z = +X, Z = -X and Z = O. The remaining error (Figure 13) consists primarily of scale factor error, output offset and an irreducible nonlinearity component.

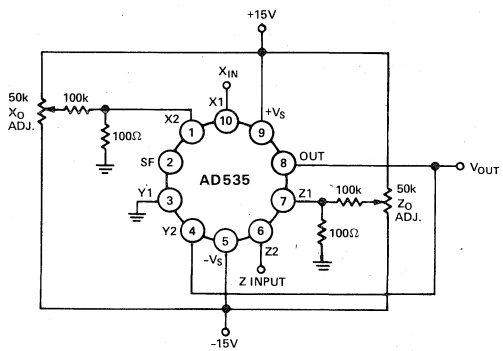


Figure 5. Precision Divider Using Two Trims

In certain applications, the user may elect to adjust SF for values between 10.00 and 3 by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\ \frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} ±25% using the potentiometer. Note that the peak signal is always limited to 1.25 SF (i.e. ±5V for SF = 4).

The scale factor may also be adjusted using a feedback attenuator between V_{OUT} and Y2 as indicated in Figure 6. The input signal range is unaffected using this scheme.

Scale factor and output offset error can be minimized utilizing the four trim circuit of Figure 6. Adjustment is as follows:

1. Apply X = +0.2V (or the smallest required denominator value), Z = 0 and adjust Z_O for V_{OUT} = 0.
2. Apply X = 0.2V. Then adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V.)
3. Apply X = +10V, Z = 0 and adjust Y_O for V_{OUT} = 0.
4. Apply X = +10V. Then adjust the scale factor (SF) trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V).
5. Repeat steps 1 and 2.
6. Apply X = 0.2V. Then adjust the Z trim for the best compromise when Z = X (V_{OUT} = +10V), Z = 0 (V_{OUT} = 0) and Z = -X (V_{OUT} = -10V).

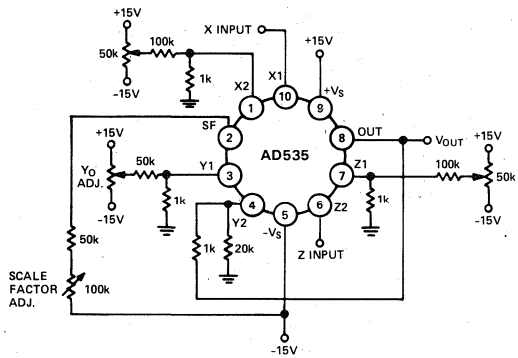


Figure 6. Precision Divider with Four External Adjustments

These trim adjustments can be made either by using two calibrated voltage sources and a DVM, or by using a differential scope, a low frequency generator, a voltage source and a precision attenuator. As shown in Figure 7, the differential scope subtracts the expected ideal output and thus displays only errors. Set the attenuation to $\frac{X}{10}$.

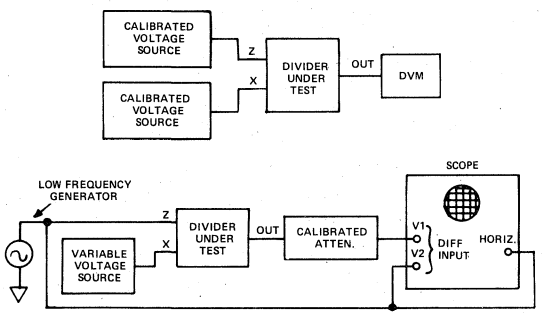


Figure 7. Alternate Trim Adjustment Set-Up

PIN-CUSHION CORRECTION

A pin-cushion corrector eliminates the distortion caused by flat screen CRT tubes. The correction equations are:

$$V_{OH} = \frac{V_{IH}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

and

$$V_{OV} = \frac{V_{IV}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

where: V_{OH} and V_{OV} are the horizontal and vertical output signals, respectively.

V_{IH} and V_{IV} are the horizontal and vertical input signals, respectively.

L is the length of the CRT tube.

In typical applications L (expressed in voltage) is roughly equal to full scale V_{IH} or V_{IV}. The result is that the expression, $\sqrt{(V_{IH}^2 + V_{IV}^2 + L^2)}$, varies less than 2:1 over the full range of values of V_{IH} and V_{IV}.

Major sources of divider error associated with small denominator values can thereby the minimized.

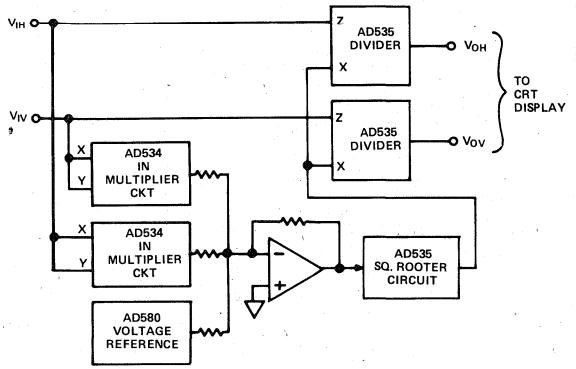


Figure 8. Pin-Cushion Corrector

Figure 9 shows an AGC loop using an AD535 divider. The AD535 lends itself naturally in this application since it is configured to provide gain rather than loss. Overall gain varies from 1 to ∞ as the denominator is servoed to maintain V_{OUT} at a constant level.

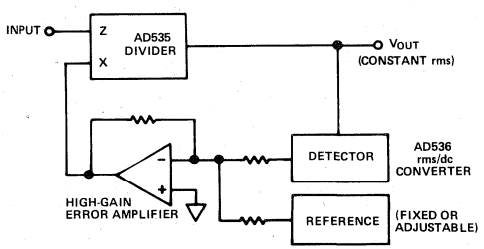


Figure 9. AGC Loop Using the AD536 rms/dc Converter as a Detector

Figure 10 shows a method for obtaining the time average as defined by:

$$\bar{X} = \frac{1}{T}\int_0^T X\,dt$$

where T is the time interval over which the average is to be taken. Conventional techniques typically provide only a crude approximation to the true time average, and furthermore, require a fixed time interval before the average can be taken. In Figure 10, the AD535 is used to divide the integrator output by the ramp generator output. Since the ramp is proportional to time, the integrator is divided by the time interval, thus allowing continuous, true time processing of signals over intervals varying by as much as 50:1.

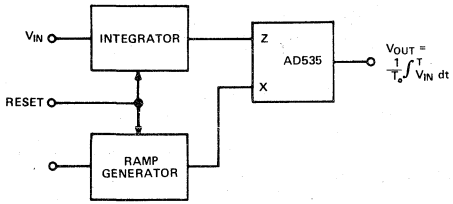


Figure 10. Time Average Computation Circuit

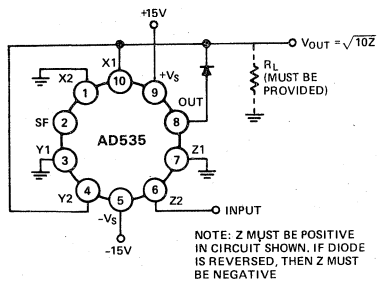


Figure 11. Square Rooter

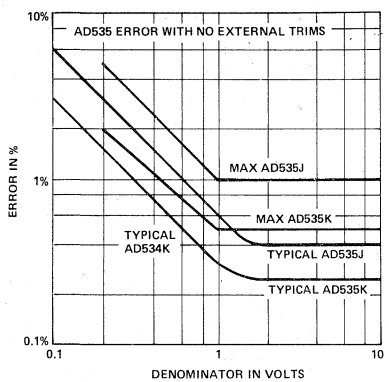


Figure 12. AD535 Error with No External Trims

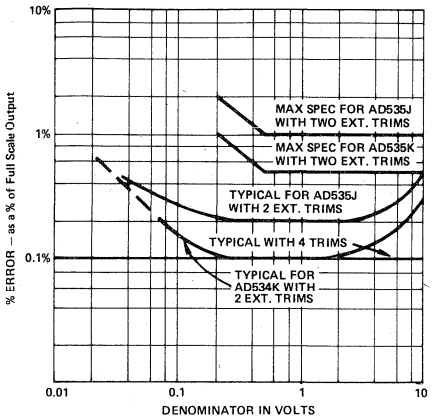


Figure 13. Errors with External Trims at 25°C

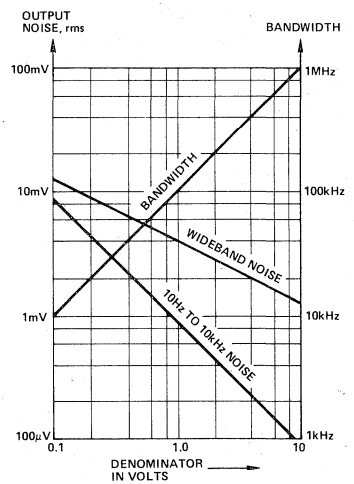


Figure 14. -3dB Bandwidth and Noise vs. Denominator

ANALOG DEVICES

Accurate, Wideband, Multiplier, Divider, Square Rooter

MODEL 429

FEATURES:
1.0%/0.5% Accuracy without Trimming (429A/B)
Low Drift to 1.0mV/°C max
Wideband – 10MHz
0.2% Nonlinearity max (429B)
External Amplifiers not Required
MTBF: 775,194 Hours @ +25°C

APPLICATIONS:
Fast Divider
Modulation and Demodulation
Phase Detection
Instrumentation Calculations
Analog Computer Functions
Adaptive Process Control
Trigonometric Computations

GENERAL DESCRIPTION

The model 429, an extremely fast multiplier/divider, should be considered if bandwidth, temperature coefficient, or accuracy are critical parameters. Based on the transconductance principle to achieve high speed, the model 429 offers a unique combination of features, those being ½% max error (429B) and 10MHz small signal bandwidth.

Both models 429A and 429B are internally trimmed achieving max errors of 1.0% and 0.5% respectively. By fine trimming the offset and feedthrough with external trim potentiometers typical performance may be improved to 0.5% for the 429A and 0.2% for the 429B.

In addition to high accuracy and high bandwidth, the model 429 offers exceptionally good stability for changes in ambient temperature. Model 429B is 100% temperature tested in order to guarantee an overall accuracy temperature coefficient of only 0.04%/°C max. Additionally, offset drift is held to only 1mV/°C max. To satisfy OEM requirements of low cost, the 429 uses transconductance principles with the latest design techniques and components to achieve guaranteed performance at competitive prices.

MULTIPLICATION ACCURACY

Multiplication accuracy is generally specified as a percentage of full scale output. This implies that error is independent of signal level. However, for signal levels less than 2/3 of full scale, error tends to decrease roughly in proportion to the input signal. A good approximation of error behavior is:

$f(X, Y) \cong |X| \epsilon_x + |Y| \epsilon_y$, where ϵ_x and ϵ_y are the fractional nonlinearities specified for the X and Y inputs

EXAMPLE: For Model 429A, $\epsilon_x = 0.5\%$, $\epsilon_y = 0.3\%$. What maximum error can one expect for x = 5V, y = 1V, providing the offset is zeroed out? Can one get less by interchanging inputs?

1. Nominal output is XY/10 = (5)(1)/10 = 500mV
2. Expected error is (5) (0.5%) + (1) (0.3%) = 28mV, 5.6% of output (0.28% of F.S.)
3. Interchanging inputs (1) (0.5%) + (5) (0.3%) = 20mV, 4.0% of output (0.20% of F.S.)

Compare this with the overly conservative error predicted by the overall 1% of full scale specification: 100mV, or 20% of output.

FREQUENCY RELATED SPECIFICATIONS

Accuracy, and its components, feedthrough, linearity, gain, (and phase shift) are frequency dependent. Feedthrough is constant up to 100kHz for the Y input, and up to 400kHz for the X input. Beyond these frequencies it rises at approximately a 6dB/octave rate due to distributed capacitive coupling. A plot of typical feedthrough vs. frequency is shown in Figure 1. For this measurement one input is driven with a 20V p-p sine wave while the other input is grounded and the feedthrough is measured at the output. This error will decrease roughly in proportion to the input signal, and will also vary with temperature (about 0.01%/°C of the nonzero input). Low frequency feedthrough error can be further reduced from the internally trimmed limits by the use of optional external potentiometers.

Nonlinearity likewise increases with frequency at a 6dB/octave rate above the break frequency. With the Y input driven

(continued on page 4-33)

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	429A	429B
MULTIPLICATION CHARACTERISTICS		
Output Function	XY/10	*
Error, with Internal Trim, at +25°C	±1% max	±0.5% max
Error, with External Trim, at +25°C	±0.7%	±0.3%
Avg vs. Temp (-25°C to +85°C)	±0.05%/°C	±0.04%/°C max
Avg vs. Supply	±0.05%/%	*
SCALE FACTOR		
Initial Error at +25°C	0.5%	0.25%
Avg vs. Temp (-25°C to +85°C)	0.03%/°C	0.02%/°C
Avg vs. Supply	0.03%/%	*
OUTPUT OFFSET		
Initial at +25°C (Adjustable to Zero)	±20mV max	±10mV max
Avg vs. Temp (-25°C to +85°C)	±2mV/°C	±1mV/°C max
Avg vs. Supply	±1mV/%	*
NONLINEARITY		
X Input (X = 20V p-p 50Hz, Y = ±10V)	0.5% max	0.2% max
Y Input (Y = 20V p-p 50Hz, X = ±10V)	0.3% max	0.2% max
FEEDTHROUGH		
X = 0, Y = 20V p-p, 50Hz	50mV p-p, max	20mV p-p, max
With External Trim	16mV p-p	10mV p-p
Y = 0, X = 20V p-p, 50Hz	100mV p-p, max	30mV p-p, max
With External Trim	50mV p-p	20mV p-p
BANDWIDTH		
-3dB	10MHz	*
Full Power Response	2MHz min	*
Slew Rate	120V/μs min	*
1% Amplitude Error	300kHz min	*
1% Vector Error (0.57°)	50kHz min	*
Differential Phase Shift ($\theta_X - \theta_Y$)	1° @ 1MHz	*
Small Signal Rise Time 10-90%	40ns	*
Settling to ±1% (±10V step)	500ns	*
Overload Recovery	0.2μs	*
OUTPUT NOISE		
5Hz to 10kHz	0.6mV rms	*
5Hz to 10MHz	3.0mV rms	*
OUTPUT CHARACTERISTICS		
Voltage, 1kΩ load	±11V min	*
Current	±11mA min	*
Load Capacitance	0.01μF max	*
INPUT RESISTANCE		
X Input	10kΩ±5%	*
Y Input	11kΩ±2%	*
Z Input	27kΩ±10%	*
INPUT BIAS CURRENT		
Input X, Y, Z	±100nA	*
Z	±20μA	*
MAXIMUM INPUT VOLTAGE		
For Rated Accuracy	±10.5V	*
Maximum Safe	±16V	*
WARM UP		
To Rated Specifications	1 second	*
POWER SUPPLY[1]		
Rated Performance	±(14.8 to 15.3)V dc	*
Operating	±(14 to 16)V dc	*
Quiescent Current	±12mA	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Weight	2 oz.	*
Socket	AC1023	*
Case Dimensions	1.5" x 1.5" x 0.62"	*

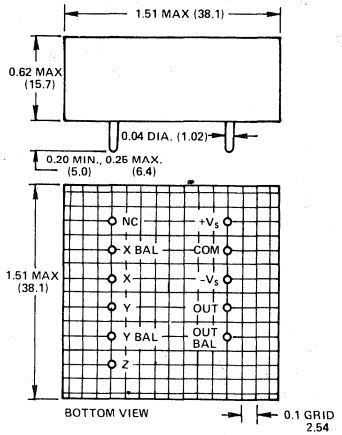
*Specifications same as Model 429A

[1] Recommended power supply Model 904 available from Analog Devices.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

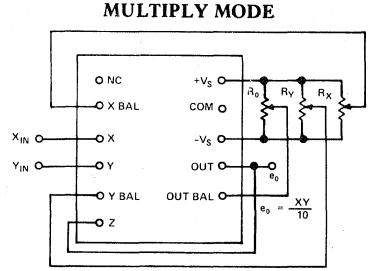
Dimensions shown in inches and (mm).



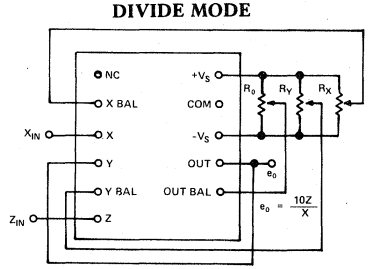
PIN CONNECTIONS

Bottom View Shown in all Cases.
Optional Trim Pots Shown are not Required for Rated Accuracy.

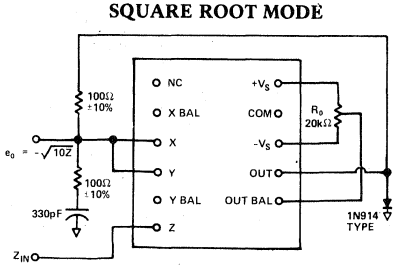
MULTIPLY MODE



DIVIDE MODE



SQUARE ROOT MODE



All trim pots 20kΩ; PN79PR20k

(continued from page 4-31)

at 10V p-p, and the X input anywhere between ±10V dc, the break frequency is 25kHz. For corresponding X input conditions, the break occurs at 60kHz. Figure 2 is a plot of the typical nonlinearity vs. frequency for the model 429.

Gain and input to output phase shift for the model 429 are shown in Figure 2. Naturally, no multiplier will maintain accuracy at frequencies approaching the small signal bandwidth. For the model 429, the 1% amplitude error will occur at 500kHz. If input to output phase shift is a criterion, then the 1% "vector" error occurs at 50kHz.

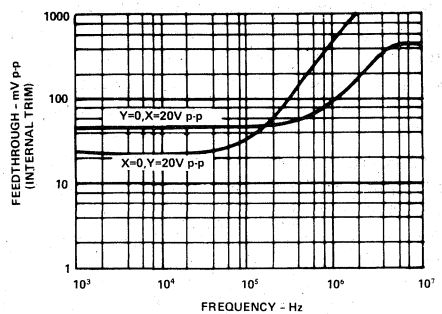


Figure 1. Feedthrough vs Frequency

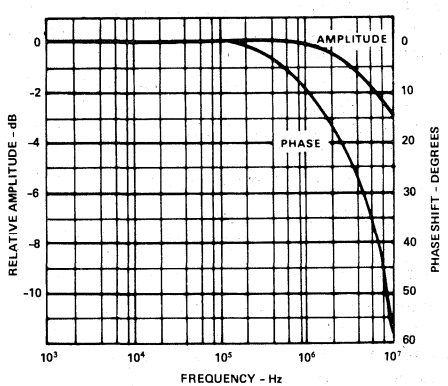


Figure 2. Typical Amplitude and Phase vs Frequency

OPTIONAL TRIM – MULTIPLY MODE

As shipped, the multiplier meets its listed specifications without use of any external trim potentiometers. Terminals are provided for optional feedthrough and offset adjustments. Using these adjustments overall static multiplication error may be reduced to only 0.2%. The 20kΩ trim potentiometers should be connected across the ± supply voltage terminals with the arm of each potentiometer connected to the desired balance terminal (see previous page).

ADJUSTMENT PROCEDURE FOR OFFSET

1. Jumper X input and Y input to ground.
2. Adjust R_0 for an output of zero volts.
3. Remove jumper from X and Y inputs.

ADJUSTMENT PROCEDURE FOR FEEDTHROUGH

1. Jumper Y input to ground and apply 20 VPP at 1kHz to X input.
2. Adjust R_Y for minimum output voltage.
3. Remove jumper from Y input.
4. Jumper X input to ground and apply 20 VPP at 1kHz to Y input.
5. Adjust R_X for minimum output voltage.
6. Remove jumper from X terminal.

DIVISION

The high bandwidth and excellent linearity of model 429 allows it to be used in divider applications achieving high performance in the dc to 8MHz region. Restrictions imposed on divide operation, and the contribution of error terms are illustrated in the error analysis below.

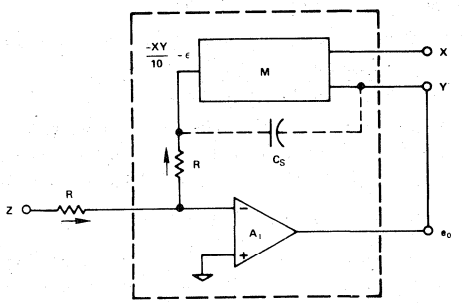


Figure 3. Divider Circuit

Shown in Figure 3 is a typical multiplier/divider which has been connected for divide operation by inserting the multiplier cell, M, in the op amp's feedback loop. Errors associated with the op amp, A_1, are incorporated in ϵ, which represents all errors. In order to insure negative feedback, the X input range is restricted to negative values.

Summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{\frac{XY}{10} + \epsilon}{R}$$

Solving for Y, which is also ϵ_0:

$$Y = \frac{10\,(Z - \epsilon)}{X}$$

or,

$$\epsilon_0 = \frac{10Z}{X} - \frac{10\epsilon}{X}$$

And now breaking ϵ into its constituents

$$\epsilon_0 = \underbrace{\frac{10Z}{X}}_{\text{ideal divider}} - \underbrace{\frac{10E_{NV}}{X}}_{\text{noise error}} - \underbrace{\frac{10E_{OS}}{X}}_{\text{offset error}} - \underbrace{\frac{10E_{OS}/^{\circ}C}{X}}_{\text{offset drift error}} - \underbrace{\frac{10E_{NLX}}{X}}_{\text{X non-linearity error}} - \underbrace{\frac{10E_{NLY}}{X}}_{\text{Y non-linearity error}}$$

These errors can be broken down into two categories, static errors and signal dependent errors. All of the static errors associated with the divide mode are inversely proportional to the denominator signal level. The signal dependent errors are the X and Y nonlinearities. For model 429B nonlinearity errors are 0.2% for both the X and Y inputs. Substituting these values in the error terms yields:

$$-\frac{10\,(0.2\%)\,X}{X} - \frac{10\,(0.2\%)\,Y}{X}$$

The importance of using the terminal with largest nonlinearity for the denominator is revealed by the above expression. Effects of X nonlinearity are virtually independent of signal level and may be trimmed out. Nonlinearities of Y typically contribute 200mV for X = Z = 1V i.e., (10 [0.2%] 10V) = 200mV. This error can be reduced if external trims are used to optimize divider performance.

Bandwidth is also degraded with a decrease in denominator level, due to the increase in system gain;

i.e.) for X = Z = 1V, ϵ_0 = 10V

and $\frac{\epsilon_0}{Z} = \frac{10}{1} = 10$

Since the gain bandwidth product is constant, a bandwidth of 1/10 of that obtained for full scale denominator levels will be obtained for division at 1V levels.

For other denominator levels, bandwidth is determined by:

$$\text{B. W.} = \frac{\text{Denominator Level}}{\text{Full Scale Denominator}} \times (\text{Multiplier B.W.}) \times K$$

where K is a constant having a value less than unity. It is introduced due to a combination of stray capacitance paralleling the multiplier cell and effects of feedthrough. For model 429

$$\text{B.W.} = \left(\frac{X}{10}\right) 8\text{MHz}$$

Before selecting a multiplier/divider for divide applications, errors resulting from the lowest anticipated denominator signal should be considered. After such considerations have been made, one can further appreciate the importance of starting with an accurate, high speed multiplier such as model 429. It is also highly recommended that the optional trim procedure for division be performed.

OPTIONAL TRIMMING – DIVIDE MODE

Connections are made as shown previously.

The suggested trim procedure is (starting with centered adjust adjustments):

*1. With Z = 0, trim R_0 to hold output constant, as X is varied from -10V toward -1.0V.
2. With Z = 0, trim R_Y for zero at X = -10V.
3. With Z = X and/or Z = -X, trim R_X for minimum worst-case variation as X is varied from -10V to -1.0V.
4. Repeat 1 and 2 if step 3 required large initial adjustment.

*For best accuracy X should be allowed to vary from -10V to lowest expected denominator.

SQUARE ROOTING

When connected as shown previously, the model 429 will provide the square root of Z_{IN}.

By summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{XY}{10R} + \frac{\epsilon}{R} = \frac{Y^2}{10R} + \frac{\epsilon}{R}$$

where ϵ represents all errors associated with the multiplier. Solving for the output voltage, Y.

$$\epsilon_0 = \pm \sqrt{10\,(Z - \epsilon)}$$

There are two values of ϵ_0 for every value of Z. However, only negative values of ϵ_0 will provide the negative feedback necessary for circuit stability. To restrict the output from going positive, a diode is connected as shown previously. The output is then:

$$\epsilon_0 = -\sqrt{10\,(Z - \epsilon)}$$

Errors, ϵ, associated with the multiplier, are inside the square root and consequently their effect, for large values of Z, is reduced. The reason for the improved performance can be seen by inspecting the circuit. The output is fed back to both the X and Z terminals, resulting in twice the feedback as would be obtained for the divide mode. An alternative method of considering error performance is to consider errors as being at the Z terminal. By differentiating the ideal transfer function with respect to Z, errors for various values of Z may be determined:

$$\frac{de_0}{dZ} = \frac{d}{dZ}\sqrt{10Z} = \tfrac{1}{2}\sqrt{\frac{10}{Z}}$$

The factor of ½ has the advantage of reducing errors by a factor of 2 for Z = 10, but also introduces the potential problem of instability. Since the feedback gain is the reciprocal of the forward gain, the slope of the forward gain is 2. Additional phase margin is required to support the increased gain in the feedback path. Model 429 is optimized for phase margin in the multiply and divide modes producing minimum vector errors at high frequencies. To avoid the potential problem of instability, the RC network shown previously is recommended. This network restricts the bandwidth and guarantees stability for all positive values of Z.

OPTIONAL ADJUSTMENT PROCEDURE – SQUARE ROOT

1. Apply a voltage to the Z terminal equal to the lowest anticipated input voltage.
2. Adjust R_0 such that $e_0 = -\sqrt{10Z}$, where Z is the voltage applied in step 1.

DIVISION SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	10(Z)/X
Numerator Range	±10V
Denominator Range, 1% Accuracy	-1 to -10V
Denominator Range, 5% Accuracy	-0.2V to -10V
Bandwidth Formula, (Hz, -3dB)	(8MHz)(X)/10

SQUARE ROOTING SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	$-\sqrt{10(Z)}$
Dynamic Range	1000 to 1 (+0.010V ≤Z≤+10V)
Accuracy (% of Full Scale)	0.5%
Bandwidth Formula, (Hz, -3dB)	(5MHz) $\sqrt{\lvert X\rvert/10}$

Table 1. Division & Square Rooting Specifications

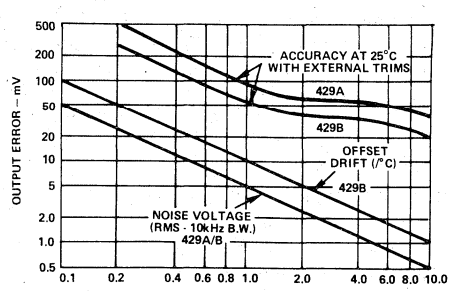


Figure 3. Typical Error Performance of Model 429 in Divide Mode for Worst Case of $|e_0| = 10V$

ANALOG DEVICES

Programmable Multifunction Module

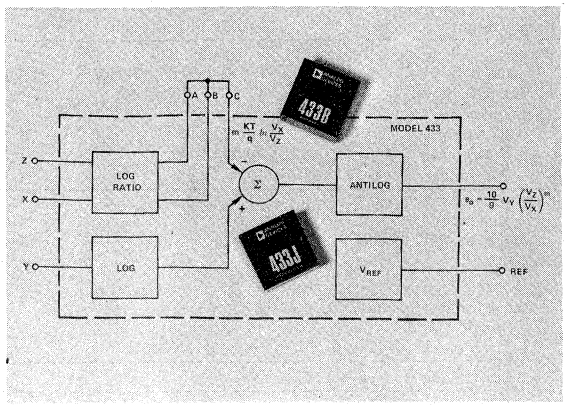
MODEL 433

FEATURES

Versatility: Provides Transfer Characteristics of Several Function Modules
Divides Over a 100:1 Range With a Max Error of 0.25% (433B)
Internal Voltage Reference
Hermetically Sealed Semiconductors
No External Trims Required
Low Noise

APPLICATIONS

Transducer Linearization
Signal Processing
Raising to Arbitrary Powers
Vector Functions
Trigonometric Functions (Sine, Cosine, Arctangent)



GENERAL DESCRIPTION

The model 433 is an extremely versatile function module which implements the transfer function:

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \quad 0.2 \leqslant m \leqslant 5.0$$

V_{REF} = +9.0 Volts

By either jumper connections on the pins, or selection of two external resistors the user can program the 433 to: multiply, divide, square, square root, root of a ratio, square of a ratio, or raise voltage ratios to an arbitrary power, *m*.

When used with a low cost op amp, such as AD741, the model 433 may be used to compute the true rms value of a varying signal. With two such op amps, the 433 can be used to perform accurate vector computations over wide ranges of the vector sum.

Due to its log/antilog circuit approach, signal levels of 100mV to 10V may be processed with a maximum output error of 0.25% F.S. (433B). The allowable input range for the three input variables is 0.01 to +10V, for which there is a typical error of ±5mV ±0.3% of the theoretical output voltage for model 433J, and ±1mV ±0.15% for 433B.

Because of its small size, accuracy, versatility, and speed (and all at low cost), the model 433 will prove to be an essential component in equipment requring on-the-spot computations in real time, or for linearizing a wide range of transducer characteristics in medical, industrial, and process control equipment. Designed with the OEM's needs in mind, the model 433 is attractively priced for new equipment designs.

PRINCIPLE OF OPERATION

The model 433 is comprised of log and antilog circuits interconnected as shown in Figure 1. The log ratio circuit provides

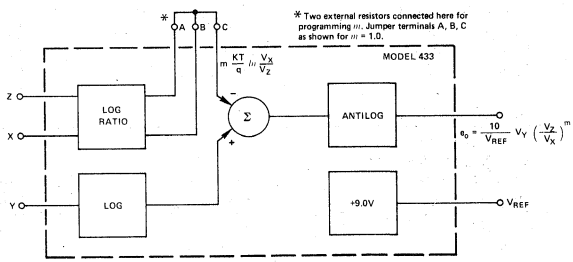


Figure 1. Functional Block Diagram

the log of V_x/V_z to terminals A, B, C where, for exponents other than unity, it is scaled by two external programming resistors (see hook-up diagrams for connection and values of these two resistors). The scaled log ratio from terminal C is subtracted from a signal proportional to the log of V_y. The resulting expression is operated on by the antilog circuit, yielding an output of

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \quad V_{REF} = +9.0 \text{ Volts}$$

The voltage reference circuit is a high stability (0.005%/°C) voltage source which is generated internally. It is provided as an output terminal for user convenience, and may be used as a constant at any of the input terminals.

ONE-QUADRANT DIVIDER

When connected as a divider, the model 433B has less than ¼% output error over an input signal range of 100:1. This performance is obtained with no external trims, and is nearly twenty times better than that attainable with a 0.1% multiplier/divider connected in a feedback loop.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Model	433J	433B
Transfer Function	$e_o = +\frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m$	*
Reference Terminal Voltage[1]		
V_{ref} (Internal Source)	+9.0V ±5% @ 1mA	*
vs Temp (−25°C to +85°C)	±0.005%/°C	*
Rated Output[1]	+10.5V @ 5mA, min	*
Input		
Signal Range	$0 \leqslant V_x, V_y, V_z \leqslant +10V$,	*
Max Safe Input	$V_x, V_y, V_z \leqslant \pm 18V$	*
Resistance		
X Terminal	100kΩ ±1%	*
Y Terminal	90kΩ ±10%	*
Z Terminal	100kΩ ±1%	*
External Adjustment of the Exponent, m		
Range for m <1 (Root)	$1/5 \leqslant m < 1$, $m = \frac{R_2}{R_1 + R_2}$	*
Range for m > 1 (Power)	$1 \leqslant m < 5$, $m = \frac{R_1 + R_2}{R_2}$	*
	$(R_1 + R_2) \leqslant 200\Omega$	*
Accuracy (Divide Mode, m = 1, $V_y = V_{REF}$)[2,3]		
Total Output Error @ +25°C (for specified input range)		
Typical (RTO)	±5mV ±0.3% of output	±1mV ±0.15% of output
Max Error (RTO)	±50mV	±25mV
Input Range ($V_z \leqslant V_x$)	0.01V to 10V, V_z	*
	0.1V to 10V, V_x	*
Over Specified Temp. Range	±1%	±1% max
Output Offset Voltage (Not Adjustable)		
Initial @ +25°C	±5mV	±2mV max
Offset vs Temp.	±1mV/°C	±1mV/°C max
Noise, 10Hz to 1kHz		
V_x = +10V	100μV rms	*
V_x = +0.1V	500μV rms	*
Bandwidth, V_y, V_z Small Signal (-3dB), 10% of dc Level	V_y or V_z	*
$V_y = V_z = V_x$ = 10V	100kHz	*
$V_y = V_z = V_x$ = 1V	20kHz	*
$V_y = V_z = V_x$ = 0.1V	1kHz	*
$V_y = V_z = V_x$ = 0.01V	400Hz	*
Full Output (V_y or V_z = 5V dc ±5V ac)	(V_x) x (5kHz)	*
Power Supply Range		
Rated Performance	±15V dc @ 10mA	*
Operating	±(12 to 18)V dc	*
Temperature Range		
Rated Performance	0 to +70°C	−25°C to +85°C
Storage	−55°C to +125°C	−55°C to +125°C
Mechanical		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1038	*

*Same specifications as 433J.

[1] Terminals short circuit protected to ground.

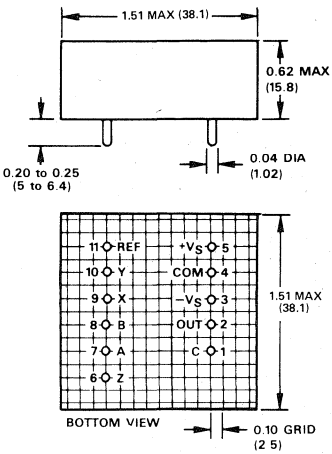
[2] Accuracy is specified in divide mode. Input range is 10mV to 10V for specified accuracy when connected as a multiplier.

[3] Error is defined as the difference between the measured output and the theoretical output for any given pair of specified input voltages.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

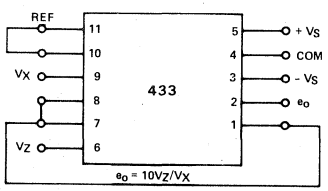


Mating Socket AC1038

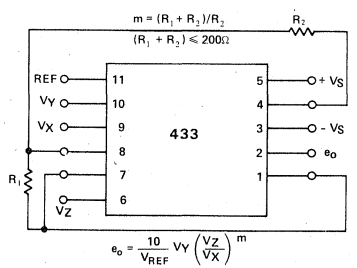
WIRING CONNECTIONS

Bottom View Shown in All Cases

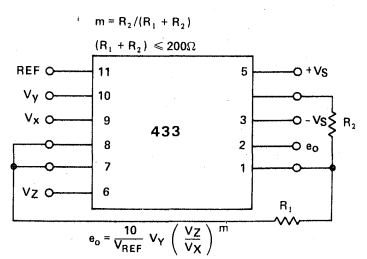
DIVIDE MODE (m = 1, $V_y = V_{REF}$)



POWERS m ⩾ 1



ROOTS m ⩽ 1



MODEL 433B – 0.25% DIVIDER, WIDE DYNAMIC RANGE

Probably the most impressive performance improvement owing to model 433's log/antilog circuit approach, is its ability to hold high divider accuracies over a wide 100:1 input signal range.

When using a conventional multiplier/divider as a divider, accuracy, offset drift, and noise performance are all degraded as the denominator is decreased.

For model 433, accuracy, offset drift, and noise performance are all virtually independent of denominator level as illustrated in Figure 2 and this performance is obtained with no external trims.

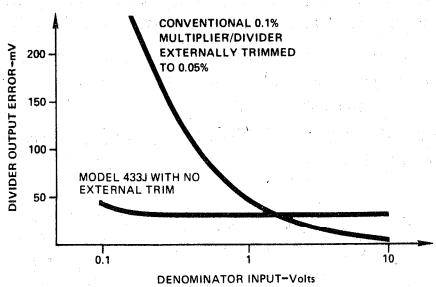


Figure 2. Comparison of Divider Error vs. Denominator Level for Model 433J and a Conventional Mult./Div.

FREQUENCY RESPONSE

A curve of amplitude vs. bandwidth for model 433 is shown in Figure 3. For all input terminals, the small signal frequency response (-3dB point) is signal level dependent, decreasing from 100kHz for a 10V input to 400Hz for a 10mV input. These small signal measurements are made by superimposing a 10% small signal amplitude on the dc level being characterized.

Full output for a ±5 volt signal superimposed on a 5V dc level is 50kHz for the multiplier, and V_X x 5kHz for the divider.

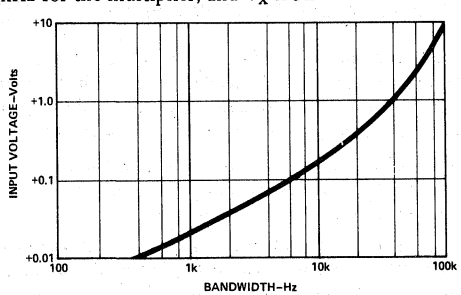


Figure 3. 433 Small Signal Bandwidth vs. Input Voltage

VARYING THE EXPONENT, m

Presented in Figure 4 is a family of curves which illustrates the effect of varying the exponent, m. All curves have been scaled for the full scale output of 10V by reducing the 433's transfer equation to $e_O = 10\ (V_Z/V_X)^m$. For applications where a continuous variation in m is desired, connections should be made as shown in Figure 5C. Model 433 features very small accuracy changes (≈0.1%) as m is adjusted over the entire range from 0.2 to 5.

Various values of m are programmed by two external resistors, R_1 and R_2. For values of $m < 1$ resistor connections are made

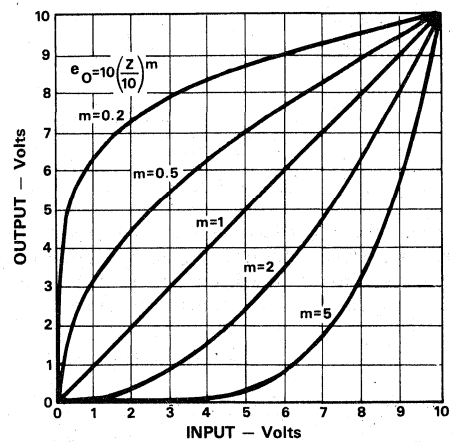


Figure 4. Varying the Exponent, m

to terminals, 1, 7, 8 as shown in Figure 5A. For values of $m > 1$, see Figure 5B. For $m = 1$, connect terminals 1, 7 and 8 together.

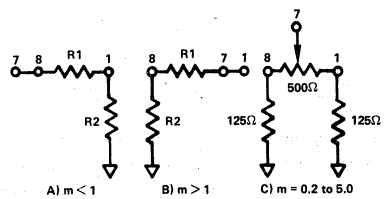


Figure 5. Resistor Programming for the Exponent, m

NOISE PERFORMANCE

The curves shown in Figure 6 are for output noise vs. signal level in a 1kHz BW for worst case conditions. These conditions exist when V_X is equal to V_Z and is varied over the specified range. It should be noted that for 0.1V inputs the effective gain is 100. To retain the full performance capability of model 433, all external noise sources should be isolated from the input terminals.

An exceptional advantage of the 433 over other means of dividing is revealed by these curves. That feature being that noise is virtually independent of signal level. For a 100:1 signal level change of the denominator, the output noise is changed only 3:1. Division by using a multiplier in the feedback loop exhibits a 100:1 increase in output noise for a denominator signal level change of 100:1.

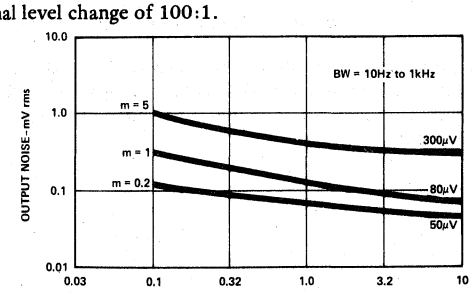


Figure 6. Model 433 Noise vs. Denominator for Various Exponents, m

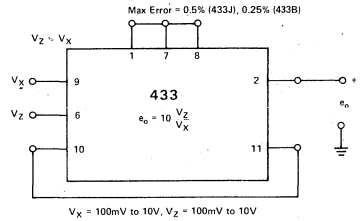


Figure 7. Divider

When connected as a divider as shown above, the 433 has less than ½% error (50mV) for input signals from 100mV to 10V. Output noise, offset drift and accuracy are all virtually independent of signal level and no trims are required.

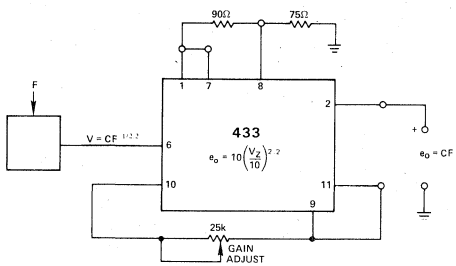


Figure 8. Transducer Linearization

A transducer's output may be linearized by utilizing the 433 as an exponentiator. In the example above, a transducer is used to convert a force, F, to a voltage, V. The desired relationship being V directly proportional to F; i.e., V = CF where C is constant.

The actual output for this example is proportional to F, but is a nonlinear relation which can be approximated by $CF^{1/2.2}$. Connecting the 433 as shown with m = 2.2 provides the desired relation of $e_O = CF$.

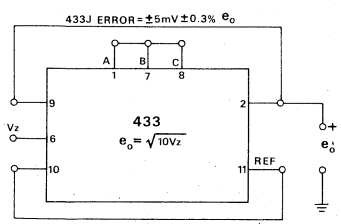


Figure 9. Square Root

The square root of a single variable may be obtained with no external components when connected as shown above. Noise performance is even better than that for the multiply or divide mode.

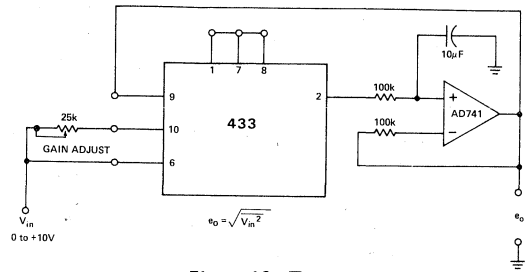
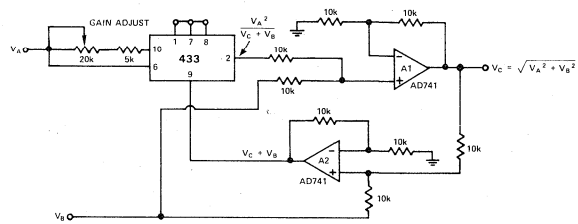


Figure 10. True rms

By combining the 433 with a simple filter, using an external op amp as shown above, the true rms value of a one quadrant input signal may be computed. Accuracy is not degraded by crest factor, provided the maximum input is 10V or less.

The 433 output is applied to an integrator to average the signal and is then fed back to the X input to obtain the square root of the mean square of the input.

Accuracy of 5mV + 0.1% of reading may be achieved over an input range of 500:1.



$V_C = \sqrt{V_A^2 + V_B^2}$

$V_C^2 = V_A^2 + V_B^2$

$V_A^2 = V_C^2 - V_B^2$

$V_A^2 = (V_C - V_B)(V_C + V_B)$

$\frac{V_A^2}{V_C + V_B} = (V_C - V_B)$

$V_C = \frac{V_A^2}{V_C + V_B} + V_B$

Figure 11. Vector Computation $V_C = \sqrt{V_A^2 + V_B^2}$

The vector computation circuit shown in Figure 11 illustrates the extreme versatility of model 433. Used with two inexpensive op amps the 433 is used as a basic building block, which in this case, provides the square root of the sum of the squares.

This application is based on the identity for the difference of squares. The derivation is shown by the equations above and the final equation for V_C is implemented.

Due to the excellent inherent accuracy of the above circuit (error = 0.1% of reading), matched resistors with a low T.C. should be used. Errors of only 0.1% of the theoretical output may be achieved over signal levels of +100mV to +10V.

The usefulness of model 433 extends beyond the illustrative examples shown above. Model 433 may also be used to generate basic trigonometric functions (sine, cosine, arctangent). Further detailed applications information on model 433 is provided in the Nonlinear Circuits Handbook, published by Analog Devices.

ANALOG DEVICES

High Accuracy, Two Quadrant Analog Divider

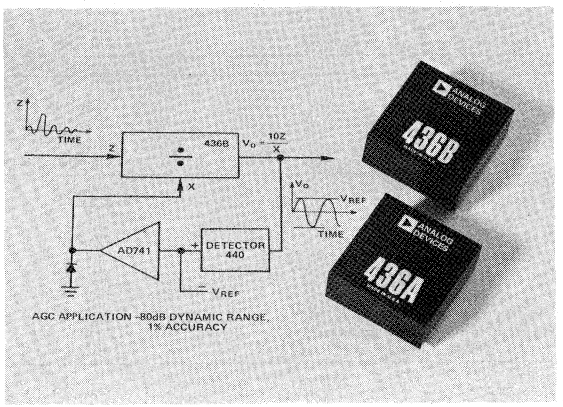
MODEL 436

FEATURES

- Two Quadrant: Numerator Range: ±10V
- High Accuracy: 0.5% max (436A), 0.25% max (436B) over 100:1 Dynamic Range
- No Trimming Required to Achieve Rated Accuracy
- 1000:1 Denominator Range: With External Trim
- Low Nonlinearity: 0.05% (436B)
- Low Harmonic Distortion: -66dB (436B)
- All Hermetically-Sealed Semiconductors
- Wide Operating Temperature Range, -25°C to +85°C

APPLICATIONS

- Linear Gain Control (80dB Range)
- Transducer Linearization
- Instrumentation Calculation
- Adaptive Process Control



GENERAL DESCRIPTION

Model 436 is a precision, two-quadrant variable transconductance analog divider featuring guaranteed accuracy of ±0.5% (model 436A) and ±0.25% (model 436B) over a 100:1 denominator signal range (100mV to 10V) with no external adjustments. With the use of optional external trimming, accuracy may be improved to ±0.05% (436B) over a 1000:1 denominator signal range (10mV to 10V). In addition to this excellent accuracy, model 436 offers a small signal bandwidth (-3dB) of 300kHz and typical numerator nonlinearity of less than ±0.05% (5Hz to 30kHz).

Through the use of hermetically-sealed semiconductors, the model 436 affords exceptional reliability over a wide operating temperature range (-25°C to +85°C). This compact (1.5″ x 1.5″ x 0.6″) epoxy module provides further reliability by protecting the output against damage due to short circuits to ground. The model 436 is pin compatible with most modular multipliers. This allows the model 436 to replace inverted multiplier type dividers in existing sockets to give improved accuracy and increased dynamic range.

TWO QUADRANT OPERATION

Dividers are generally available as single and two-quadrant devices. Dividers that are formed by closing the loop around a four-quadrant transconductance multiplier are capable of operating in two quadrants. Unfortunately, because of the feedback around the multiplier, these dividers suffer from errors which increase directly as the denominator decreases. Even using 0.1% multipliers, these errors become large as the denominator becomes small and high performance is possible only over a limited range of input levels. This denominator dependency of divider errors can be greatly reduced by application of log-antilog techniques, as in the model 434 that has a 0.25% accuracy for denominators within 0.1 to 10V. However, while dividers that use log-antilog circuits are inherently more accurate than inverted multiplier devices, they are limited to single-quadrant operation by the nature of the log function.

The model 436 employs a unique log-antilog circuit to provide two-quadrant operation with high accuracy over a very wide range of denominators.

THEORY OF OPERATION

Model 436 is comprised of summing networks, log circuits and a transconductance differential amplifier as shown in Figure 1.

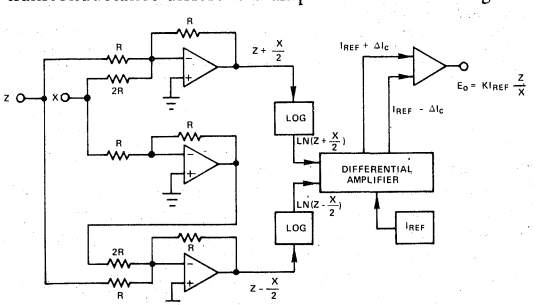


Figure 1. Functional Block Diagram

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL		436A	436B
TRANSFER FUNCTION	$\|V_Z\| \leq V_X; V_X > 0$	$e_O = 10V_Z/V_X$	*
ACCURACY[1]			
Total Output Error, @ +25°C	$\|V_Z\| \leq 10V$		
No External Trim	$+0.1 \leq V_X \leq +10V$	±0.5%, max	±0.25%, max
External Trim	$+0.1 \leq V_X \leq +10V$	±0.3%, max	±0.1%, max
Over Temperature	$+0.1 \leq V_X \leq +10V$		
No External Trim	0 to +70°C	±2.0%, max	±1.0%, max
No External Trim	-25°C to +85°C	±4.0%, max	±2.0%, max
Vs. Supply Voltage		±0.02%/%	*
Warm Up Time to Rated Performance		5 Minutes	*
NONLINEARITY	$\|V_Z\|/V_X, +0.1 \leq V_X \leq +10V$	±0.15% max (0.1% typ)	±0.1% max (0.05% typ)
RATED OUTPUT[2]			
Voltage		±10V, min	*
Current		±5mA, min	*
Resistance		0.1Ω	*
Capacitance Load		0 to 1000pF, min	*
INPUT SPECIFICATIONS			
Voltage, Numerator Signal (V_Z)	$\|V_Z\| \leq V_X$	±10V	*
Voltage, Denominator (V_X)	$V_X > 0$	+10V	*
Safe Input Voltage, V_Z and V_X		$\pm V_S$, max	*
Offset Voltage, @ +25°C, V_Z and V_X		±100μV	*
vs. Temperature	-25°C to +85°C, V_Z, V_X	±20μV/°C	*
vs. Supply Voltage, V_Z and V_X		±30μV/%	*
External Trim Adjustment Range, V_Z		±4.5mV	*
External Trim Adjustment Range, V_X		±1.5mV	*
Voltage Noise, 10Hz to 10kHz, V_X and V_Z		15μV, rms	*
INPUT IMPEDANCE			
Numerator, V_Z		9kΩ, ±2%	*
Denominator, V_X		25kΩ, ±1%	*
OUTPUT SPECIFICATIONS[3]			
Offset Voltage, @ +25°C, V_X = +10V		±10mV	*
vs. Temperature -25°C to +85°C, V_X = +10V		±500μV/°C	*
vs. Supply Voltage		±50μV/%	*
External Trim Adjustment Range		±20mV	*
Voltage Noise, 10Hz to 10kHz V_X = +10V		200μV, rms	*
10Hz to 300kHz, V_X = +10V		750μV, rms	*
FREQUENCY RESPONSE			
Small Signal, -3dB,	$+0.1 \leq V_X \leq +10V$	300kHz	*
Full Power	$+0.1 \leq V_X \leq +10V$	30kHz	*
Slew Rate	$+0.1 \leq V_X \leq +10V$	2V/μs	*
Settling Time, to ±0.5%, ±10 Volt Step, V_X = +10V		10μs	*
Settling Time, to ±0.5%, ±10 Volt Step, V_X = +0.1V		10μs	*
Overload Recovery, $+0.1 \leq V_X \leq +10V$		5μs	*
POWER SUPPLY[4]			
Voltage, Rated Performance		±15V dc	*
Voltage, Operating		±(12 to 18)V dc	*
Current, Quiescent		±9mA	*
TEMPERATURE RANGE			
Rated Performance		-25°C to +85°C	*
Storage		-55°C to +125°C	*
MECHANICAL			
Case Size		1.5" x 1.5" x 0.62"	*
Mating Socket		AC-1041	*
Weight, grams		36	*

*Specifications same as model 436A.

[1] Error is specified as a percentage of full scale output where full scale output is 10 volts.

[2] Output is protected for short circuits to ground, indefinite.

[3] Output offset is specified with no external trimming; optional 50kΩ potentiometer may be connected to zero the output offset voltage.

[4] Recommended power supply; model 904, ±15V @ 50mA output.

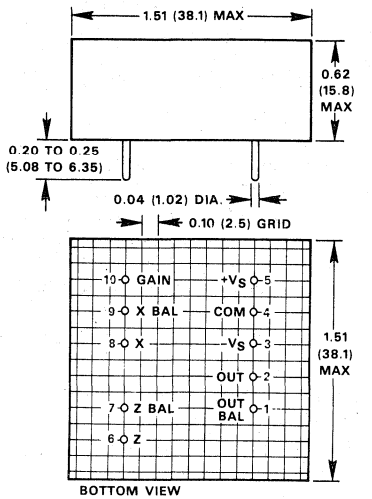
Specifications subject to change without notice.

NONLINEAR CIRCUITS HANDBOOK

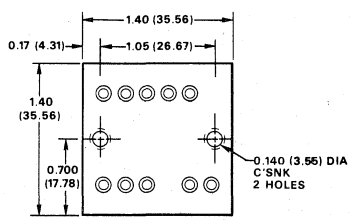
The Nonlinear Circuits Handbook, available from Analog Devices, is an invaluable source of information on principles, circuitry, performance specifications, testing and application of the class of devices designed for use in nonlinear applications. This text provides you with all the fundamentals and guidelines necessary for the proper selection and use of function modules.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC-1041



WIRING CONNECTIONS

Bottom View Shown in all Cases

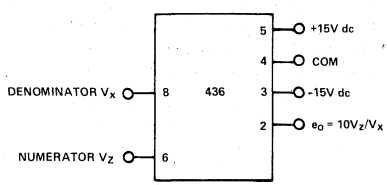


Figure 2. Divide Mode Connections

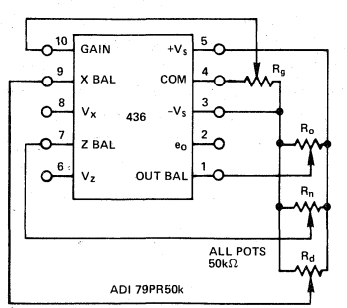


Figure 3. Optional Trim Connections

The summing and log circuits provide signals to the input of the differential amplifier that are proportional to the sum and difference of the X and Z inputs. The difference between these two signals causes an imbalance current, ΔI_C, in the differential amplifier. The resultant output currents of the differential amplifier are equal to $I_{REF}/2 + \Delta I_C$ and $I_{REF}/2 - \Delta I_C$, where I_{REF} is a stable reference current supply. These two output currents bear a relationship to the input signals that is expressed by:

$$\frac{X + Z/2}{X - Z/2} = \frac{I_{REF}/2 + \Delta I_C}{I_{REF}/2 - \Delta I_C}$$

The final amplifier stage of the model 436 processes these currents and yields an output voltage whose expression is,

$$E_O = KI_{REF}\frac{Z}{X} = \frac{10Z}{X}$$

This ratio relationship between X and Z is very accurate even for small value of X. Also by virtue of the log-antilog nature of this technique, output errors remain reasonably constant over the specified range of denominator inputs. Beyond the specified denominator range, second order effects, due to input offsets, cause the output error to increase with decreasing denominator. In the model 436, these second order effects are minimized. Input offsets can be further reduced by means of external trims. Trimming allows the 436 to maintain rated accuracy over a 1000:1 range of denominator inputs. Therefore, model 436 provides excellent performance and stability over a wide range of input signals and operating conditions. For a detailed explanation of the design used in the 436, refer to Analog Devices' Nonlinear Circuits Handbook ($5.95).

ACCURACY VS. DENOMINATOR

By virtue of the nature of the log function, the errors associated with log-antilog type dividers can be expressed as a constant plus a constant fraction of the output over the specified input range. Therefore, unlike inverted multiplier type dividers which demonstrate an inverse relationship between accuracy and denominator, the model 436 has outstanding accuracy which is reasonably denominator independent over a 100:1 range. Model 436A and 436B are guaranteed to have maximum output error of 0.5% and 0.25% respectively for denominator values from 100mV to 10 volts. A plot of typical output error vs. denominator for the 436 is shown in Figure 4.

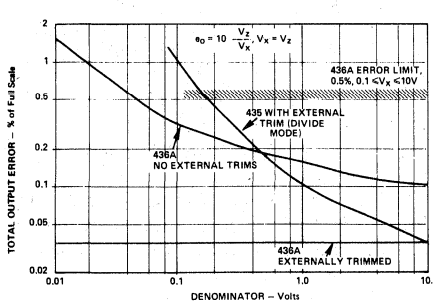


Figure 4. Total Output Error vs. Denominator at Constant Ratio $V_Z/V_X = 1$. Comparison of Model 436 with Model 435, 0.1% Multiplier-Divider.

The accuracy of the 436 can be further improved by use of external trims (see Optional Adjustment Procedure). Figure 4 shows accuracy vs. denominator for a 436 with external trim. Optional trimming allows the 436B to maintain better than 0.1% accuracy over a 1000:1 range of the denominator signal.

ACCURACY VS. TEMPERATURE

The output offset drift vs. temperature of the model 436 remains fairly constant over a 100:1 range of denominators. Total error drift is typically 1mV/°C at V_X = 10V and 2mV/°C at V_X = 100mV. Model 436 is therefore capable of maintaining outstanding accuracy over a wide range of temperature and denominator signal level. Figure 5 shows total error drift vs. denominator for the 436.

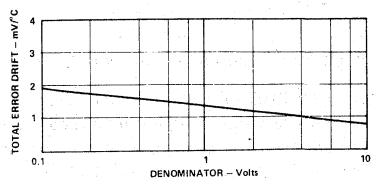


Figure 5. Total Error Drift vs. Denominator

NONLINEARITY

The symmetry of the type of circuit used in model 436 provides low numerator distortion independent of denominator level. Figure 6 shows nonlinearity vs. denominator.

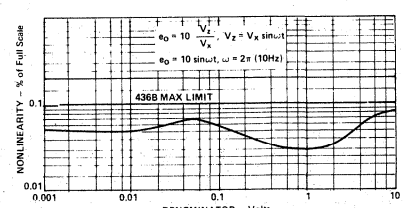


Figure 6. Nonlinearity vs. Signal Level for Constant Output = 10 sinωt (10Hz)

FREQUENCY RESPONSE

The bandwidth of any divider decreases with a decrease in denominator due to the increase in system gain. Figure 7 shows a typical plot of the small signal and full power bandwidth vs. denominator for the model 436.

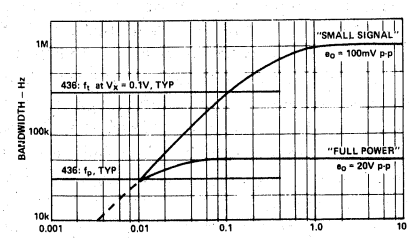


Figure 7. Small Signal Bandwidth (-3dB) and Full Power Bandwidth vs. Denominator

NOISE PERFORMANCE

Model 436 offers very good output noise performance in addition to its other excellent operating characteristics. Output noise can be an important parameter in dynamic computing. The model 436 typically has a 200μV rms output noise level in the 10 to 10kHz band for V_X = +10V.

Figure 8 shows output noise vs. denominator for model 436.

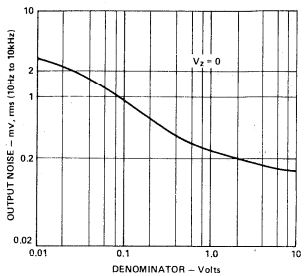


Figure 8. Output Noise vs. Denominator – 5Hz to 10kHz

OPTIONAL ADJUSTMENT PROCEDURE

One of model 436's features is high untrimmed accuracy. As shown in Figure 4, significant improvement in performance can be achieved with external trimming. Model 436 can be typically trimmed to less than ±0.1% of full scale accuracy (±10mV error) for a denominator signal range from +10mV to +10V (1000:1). To achieve this performance, the following adjustment procedure is recommended: (see Figure 3)

1) Allow unit to warm up for approximately 5 minutes. Let denominator (V_X) = +10V and numerator (V_Z) = 0V (connect to common pin). Adjust OUTPUT OFFSET potentiometer (R_O) for 0mV output.

2) Let denominator = +10mV and numerator = 0V (connect to common pin). Adjust NUMERATOR OFFSET potentiometer (R_n) for 0mV output.

3) a. Let denominator = numerator = +10.000V and adjust GAIN potentiometer (R_g) for +10.000V output.
b. Reverse the polarity of numerator (to - 10.000V), and note the output voltage error (error = 10.000 - $|e_o|$). The GAIN potentiometer R_g should be readjusted to achieve the lowest error for both step a. and step b.

4) Connect both numerator/denominator together and apply a +10mV input. Adjust DENOMINATOR OFFSET potentiometer (R_d) for +10.000V output.

REPLACEMENT OF 0.1% MULTIPLIERS

In divider applications requiring high accuracy over a wide range of denominators, the model 436 provides significant advantages over 0.1% multipliers used in the inverted multiplier divide mode. As shown in Figure 4, an untrimmed 436 yields better overall accuracy than the most accurate available multiplier (435K) for a 100:1 change in denominator. With external trimming, model 436 delivers vastly superior performance over an even wider spread of denominator levels. The inverted multiplier type dividers suffer from the magnification of errors by $10/V_X$ whereas the errors of the variable transconductance circuit of model 436 are nearly independent of denominator. This advantage of the 436 design also is reflected in the reduced dependency of total error drift and bandwidth on the value of V_X. Figure 9 shows small signal bandwidth vs. denominator for the 436 and for 0.1% multiplier-dividers.

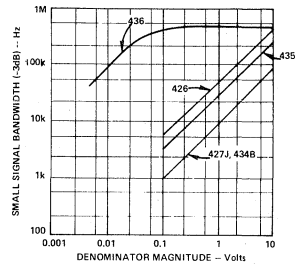


Figure 9. Bandwidth (-3dB) vs. Denominator

APPLICATIONS

Ratiometric Measurements

Dividers are useful for direct readout of such ratios as efficiencies, losses or gains, % distortion, impedance magnitudes, elasticity (stress/strain). Ratios may be taken of instantaneous, average, RMS or peak quantities. Furthermore, in conjunction with sample/hold devices, ratios may be taken of any of these measurements at different instants of time.

Ratiometric measurements are not new, but the low cost of precision analog dividers, like the model 436, should serve as an encouragement to designers to consider employment of the technique as a realistic alternative to expensive, tightly regulated reference sources for measurement. The divider output can profitably provide constant direct readout information on a DPM, such as the AD2026. In addition to eliminating the need for precise sources, the cost of calibration time required in systems currently depending on these sources can be reduced by ratiometric techniques employing the 436 divider.

A simple example involving the use of dividers in eliminating the effects of a common parameter is found in bridge measurements, where variations of the power supply directly affect the scale factor. But, if the output is divided by the bridge supply voltage, the scale factor depends only on the stability of the divider. The model 436 has the initial accuracy and stability which makes it useful in many ratio applications.

Compensation for reference-voltage variations is an example of reducing the effects of a common electrical parameter. However, ratios can also be used to eliminate the effects of a common physical parameter. For example, in light transmission measurements, it is common to compensate for variations in light intensity by transmitting two beams, one through a reference medium, the other through the medium being measured, and to take the ratio of the two measurements.

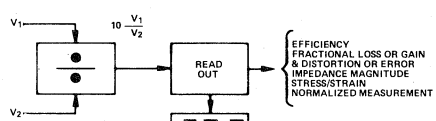


Figure 10. Ratio Measurements

The resultant output of ratiometric measurements may also be used as a feedback signal in adaptive process control networks. This technique facilitates accurate on-line monitoring and control of vital system parameters.

Log/Antilog Amplifiers

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5

Selection Guide
Log/Antilog Amplifiers

This Selection Guide includes both log/antilog amplifiers and log-ratio modules. The suffixes "N" and "P" refer to the specified polarity of input current or voltage when connected as a log amplifier, or the polarity of output voltage as an antilog amplifier. "N" designates *positive* voltage, "P" *negative*.

General information and definitions of specifications can be found in the following pages. All specifications are typical at rated supply and load, and T_A = +25°C, unless noted otherwise.

Model	Characteristics	Page
Model 755N/P Log-antilog amplifier	High performance: ±1% max log-conformity error for 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V), and 0.5% max conformity error for 4 decades of current (10nA to 100μA) and 3 decades of voltage (1mV to 1V), 1.5″ x 1.5″ x 0.4″ module. Antilog output range: 4 decades, 1mV to 10V, K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	5-7
Model 759N/P Log-antilog amplifier	Small size and low cost: 1.13″ x 1.13″ x 0.4″ module, wide bandwidth 200kHz @ 1μA, ±2% max log-conformity error for 5 decades of current (10nA to 1mA) or 4 decades of voltage (1.0mV to 10V), and ±1% max conformity error for 4 decades of current (20nA to 200μA). Log operating range: 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). Antilog output range: 4 decades (1mV to 10V), K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	5-15
Model 757N/P Log-ratio module	Input dynamic range, 6 decades of current (1nA to 1mA), either channel, log conformity error ±1.0% max; for 4 decades (10nA to 100μA), log conformity error ±0.5% max. Log of voltage by using external resistors. K = 1 V/decade, ±1%, max, or externally programmable. Can be used for antilog operations.	5-11

Orientation
Log/Antilog Amplifiers

The devices catalogued in this section are complete, self-contained modules that provide output voltage proportional to the logarithm or the antilogarithm (exponential) of an input quantity. These modules operate on the instantaneous values of inputs from dc to an upper cutoff frequency below 1MHz.

LOGS AND LOG RATIOS

In the *logarithmic* mode, the ideal output equation is

$$E_o = -K \log_{10} \left(\frac{I_{in}}{I_{ref}}\right)$$

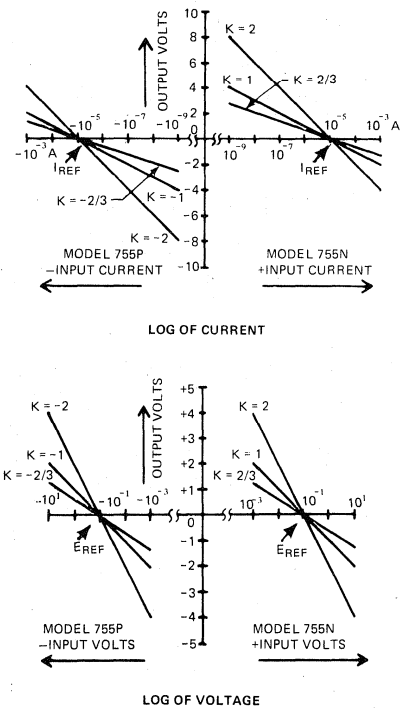
E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin-programmable to be either 1V, 2V, or 2/3V, or externally adjustable to any value $\geqslant$ 2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V, or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted; but model 757 is a *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive;* "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 759N, with K = +1V, would produce an output voltage, $E_o = -1V \log (100) = -2V$; on the other hand, -10V applied to model 759P, with K = 1V, would produce an output voltage, $E_o = -(-1V) \log (100) = +2V$. The figure shows, in condensed form, the outputs of P and N log-amps, with differing K values, for voltage and current inputs.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs, and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

*A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1000 (3 decades), the output would change by 6V.



Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

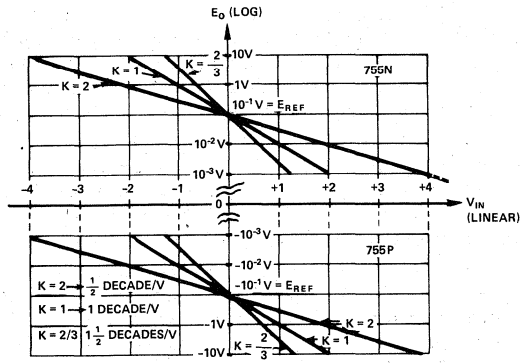
$$E_o = E_{ref} \exp_{10} (-E_{in}/K)$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = -2V, if E_{in} = +4V, and E_{ref} = -0.1V, then

$E_o = -0.1V \cdot 10^{-4/-2}$, or -10V; if $E_{in} = -4V$, then

$E_o = -0.1V \cdot 10^{-(-4)/-2} = -1mV$. The figure on the next page shows, in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.



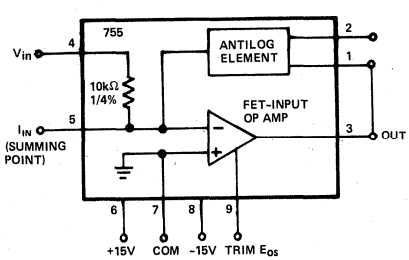
Antilog Operator Response Curves, Semilog Scale
$E_O = E_{REF}\ 10^{V_{IN}/-K}$

LOG-ANTILOG AMPLIFIER PERFORMANCE

Considerable information regarding log- and antilog-amplifier circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK[1]. Several salient points will be covered here, and specifications will be defined.

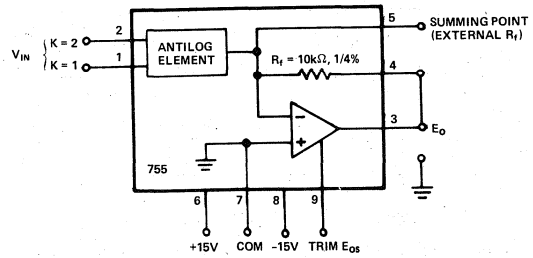
A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)

[1] *Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete Master-Charge data to P.O. Box 796, Norwood MA 02062



b) Log/Antilog Amplifier Connected in the Exponential Mode

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

$$I = I_o(\epsilon^{qV/kT} - 1) \cong I_o\epsilon^{qV/kT}$$

and $V = (kT/q) \ln (I/I_o)$

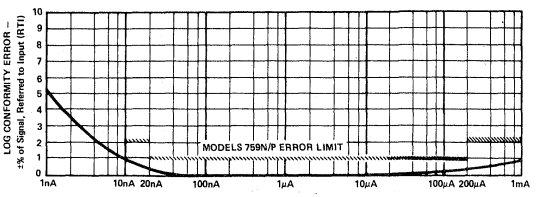
where I is the collector current, I_o is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11605° K/V) is the ratio of charge of an electron to Boltzmann's constant, and T is junction temperature kelvin. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_o's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q) \ln (I_{in}/I_o) - (kT/q) \ln (I_{ref}/I_o)\\ &= (kT/q) (\ln I_{in} - \ln I_{ref}) + (kT/q) (\ln I_o - \ln I_o)\\ &= (kT/q) \ln (I_{in}/I_{ref})\end{aligned}$$

The temperature-dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade (kT/q) ln10 at room temperature) to 1V/decade.

Errors are introduced by the offset current of the amplifier, and the offset voltage, for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog paper. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA. A plot of log conformity error for model 759 is shown here.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at what-



Log Conformity Error for Models 759N and 759P

ever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output}\\ &= 1V\cdot\log(1.01\ I/I_{ref}) - 1V\cdot\log(I/I_{ref})\\ &= 1V\cdot\log 1.01 = 0.0043V = 4.3mV\end{aligned}$$

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17.	5.7
3.0	13.	26.	8.6
4.0	17.	34.	11.
5.0	21.	42.	14.
10.0	41.	83.	28.

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{in}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation, E_{os} appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

6-Decade, High Accuracy Log, Antilog Amplifiers

MODELS 755N, 755P

FEATURES

- Complete Log/Antilog Amplifier
  - External Components Not Required;
  - Internal Reference; Temperature Compensated
- 6 Decades Current Operation – 1nA to 1mA
  - 1/2% max Error – 10nA to 100μA
  - 1% max Error – 1nA to 1mA
- 4 Decades Voltage Operation – 1mV to 10V
  - 1/2% max Error – 1mV to 1V
  - 1% max Error – 1mV to 10V

APPLICATIONS

- Log Current or Voltage
- Antilog Voltage
- Data Compression or Expansion
- Absorbence Measurements
- Computing Powers and Log Ratios

GENERAL DESCRIPTION

Model 755 is a complete dc logarithmic amplifier consisting of an accurate temperature compensated antilog element, and a low bias current FET amplifier. In addition to offering 120dB of current logging (1nA to 1mA) and 80dB of voltage logging (1mV to 10V), the 755 features exceptionally low bias currents of 10pA and 15μV/°C voltage drift to satisfy most wide range applications. Conformance to ideal log operation is held to ±1% over its total 120dB current range (1nA to 1mA), with ±0.5% conformity guaranteed over an 80dB range (10nA to 100μA). Two models are available, model 755N and model 755P. The N version computes the log of positive input signals and the P version computes the log of negative input signals.

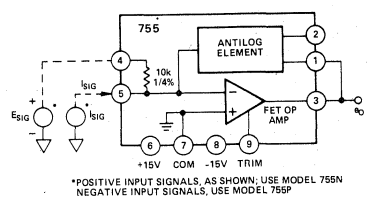
Advanced design techniques and improved component selection are used to obtain exceptionally good performance. For example, the use of monolithic devices greatly reduces the influence of temperature variations. Offering both log and antilog operation, model 755's price and performance are especially attractive as an alternative to in-house designs of OEM applications. This log design also improves significantly over competitive designs in price, performance, and package size.

MAJOR IMPROVEMENTS IN I_{OS}

For most low level applications, the input bias current I_{OS}, is especially critical, since it is the major source of error when processing low level currents. At 1nA of input current there is an error contribution of 1% for every 10pA of I_{OS}. Recognizing the importance of this parameter, bias current of model 755 is maintained below 10pA.

APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the model 755 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.



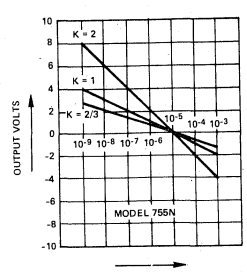


Figure 1. Functional Block Diagram and Transfer Function

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

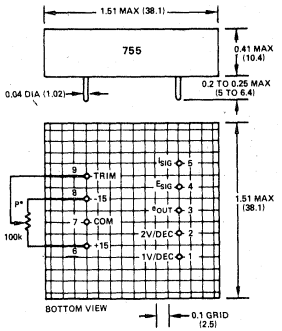
MODEL	755N/P
TRANSFER FUNCTIONS	
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$
Antilog Mode	$e_O = E_{REF}\,10^{-\left(\frac{E_{SIG}}{K}\right)}$
TRANSFER FUNCTION PARAMETERS	
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade
Error @ +25°C	±1% max
vs. Temperature (0 to +70°C)	±0.04%/°C max
Reference Voltage (E_{REF})[2]	0.1V
Error @ +25°C	±3% max
vs. Temperature (0 to +70°C)	±0.1%/°C max
Reference Current (I_{REF})[2]	10μA
Error @ +25°C	±3% max
vs. Temperature (0 to +70°C)	±0.1%/°C max
LOG CONFORMITY ERROR	
I_{SIG} Range / E_{SIG} Range / R.T.I. / R.T.O. (K = 1)	
1nA to 10nA / – / ±1% max / ±4.3mV max	
10nA to 100μA / 1mV to 1V / ±0.5% max / ±2.17mV max	
100μA to 1mA / 1V to 10V / ±1% max / ±4.3mV max	
1nA to 1mA / – / ±1% max / ±4.3mV max	
INPUT SPECIFICATIONS	
Current Signal Range	
Model 755N	+1nA to +1mA min
Model 755P	−1nA to −1mA min
Max Safe Input Current	±10mA max
Bias Current @ +25°C	(0, +) 10pA max
vs. Temperature (0 to +70°C)	x2/+10°C
Voltage Signal Range (Log Mode)	
Model 755N	+1mV to +10V min
Model 755P	−1mV to −10V min
Voltage Signal Range, Antilog Mode Model 755N, 755P	$-2 \leqslant \frac{E_{SIG}}{K} \leqslant 2$
Offset Voltage @ +25°C (Adjustable to 0)	±400μV max
vs. Temperature (0 to +70°C)	±15μV/°C max
vs. Supply Voltage	±15μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Bandwidth, −3dB	
I_{SIG} = 1nA	80Hz
I_{SIG} = 1μA	10kHz
I_{SIG} = 10μA	40kHz
I_{SIG} = 1mA	100kHz
RISE TIME	
Increasing Input Current	
10nA to 100nA	100μs
100nA to 1μA	7μs
1μA to 1mA	4μs
Decreasing Input Current	
1mA to 1μA	7μs
1μA to 100nA	30μs
100nA to 10nA	400μs
INPUT NOISE	
Voltage, 10Hz to 10kHz	2μV rms
Current, 10Hz to 10kHz	2pA rms
OUTPUT SPECIFICATIONS[3]	
Rated Output	
Voltage	±10V min
Current	
Log Mode	±5mA
Antilog Mode	±4mA
Resistance	0.5Ω
POWER SUPPLY[4]	
Rated Performance	±15Vdc
Operating	±(12 to 18)Vdc
Current, Quiescent	±7mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	−25°C to +85°C
Storage	−55°C to +125°C
CASE SIZE	1.5" x 1.5" x 0.4"

[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 or 2 (shorted together) for K = 2/3V/decade.
[2] Specification is + for model 755N; - for model 755P.
[3] No damage due to any pin being shorted to ground.
[4] Recommended power supply, model 904, ±15V @ ±50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

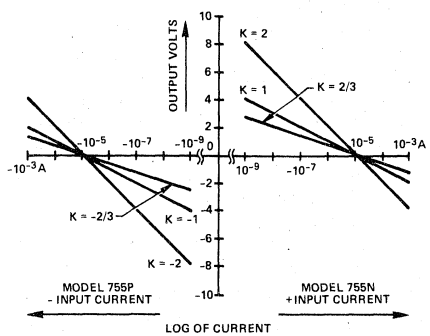
Dimensions shown in inches and (mm).



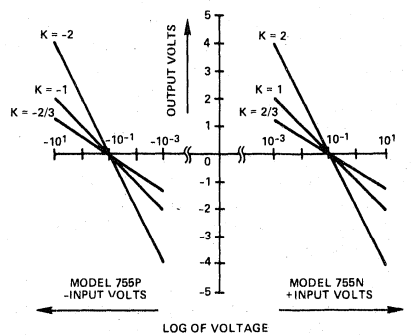
*Optional 100kΩ external trim pot – ADI PN79PR100k. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV maximum.

MATING SOCKET AC1016

TRANSFER CURVES



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Model 755 Connected in the Log Mode

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

A graph of the ideal transfer function for model 755N is presented in Figure 2, for one decade of operation. Although specific values of i_{in} and e_{out} are presented for n = 1, other values may be plotted by varying n.

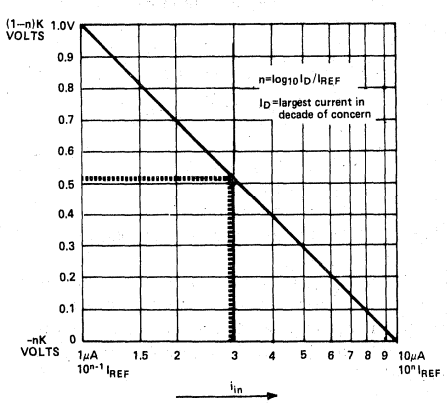


Figure 2. Input vs. Output for Any One Decade of Operation

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{out} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{out} = \underbrace{1V \log_{10} I_{SIG}/I_{REF}}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} 1.01}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

TABLE 1

Error R.T.I. (N)	Error R.T.O. K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table 1. Converting Output Error in mV to Input Error in %

NOTE:
Data may be interpolated with reasonable accuracy, for small errors by adding various values of N and their corresponding R.T.O. terms. That is, for N = 2.5% and K = 1, combine 2% and 0.5% terms to obtain 10.77mV.

SOURCES OF ERROR

When applying the model 755, a firm understanding of error sources associated with log amplifiers is beneficial for achieving maximum performance. The definitions, limitations and compensation techniques for errors specified on log amplifiers will be discussed here.

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated or taken into account. For model 755, the best linearity performance is obtained in the middle 4 decades (10nA to 100μA). For this range, log conformity error is ±0.5% R.T.I. or 2.17mV R.T.O. To obtain optimum performance, the input data should be scaled to this range.

Offset Voltage (E_{OS}) – The offset voltage, E_{OS}, of model 755 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Offset Current (I_{OS}) – The offset current, I_{OS}, of model 755 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, I_{OS}, for model 755, is held within a conservative 10pA max.

Reference Current (I_{REF}) – I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3%, referred to the input, and, from Table 1, corresponds to a dc offset of ±12.84mV, for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage (E_{REF}) – E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation: $E_{REF} = I_{REF} \times R_{in}$, where R_{in} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor (K) – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

EXTERNAL ADJUSTMENTS FOR LOG OPERATION (OPTIONAL)

Trimming E_{os} – The amplifier's offset voltage, E_{os}, may be trimmed for improved accuracy with the model 755 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3, and the input terminal, pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{out} = -K \log_{10} E_{os}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for model 755N, and −3 to −4V for model 755P.

For other values of K, the trim pot should be adjusted for an output of $e_{out} = 3 \times K$ to $4 \times K$ where K is the scale factor.

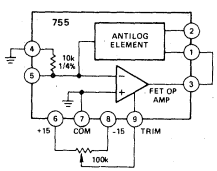


Figure 3. Trimming E_{OS} in Log Mode

REFERENCE CURRENT OR REFERENCE VOLTAGE

The reference current or voltage of model 755 may be shifted by injecting a constant current into the unused scale factor terminal (pin 1 or pin 2). Each 66μA of current injected will shift the reference one decade, in accordance with the expression: $I_I = 66\mu A \log 10\mu A/I_{REF}$, where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, $E_{REF} = I_{REF} \times R_{in}$. An alternate method for rescaling E_{REF} is to connect an external R_{in}, at the I_{in} terminal (pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, $E_{REF} = R_{in} I_{REF}$. Care must be taken to choose R_{in} such that $(e_{in}\ max)/R_{in} \leqslant 1mA$.

Scale Factor (K) Adjustment – Scale factor may be increased from its nominal value by inserting a series resistor between the output terminal, pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

TABLE 2

Range of K	Connect Series R to Pin	Value of R	Note
2/3V to 1.01V	1	15kΩ x (K − 2/3)	use pins 1, 2
1.01V to 2.02V	1	15kΩ x (K − 1)	use pin 1
> 2.02V	2	15kΩ x (K − 2)	use pin 2

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The model 755 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{out} = E_{REF}\ 10^{-e_{in}/K}$$

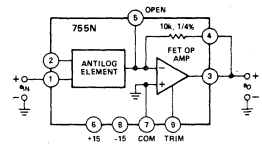


Figure 4. Functional Block Diagram

Principle of Operation – The antilog element converts the voltage input, appearing at terminal 1 or 2, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{out} = E_{REF}\ 10^{-e_{in}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{os}) Adjustment – Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to $e_{out}/100$. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from pin 1 to +15V. For 755P, use the same procedure but connect pin 1 to −15V.

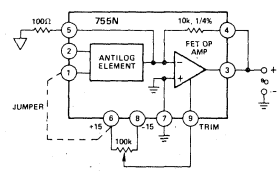


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment – In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from pin 5 to pin 3, in place of the internal 10kΩ. The value of R is determined by:

$$R = E_{REF}\ \text{desired}/10^{-5}\ A$$

Scale Factor (K) Adjustment – The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K, less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$$R1/R_G = (1/K - 1) \text{ where K = desired scale factor}$$

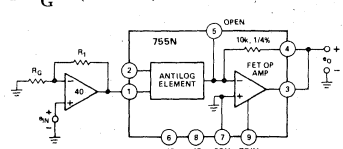


Figure 6. Method for Adjusting K<2/3V

6-Decade, High Accuracy Log Ratio Module

MODEL 757N, 757P

FEATURES
- 6 Decade Operation – 1nA to 1mA
- 1/2% Log Conformity – 10nA to 100μA
- Symmetrical FET Inputs
- Voltage or Current Operation
- Temperature Compensated
- Antilog Operation

APPLICATIONS
- Absorbence Measurements
- Log/Antilog Ratios of Voltages or Currents
- Data Compression
- Transducer Linearization

GENERAL DESCRIPTION

Model 757 is a complete, temperature compensated, dc-coupled log ratio module. It is comprised of two input channels for processing signals spanning up to 6 decades in dynamic range (1nA to 1mA). By virtue of its symmetrical FET input stages, the 757 can accommodate this 6 decade signal range at either channel. Log conformity is maintained to within 1/2% over 4 decades of input (10nA to 100μA) and to within 1% over the full input range. Unlike other log ratio designs, model 757 does not restrict the relative magnitude of the two signal inputs to achieve rated performance. Either input can be operated within the specified range regardless of the signal level at the other channel.

The model 757 log-ratio module design makes available both input amplifier summing junctions. As a result, it can directly interface with photo diodes operating in the short-circuit current mode without the need of additional input circuitry.

The excellent performance of model 757 can be further improved by means of external scale factor and output offset adjustments. A significant feature of model 757 not found on competing devices is that, when the offset adjustment is used to establish a fixed bias at the output, the output offset level does not vary as a function of input signal magnitude. On other designs, the sensitivity of output offset to input levels results in output effects resembling log conformity errors.

Model 757 can operate with either current or voltage inputs. Its excellent performance makes it ideally suited for log ratio applications such as blood analysis, chromatography, chemical analysis of liquids and absorbence measurements.

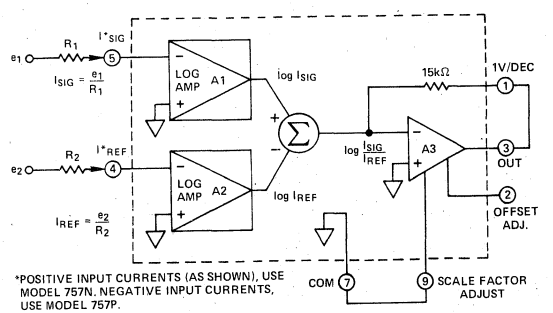


Figure 1. Functional Block Diagram of Model 757

CURRENT LOG RATIO

Current log ratio is accomplished by model 757 when two currents, I_{SIG} and I_{REF}, are applied directly to the input terminals (see Figure 1). The two log amps process these signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, higher scale factors may be achieved by connecting external scale factor adjusting resistors. (See section on optional adjustments and trims.)

VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	757N/P
TRANSFER FUNCTION [1]	
Current Mode	$e_O = -K \log_{10} \frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_O = -K \log_{10} \left[\frac{e_1}{e_2} \times \frac{R_2}{R_1}\right]$
ACCURACY	
Log Conformity [2]	
I_{SIG}, I_{REF} = 10nA to 100µA	±0.5%, max
I_{SIG}, I_{REF} = 1nA to 1mA	±1%, max
Scale Factor (1V/Dec)	(+0, -2%) max
vs. Temperature (0 to +70°C)	±0.04%/°C max
INPUT SPECIFICATIONS — Both Input Channels	
Current	
Signal Range, Rated Performance	
Model 757N	+1nA to +1mA
Model 757P	-1nA to -1mA
Max Safe	±10mA
Bias Current, @ +25°C	-10pA
vs. Temperature (0 to +70°C)	x2/+10°C
Offset Voltage, @ +25°C	±1mV max
vs. Temperature (0 to +70°C)	
I_{SIG} Channel	±25µV/°C max
I_{REF} Channel	±85µV/°C max
vs. Supply Voltage	±5µV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Response (-3dB)	
Signal Channel	
I_{SIG} = 1nA	300Hz
I_{SIG} = 1µA	25kHz
I_{SIG} = 100µA	50kHz
Reference Channel	
I_{REF} = 1nA	3kHz
I_{REF} = 1µA	25kHz
I_{REF} = 100µA	50kHz

RISE TIME	Signal Channel (I_{REF} = 10µA)	Reference Channel (I_{SIG} = 10µA)
Increasing Input Current		
1nA to 10nA	250µs	80µs
10nA to 100nA	50µs	40µs
100nA to 1µA	30µs	30µs
1µA to 100µA	25µs	25µs
Decreasing Input Current		
100µA to 1µA	25µs	25µs
1µA to 100nA	30µs	30µs
100nA to 10nA	100µs	40µs
10nA to 1nA	600µs	70µs

INPUT NOISE	
Voltage (10Hz to 10kHz)	3µV rms
Current (10Hz to 10kHz)	0.1pA rms
OUTPUT SPECIFICATIONS	
Rated Output	
Voltage	±10V min
Current	
Log Mode	±5mA, min
Antilog Mode	±4mA, min
Resistance	0.1Ω
Offset Voltage [3] (K = 1V/Decade)	±10mV max
vs. Temperature (0 to +70°C)	±0.3mV/°C
vs. Supply	±5µV/V
POWER SUPPLY [4]	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±8mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Case Size	1.5" x 1.5" x 0.4"
Mating Socket	AC1048
Weight	21 grams

[1] For model 757N, K = +1V/Decade and input currents must be positive. For model 757P, K = -1V/Decade and input currents must be negative. (Input currents are defined as positive when flowing into the input terminals, 4 and 5. Refer to TRANSFER CURVES.)

[2] The log conformity error is referred to input (RTI). 1% error RTI is equivalent to 4.3mV of error at the output for K = 1V/Dec.

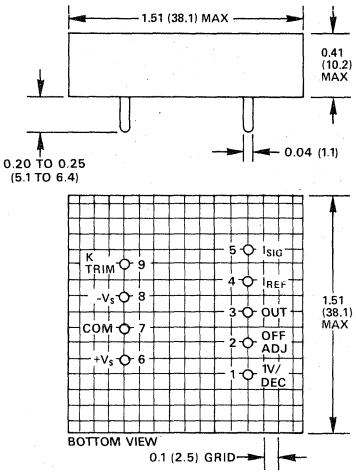
[3] Externally adjustable to zero.

[4] Recommended power supply: Analog Devices model 904, ±15V @ 50mA.

Specifications subject to change without notice.

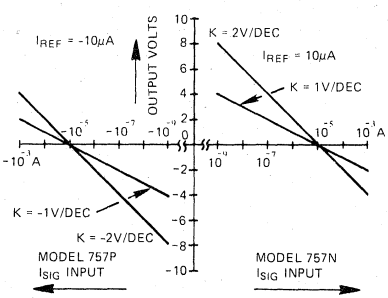
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Mating Socket AC1048

TRANSFER CURVES



Log mode output voltage vs. input current for I_{REF} = 10µA. For voltage input calculate I_{SIG} as e_1/R_1 (see Figure 1).

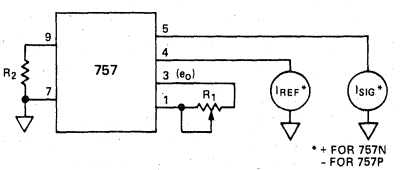


Figure 2. Scale Factor Adjustment

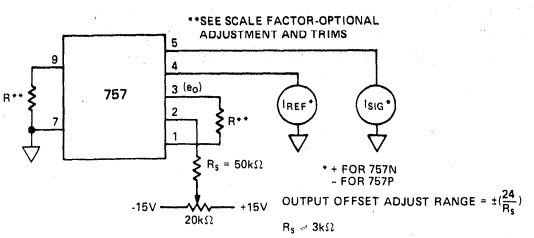


Figure 3. Output Voltage Offset Adjustments

resistor is attached from the voltage signal to the appropriate input current terminal of the 757. Input currents are then determined by:

$$I_{SIG} = \frac{e_1}{R_1}, I_{REF} = \frac{e_2}{R_2}$$

OPTIONAL ADJUSTMENTS AND TRIMS

Scale Factor – A one volt per decade scale factor is available when pin 1 is tied to 3 and pin 7 is connected to 9. Higher scale factors are possible by using a potentiometer, R_1, between pins 1 and 3 and a resistor, R_2, between pins 7 to 9 as shown in Figure 2. The value of the required resistor is (15kΩ) (K-1) where K is the desired scale factor. The approximate potentiometer value is also (15kΩ) (K-1). The scale factor adjustment procedure is as follows:

1. Connect the appropriate value of resistor between pins 7 and 9.
2. Set I_{REF} = 1μA, I_{SIG} = 10μA. Measure e_O.
3. Set I_{REF} = 1μA, I_{SIG} = 100μA. Adjust R_1 until the difference in e_O corresponding to steps 2 and 3 is K volts.
4. Repeat steps 2 and 3 until the change in e_O = K volts.

Output Voltage Offset – Output voltage offset must be adjusted after the desired scale factor is established as indicated above. To adjust the offset, inject equal dc input currents into the reference and signal channels. The value of the input currents should approximate the average input current levels expected to be encountered in normal operation. Adjust the potentiometer shown in Figure 3 until the output voltage is zero.

INTERCHANGEABILITY WITH MODEL 756

Model 757 is a functional, pin compatible replacement for model 756 in applications that do not require external trims. The user need only short pin 7 to pin 9 in order to establish a scale factor of 1V/decade. In applications requiring external adjustments, the scale factor and offset trims should be configured to the model 757 requirements as outlined above.

LOG CONFORMITY

Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the theoretical value of the log of a ratio and the actual value that appears at the output of the log-ratio module after scale factor errors have been eliminated. Measurement of this error is made after initially zeroing the module at unity-ratio and adjusting the desired scale factor.

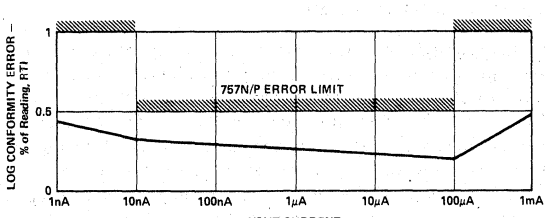


Figure 4. Log Conformity Error for Model 757. Curve is for Either Input Channel with Current Held Constant at 10μA On Other Channel.

Figure 4 shows the log conformity performance of model 757 over a 6 decade input range. Log conformity for each channel does not vary noticeably as the current is varied in the other channel.

FREQUENCY CHARACTERISTICS

Figure 5 shows a plot of small signal response (-3dB) as a function of input signal current. The graph demonstrates the frequency response performance for each input channel over the range of 1nA to 1mA, independent of current on the other channel.

As shown in the graph, the reference channel is faster than the signal channel at low input levels. If an application requires higher speed in the input signal channel than in the reference channel, then the channels can be interchanged with a resulting polarity reversal of the output signal

$$(\log \frac{I_{SIG}}{I_{REF}} = \log I_{SIG} - \log I_{REF} = -\log \frac{I_{REF}}{I_{SIG}}).$$

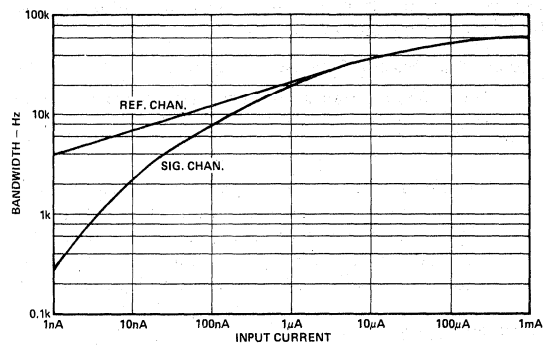


Figure 5. Small Signal Bandwidth (-3dB) vs. Input Signal Level

OUTPUT OFFSET VOLTAGE DRIFT

The curves of Figure 6 illustrate the output offset voltage changes over the operating temperature range of 0 to +70°C, at K = 1V/decade. Since output offset voltage changes are minimum at +25°C, best accuracy operation is obtained over the range of +25°C ±20°C.

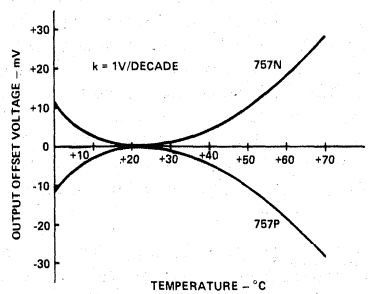


Figure 6. Output Offset Voltage vs. Temperature

ANTILOG OPERATION

The antilogarithm is the inverse of the logarithm. It is by definition the exponential in which the logarithmic base (B) is raised to a power (Y). That is,

$$X = \log^{-1}{}_B (Y) = B^Y$$

The model 757 log ratio module with the transfer function

$$E_O = -K \log_{10} \frac{E_{SIG}}{E_{REF}} \quad (R_1 = R_2)$$

can be connected as shown in Figure 7 to compute

$$E_O = E_{REF} \times 10^{(E_{SIG}/-K)}$$

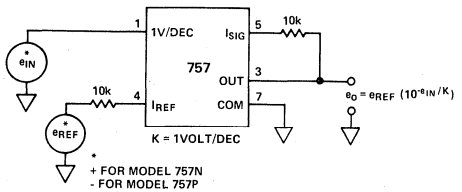


Figure 7. Model 757 Antilog Connection

Thus, when K = 1, the log ratio operation provides an output of 1 volt per decade of input ratio, while the antilog mode yields an output that changes 1 decade per volt of input.

In antilog operation, E_{REF} is the normalized value of the exponential and each volt of increase of the input multiplies E_{REF} by an additional factor of 10.

Exponential devices can be used when:

1. Compound multiplications involving roots and powers are performed.
2. Devices with logarithmic responses must be linearized.
3. Function fitting and generation is required to obtain relationships or generate curves having voltage-programmable rates of growth or decay. (e.g. if E_{SIG} is a ramp, E_O will be a widely varying exponential function of time that can be further modified by varying E_{REF} and K).

APPLICATIONS

Data Compression – Processing signals with wide dynamic range is a common problem in instrumentation and data transmission. For example, digitizing an analog signal with a range of 10nA to 100μA with 1% accuracy requires a 20 bit A/D converter. (Required resolution = 1/100 x 1/10,000 = $1/10^6 \cong 1/2^{20}$).

By using the 757 with I_{REF} adjusted to 10nA and K set for 5/4 V/decade, the input data can be compressed into a 5 volt output range. For a 1% resolution of any signal, the allowable output error is 4.32mV x K. Log conformity contributes 2.17mV x K (0.5%) over this range. The remaining error with K = 5/4 is 2.69mV and should correspond to less than the LSB of the converter. With a 5 volt output range 2.69mV corresponds just over the LSB of an 11-bit converter. Thus the 757 module can compress the data for use with a 12 bit A/D (such as Analog Devices ADC-12QZ) to obtain the desired 1% resolution.

Absorbence Measurements – Critical properties of materials, which are of particular interest in the fields of chemistry, medicine, spectrometry and pollution control are characterized by absorbence. The relationship between absorbence, A, and light intensity, I, is: $A = \log I_O/I_T$ where I_O = intensity of incident light, and I_T = intensity of transmitted light.

Figure 8 shows the 757 log-ratio module used in such a photometer application. Two inputs represent the intensities of light transmitted through space and through a medium that absorbs light. The absorbence of the medium is given by the formula

$$A = \log \frac{I_{SIGNAL}}{I_{REFERENCE}}$$

where I_{SIGNAL} and $I_{REFERENCE}$ are the currents representing the light intensities.

The transducers used in this application are photodiodes, which provide a short-circuit current proportional to the intensity of applied light. The lowest value of absorbence is determined by the value of I_{REF}, since when $I_{SIG} = I_{REF}$, A = 0. The output of the log-ratio module is externally trimmed to 1V/decade and applied to the input of a 3½-digit DPM through the scaling network R1 and R2.

Model 757 was chosen for this design because it makes available both amplifier summing junctions. When the photodiodes are connected to the summing junctions, they are operated in the short-circuit mode, that is, with zero volts across the diodes. Short-circuit loading is necessary, because accuracy of the photodiodes can be degraded several percent when operated with as little as 100mV across the diode junction.

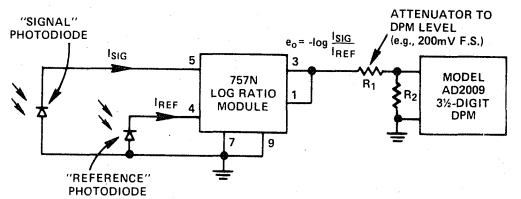


Figure 8. Model 757N Applied to Absorbance Measurements

INTERCONNECTION GUIDELINES

Model 757 is a complete log ratio module that requires no additional frequency compensation for proper operation.

Input Capacitance – Model 757 is able to operate with 1000pF at both input terminals. Therefore, the 757 can be used in applications requiring long cable lengths between the module and the signal transducers.

Input-to-Output Capacitance – When using a log ratio module the user should take care in system configurations to avoid excessive stray capacitance between input and output terminals. Such precautions include avoiding running input and output signal lines close together. If long cable runs are required where inputs and output are closely bundled together, it is advisable to enclose the inputs and/or output in separate, grounded electrostatic shields. By observing simple rules of good circuit layout, problems with oscillations that may result from excessive input-to-output capacitance can easily be avoided. Model 757 can accommodate up to 150pF of input-to-output capacitance without oscillation.

Leakage Resistance – Since model 757 can operate at extremely low input current levels, precautions must be taken to prevent current leakage into the input terminals. Such leakage can cause errors when small input or reference currents are used. This problem may arise on printed circuit layouts if the inputs are run too close to the power supply busses. Providing an etched guard around the input lines, connected to analog signal ground will also reduce unwanted current leakage.

Economy, Wideband Log/Antilog Amplifiers

MODELS 759N, 759P

FEATURES

- Low-Cost, Complete Log/Antilog Amplifier
  - External Components Not Required;
  - Internal Reference; Temperature Compensated
- Small Size: 1.1″ x 1.1″ x 0.4″
- Fast Response: 200kHz Bandwidth (I_{SIG} = 1μA)
- 6 Decades Current Operation – 1nA to 1mA
  - 1% max Error – 20nA to 200μA
  - 2% max Error – 10nA to 1mA
- 4 Decades Voltages Operation – 1mV to 10V
  - 1% max Error – 1mV to 2V
  - 2% max Error – 1mV to 10V
- Log Current or Voltage
- Antilog Voltage
- Data Compression or Expansion

GENERAL DESCRIPTION

Models 759N and 759P are low cost, fast response, dc logarithmic amplifiers offering 1% conformance to ideal log operation over four decades of current operation – 20nA to 200μA, as well as 2% conformance over four decades of voltage operation – 1mV to 10V. Featuring 200kHz bandwidth at I_{SIG} = 1μA, these new economy designs are the industry's fastest log/antilog amplifiers and offer an attractive alternative to in-house designs.

Designed for ease of use, models 759N/P are complete, temperature compensated, log or antilog amplifiers packaged in a small 1.1″ x 1.1″ x 0.4″ epoxy encapsulated module. External components are not required for logging currents over the complete six decade operating range from 1nA to 1mA. Both the scale factor (K = 2, 1, 2/3 volt/decade) and log/antilog operation can be selected by simple pin interconnection. In addition both the internal 10μA reference current as well as the offset voltage may be externally adjusted to improve overall accuracy performance.

MODEL SELECTION

Model 759N computes the log of positive input signals (voltage or current), while model 759P computes the log of negative input signals (voltage or current). In the antilog mode of operation, both models accept bipolar voltage input signals ($-2V \leqslant E_{SIG}/K \leqslant 2V$), with model 759N producing a positive output signal and model 759P producing a negative output signal.

APPLICATIONS

Model 759N and 759P can operate with either current or voltage inputs when connected as shown in Figure 1. To illustrate the logarithmic transfer characteristics, a plot of input current versus output voltage is also presented. Model 759 is ideally suited for log applications whenever low cost implementation of logarithmic natural relationships is advantages. Examples are absorbence measurements, data compression and expansion, chemical analysis of liquids, computing powers, roots and ratios and conversion of exponential quantities to linear form.

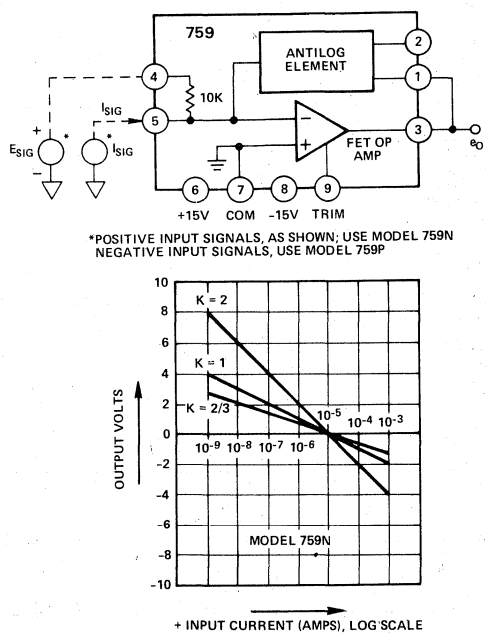


Figure 1. Functional Block Diagram and Transfer Function

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	759N/P
TRANSFER FUNCTIONS	
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$
Antilog Mode	$e_O = E_{REF}\ 10^{-\left(\frac{E_{SIG}}{K}\right)}$
TRANSFER FUNCTION PARAMETERS	
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade
Error @ +25°C	±1% max
vs. Temperature (0 to +70°C)	±0.04%/°C max
Reference Voltage (E_{REF})[2]	0.1V
Error @ +25°C	±4% max
vs. Temperature (0 to +70°C)	±0.05%/°C
Reference Current (I_{REF})[2]	10μA
Error @ +25°C	±3% max
vs. Temperature (0 to +70°C)	±0.05%/°C

LOG CONFORMITY ERROR			
I_{SIG} Range	E_{SIG} Range	R.T.I.	R.T.O. (K = 1)
20nA to 200μA	1mV to 2V	±1% max	±4.3mV max
10nA to 1mA	1mV to 10V	±2% max	±8.64mV max
1nA to 10nA		±5%	±21mV

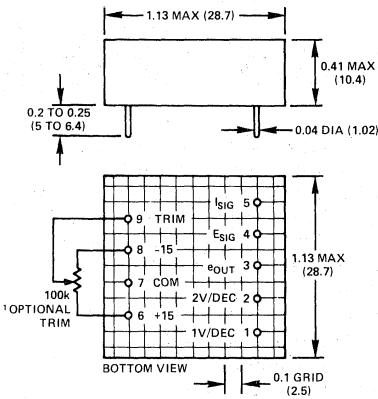
INPUT SPECIFICATIONS	
Current Signal Range	
Model 759N	+1nA to +1mA min
Model 759P	−1nA to −1mA min
Max Safe Input Current	±10mA max
Bias Current @ +25°C	(0, +) 200pA max
vs. Temperature (0 to +70°C)	x2/+10°C
Voltage Signal Range	
Model 759N	+1mV to +10V min
Model 759P	−1mV to −10V min
Offset Voltage @ +25°C (Adjustable to 0)	±2mV max
vs. Temperature (0 to +70°C)	±10μV/°C
vs. Supply Voltage	±15μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Bandwidth, −3dB	
I_{SIG} = 1nA	250Hz
I_{SIG} = 10nA	1.8kHz
I_{SIG} = 100nA	25kHz
I_{SIG} = 1μA	200kHz
I_{SIG} = 10μA	300kHz
I_{SIG} = 100μA	300kHz
I_{SIG} = 1mA	300kHz
RISE TIME	
Increasing Input Current	
10nA to 100nA	20μs
100nA to 1μA	3μs
1μA to 100μA	2.5μs
100μA to 1mA	2.5μs
Decreasing Input Current	
1mA to 100μA	3μs
100μA to 1μA	3μs
1μA to 100nA	10μs
100nA to 10nA	80μs
INPUT NOISE	
Voltage, 10Hz to 10kHz	10μV rms
Current, 10Hz to 10kHz	10pA rms
OUTPUT SPECIFICATIONS[3]	
Rated Output	
Voltage	±10V min
Current	
Log Mode	±5mA
Antilog Mode	±4mA
Resistance	0.5Ω
POWER SUPPLY[4]	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±4mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	−25°C to +85°C
Storage	−55°C to +125°C
CASE SIZE	1.125" x 1.125" x 0.4"

[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 and 2 (shorted together) for K = 2/3V/decade.
[2] Specification is + for model 759N; − for model 759P.
[3] No damage due to any pin being shorted to ground.
[4] Recommended power supply, model 904, ±15V @ ±50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

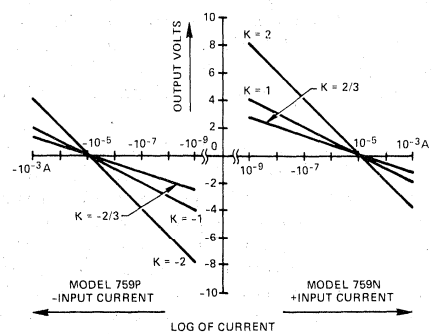
Dimensions shown in inches and (mm).



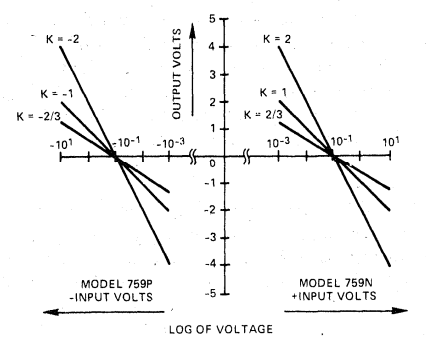
WEIGHT: 10 GRAMS
MATING SOCKET AC1016

[1] Optional 100kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±2mV maximum.

TRANSFER CURVES



Plot of Output Voltage vs Input Current for Model 759 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Model 759 Connected in the Log Mode

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{OUT} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{OUT} = \underbrace{1V \log_{10} (I_{SIG}/I_{REF})}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} (1.01)}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

	ERROR R.T.O.		
ERROR R.T.I.	K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table 1. Converting Output Error in mV to Input Error in %

SOURCES OF ERROR

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated or taken into account. Figure 2 below illustrates the log conformity performance of model 759 over a 6 decade input range. The best linearity performance is obtained in the 5 decades from 10nA to 1mA. To obtain optimum performance, the input data should be scaled to this range.

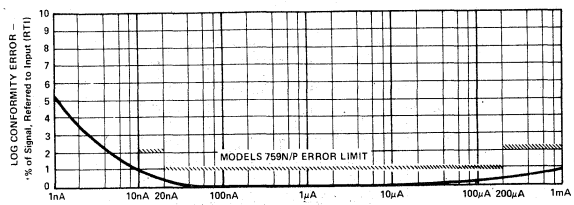


Figure 2. Log Conformity Error for Models 759N and 759P

Offset Voltage – The offset voltage, E_{os}, of model 759 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Bias Current – The bias current of model 759 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, the bias current for model 759 is 200pA, maximum.

Reference Current – I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3% referred to the input, and, from Table 1, corresponds to a dc offset of ±12.84mV for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage – E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation:
$E_{REF} = I_{REF} \times R_{IN}$, where R_{IN} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

OPTIONAL EXTERNAL ADJUSTMENTS FOR LOG OPERATION

Trimming E_{OS} – The amplifier's offset voltage, E_{OS}, may be trimmed for improved accuracy with the model 759 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3. The input terminal, Pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{OUT} = -K \log_{10} E_{OS}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for model 759N, and −3 to −4V for model 759P.

For other values of K, the trim pot should be adjusted for an output of e_{OUT} = 3 x K to 4 x K where K is the scale factor.

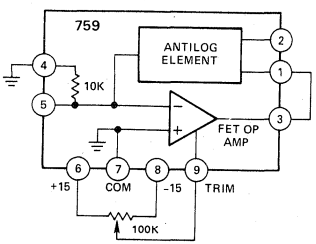


Figure 3. Trimming E_{OS} in Log Mode

Reference Current or Reference Voltage – The reference current or voltage of model 759 may be shifted by injecting a constant current into the unused scale factor terminal (Pin 1 or Pin 2). Each 330μA of current injected will shift the reference one decade, in accordance with the expression: I_I = 330μA log 10μA/I_{REF}, where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, $E_{REF} = I_{REF} \times R_{IN}$. An alternate method for rescaling E_{REF} is to connect an external R_{IN}, at the I_{IN} terminal (Pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, $E_{REF} = R_{IN} I_{REF}$. Care must be taken to choose R_{IN} such that $(e_{SIG}\ max)/R_{IN} \leqslant 1mA$.

Scale Factor (K) Adjustment – Scale factor may be increased from its nominal value by inserting a series resistor between the output terminal, Pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

RANGE OF K	CONNECT SERIES R TO PIN	VALUE OF R	NOTE
2/3V to 1.01V	1	3kΩ x (K − 2/3)	use pins 1, 2
1.01V to 2.02V	1	3kΩ x (K − 1)	use pin 1
>2.02V	2	3kΩ x (K − 2)	use pin 2

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The model 759 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} \qquad [-2 \leqslant e_{IN}/K \leqslant 2]$$

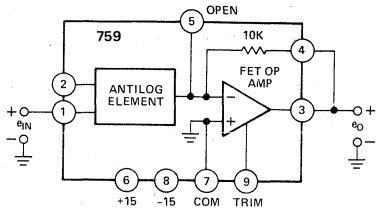


Figure 4. Functional Block Diagram

Principle of Operation – The antilog element converts the voltage input, appearing at terminal 1 or 2, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{OS}) Adjustment – Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to e_{OUT}/100. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from Pin 1 to +15V. For 759P use the same procedure but connect Pin 1 to −15V.

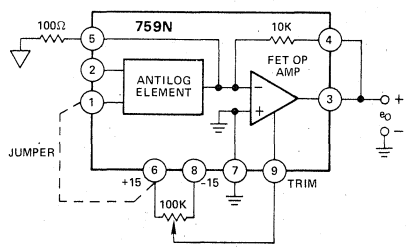


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment – In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from Pin 5 to Pin 3, in place of the internal 10kΩ. The value of R is determined by:

$$R = E_{REF}\ \text{desired}/10^{-5}\ A$$

Scale Factor (K) Adjustment – The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K, less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$$R1/R_G = (1/K - 1) \text{ where K = desired scale factor}$$

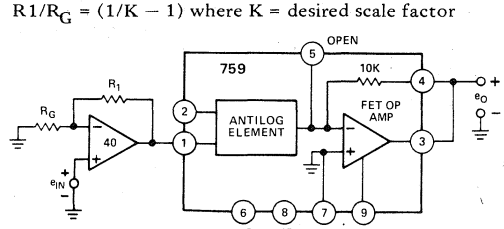


Figure 6. Method for Adjusting K<2/3V

RMS-to-DC Converters

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AD536AJ/AK/AS Monolithic IC true rms-to-dc and dB converter	6–7

6

Selection Guide
RMS-to-DC Converters

Model	Characteristics	Page
AD536AJ/AK/AS	Monolithic IC rms/dB converter. Laser-wafer-trimmed for total max error ±2mV ±0.2% of reading (AD536AK), sine waves at 1kHz (20kHz typ), 0 to 7V rms. Crest factor of 7 for 1% additional error. ±3dB bandwidth 2MHz ($1V<V_{IN}\leqslant 7V$). Averaging time constant per μF of C_{ext}, 25ms/μF. Total-error tempco (±50μV ±0.005% rdg)/°C max (AK). Additional features include dB output with 60dB range, single-or dual-supply operation, and low power consumption – 1mA. AD536AJ/K are specified for 0 to +70°C, AD536AS for -55°C to +125°C. Monolithic chips with guaranteed specifications are available for precision hybrids. A 120-page chip catalog is available upon request.	6-7

Orientation
RMS-to-DC Converters

The devices catalogued here are high-accuracy true-rms-to-dc-conversion ICs. Devices of this class compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage that is proportional to the rms of the input (and, in the case of the AD536A, an auxiliary dc voltage that is proportional to the *log* of the rms, for dB measurements).

Excellent pre-trimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of (i.e., full-wave or half-wave rectifying) a signal, filtering it, and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform and will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

Examples of applications include noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True-rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

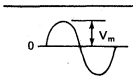
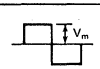
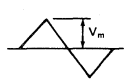
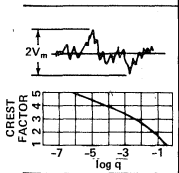
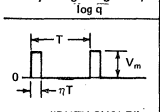
True-rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise, and acoustical noise. The electrical signals produced by these mechanical actions are often noisy, non-periodic, nonsinusoidal, and superimposed on dc levels, and require true-rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms is to take the absolute value, square it, and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_o = \text{Avg.}\left[\frac{V_{in}^2}{E_o}\right] \cong \sqrt{\text{Avg.}\,(V_{in}^2)}$$

is valid if the averaging time-constant is sufficiently long compared with the periods of the lowest-frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter, using an external filtering capacitance. Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, the data sheets show how an additional stage of 2-pole filtering is useful (the internal buffer amplifier of the AD536A permits this to be accomplished without external active elements). The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{ext}.

WAVEFORM		RMS	MAD	$\frac{\text{RMS}}{\text{MAD}}$	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0.707 V_m	$\frac{2}{\pi} V_m$ 0.637 V_m	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\sqrt{2} = 1.414$
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}} = 1.155$	$\sqrt{3} = 1.732$
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2×10^{-9}
	PULSE TRAIN η: "DUTY CYCLE"	$V_m\sqrt{\eta}$	$V_m\eta$	$\frac{1}{\sqrt{\eta}}$	$\frac{1}{\sqrt{\eta}}$
	η = 1	V_m	V_m	1	1
	η = 0.25	$0.5V_m$	$0.25V_m$	2	2
	η = 0.0625	$0.25V_m$	$0.0625V_m$	4	4
	η = 0.0156	$0.125V_m$	$0.0156V_m$	8	8
	η = 0.01	$0.1V_m$	$0.01V_m$	10	10
	MARK/SPACE η = 1 / ∞ η = 0.3333 / 0.0667 η = 0.0159 / 0.0101				

PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK.[1] In addition, useful applications information on auxiliary filtering can be found in the article "Measure RMS with Less Ripple in Less Time,"[2] and a discussion of the design of the AD536A can be found in the 1976 IEEE International Solid-State Circuits Conference *Digest of Technical Papers*, page 10.

The most-salient feature of a true rms-to-dc converter is that it ideally has no error due to an indirect approximation to the rms. Static errors are due only to scale-factor, linearity, and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error A specification for quick reference, this is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output ("% of reading"). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error-component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, external trim (adjustment) is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter.

Total Error vs. Temperature is the average change of %-of-full-scale error component plus the average change of percent of reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for ±3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal 30% of reading. It is a function of amplitude.

Crest Factor (a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case – rectangular pulse – input signal.

Filter Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance.

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation, and quiescent current drain. Note that the AD536 can be operated from single or dual supplies.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements ($T_H - 25°C$), ($25°C - T_L$), when measured.

[1] *Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete Master-Charge data to P.O. Box 796, Norwood MA 02062

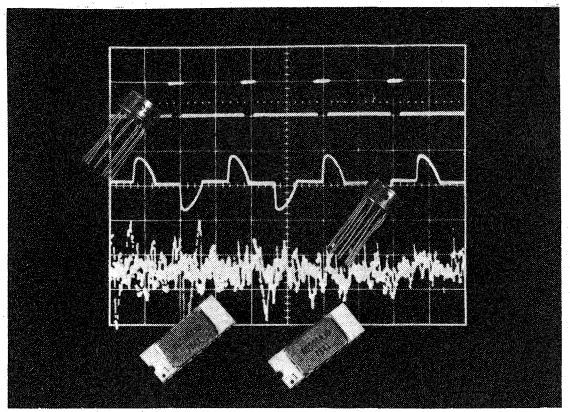
[2] ANALOG DIALOGUE 9-3, 1975, pp 21-22

Integrated Circuit True rms-to-dc Converter

AD536A

FEATURES

- True rms-to-dc Conversion
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 300kHz Bandwidth: $V_{rms} > 100mV$
  - 2MHz Bandwidth: $V_{rms} > 1V$
  - Signal Crest Factor of 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- -55°C to +125°C Operation (AD536AS)
- Low Cost



PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the full -55°C to +125°C military range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or a 10-pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536, and provides improved bandwidth and temperature drift specifications.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD536AJ	AD536AK	AD536AS
TRANSFER EQUATION	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	*	*
CONVERSION ACCURACY			
Total Error, Internal Trim[1] (Fig. 1)	±5mV ±0.5% of Reading, max	±2mV ±0.2% of Reading, max	*
vs. Temperature, T_{min} to +70°C	±(0.1mV ±0.01% Reading)/°C max	±(0.05mV ±0.005% of Reading)/°C max	±(0.1mV ±0.005% of Reading)/°C max
+70°C to +125°C	—	—	±(0.3mV ±0.005% of Reading)/°C max
vs. Supply Voltage	±(0.1mV ±0.01% Reading)/V	*	*
dc Reversal Error	±0.05% of Reading	*	*
Total Error, External Trim[1] (Fig. 2)	±3mV ±0.3% of Reading	±2mV ±0.1% of Reading	*
ERROR vs CREST FACTOR[2]			
Crest Factor 1 to 2	Specified Accuracy	*	*
Crest Factor = 3	−0.1% of Reading	*	*
Crest Factor = 7	−1% of Reading	*	*
FREQUENCY RESPONSE[3]			
Bandwidth for 1% additional error (0.1dB)			
$10mV < V_{IN} \leq 100mV$	6kHz	*	*
$100mV < V_{IN} \leq 1V$	40kHz	*	*
$1V < V_{IN} \leq 7V$	100kHz	*	*
±3dB Bandwidth			
$10mV < V_{IN} \leq 100mV$	50kHz	*	*
$100mV < V_{IN} \leq 1V$	300kHz	*	*
$1V < V_{IN} \leq 7V$	2MHz	*	*
AVERAGING TIME CONSTANT (Fig. 5)	25ms/μF C_{AV}	*	*
INPUT CHARACTERISTICS			
Signal Range, ±15V Supply	±20V Peak	*	*
Signal Range, +5V Supply	±5V Peak	*	*
Safe Input, All Supply Voltages	±25V max	*	*
Input Resistance	16.7kΩ ±25%	*	*
Input Offset Voltage	±2mV max	±1mV max	*
OUTPUT CHARACTERISTICS			
Offset Voltage	±2mV max	±1mV max	*
vs. Temperature	±0.1mV/°C	*	±0.2mV/°C max
vs. Supply Voltage	±0.1mV/V	*	±0.2mV/V max
Voltage Swing, ±15V Supplies	0 to +10V min	*	*
±5V Supply	0 to +2V min	*	*
Output Current	(+5mA, −130μA) min	*	*
Short Circuit Current	+20mA	*	*
Resistance	0.5Ω max	*	*
dB OUTPUT (Fig. 13)			
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms	±0.5dB	±0.2dB	*
Scale Factor	−3mV/dB	*	*
Scale Factor TC (Uncompensated, see Fig. 13 for Temperature Compensation)	−0.3% Reading/°C (−0.03dB/°C)	*	*
I_{REF} for 0dB = 1V rms	20μA (5μA min, 80μA max)	*	*
I_{REF} Range	1μA to 100μA	*	*
I_{OUT} TERMINAL			
I_{OUT} Scale Factor	40μA/Volt rms	*	*
I_{OUT} Scale Factor Tolerance	±25%	*	*
Output Resistance	$10^8\Omega$	*	*
Voltage Compliance	$-V_S$ to $(+V_S - 2.5V)$	*	*
BUFFER AMPLIFIER			
Input and Output Voltage Range	$-V_S$ to $(+V_S - 2.5V)$min	*	*
Input Offset Voltage, R_S = 25k	±4mV max	*	*
Input Current	100nA typ, 300nA max	*	*
Input Resistance	$10^8\Omega$	*	*
Output Current	(5mA, −130μA) min	*	*
Short Circuit Current	+20mA	*	*
Small Signal Bandwidth	1MHz	*	*
Slew Rate[4]	5V/μs	*	*
POWER SUPPLY			
Voltage, Rated Performance			
Dual Supply	±3.0V to ±18V	*	*
Single Supply	+5V to +36V	*	*
Quiescent Current			
Total V_S 5V to 36V, T_{min} to T_{max}	2mA max (1mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−55°C to +150°C	*	*

[1] Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.
[2] Error vs crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.
[3] Input voltages are expressed in volts rms, and error is percent of reading.
[4] With 2k external pulldown resistor.

*Specifications same as AD536AJ.

Specifications subject to change without notice.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 17. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input, positive out.

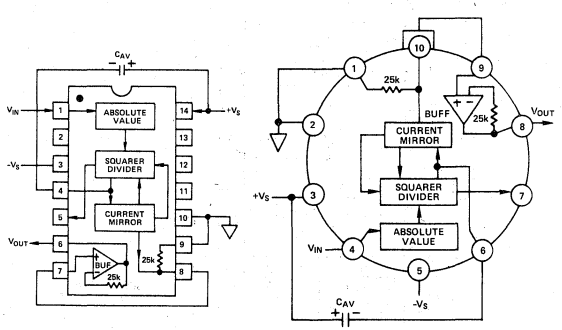


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 249Ω in series with the internal 25kΩ resistor. This will cause a 1% increase in scale factor, which is trimmed out by using R_1 as shown.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range.

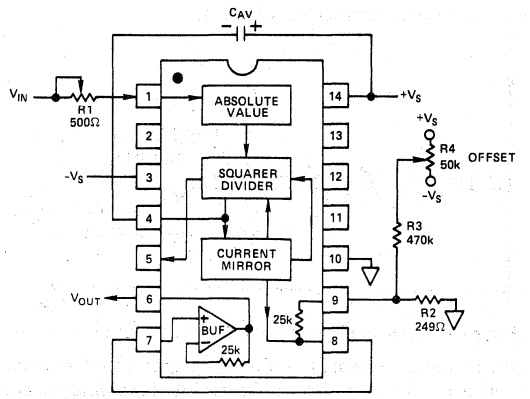


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into pin 10 (pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 17. The load resistor, R_L, is necessary to provide output sink current.

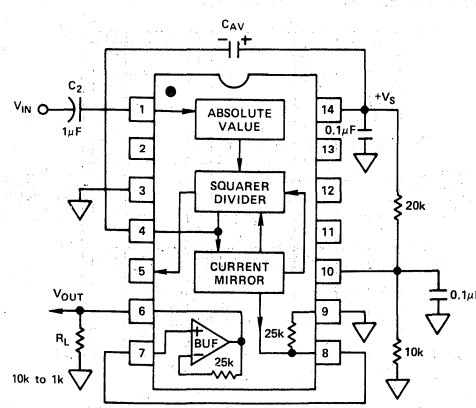


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by an average (or dc) error and some amount of ripple, as demonstrated in Figure 4.

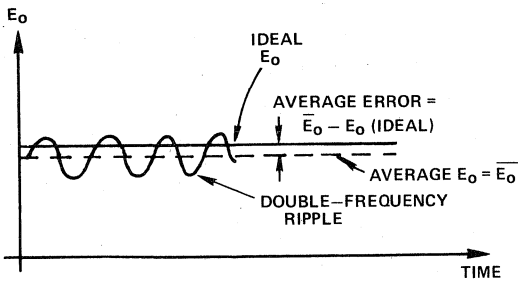


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% dc error above a given frequency. For example, if a 60Hz waveform is to be measured with a dc error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

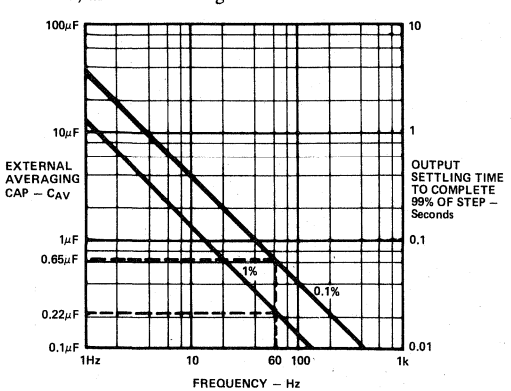


Figure 5. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

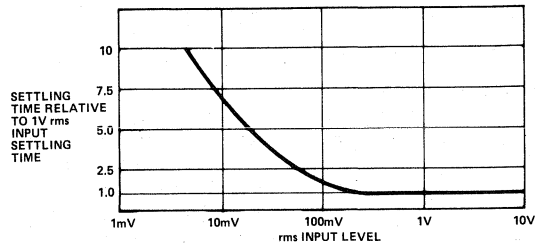


Figure 6. Settling Time vs Input Level

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 2.2μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

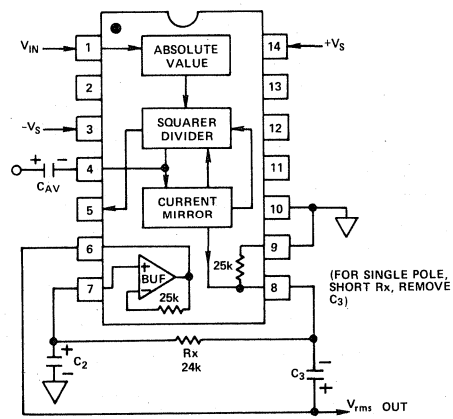


Figure 7. 2 Pole "Post" Filter

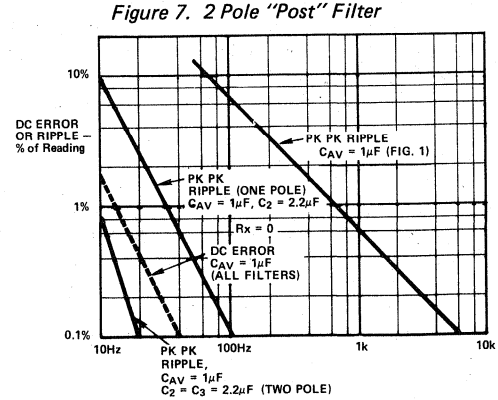


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN} \text{ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

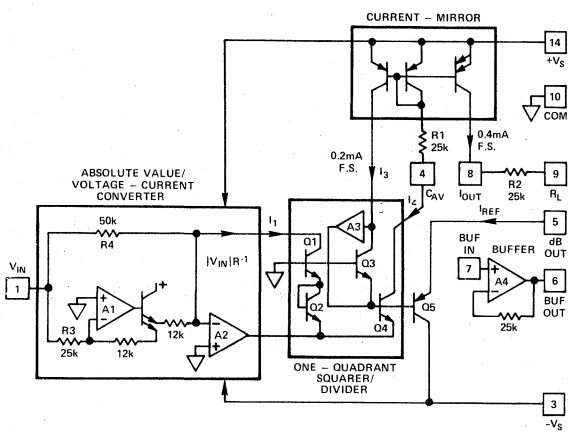
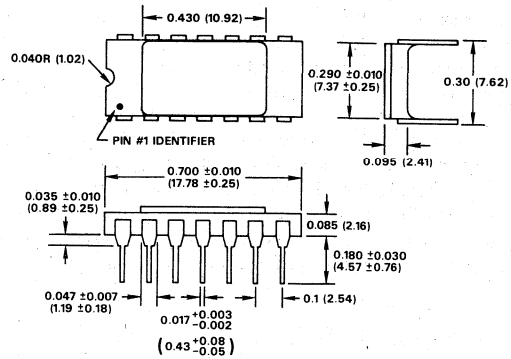


Figure 9. Simplified Schematic

"D" PACKAGE (TO-116)



"H" PACKAGE (TO-100)

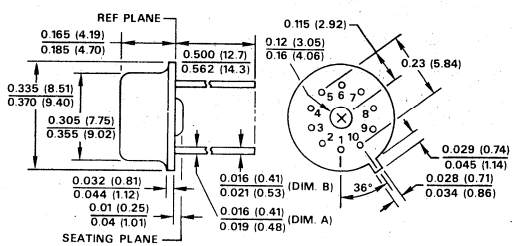
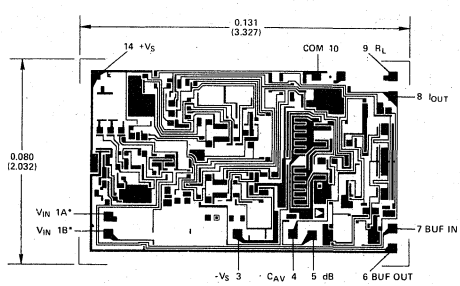


Figure 10. Physical Dimensions
Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14 PIN CERAMIC DIP PACKAGE.

NOTE:
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.

THE AD536A IS AVAILABLE IN LASER-TRIMMED CHIP FORM. CONSULT ANALOG DEVICES' CHIP CATALOG FOR SPECIFICATIONS AND APPLICATION DETAILS.

Figure 11. Chip Dimensions and Pad Layout.
Dimensions shown in inches and (mm).

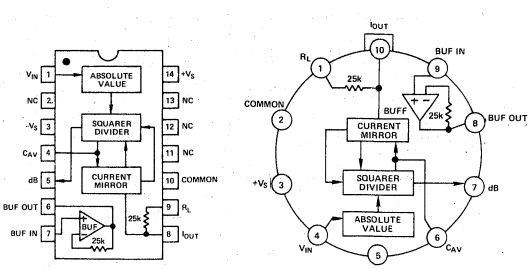


Figure 12. AD536A Pin Connections and Functional Diagram

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A, which is not available in any other computing rms circuit, is the logarithmic or decibel output. The internal circuit which computes dB is very accurate and works well over a 60dB range. The connection for dB measurements is shown in Figure 13. The user selects the 0dB level by setting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor, R_3, is available from Tel Labs, Londonderry, NH, type number Q-81. The linear rms output is available at pin 8 with an output impedance of 25kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc
4. Adjust R_2 for dB out = -2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_2 for the proper gain automatically gives the correct temperature compensation.

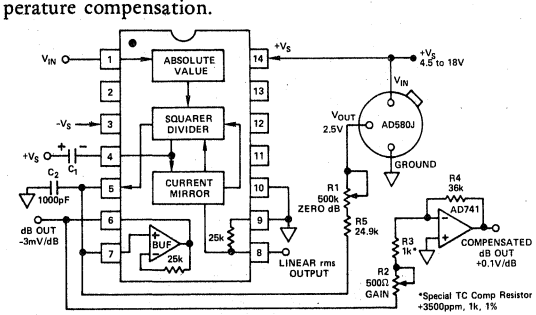


Figure 13. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 100kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to only 6kHz.

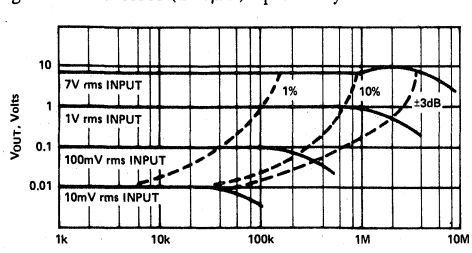


Figure 14. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 15 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 10. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

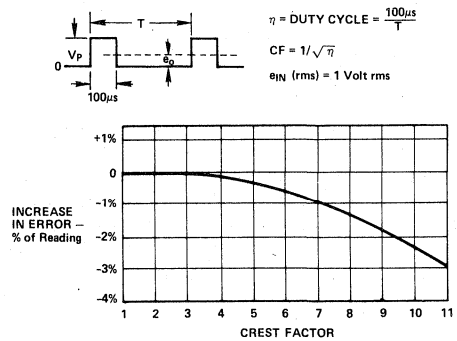


Figure 15. Error vs. Crest Factor

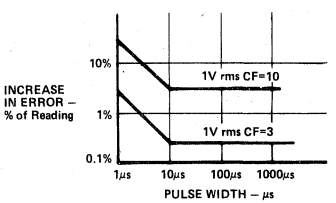


Figure 16. AD536A Error vs. Pulse Width Rectangular Pulse

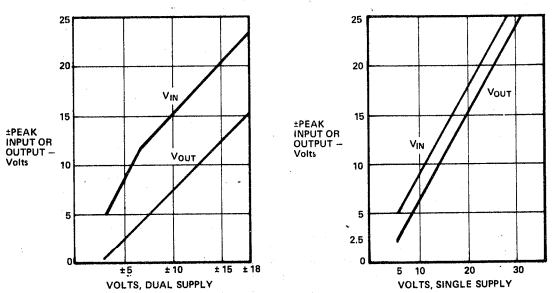


Figure 17. AD536A Input and Output Voltage Ranges vs. Supply

Voltage References

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●New product since the 1979 *Data Acquisition Products Catalog Supplement.*

7

Selection Guide
Voltage References

In this Selection Guide, Voltage-Reference families are divided into four categories:

1. Pin-Programmable Multiple-Voltage Monolithic References
2. 10V Monolithic and Hybrid References
3. 2.5V Monolithic References
4. 1.2V Monolithic References

The specifications and features are key for each device. Complete and detailed descriptions, specifications, and application information can be found on the data sheets. Definitions of important specifications can be found below and on the next page.

All specifications are typical at 15V supply, connected for the voltage-in, voltage-out mode, and +25°C, unless noted otherwise—except for the two-terminal AD589 (500μA, +25°C). J/K/L/M suffixes denote 0 to +70°C operation, S/T/U −55°C to +125°C.

1. PIN-PROGRAMMABLE MULTIPLE-VOLTAGE MONOLITHIC REFERENCES

Voltage	Device Family	Characteristics	Page
10, 7.5, 5, 2.5	AD584J/K/L/S/T/U#	Monolithic, laser-trimmed to provide four programmable values of output voltage: 10.000V, 7.500V, 5.000V, 2.500V, with max error of ±5mV, ±4mV, ±3mV, ±2.5mV (L version) and max tempco of 5ppm/°C (L version on 10V, 7.5V, 5V ranges). Other values of voltage available by connection of external resistors. Can be used in 2-terminal connection as high-performance "Zener Diode" for negative reference (>|5V|) or as a current limiter. Simultaneous outputs available with external buffering.	7-15

2. 10V MONOLITHIC AND HYBRID REFERENCES

Voltage	Device Family	Characteristics	Page
10	AD581J/K/L/S/T/U#	Monolithic 3-terminal laser-trimmed 10.000V ±5mV (L, U) @ 10mA voltage reference. Tempcos trimmed to within 5ppm/°C max (0 to +70°C—L), and 10ppm/°C max (−55°C to +125°C—U). Can be used in 2-terminal connection as high-performance "Zener Diode" for positive or negative reference voltage.	7-9
	AD2700J/L/S	Hybrid high-accuracy +10V ±2.5mV (L, U) @ 10mA, 3ppm/°C (L, S, U)	7-29
	AD2701J/L/S	Hybrid high-accuracy −10V ±2.5mV (L, U) @ 10mA, 3ppm/°C (L, S, U)	7-29
	AD2702J/L/S	Hybrid high-accuracy dual ±10V ±2.5mV (L, U) @ 10mA, 3ppm/°C (U)	7-29

3. 2.5V MONOLITHIC REFERENCES

Voltage	Device Family	Characteristics	Page
+2.5	AD580JH/KH/LH/MH/SH/TH/UH#	Monolithic 3-terminal 2.5V @ 10mA reference. Output voltage to within ±0.4% (M, U), better than 3mV line regulation (4.5V to 30V – L, M, T, U), 10mV max load regulation (10mA change), and 10ppm/°C change with temperature (M, U).	7-5
	AD1403/AD1403A#●	Monolithic 3-terminal 2.5V @ 10mA reference; Improved low-cost replacement for standard 1403/1403A; Laser-trimmed to 2.500V ±10mV (max – 1403A); Temperature stability to within 25ppm/°C max (1403A – 0 to 70°C); Quiescent current 1.5mA max; Mini-DIP package.	7-25

4. 1.2V MONOLITHIC REFERENCES

Voltage	Device Family	Characteristics	Page
1.2	AD589JH/KH/LH/MH SH/TH/UH#●	Monolithic two-terminal 1.23V bandgap "Zener Diode"; Superior replacement for other 1.2V references; Operating range 50μA to 5mA; Tempco 10ppm/°C max, 0 to 70°C (M), 25ppm/°C max, -55°C to +125°C (U); Low output impedance, 0.6Ω, low dissipation, 60μW total at 50μA; No frequency compensation required.	7-21

#Monolithic chips with guaranteed specs available for precision hybrids. Information available upon request.
All but AD1403/A and the AD589 family can be found in the 1979 chip catalog, available upon request.

●New product since the 1979 *Data Acquisition Products Catalog Supplement.*

Orientation
Voltage References

A voltage reference is used to provide an accurately known voltage which can be utilized in a circuit or system. For example, measurement systems rely on precision references in order to establish a basis for absolute measurement accuracy. Any reference inaccuracy will undermine the accuracy of the overall system. Thus, ideal references are characterized by accurately set (and traceable to recognized fundamental standards) constant output voltage, independent of temperature, load changes, input voltage variation, and time.

Types of References

The majority of available IC reference circuits use the bandgap principle: the V_{BE} of any silicon transistor has a negative tempco of about 2mV/°C, which can be extrapolated to approximately 1.2 volts at absolute zero (the *bandgap* voltage of silicon). Since identical transistors operating at constant current densities will have predictably different temperature coefficients of base-emitter voltage, it is possible to arrange circuit elements so as to null out the temperature coefficients associated with the two phenomena and produce a constant voltage (usually 1.2 volts). This temperature-invariant voltage can be amplified and buffered to produce a standard voltage value, such as 2.5V or 10.0V. The bandgap types catalogued here include the AD1403 and the AD580 (2.5V), the AD581 (10.0V), and the multi-output AD584 (2.5, 5.0, 7.5, and/or 10.0V).

Another popular form of reference circuit uses a selected low-drift Zener diode, followed by a buffer-amplifier-and-precision-gain stage to provide a standard output voltage. The AD2700/AD2701/AD2702 families provide +10V, −10V, and ±10V (dual output) using this technique. Laser-trimmed thin-film resistors are essential to secure ±2.5mV accuracy and ±3ppm/°C max drift in these hybrid devices.

The AD589 family are two-terminal 1.2V bandgap ICs used like Zener diodes. They are ideally suited to battery-powered instruments or portable equipment where low power consumption (and often low supply voltages) are essential. Power requirements as low as 60μW, combined with low temperature drift, provide precision performance at low cost.

Definitions of Specifications

Line regulation. The change in output voltage due to a specified change in input voltage. It is usually expressed in percent per volt or microvolts per volt of input change.

Load regulation. The change in output voltage for a specified change in load current. It is generally expressed in microvolts per milliampere, or ohms of dc output resistance. This specification includes the effect of self-heating due to increased power dissipation at higher load currents.

Output voltage tolerance. The deviation from the nominal output voltage at 25°C and specified input voltage as measured by a device traceable to a recognized fundamental voltage standard.

Output voltage change with temperature. The change in output voltage from the value at 25°C ambient; it is independent of variations in the other operating conditions. Analog Devices specifies both an error band and an equivalent temperature coefficient (in ppm/°C) for most references. The error band (e.g., ±5mV, −55°C to +125°C), is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{max} and 25°C to T_{min}, with a slope equal to the stated temperature coefficient. Thus, the total absolute error for a particular reference over its specified temperature range is equal to the output voltage tolerance at 25°C plus the error band.

Turn-on settling time. The time, from a cold start, for the reference output to settle within a specified error band. This definition relates only to the electrical turn-on of the chip, and does not include thermal settling time, which depends on the package, heat-sinking, and load-current change.

ANALOG DEVICES

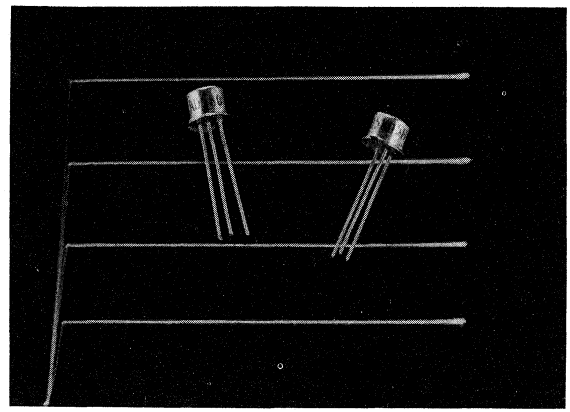
High Precision 2.5 Volt IC Reference

AD580

IMPROVED PERFORMANCE

FEATURES

- Laser Trimmed to Higher Accuracy: 2.500V ±0.4%, Improved from ±1.0% (AD580M)
- 3-Terminal Device: Voltage In/Voltage Out
- Excellent Temperature Stability: 10ppm/°C (AD580M, U)
- Excellent Long Term Stability: 250μV (25μV/Month)
- Low Quiescent Current: 1.0mA max
- Small, Hermetic IC Package: TO-52 Can
- 10mA Current Output Capability
- Low Cost
- 3 MIL Temperature Grades (-55°C to +125°C) with MIL-STD-883, Class B Processing Available



PRODUCT DESCRIPTION

The AD580 is an improved three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output voltage for inputs between 4.5V and 30V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provide the AD580 with an improved initial tolerance of ±0.4%, a temperature stability of better than 10ppm/°C and long term stability of better than 250μV. In addition, the low quiescent current drain of 1.0mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580 allows operation with 5 volt logic supplies making the AD580 ideal for digital panel meter applications or whenever only a single logic power supply is available.

The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Laser-trimming the thin-film resistors has reduced the AD580 output error. For example, AD580K output tolerance is now ±10mV, improved from ±50mV.
2. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
3. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for systems that contain a single logic power supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities to 10ppm/°C and long term stability better than 250μV.
5. The low quiescent current drain of the AD580 makes it ideal for CMOS and other low power applications.
6. The three grades of AD580 rated for operation over the -55°C to +125°C "military" temperature range are available with processing to MIL-STD-883, Class B.

OTHER ANALOG DEVICES REFERENCES

AD1403/AD1403A	Industry Standard 2.5 Volt IC Reference
AD581	High Precision 10 Volt IC Reference
AD584	Pin Programmable Precision IC Voltage Reference
AD589	Two Terminal 1.2 Volt IC Reference
AD2700	High Performance +10.000 Volt Reference
AD2701	High Performance -10.000 Volt Reference
AD2702	High Performance Tracking ±10.000 Volt Reference

SPECIFICATIONS (typical @ E_{in} and 25°C unless otherwise specified)

MODEL	AD580JH	AD580KH	AD580LH	AD580MH
ABSOLUTE MAXIMUM RATINGS				
Input Voltage	40V E_{IN}	*	*	*
Power Dissipation @ +25°C				
Ambient Temperature	350mW	*	*	*
Derate Above +25°C	2.8mW/°C	*	*	*
Operating Junction Temperature Range	-55°C to +150°C	*	*	*
Storage Temperature Range	-65°C to +175°C	*	*	*
Lead Temperature (Soldering, 10 sec)	+300°C	*	*	*
Thermal Resistance				
Junction-to-Case	100°C/W	*	*	*
Junction-to-Ambient	360°C/W	*	*	*
Specified Operating Temperature Range	0 to +70°C	*	*	*
OUTPUT VOLTAGE TOLERANCE				
(Error from Nominal 2.500 Volt Output)	±75mV max	±25mV max	±10mV max	±10mV max
OUTPUT VOLTAGE CHANGE				
T_{min} to T_{max}	15mV max (85ppm/°C)	7mV max (40ppm/°C)	4.3mV max (25ppm/°C)	1.75mV max (10ppm/°C)
LINE REGULATION				
$7V \leqslant V_{IN} \leqslant 30V$	6mV max (1.5mV typ)	4mV max (1.5mV typ)	2mV max	2mV max
$4.5 \leqslant V_{IN} \leqslant 7V$	3mV max (0.3mV typ)	2mV max (0.3mV typ)	1mV max	1mV max
LOAD REGULATION				
ΔI = 10mA	10mV max	*	*	*
QUIESCENT CURRENT	1.5mA max (1.0mA typ)	*	*	*
NOISE (0.1Hz to 10Hz)	60μV (p-p)	*	*	*
STABILITY				
Long Term	250μV	*	*	*
Per Month	25μV	*	*	*

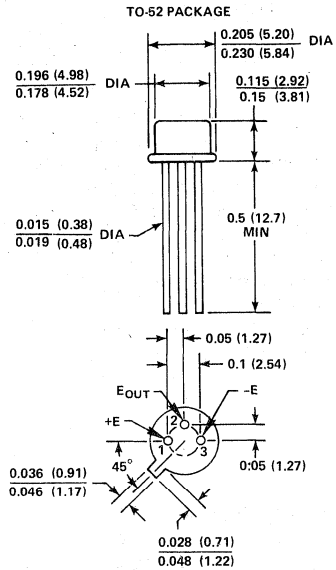
MODEL	AD580SH (AD580SH/883B)[1]	AD580TH (AD580TH/883B)[1]	AD580UH (AD580UH/883B)[1]
ABSOLUTE MAXIMUM RATINGS			
Input Voltage	40V E_{IN}	**	**
Power Dissipation @ +25°C			
Ambient Temperature	350mW	**	**
Derate Above +25°C	2.8mW/°C	**	**
Operating Junction Temperature Range	-55°C to +150°C	**	**
Storage Temperature Range	-65°C to +175°C	**	**
Lead Temperature (Soldering, 10 sec)	+300°C	**	**
Thermal Resistance			
Junction-to-Case	100°C/W	**	**
Junction-to-Ambient	360°C/W	**	**
Specified Operating Temperature Range	-55°C to +125°C	**	**
OUTPUT VOLTAGE TOLERANCE			
(Error from Nominal 2.500 Volt Output)	±25mV max	±10mV max	±10mV max
OUTPUT VOLTAGE CHANGE			
T_{min} to T_{max}	25mV max (55ppm/°C)	11mV max (25ppm/°C)	4.5mV max (10ppm/°C)
LINE REGULATION			
$7V \leqslant V_{IN} \leqslant 30V$	6mV max (1.5mV typ)	2mV max	2mV max
$4.5 \leqslant V_{IN} \leqslant 7V$	3mV max (0.3mV typ)	1mV max	1mV max
LOAD REGULATION			
ΔI = 10mA	10mV max	**	**
QUIESCENT CURRENT	1.5mA max (1.0mA typ)	**	**
NOISE (0.1Hz to 10Hz)	60μV (p-p)	**	**
STABILITY			
Long Term	250μV	**	**
Per Month	25μV	**	**

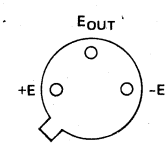
*Specifications same as AD580JH
**Specifications same as AD580SH
[1]The AD580SH, TH and UH are available fully processed and screened to the requirements of MIL-STD-883, Class B. When ordering, specify AD580XH/883B. Prices are in parenthesis ( ).

Specifications and prices subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

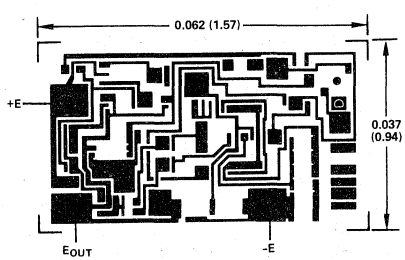




BOTTOM VIEW

CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



The AD580 is also available in chip form. Consult the factory for specifications and applications information.

THEORY OF OPERATION

Most precision IC references use complex multichip hybrid designs based on expensive temperature-compensated zener diodes. Others are monolithic with on-chip zener diodes; these often require more than one power supply and, with the zener breakdown occuring near 6.3 volts, will not operate from a low voltage logic supply.

The AD580 family (AD580, AD581, AD584, AD589) uses the "bandgap" concept to produce a stable, low-temperature-coefficient voltage reference suitable for high accuracy data-acquisition components and systems. The device makes use of the underlying physical nature of a silicon transistor base-emitter voltage in the forward-biased operating region. All such transistors have approximately a $-2mV/^{\circ}C$ temperature coefficient, unsuitable for use directly as a low TC reference; however, extrapolation of the temperature characteristic of any one of these devices to absolute zero (with emitter current proportional to absolute temperature) reveals that it will go to a V_{BE} of 1.205 volts $0^{\circ}K$, as shown in Figure 1. Thus, if a voltage could be developed with an opposing temperature coefficient to sum with V_{BE} to total 1.205 volts, a zero-TC reference would result and operation from a single, low-voltage supply would be possible. The AD580 circuit provides such a compensating voltage, V_1 in Figure 2, by driving two transistors at different current densities and amplifying the resulting V_{BE} difference (ΔV_{BE} – which now has a positive TC); the sum (V_Z) is then buffered and amplified up to 2.5 volts to provide a usable reference-voltage output. Figure 3 is the schematic diagram of the AD580.

The AD580 operates as a three-terminal reference, that means that no additional components are required for biasing or current setting. The connection diagram, Figure 4 is quite simple.

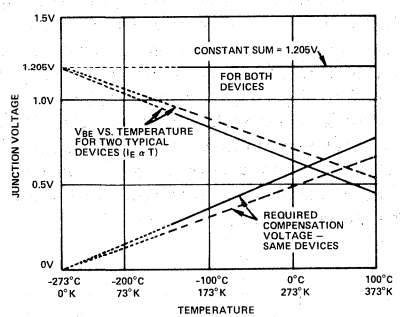


Figure 1. Extrapolated Variation of Base-Emitter Voltage with Temperature ($I_E \alpha T$), and Required Compensation, Shown for Two Different Devices

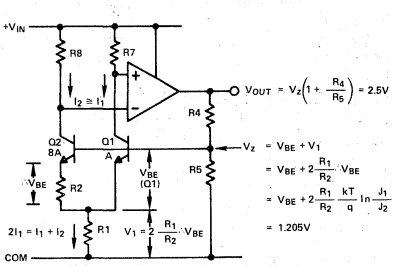


Figure 2. Basic Bandgap-Reference Regulator Circuit

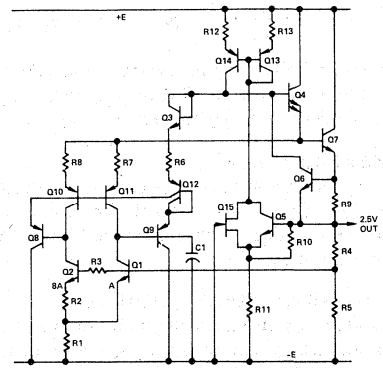


Figure 3. AD580 Schematic Diagram

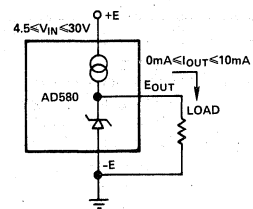


Figure 4. AD580 Connection Diagram

VOLTAGE VARIATION VS. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD580 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

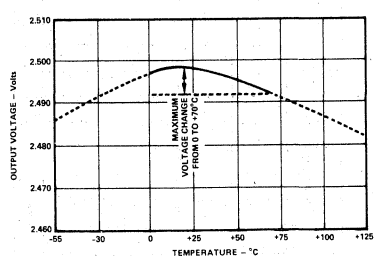


Figure 5. Typical AD580K Output Voltage vs. Temperature

The AD580M guarantees a maximum deviation of 1.75mV over the 0 to +70°C temperature range. This can be shown to be equivalent to 10ppm/°C average maximum; i.e. . .

$$\frac{1.75\text{mV max}}{70^\circ\text{C}} \times \frac{1}{2.5\text{V}} = 10\text{ppm}/^\circ\text{C max average}$$

The AD580 typically exhibits a variation of 1.5mV over the power supply range of 7 to 30 volts. Figure 6 is a plot of AD580 line rejection versus frequency.

NOISE PERFORMANCE

Figure 7 represents the peak-to-peak noise of the AD580 from 1Hz (3dB point) to a 3dB high end shown on the horizontal axis. Peak-to-peak noise from 1Hz to 1MHz is approximately 600μV.

THE AD580 AS A CURRENT LIMITER

The AD580 represents an excellent alternative to current limiter diodes which require factory-selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD580 approach is not limited to a specially selected factory set current limit; it can be programmed from 1 to 10mA with the insertion of a single external resistor. The approximate temperature coefficient of current limit for the AD580 used in this mode is 0.13%/°C for I_{LIM} = 1mA and 0.01%/°C for I_{LIM} = 13mA (see Figure 9). Figure 8 displays the high output impedance of the AD580 used as a current limiter for I_{LIM} = 1, 2, 3, 4, 5mA.

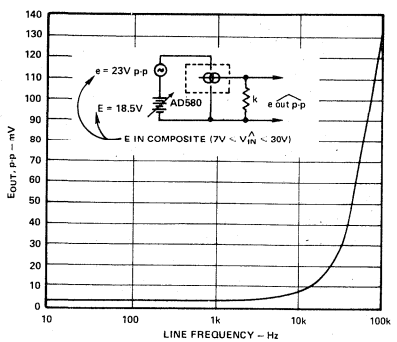


Figure 6. AD580 Line Rejection Plot

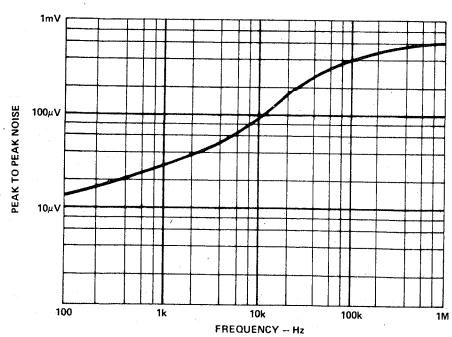


Figure 7. Peak-to-Peak Output Noise vs. Frequency

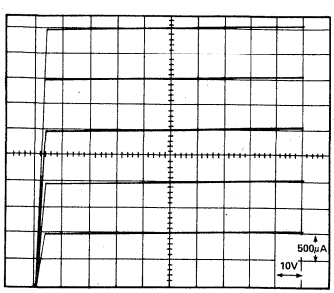


Figure 8. Input Current vs. Input Voltage (Integral Loads)

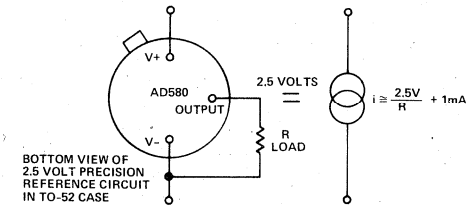


Figure 9. A Two-Component Precision Current Limiter

THE AD580 AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD580 has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

Figure 10 shows the AD580 used as a reference for the AD7542 12-bit CMOS DAC with complete microprocessor interface. The AD580 and the AD7542 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7542 includes three 4-bit data registers, a 12-bit DAC register, and address decoding logic; it may thus be interfaced directly to a 4-, 8- or 16-bit data bus. Only 8mA of quiescent current from the single +5 volt supply is required to operate the AD7542 which is packaged in a small 16-pin DIP. The AD544 output amplifier is also low power, requiring only 2.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7542KN without user trims and it typically settles to ±1/2 LSB in less than 3μs. It will provide the 0 to -2.5 volt output swing from ±5 volt supplies.

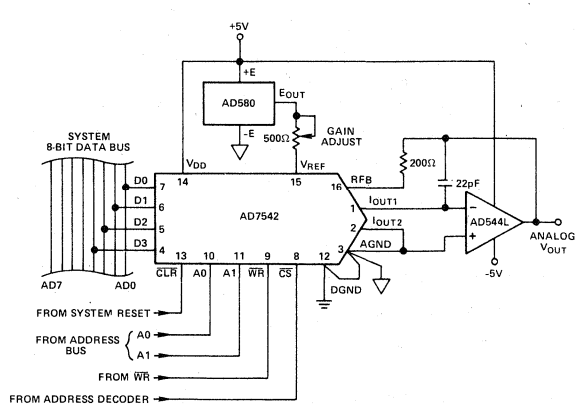


Figure 10. Low Power, Low Voltage Reference for the AD7542 Microprocessor-Compatible 12-Bit DAC

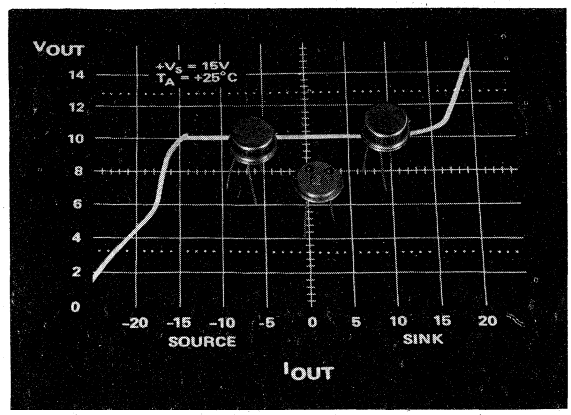
ANALOG DEVICES

High Precision 10 Volt IC Reference

AD581

FEATURES

- Laser-Trimmed to High Accuracy:
  - 10.000 Volts ±5mV (L and U)
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (L)
  - 10ppm/°C max, -55°C to +125°C (U)
- Excellent Long-Term Stability:
  - 25ppm/1000 hrs. (Non-Cumulative)
- Negative 10 Volt Reference Capability
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- 3-Terminal TO-5 Package
- Low Cost



PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 40 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. The AD581S, T, and U grades are also available processed to MIL-STD-883A, Level B. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 12 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.
5. Every AD581 receives a 24 hour stabilization bake at +150°C, a gross leak test and a 48 hour burn-in at +125°C to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ V_{IN} = +15V and +25°C unless otherwise noted)

MODEL	AD581J	AD581K	AD581L	AD581S	AD581T	AD581U
ABSOLUTE MAX RATINGS						
Input Voltage V_{IN} to Ground	40V	*	*	*	*	*
Power Dissipation @ +25°C	600mW	*	*	*	*	*
Operating Junction Temp. Range	-55°C to +150°C	*	*	*	*	*
Storage Temperature Range	-65°C to +175°C	*	*	*	*	*
Lead Temperature (Soldering, 10sec)	+300°C	*	*	*	*	*
Thermal Resistance Junction-to-Ambient	150°C/Watt	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	-55°C to +125°C	**	**
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10.000V output)	±30mV max	±10mV max	±5mV max	±30mV max	±10mV max	±5mV max
OUTPUT VOLTAGE CHANGE Maximum Deviation from +25°C Value T_{min} to T_{max} (Temperature Coefficient)	±13.5mV (30ppm/°C)	±6.75mV (15ppm/°C)	±2.25mV (5ppm/°C)	±30mV (30ppm/°C)	±15mV (15ppm/°C)	±10mV (10ppm/°C)
LINE REGULATION $15V \leq V_{IN} \leq 30V$	3mV max (0.002%/V)	*	*	*	*	*
$13V \leq V_{IN} \leq 15V$	1mV max (0.005%/V)	*	*	*	*	*
LOAD REGULATION $0 \leq I_{OUT} \leq 5mA$	500µV/mA max	*	*	*	*	*
	200µV/mA typ	*	*	*	*	*
QUIESCENT CURRENT	1.0mA max	*	*	*	*	*
	750µA typ	*	*	*	*	*
TURN-ON SETTLING TIME TO 0.1%[1]	200µs	*	*	*	*	*
NOISE (0.1 to 10Hz)	50µV p-p	*	*	*	*	*
LONG-TERM STABILITY	25ppm/1000 Hrs. (Non-Cumulative)	*	*	*	*	*
SHORT CIRCUIT CURRENT	30mA	*	*	*	*	*
OUTPUT CURRENT						
Source @ +25°C	10mA min	*	*	*	*	*
Source T_{min} to T_{max}	5mA min	*	*	*	*	*
Sink T_{min} to T_{max}	5mA min	*	*	200µA min	**	**
Sink -55°C to +85°C	—	—	—	5mA min	**	**

*Specifications same as AD581J.
**Specifications same as AD581S.
[1] See Figure 8.

Specifications subject to change without notice.

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 40 volts.

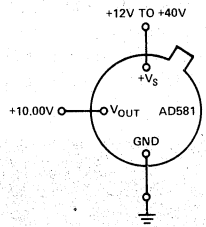
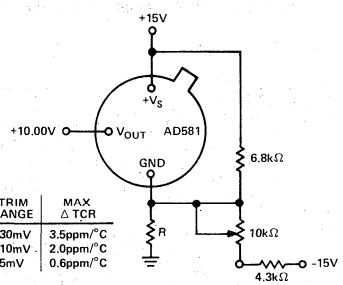


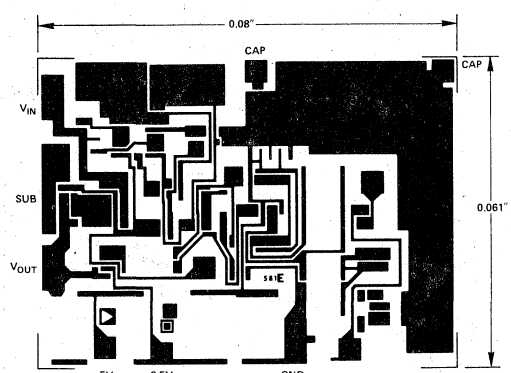
Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.



R	TRIM RANGE	MAX Δ TCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration



THE AD581 IS ALSO AVAILABLE IN LASER-TRIMMED CHIP FORM WITH ALL SPECIFICATIONS GUARANTEED TO J-GRADE. THE CHIP HAS ADDITIONAL APPLICATION FLEXIBILITY NOT AVAILABLE IN THE THREE-TERMINAL PACKAGED DEVICE. CONSULT FACTORY FOR FURTHER DETAILS.

Figure 3. AD581 Bonding Diagram

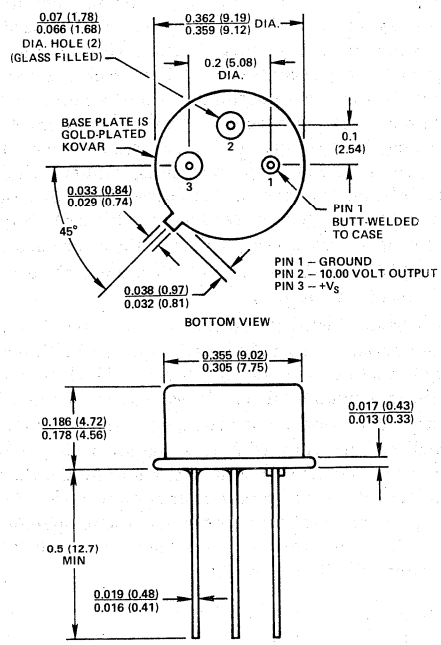


Figure 4. Outline Dimensions and Pin Designations. Dimensions shown in inches and (mm).

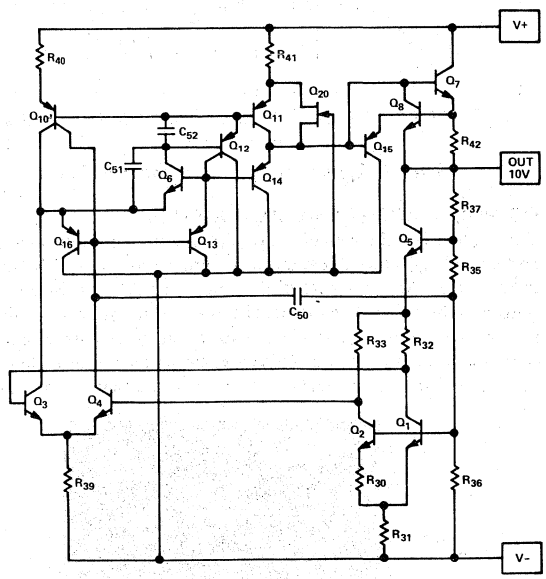


Figure 5. Simplified Schematic

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 6. Five-point measurement of each device guarantees the error band over the −55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from −55°C to +125°C).

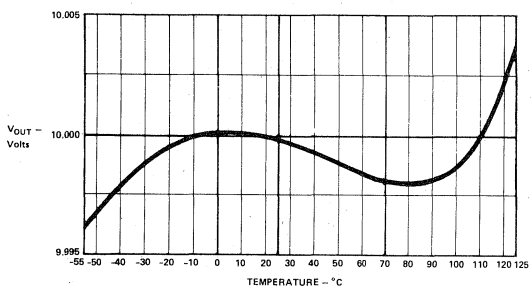


Figure 6. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 7. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

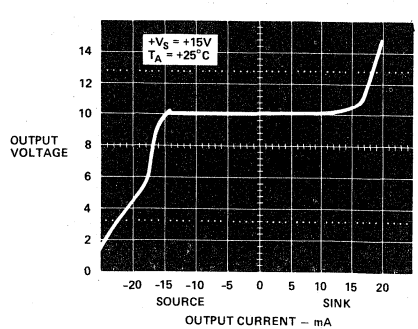


Figure 7. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 8 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

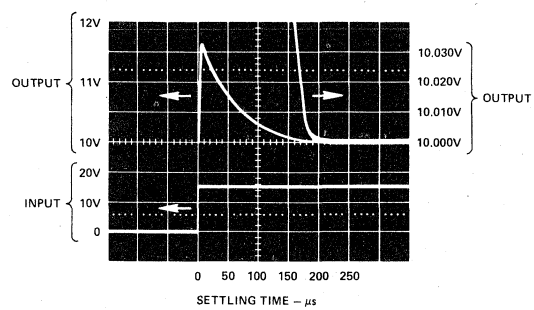


Figure 8. Output Settling Characteristic

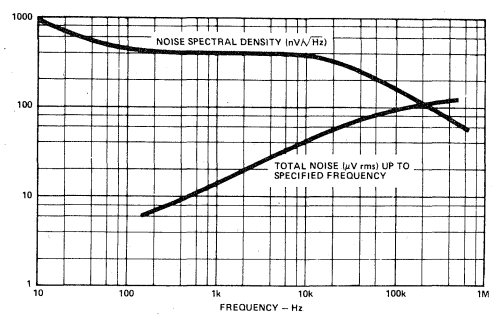


Figure 9. Spectral Noise Density and Total rms Noise vs. Frequency

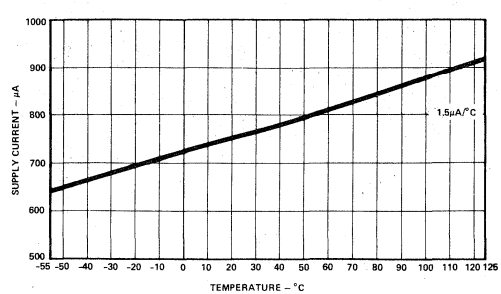


Figure 10. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 11 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

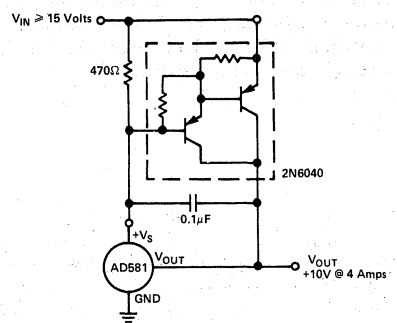


Figure 11. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 12. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

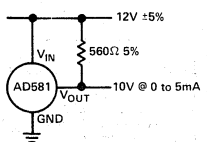


Figure 12. 12 Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

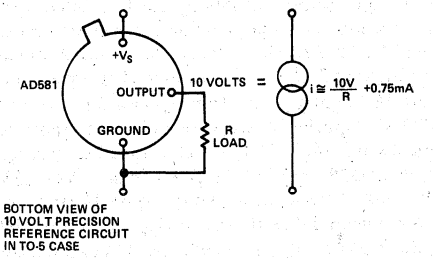


Figure 13. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "zener" mode to provide a precision -10.00 volt reference. As shown in Figure 14, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

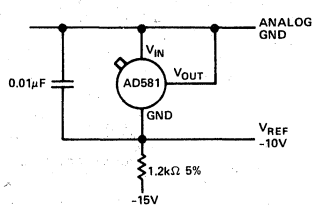


Figure 14. Two-Terminal -10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 15, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to -10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its -10 volt "zener" mode, as shown in Figure 14 (the $-10V_{REF}$ output is connected directly to the $V_{REF\ IN}$ of the CMOS DAC). The AD581 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

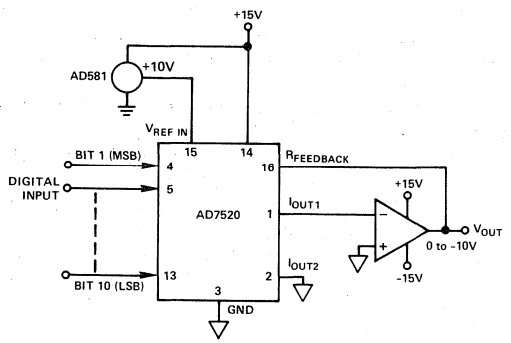


Figure 15. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

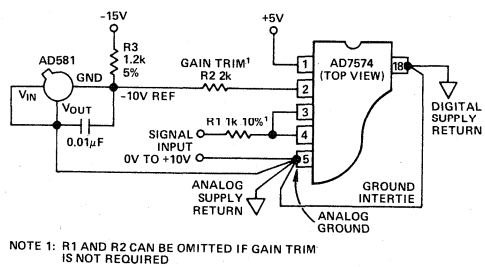


Figure 16. AD581 as Negative 10 Volt Reference for CMOS ADC

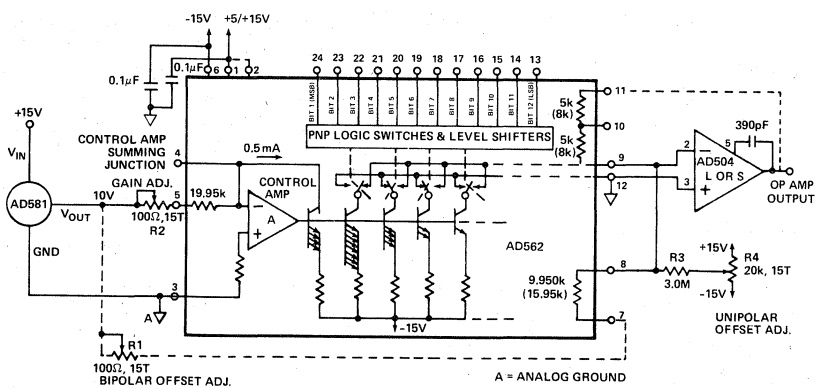


Figure 17. Precision 12-Bit D/A Converter

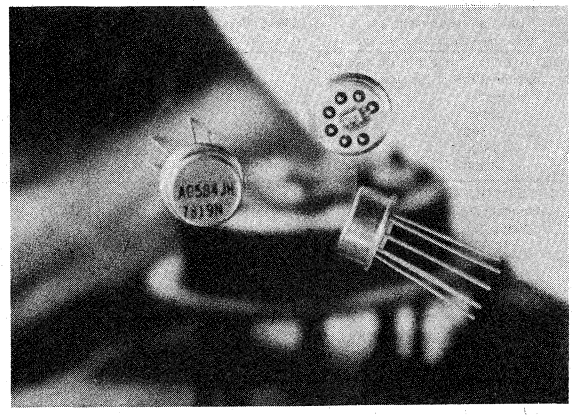
ANALOG DEVICES

Pin Programmable Precision Voltage Reference

AD584*

FEATURES

- Four Programmable Output Voltages:
  - 10.000V, 7.500V, 5.000V, 2.500V
- Laser-Trimmed to High Accuracies
- No External Components Required
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (AD584LH)
  - 10ppm/°C max, -55°C to +125°C (AD584UH)
- Zero Output Strobe Terminal Provided
- Two Terminal Negative Reference
  - Capability (5V & Above)
- Output Sources or Sinks Current
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- Low Cost



PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 40 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C; the AD584S, T, and U are specified for the -55°C to +125°C range. The AD581S, T, and U grades are also available processed to MIL-STD-883B, Level B. All grades are packaged in a hermetically-sealed eight-terminal TO-99 metal can.

***COVERED BY U.S. PATENT NO. 3,887,863.**

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD584UH guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).
5. Every AD584 receives a 24 hour stabilization bake at 150°C and a gross leak test to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ V_{IN} = +15V and +25°C unless otherwise noted)

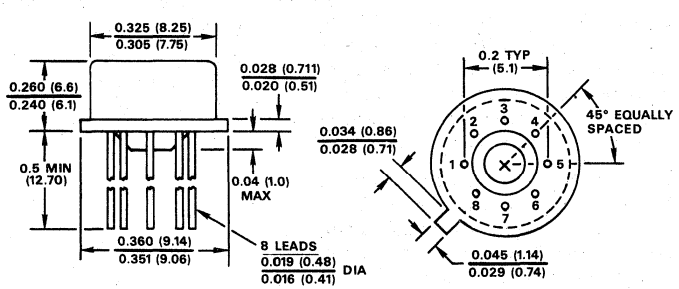
MODEL	AD584JH	AD584KH	AD584LH	AD584SH	AD584TH	AD584UH
ABSOLUTE MAX RATINGS						
Input Voltage V_{IN} to Ground	40V	*	*	*	*	*
Power Dissipation @ +25°C	600mW	*	*	*	*	*
Operating Junction Temp. Range	-55°C to +150°C	*	*	*	*	*
Storage Temperature Range	-65°C to +175°C	*	*	*	*	*
Lead Temperature Soldering, 10sec)	+300°C	*	*	*	*	*
Thermal Resistance Junction-to-Ambient	150°C/Watt	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	-55°C to +125°C	**	**
OUTPUT VOLTAGE TOLERANCE Maximum Error[1] for Nominal Outputs of:						
10.000V	±30mV	±10mV	±5mV	±30mV	±10mV	±5mV
7.500V	±22mV	±8mV	±4mV	±22mV	±8mV	±4mV
5.000V	±15mV	±6mV	±3mV	±15mV	±6mV	±3mV
2.500V	±7.5mV	±3.5mV	±2.5mV	±7.5mV	±3.5mV	±2.5mV
OUTPUT VOLTAGE CHANGE Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]						
10.000, 7.500, 5.000V Outputs	30ppm/°C	15ppm/°C	5ppm/°C	30ppm/°C	15ppm/°C	10ppm/°C
2.500V Output	30ppm/°C	15ppm/°C	10ppm/°C	30ppm/°C	20ppm/°C	15ppm/°C
Differential Temperature Coefficients Between Outputs	5ppm/°C typ	3ppm/°C typ	3ppm/°C typ	5ppm/°C typ	3ppm/°C typ	3ppm/°C typ
QUIESCENT CURRENT	1.0mA max	*	*	*	*	*
	750μA typ	*	*	*	*	*
Temperature Variation	1.5μA/°C typ	*	*	*	*	*
TURN-ON SETTLING TIME TO 0.1%	200μs	*	*	*	*	*
NOISE (0.1 to 10Hz)	50μV p-p	*	*	*	*	*
LONG-TERM STABILITY	25ppm/1000 Hrs. (Non-Cumulative)	*	*	*	*	*
SHORT CIRCUIT CURRENT	30mA	*	*	*	*	*
LINE REGULATION (No Load)						
$15V \leq V_{IN} \leq 30V$	0.002%/V	*	*	*	*	*
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$	0.005%/V	*	*	*	*	*
LOAD REGULATION						
$0 \leq I_{OUT} \leq 5mA$, All Outputs	50ppm/mA max	*	*	*	*	*
	(20ppm/mA typ)	*	*	*	*	*
OUTPUT CURRENT $V_{IN} \geq V_{OUT} + 2.5V$						
Source @ +25°C	10mA min	*	*	*	*	*
Source T_{min} to T_{max}	5mA min	*	*	*	*	*
Sink T_{min} to T_{max}	5mA min	*	*	200μA min	**	**
Sink -55°C to +85°C	–	–	–	5mA min	**	**

*Specifications same as AD584JH.
**Specifications same as AD584SH.
[1] At Pin 1.
[2] Calculated as average over the operating temperature range.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

TO-99 CAN



APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

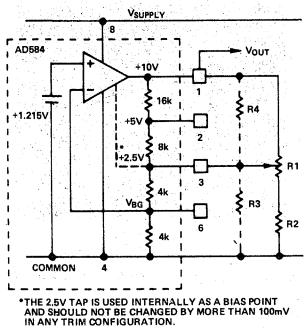


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 5 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

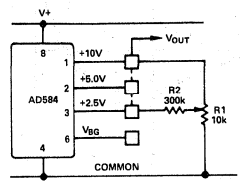


Figure 2. Output Trimming

PIN DESIGNATION

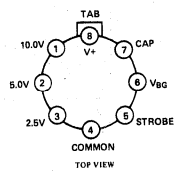


Figure 3. Pin Designations

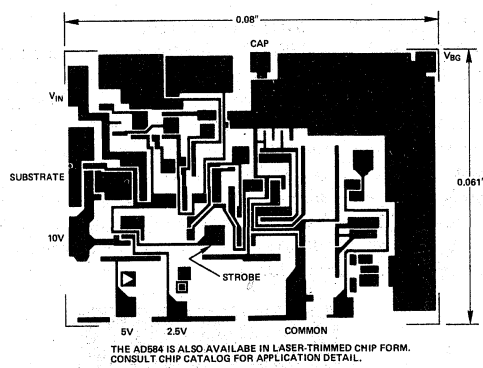


Figure 4. Bonding Diagram

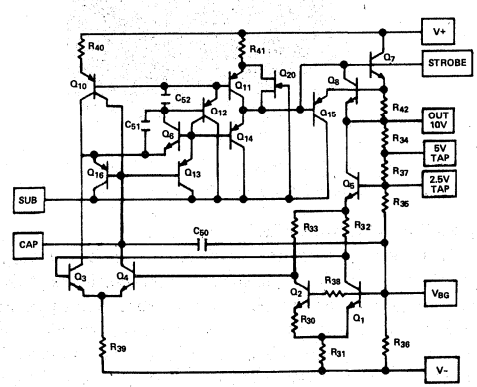


Figure 5. Schematic Diagram

Performance of the AD584

PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at five temperatures over the -55°C to +125°C range to ensure that each device falls within the Maximum Error Band (see Figure 6) specified for a particular grade (i.e., S, T, or U grades); three-point measurement guarantees performance within the error band from 0 to +70°C (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at +25°C. Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is ±10mV and the error band is ±15mV. Hence, the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C.

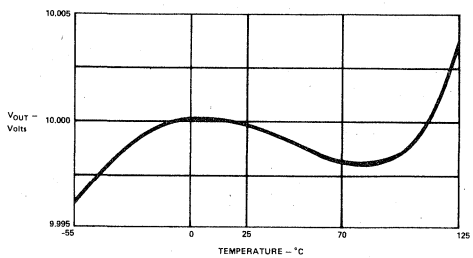


Figure 6. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 7. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

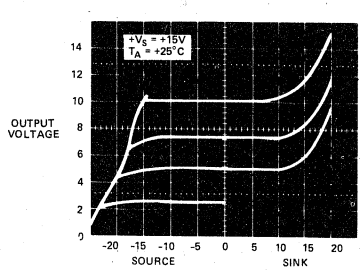


Figure 7. AD584 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 8 displays the turn-on characteristic of the AD584. Figure 8A is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point. Figure 8B demonstrates the settling characteristics using the strobe input (see Figure 11). Without compensation, the output of the AD584 typically settles within 225μs. With a 90pF capacitor across pins (5) and (3), critical damping is approximated, as shown in Figure 8B, with settling times <5μs.

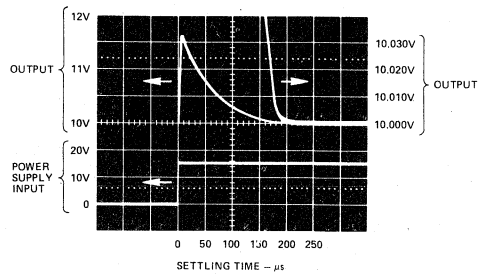


Figure 8a. Output Settling Characteristic

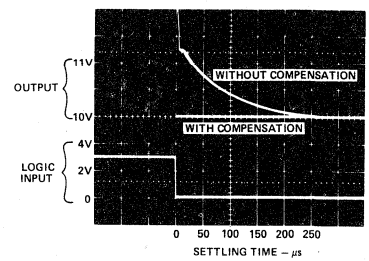


Figure 8b. Output Settling Characteristic

NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between 0.01μF and 0.1μF connected between the Cap and V_{BG} terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 10.

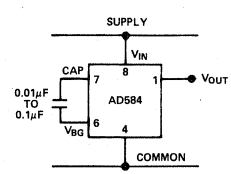


Figure 9. Additional Noise Filtering with an External Capacitor

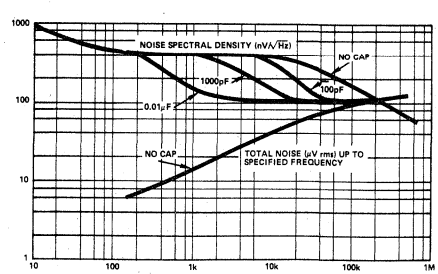


Figure 10. Spectral Noise Density and Total rms Noise vs. Frequency

USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 11 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 11.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

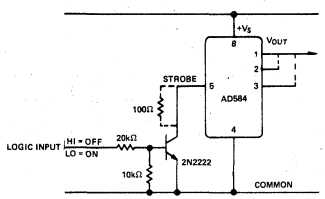


Figure 11. Use of the Strobe Terminal

PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 12 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

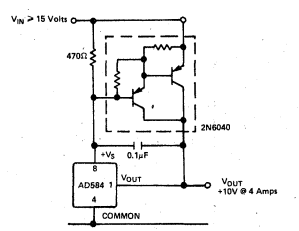


Figure 12. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 13. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 14). Of course, the minimum voltage required to drive the connection is 5 volts.

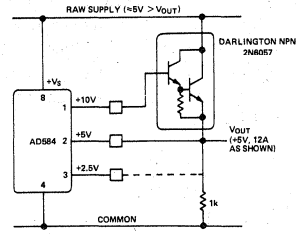


Figure 13. NPN Output Current Booster

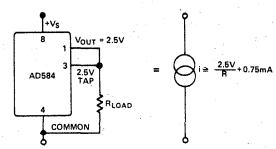


Figure 14. A Two-Component Precision Current Limiter

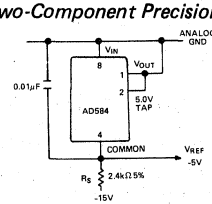


Figure 15. Two-Terminal -5 Volt Reference

NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision -10, -7.5 or -5.0 volt reference. As shown in Figure 15, the V_{IN} and V_{OUT} terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of V_{OUT}. With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD584 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD584 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA.

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up as shown in Figure 16, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. The AD584 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 18. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

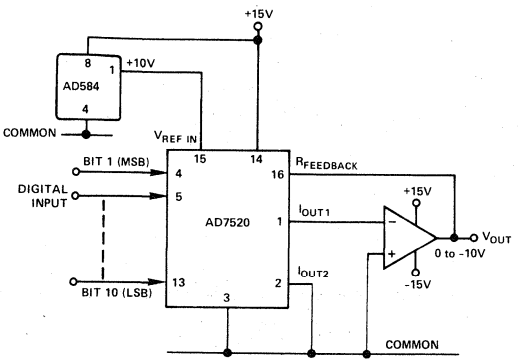
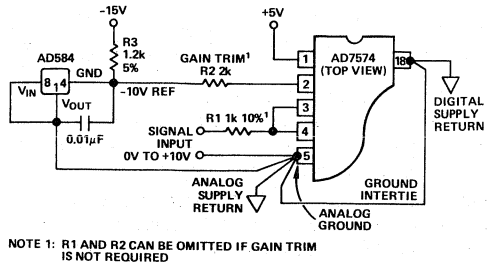


Figure 16. Low Power 10-Bit CMOS DAC Application

PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 17). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD584L (at 5ppm/°C) as the 10 volt reference



NOTE 1: R1 AND R2 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED

Figure 18. AD584 as Negative 10 Volt Reference for CMOS ADC

guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 19 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.

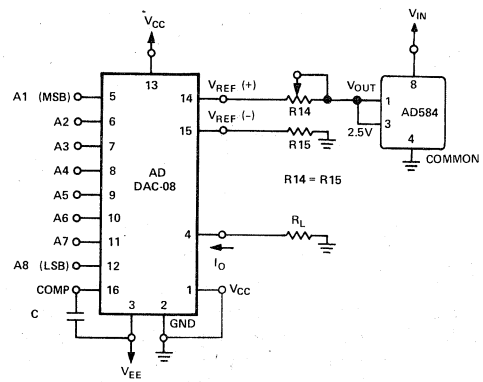


Figure 19. Current Output 8-Bit D/A

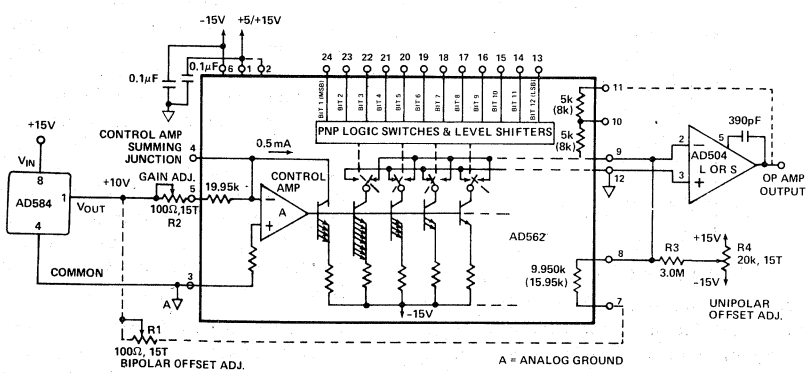


Figure 17. Precision 12-Bit D/A Converter

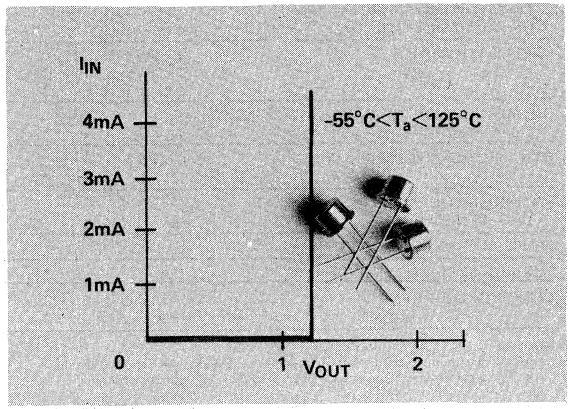
ANALOG DEVICES

Two-Terminal IC 1.2 Volt Reference

AD589

FEATURES

Superior Replacement for Other 1.2V References
Wide Operating Range: 50μA to 5mA
Low Power: 60μW Total P_D at 50μA
Low Temperature Coefficient:
10ppm/°C max, 0 to +70°C (AD589M)
25ppm/°C max, -55°C to +125°C (AD589U)
Two Terminal "Zener" Operation
Low Output Impedance: 0.6Ω
No Frequency Compensation Required
Low Cost



PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0 to +70°C operation, while the S, T and U grades are rated for the full -55°C to +125°C temperature range. Processing to MIL-STD-883B is available on the three military grades.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6Ω and temperature coefficients as low as 10ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50μA (60μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589S, T, and U grades are available 100% screened to the requirements of MIL-STD-883, Method 5004, Level B.
6. The AD589 is an exact replacement for other 1.2V references, offering superior temperature performance and reduced sensitivity to capacitive loading.

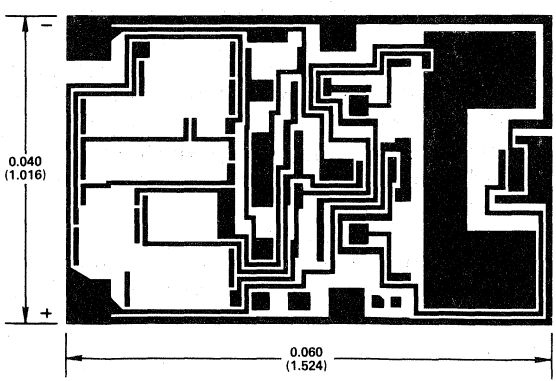
SPECIFICATIONS (typical @ I_{IN} = 500μA and T_A = 25°C unless otherwise noted)

Model	AD589JH	AD589KH	AD589LH	AD589MH	AD589SH	AD589TH	AD589UH
ABSOLUTE MAXIMUM RATINGS							
Current	10mA	*	*	*	*	*	*
Reverse Current	10mA	*	*	*	*	*	*
Power Dissipation[1]	125mW	*	*	*	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*	*	*	*
Operating Junction Temperature Range	−55°C to +150°C	*	*	*	*	*	*
Lead Temperature (Soldering, 10sec)	300°C	*	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	*	−55°C to +125°C	**	**
OUTPUT VOLTAGE	1.200V min	*	*	*	*	*	*
	1.235V typ	*	*	*	*	*	*
	1.250V max	*	*	*	*	*	*
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA − 5mA)	5mV max	*	*	*	*	*	*
DYNAMIC OUTPUT IMPEDANCE	0.6Ω typ	*	*	*	*	*	*
	2Ω max	*	*	*	*	*	*
RMS NOISE VOLTAGE 10Hz < f < 10kHz	5μV	*	*	*	*	*	*
TEMPERATURE COEFFICIENT[2] − ppm/°C	100 max	50 max	25 max	10 max	100 max	50 max	25 max
TURN-ON SETTLING TIME TO 0.1%	25μs	*	*	*	*	*	*
OPERATING CURRENT[3]	50μA min	*	*	*	*	*	*
	5mA max	*	*	*	*	*	*

NOTES
[1] Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and $\theta_{JA} = 400°C/W$.
[2] See following page for explanation of temperature coefficient measurement method.
[3] Optimum performance is obtained at currents below 500μA. Stray shunt capacitances should be minimized. If strays cannot be avoided, a shunt capacitor of at least 1000pF is recommended.

*Specifications same as AD589J.
**Specifications same as AD589S.
Specifications subject to change without notice.

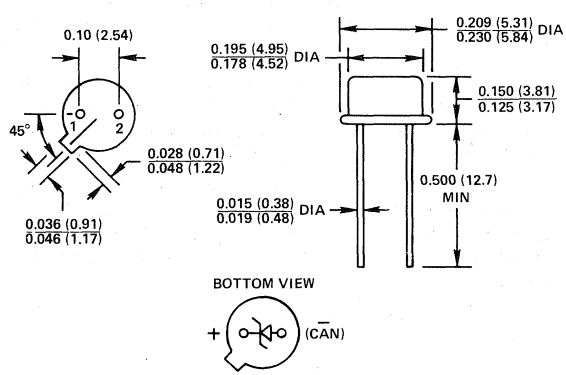
AD589 BONDING DIAGRAM



THE AD589 IS AVAILABLE IN CHIP FORM WITH FULLY TESTED AND GUARANTEED SPECIFICATIONS. CONSULT FACTORY FOR AVAILABLE GRADES AND PRICING.

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD589 consistently follows the curve shown in Figure 1. Three-point measurement guarantees the error band over the specified temperature range. The temperature coefficients specified on page 2 represent the slopes of the diagonals of the error band from +25°C to T_{min} and +25°C to T_{max}.

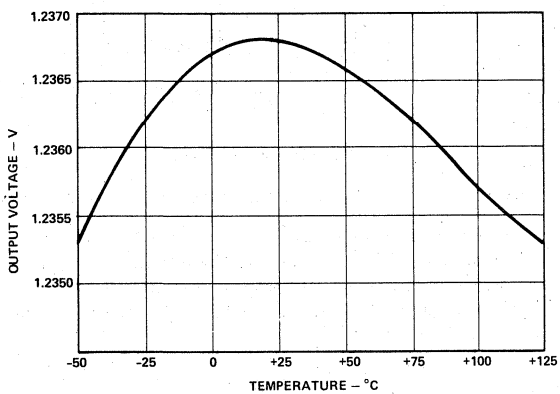


Figure 1. Typical AD589 Temperature Characteristics

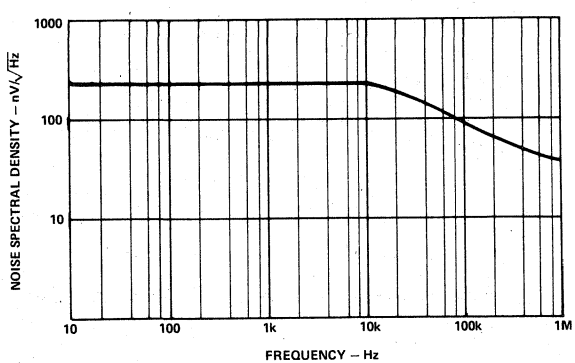


Figure 2. Noise Spectral Density

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 3 displays the turn-on characteristic of the AD589. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 25μs, and there is no long thermal tail appearing after that point.

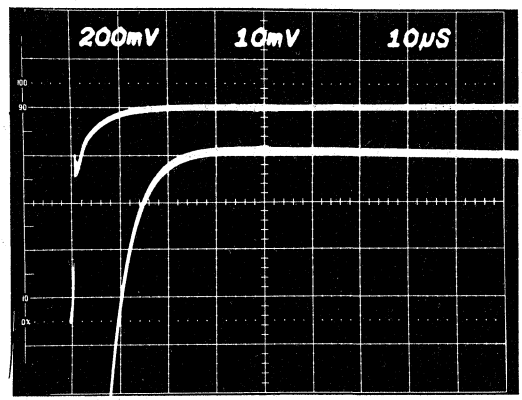


Figure 3. Output Settling Characteristics

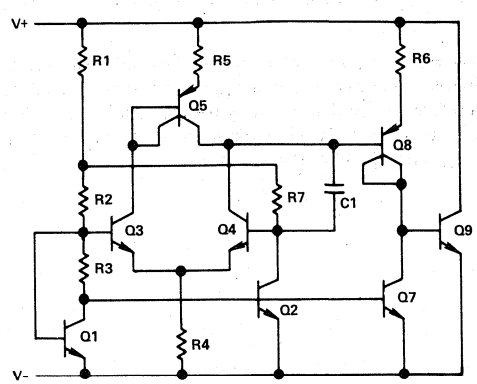


Figure 4. Schematic Diagram

APPLICATION INFORMATION

The AD589 functions as a two-terminal shunt-type regulator. It provides a constant 1.23V output for a wide range of input current from 50μA to 5mA. Figure 5 shows the simplest configuration for an output voltage of 1.2V or less. Note that no frequency compensation is required. If additional filtering is desired for ultra low noise applications, minimum recommended capacitance is 1000pF.

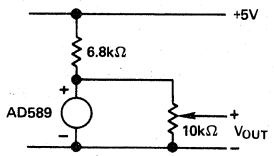


Figure 5. Basic Configuration for 1.2V or Less

The AD589 can also be used as a building block to generate other values of reference voltage. Figure 6 shows a circuit which produces a buffered 10V output. Total supply current for this circuit is approximately 2mA.

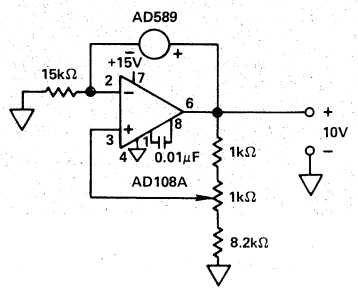
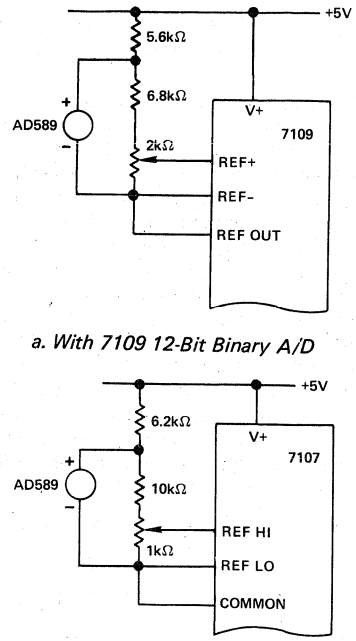


Figure 6. Single-Supply Buffered 10V Reference

The low power operation of the AD589 makes it ideal for use in battery operated portable equipment. It is especially useful as a reference for CMOS analog-to-digital converters. Figure 7 shows the AD589 used in conjunction with two popular integrating type CMOS A/D converters.



a. With 7109 12-Bit Binary A/D

b. With 7107 Panel Meter A/D

Figure 7. AD589 Used as Reference for CMOS A/D Converters

The AD589 also is useful as a reference for CMOS multiplying DACs such as the AD7533. These DACs require a negative reference voltage in order to provide a positive output range. Figure 8 shows the AD589 used to supply an equivalent −1.0V reference to an AD7533.

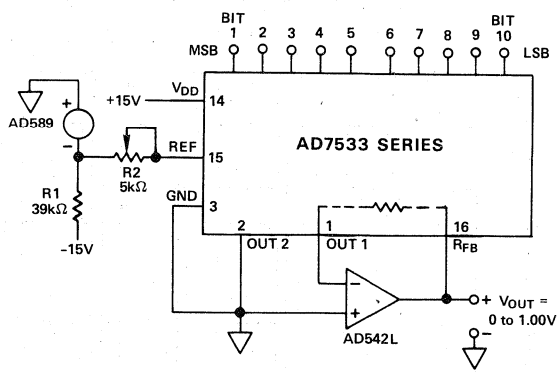


Figure 8. AD589 as Reference for 10-Bit CMOS DAC

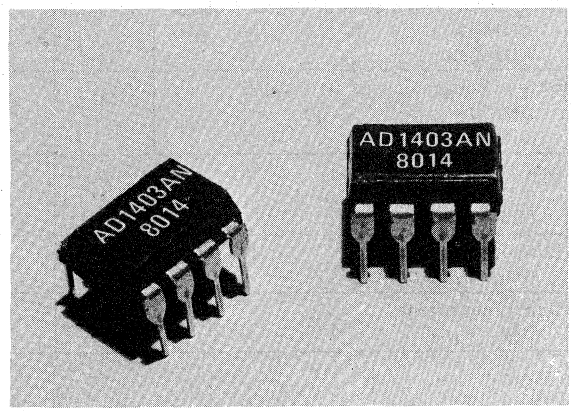
ANALOG DEVICES

Low Cost, Precision 2.5 Volt IC Reference

AD1403/AD1403A

FEATURES

Improved, Lower Cost, Replacements for Standard 1403, 1403A
3-Terminal Device: Voltage In/Voltage Out
Laser Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)
Excellent Temperature Stability: 25ppm/°C (AD1403A)
Low Quiescent Current: 1.5mA max
10mA Current Output Capability
Low Cost
Convenient MINI-DIP Package



PRODUCT DESCRIPTION

The AD1403 and AD1403A are improved three-terminal, low cost, temperature compensated, bandgap voltage references that provide a fixed 2.5V output voltage for inputs between 4.5V and 40V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provides the AD1403/AD1403A with an initial tolerance of ±10mV and a temperature stability of better than 25ppm/°C. In addition, the low quiescent current drain of 1.5mA (max) offers a clear advantage over classical zener techniques.

The AD1403 or AD1403A is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD1403/AD1403A allows operation with 5 volt logic supplies, making these devices ideal for digital panel meter applications and when only a single logic supply is available.

The AD1403 and AD1403A are specified for operation over the 0 to +70°C temperature range. The AD580 series of 2.5 volt precision IC references is recommended for applications where operation over the −55°C to +125°C range is required.

OTHER ANALOG DEVICES REFERENCES

AD580	High Precision 2.5 Volt IC Reference
AD581	High Precision 10.0 Volt IC Reference
AD584	Pin Programmable Precision IC Voltage Reference
AD589	Two Terminal 1.2 Volt IC Reference
AD2700	High Performance +10.000 Volt Reference
AD2701	High Performance −10.000 Volt Reference
AD2702	High Performance Tracking ±10.000 Volt Reference

PRODUCT HIGHLIGHTS

1. The AD1403A offers improved initial tolerance over the industry-standard 1403A: ±10mV versus ±25mV at a lower cost.
2. The three-terminal voltage in/voltage out operation of the AD1403/AD1403A provides a regulated output voltage without any external components.
3. The AD1403/AD1403A provides a stable 2.5V output voltage for input voltages between 4.5V and 40V making these devices ideal for systems that contain a single logic supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD1403A with temperature stabilities of 25ppm/°C.
5. The low 1.5mA maximum quiescent current drain of the AD1403 and AD1403A makes them ideal for CMOS and other low power applications.

SPECIFICATIONS (V_{IN} = 15V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0mA)	V_O				
AD1403		2.475	2.500	2.525	V
AD1403A		2.490	2.500	2.510	
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
AD1403		–	10	40	
AD1403A		–	10	25	
Output Voltage Change, 0 to +70°C	ΔV_O				mV
AD1403		–	–	7.0	
AD1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15V≤V_{IN}≤40V)		–	1.2	4.5	
(4.5≤V_{IN}≤15V)		–	0.6	3.0	
Load Regulation ($0mA<I_O<10mA$)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0mA)	I_I	–	1.2	1.5	mA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Storage Temperature	T_{STG}	-25 to 100	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

Specifications subject to change without notice.

ORDERING INFORMATION

Device	Initial Tolerance
AD1403N	±25mV
AD1403AN	±10mV

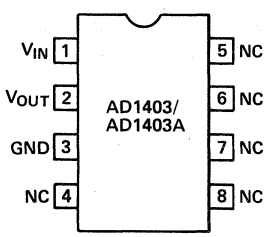


Figure 1. AD1403/AD1403A Connection Diagram

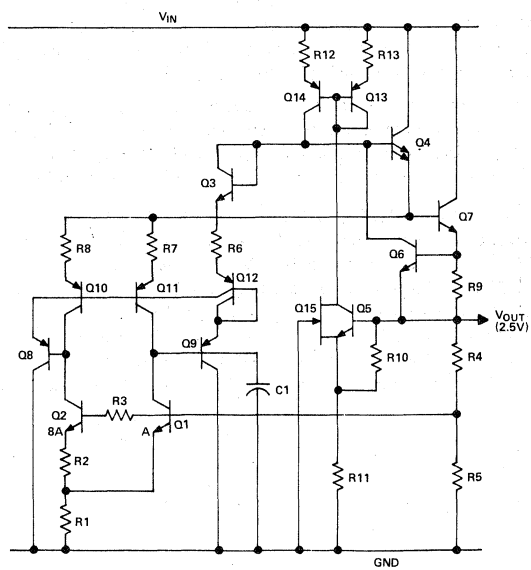


Figure 2. AD1403/AD1403A Schematic Diagram

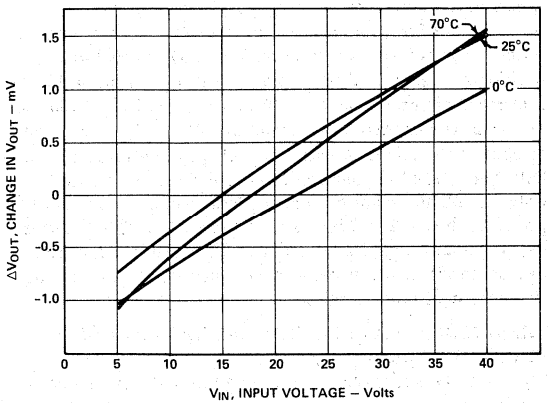


Figure 3. Typical Change in V_{OUT} vs. V_{IN} (Normalized to V_{OUT} @ V_{IN} = 15V @ T_C = 25°C)

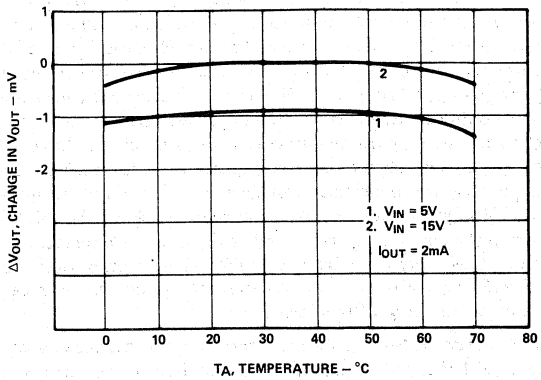


Figure 6. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V)

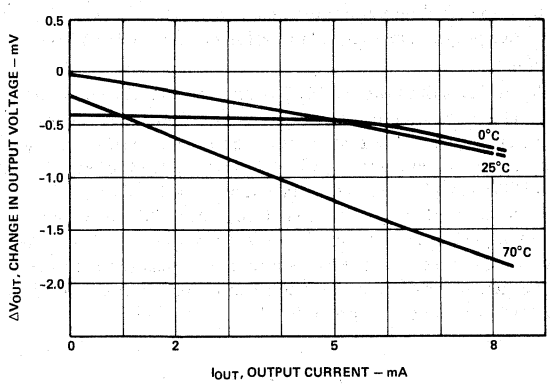


Figure 4. Change in Output Voltage vs. Load Current (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

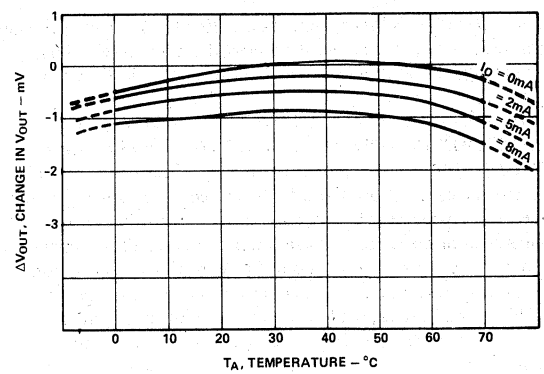


Figure 7. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

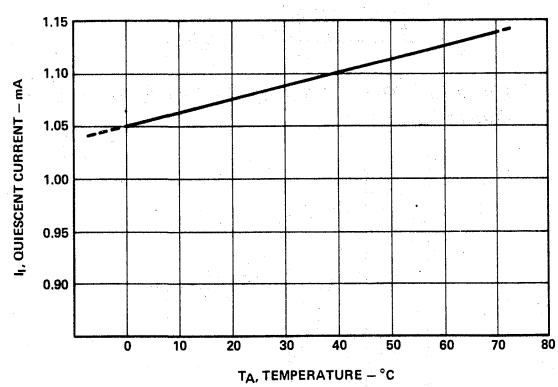


Figure 5. Quiescent Current vs. Temperature (V_{IN} = 15V, I_{OUT} = 0mA)

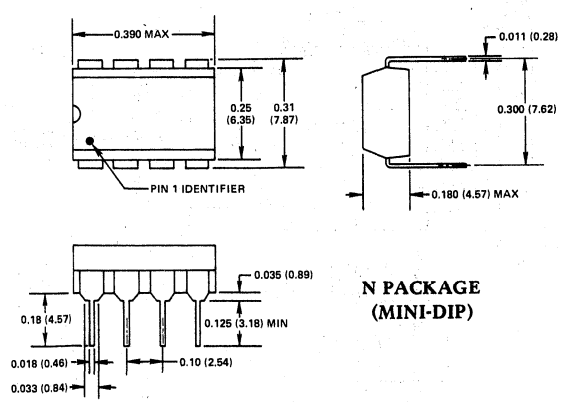


Figure 8. AD1403/1403A Package Specifications (Dimensions shown in inches and (mm))

Applying the AD1403/AD1403A

VOLTAGE VARIATION VS. TEMPERATURE AND LINE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD1403 is shown in Figure 6. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

The AD1403 exhibits a worst-case shift of 7.5mV over the entire range of operating input voltage, 4.5 volts to 40 volts. Typically, the shift is less than 1mV as shown in Figure 3.

THE AD1403A AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD1403A has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1.5mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

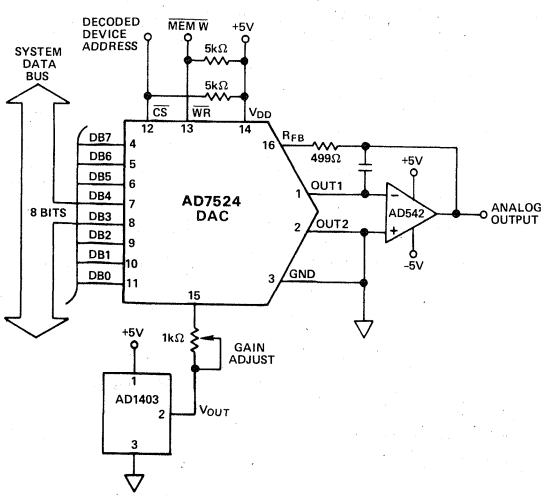


Figure 9. Low Power, Low Voltage Reference for the AD7524 Microprocessor-Compatible 8-Bit DAC

Figure 9 shows the AD1403A used as a reference for the AD7524 low-cost 8-bit CMOS DAC with complete microprocessor interface. The AD1403A and the AD7524 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7524 includes an 8-bit data register, and address decoding logic; it may thus be interfaced directly to an 8- or 16-bit data bus. Only 300μA of quiescent current from the single +5 volt supply is required to operate the AD7524 which is packaged in a small 16 pin DIP. The AD542 output amplifier is also low power, requiring only 1.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7524KN without user trims and it typically settles to ±1/2LSB in less than 5 microseconds. It will provide the 0 volt to -2.5 volt output swing from ±5 volt supplies.

THE AD1403 AS A PRECISION PROGRAMMABLE CURRENT SOURCE

The AD1403 is an excellent building block for precision current sources. Its wide range of operating voltages, 4.5V to 40V along with excellent line regulation over that range (7.5mV) result in high insensitivity to varying load impedances. The low quiescent current (I_I) of 1.5mA (max) and the maximum specified maximum load current of 10mA allows the user to program current to any value between 1.5mA and 10mA.

Figure 10a shows the AD1403 connected as a current source. Total current is equal to the quiescent current plus the load current. Most of the temperature coefficient comes from the quiescent current term I_I, which has a typical TC of +0.13%/°C (1300ppm/°C). The load voltage (and hence current) TC is much lower at ±40ppm/°C max (AD1403). Therefore, the overall temperature coefficient decreases rapidly as the load current is increased. Figure 10b shows the typical temperature coefficient for currents between 1.5mA and 10mA. Use of an AD1403A will not improve the TC appreciably.

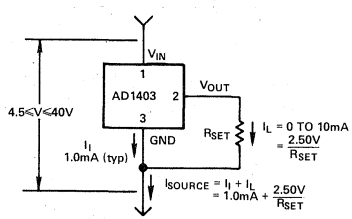


Figure 10a. The AD1403 as a Precision Programmable Current Source

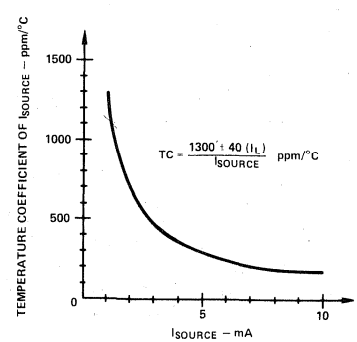


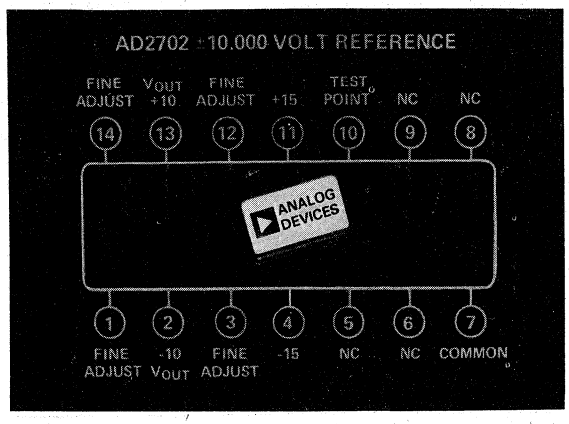
Figure 10b. Typical Temperature Coefficient of Current Source

±10 Volt Precision Reference Series

AD2700, AD2701, AD2702

FEATURES

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed -55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected



PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C. The AD2700U and AD2700S series are also available with full screening to MIL-STD-883A, Class B.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range. All units are packaged in a 14-pin dual-in-line welded metal package which offers excellent reliability, hermeticity, as well as EMI/RFI shielding.

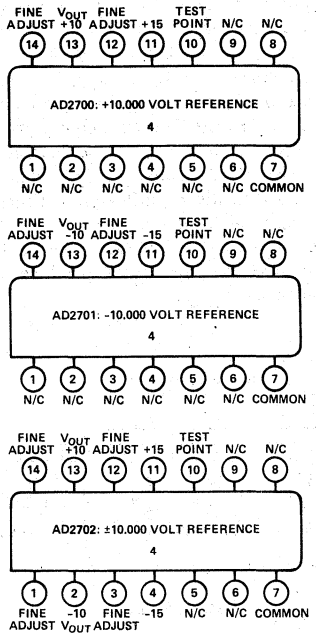
Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

SPECIFICATIONS (maximum or minimum @ E_{in} -15V @ +25°C, R_L = 2kΩ unless otherwise noted)

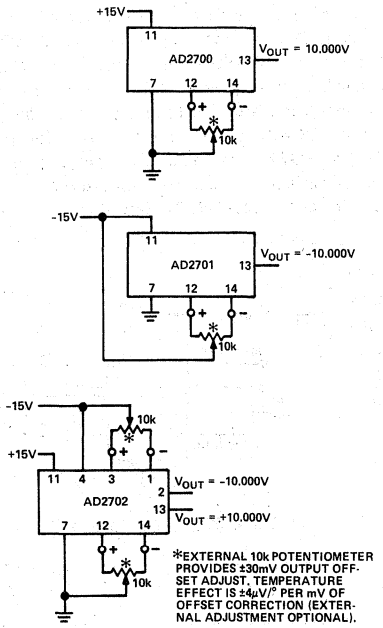
MODEL	J	L	S[1]	U[1]
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissapation @ +25°C – AD2700, 01	300mW	*	*	*
– AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE				
AD2700	10.000V ±0.005V	±0.0025V	*	**
AD2701	-10.000V ±0.005V	±0.0025V	*	**
AD2702	±10.000V ±0.005V	±0.0025V	*	**
OUTPUT CURRENT – @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE CHANGE[2] – AD2700, 01	10ppm/°C	3ppm/°C	**	**
	±11.0mV	±4.3mV	±8mV	±5.5mV
T_{min} to T_{max} AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300μV/V	*	*	*
LOAD REGULATION				
0 to ±10mA	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT – AD2700, 01	±14mA	*	*	*
– AD2702	+17mA, -3mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. typ	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust typ	*	*	*

*Same as "J" grade performance.
**Same as "L" grade performance.
***Same as "S" grade performance.
[1] Operational screening ("S or U/883") per MIL-STD-883A Method 5004.2, Class B; except that constant acceleration is 10kg. (Method 2001, Condition B. Y1 Plane).
[2] Output voltage change as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C.

Specifications subject to change without notice.



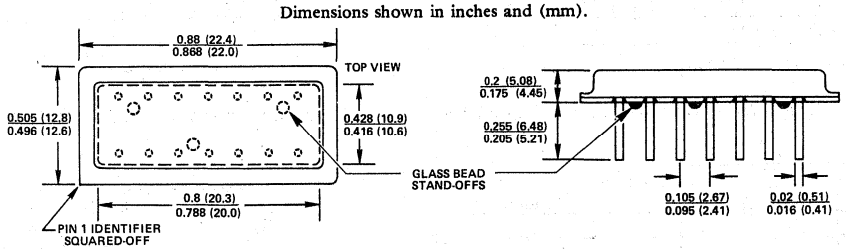
Pin Designations



Fine Trim Connections

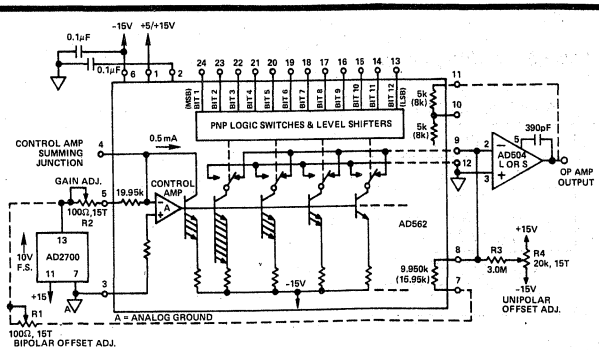
PACKAGE DIMENSIONS

Dimensions shown in inches and (mm).



Hermetically sealed 14 Pin Dual-In-Line (Fine & Gross leak tested per MIL-STD-883A, Method 1014)
Pin 7 is electrically connected to the case. Case has metal bottom surface.

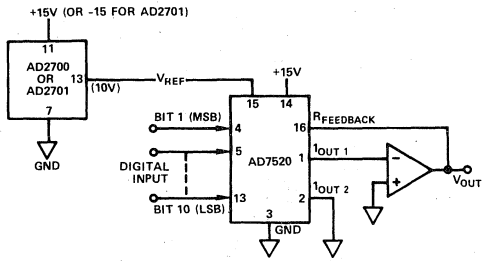
14-Pin Dual-In-Line



Using AD2700 Reference With the AD562 – 12 Bit D/A Converter

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to -10 volt output range. Alternatively, using the -10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of -10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 data sheet.

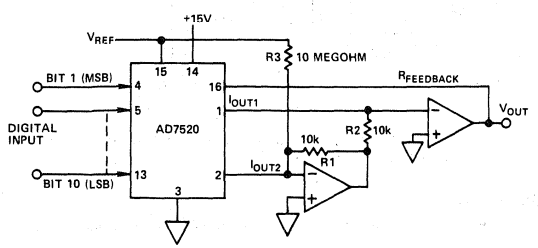


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table 1. Code Table — Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

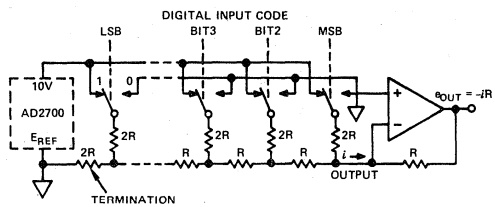
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

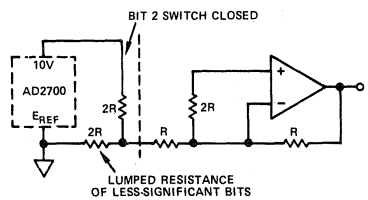
Table 2. Code Table — Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

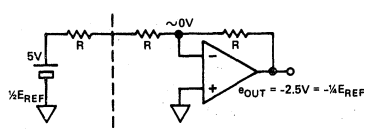
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4}E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence — because the amplifier summing point is at virtual ground — the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to 2^{-n} E_{REF}.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

Transducers, Conditioners & Instrumentation

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●New product since 1979 *Data Acquisition Products Catalog Supplement*

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Selection Guide
Transducers, Conditioners & Instrumentation

In this Selection Guide, the families of Transducers, Signal Conditioners, and transducer-readout Panel Instruments are divided into the following categories:

1. TEMPERATURE TRANSDUCERS:
   Current-Output IC Devices
   Frequency-Output IC Devices
2. SIGNAL CONDITIONERS:
   Single-Channel Modules
   Multichannel Isolated Multiplexed Modules
   Transducer Power Supply Modules
3. 4-TO-20mA LOOP TRANSMITTERS:
   Analog-to-Current Modules
   Digital-to-Current Modules
4. PANEL INSTRUMENTS:
   Single-Channel Digital Meters
   Scanning Multichannel Digital Meters

Descriptions, complete specifications, and application information can be found in the data sheets. For new devices having 2-page short-form data, additional information can be obtained by getting in touch with Analog Devices. A useful source of information on the applications of products in this section is the *Transducer Interfacing Handbook—A guide to analog signal conditioning*, (1980), available for $14.50 from Analog Devices, P.O. Box 796, Norwood MA 02062.

The DAC1420, DAC1422 and DAC1423 are catalogued in the d/a converter section (9), at the pages indicated; the AD537 is catalogued in the V/F/V converter section (11), at the indicated location. 4-to-20mA current-loop transmission is also available on RTI computer-interface boards (Section 17).

All specifications indicated here are typical at rated supply voltage and load, and T_A = +25°C, unless noted otherwise.

1. TEMPERATURE TRANSDUCERS

	Model	Characteristics	Page
Current Output	AD590I/J/K/L/M#	IC, 2-terminal, TO-52 can or miniature flatpack, -55°C to +150°C (218K to 423K) operating range, linear current output, 1μA/K, laser-trimmed for high accuracy; Output current independent of supply voltage.	8-7
	AC2626J/K/L/M	Stainless-steel temperature probe using AD590, same temperature range and electrical characteristics as the AD590, 3/16″ outside diameter, 6- or 4-inch standard lengths, includes 3 feet of Teflon-coated lead wire, 2s response in stirred water, sensor electrically isolated from sheath (±200V breakdown—case to leads).	8-5
Frequency Output	AD537JH/KH/SH/ JD/KD/SD #	IC V/f converter with 1.0V voltage reference and 1.0mV/°C absolute temperature sensing; Frequency range to 150kHz, frequency nonlinearity from 0.07% max (KH, KD, 10kHz full scale), tempco 50ppm/°C; Calibrated 25°C temperature output 298mV ±5mV, 0.02mV/°C slope error, ±0.1°C slope nonlinearity; Output a symmetrical square wave; Packaged in 14-pin DIP or 10-pin hermetic TO-100 can.	11-7

2. SIGNAL CONDITIONERS

	Model	Characteristics	Page
Single Channel	2B31J/K/L	Module; complete signal conditioning function at low cost for bridge transducers, such as strain gages and RTD's; provides programmable excitation, amplification, and 3-pole low pass filter; CMR is 140dB min (60Hz, G = 1000); low offset drift, ±0.5μV/°C max; nonlinearity ±0.0025% max.	8-41
	2B30J/K/L	Modular conditioner with same performance as 2B31, but without transducer excitation supply.	8-41

#Monolithic chips with guaranteed specs available for precision hybrids. 120-page chip catalog available upon request.

Multichannel	2B54A/B●	4-channel low-level isolated amplifier/multiplexer for thermocouples, strain gages, RTDs, etc.; Input span adjustable from ±5mV to ±100mV; Isolation ±1000V dc, channel-to-channel or to output, CMR = 156dB min at 60Hz; Input drift ±1μV/°C max (B), ±0.02% max nonlinearity; Normal-mode filtering and protection to 130V rms included; All-solid-state multiplexing permits scanning speeds up to 400 channels per second minimum; easily expandable to 64-channel system	8-49
	2B55A●	4-channel multiplexer-amplifier, similar to 2B54, but input span adjustable from ±50mV to ±5V for medium to high level signals.	8-49
	2B56A●	Cold-junction thermocouple compensator (CJC); 4 compensating functions: J, K, T and a user-determined function (E, R, S, B or none); When used with output of 2B54/2B55, multiplexer channel selection logic also chooses CJC function, allowing each input to be from a different device; Error is less than ±0.8°C max over ambients from +5°C to +45°C.	8-55
Transducer Power Supply	2B35J/K	Module; precision triple-output transducer power supply; provides ±15V amplifier power and programmable excitation output: voltage (+1V to +15V dc) or current (100μA to 10mA); provides excitation for transducers and signal conditioners.	8-47

3. 4-TO-20mA LOOP TRANSMITTERS

	Model	Characteristics	Page
Analog to Current	2B20A/B	Modular voltage to current converter; provides 4-20mA output current for 0 to +10V input; low drift and nonlinearity, single supply operation.	8-33
	2B22J/K/L	Modular isolated voltage to current converter; 4-20mA output; 1500V dc input to output isolation; internal isolated loop power supply.	8-37
	2B57A●	Module. AD590 output (1 microampere per kelvin, from -55°C to +150°C) to 4-to-20mA two-wire output, remotely powered via output lines; operating ambient temperature range -30°C to +85°C.	8-59
Digital to Current	DAC1422	10-bit latched digital input to 4-to-20mA output; Totally powered from loop supply; Guaranteed monotonic from 0 to +70°C; Auxiliary analog input for backup if the computer power fails.	9-161
	DAC1420●	Same as DAC1422, for 8-bit applications	9-161
	DAC1423●	10-bit isolated latched digital to 4-to-20mA converter; 8- or 16-bit bus microprocessor-compatible interface; Guaranteed monotonic 0 to +70°C; May be powered from +24V dc loop supply; Bumpless transfer, automatic to manual control; Isolation 1500V dc continuous; Increment/decrement digital backup control	9-165

●New product since 1979 *Data Acquisition Products Catalog Supplement.*

(continued on the next page)

4. PANEL INSTRUMENTS †

	Model	Characteristics	Page
Single Channel Readout	AD2040	3 digit low cost temperature indicator for use with AD590 or AC2626 temperature transducers; accurate to ±1° ±1 digit; user programmable to read out in Celsius, Kelvin, Fahrenheit or Rankine; single +5V and line (120V, 240V ac) power-supply options, terminal block interface, small size, panel mount.	8-29
Multichannel Readout	AD2036	6 Channel Scanning Digital Thermometer for use with J, K or T type thermocouples; provides automatic, manual or logic controlled scan, self-contained cold-junction compensation and linearization; °C or °F readout; has isolated analog input, parallel BCD output, analog output; either line powered, +5V dc or +12V dc powered.	8-15
	AD2037	6 Channel 3 1/2 digit scanning voltmeter with differential inputs and full scale programmability from ±200mV to 6V; designed to interface printers, computers, transmitters, etc. for display, control, logging, etc.; has isolated analog input, parallel BCD output, analog output; line powered.	8-21
	AD2038	6 Channel Scanning Digital Thermometer for use with the AD590 and AC2626 temperature transducers; provides automatic, manual or logic controlled scan of the 6 inputs, high accuracy, 0.1° resolution; has isolated analog input, parallel BCD output, analog output; line powered.	8-21

†In addition to the devices listed here, an extensive line of digital panel instruments is offered. 96-page *Digital Panel Instrument Catalog* available upon request.

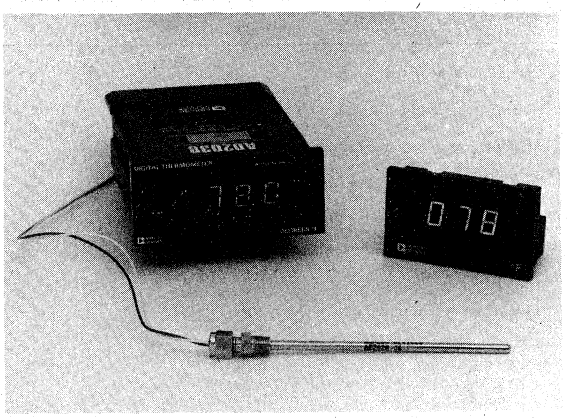
ANALOG DEVICES

General Purpose Temperature Probe

AC2626

FEATURES

- **Linear Current Output: 1μA/K**
- **Wide Range: -55°C to +150°C**
- **Laser Trimmed Sensor (AD590) to ±0.5°C Calibration Accuracy (AC2626M)**
- **Excellent Linearity: ±0.3°C Over Full Range (AC2626M)**
- **6 Inch or 4 Inch Standard, Stainless Steel Sheath**
- **3/16 Inch in Outside Diameter**
- **3 Feet Teflon Coated Lead Wire**
- **Wide Power Supply Range +4V to +30V**
- **Low Cost**
- **Fast Response: 2 Seconds (In Stirred Water)**
- **Sensor Isolated From Sheath**



PRODUCT DESCRIPTION

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the new AD590F, the probe is available in linearity grades of 0.3°C, 0.4°C, 0.8°C or 1.5°C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AC2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

PRODUCT HIGHLIGHTS

The AC2626 is based on the AD590 temperature transducer, a two terminal integrated circuit which produces an output current linearly proportional to absolute temperature.

Costly linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AC2626.

Due to the high impedance current output of the AD590, the AC2626 is particularly useful in remote sensing applications, because of its insensitivity to voltage drops over lines. The output characteristics also make the AC2626 easy to multiplex.

In addition to temperature measurement, applications include temperature compensation, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry.

DIRECT INTERFACE PRODUCTS

For display and/or control applications, two companion products are available. The AD2038, 6 channel digital thermometer, and the AD2040, low cost temperature indicator, were designed to be used in conjunction with the AC2626.

1. The AD2038 is a low cost, ac line powered 6 channel digital scanning thermometer designed to interface to printers, computers, serial data transmitters, etc., for display, control, logging or transmission of multi-point temperature data. Channel selection is made via three methods: manual, using the switch provided on the front; auto/scan, where the AD2038 cycling on an internal clock can continually scan the six input channels or external selection, where control inputs provided on the rear connector enable channel selection via external BCD coding.
2. The AD2040 is a low cost, 3 digit temperature indicator. An internal precision voltage reference, resistor network and span and zero adjusts allow the AD2040 to read out directly in °C, °F, K or R. User selectable readout as well as all other connection, i.e., +5V dc power and AC2626 interface are all made via the terminal block on the rear.

APPLICATION HINTS

1. Under all operating conditions, a minimum 4V dc must be present across the AC2626.
2. Use of twisted pair wiring is recommended, particularly for remote applications or in high noise environments. Shielded wire is desirable in severe noise environments.
3. For the lowest cost impact, the J and K grades are recommended. Where probe interchangeability is desired, grades L and M are recommended.

SPECIFICATIONS (typical @ +25°C and +5V unless otherwise specified)

MODEL	AC2626J	AC2626K	AC2626L	AC2626M
ABSOLUTE MAXIMUM RATINGS				
Forward Voltage (V_S)	+44V	*	*	*
Reverse Voltage (V_S)	-20V	*	*	*
Breakdown Voltage (Case to Leads)	±200V	*	*	*
Rated Performance Temp. Range	-55°C to +150°C	*	*	*
Storage Temperature Range	-60°C to +160°C	*	*	*
POWER SUPPLY				
Operating Voltage Range	+4V to +30V	*	*	*
OUTPUT				
Nominal Current Output @ +25°C (298.2°K)	298.2µA	*	*	*
Nominal Temperature Coefficient	1µA/°C	*	*	*
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error (over rated performance temperature range)				
Without External Calibration Adjustment	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
With +25°C Calibration Error Set to Zero	±3.0°C max	±2.0°C max	±1.6°C max	±1.0°C max
Nonlinearity	±1.5°C max	±0.8°C max	±0.4°C max	±0.3°C max
Repeatability[1]	0.1°C	*	*	*
Long Term Drift[2]	0.1°C max	*	*	*
Time Constant[3] (in stirred water)	2 sec.	*	*	*
Current Noise	40pA$\sqrt{Hz}$	*	*	*
Power Supply Rejection				
+4V≤V_S≤+5V	0.5µA/V	*	*	*
+5V≤V_S≤+15V	0.2µA/V	*	*	*
+15V≤V_S≤+30V	0.1µA/V	*	*	*
Electrical Turn-On Time	20µs	*	*	*
+ Lead Color	yellow	orange	blue	green

ORDERING GUIDE

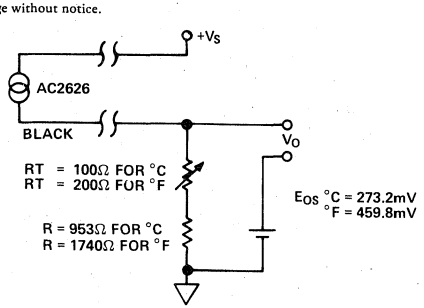
AC2626
GRADE J, K, L, M — ENTER
LENGTH 4, 6 — ENTER

AC2629
BRASS B
TYPE 316 STAINLESS SS — ENTER

NOTES
[1] Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed, not tested.
[2] Conditions: constant +5V, constant +125°C; guaranteed, not tested.
[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Specifications subject to change without notice.

CALIBRATION

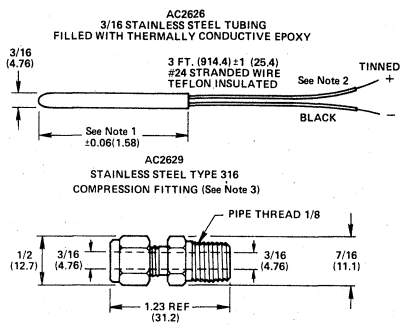


For most applications, a single point calibration is sufficient. With the probe at a known temperature, adjust R_T so that V_O corresponds to the known temperature.

If more detailed information is desired, see the AD590 data sheet and application note.

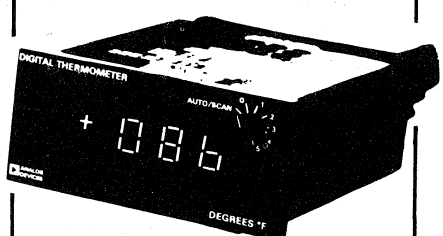
MECHANICAL OUTLINE

(Dimensions shown in inches and (mm)



NOTE 1 Probes are available in 4-inch or 6-inch lengths.
NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue; M, green.
NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

The AD2036, AUTO-SCAN DIGITAL THERMOMETER



UNIQUE COMBINATION OF FEATURES

- Automatic Scan, Manual Selection, or Remote BCD Selection of 6 Thermocouples.
- J, K, or T Thermocouples — °C or °F Display
- One Degree Resolution, Tenth Degree Optional
- Internal Linearization & Cold Junction Compensation
- Isolated Analog Input — Parallel BCD Output
- Designed for Interface with Computers, Printers and Microprocessors

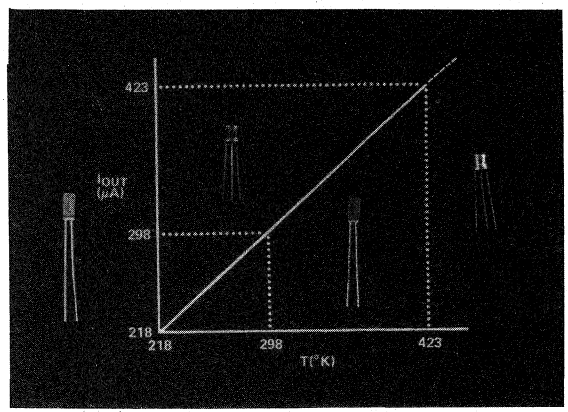
ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590

FEATURES

- **Linear Current Output: 1μA/°K**
- **Wide Range: -55°C to +150°C**
- **Probe Compatible Ceramic Sensor Package**
- **Two-Terminal Device: Voltage In/Current Out**
- **Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)**
- **Excellent Linearity: ±0.3°C Over Full Range Range (AD590M)**
- **Wide Power Supply Range: +4V to +30V**
- **Sensor Isolation from Case**
- **Low Cost**



PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/°K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.
6. The device is hermetically sealed in both a ceramic sensor package and in to TO-52 package. MIL-STD-883 processing to level B is available and, for large unit volumes, special accuracy requirements over limited temperature ranges can be satisfied by selections at final test. The device is also available in chip form.

SPECIFICATIONS (typical @ +25°C and V_S = 5V unless otherwise noted)

MODEL	AD590I	AD590J	AD590K	AD590L	AD590M
ABSOLUTE MAXIMUM RATINGS					
Forward Voltage (E+ to E–)	+44V	*	*	*	*
Reverse Voltage (E+ to E–)	–20V	*	*	*	*
Breakdown Voltage (Case to E+ or E–)	±200V	*	*	*	*
Rated Performance Temperature Range[1]	–55°C to +150°C	*	*	*	*
Storage Temperature Range[1]	–65°C to +155°C	*	*	*	*
Lead Temperature (Soldering, 10 sec)	+300°C	*	*	*	*
POWER SUPPLY					
Operating Voltage Range	+4V to +30V	*	*	*	*
OUTPUT					
Nominal Current Output @ +25°C (298.2°K)	298.2μA	*	*	*	*
Nominal Temperature Coefficient	1μA/°K	*	*	*	*
Calibration Error @ +25°C	±10.0°C max	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error[2] (over rated performance temperature range)					
Without External Calibration Adjustment	±20.0°C max	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
With +25°C Calibration Error Set to Zero	±5.8°C max	±3.0°C max	±2.0°C max	±1.6°C max	±1.0°C max
Nonlinearity	±3.0°C max	±1.5°C max	±0.8°C max	±0.4°C max	±0.3°C max
Repeatability[3]	±0.1°C max	*	*	*	*
Long Term Drift[4]	±0.1°C/month max	*	*	*	*
Current Noise	40pA$\sqrt{\text{Hz}}$	*	*	*	*
Power Supply Rejection					
+4V ≤ V_S ≤ +5V	0.5μA/V	*	*	*	*
+5V ≤ V_S ≤ +15V	0.2μA/V	*	*	*	*
+15V ≤ V_S ≤ +30V	0.1μA/V	*	*	*	*
Case Isolation to Either Lead	$10^{10}\Omega$	*	*	*	*
Effective Shunt Capacitance	100pF	*	*	*	*
Electrical Turn-On Time[5]	20μs	*	*	*	*
Reverse Bias Leakage Current[6] (Reverse Voltage = 10V)	10pA	*	*	*	*

*Specifications same as AD590I

[1] The AD590 has been used at –100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2] See page 8-10 for explanation of error components. Note that ±1°C error is the equivalent of ±1μA error.

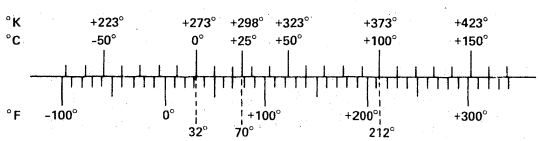
[3] Maximum deviation between +25°C readings after temperature cycling between –55°C and +150°C; guaranteed not tested.

[4] Conditions: constant +5V, constant +125°C; guaranteed, not tested.

[5] Does not include self heating effects; see page 8-11 for explanation of these effects.

[6] Leakage current doubles every 10°C.

Specifications subject to change without notice.



TEMPERATURE SCALE CONVERSION EQUATIONS

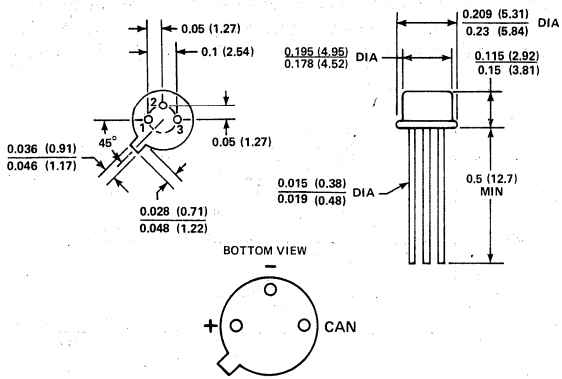
$$^\circ C = \frac{5}{9}(^\circ F - 32) \qquad ^\circ K = ^\circ C + 273.15$$

$$^\circ F = \frac{9}{5}\,^\circ C + 32 \qquad ^\circ R = ^\circ F + 459.7$$

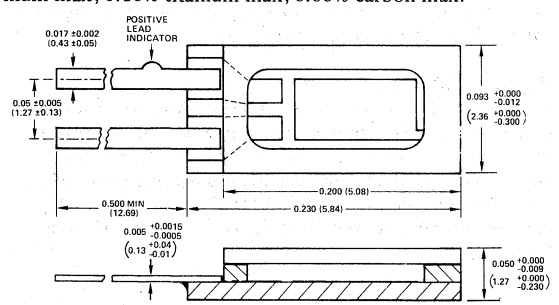
OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).

TO-52 PACKAGE: DESIGNATION "H"

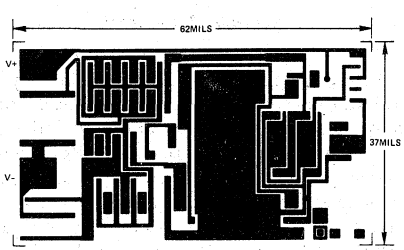


The 590H has 60μ inches of gold plating on its Kovar leads and Kovar header. A resistance welder is used to seal the nickel cap to the header. The AD590 chip is eutectically mounted to the header and ultrasonically bonded to with 1 MIL aluminum wire. Kovar composition: 53% iron nominal; 29% ±1% nickel; 17% ±1% cobalt; 0.65% manganese max; 0.20% silicon max; 0.10% aluminum max; 0.10% magnesium max; 0.10% zirconium max; 0.10% titanium max; 0.06% carbon max.



FLAT-PACK PACKAGE: DESIGNATION "F"

The 590F is a ceramic package with gold plating on its Kovar leads, Kovar lid, and chip cavity. Solder of 80/20 Au/Sn composition is used for the 1.5 mil thick solder ring under the lid. The chip cavity has a nickel underlay between the metalization and the gold plating. The AD590 chip is eutectically mounted in the chip cavity at 410°C and ultrasonically bonded to with 1 mil aluminum wire. Note that the chip is in direct contact with the ceramic base, not the metal lid.



Metalization Diagram

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

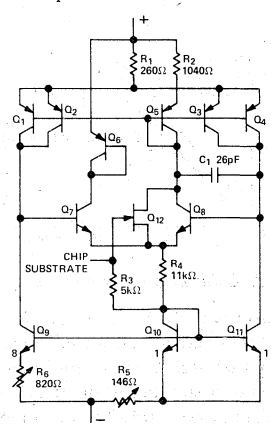


Figure 1. Schematic Diagram

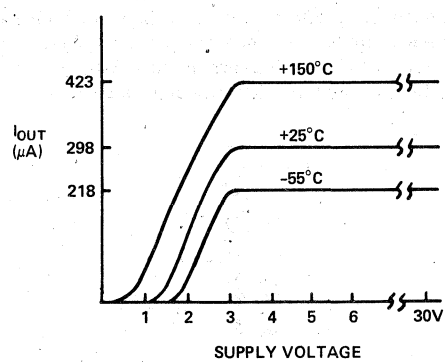


Figure 2. V–I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/°K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2°K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

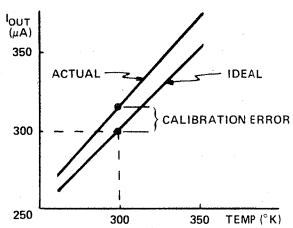


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/°K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

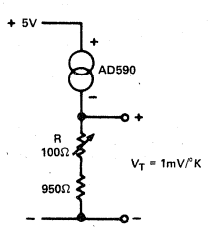


Figure 4. One Temperature Trim

[1] T(°C) = T(°K) - 273.2; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

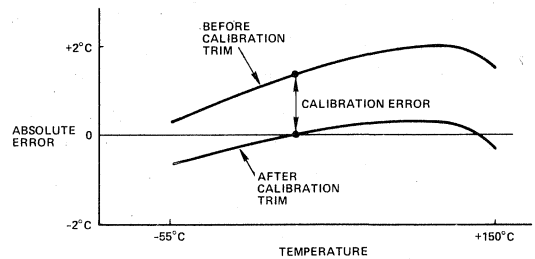


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at -55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

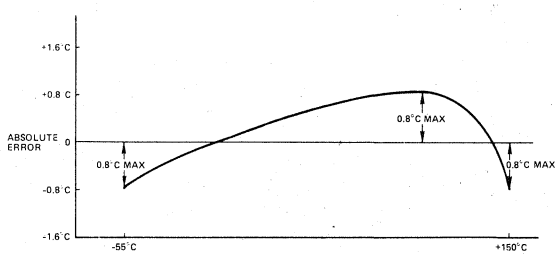


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V- should be at least -4V: if V- is ground there is no voltage applied across the device.

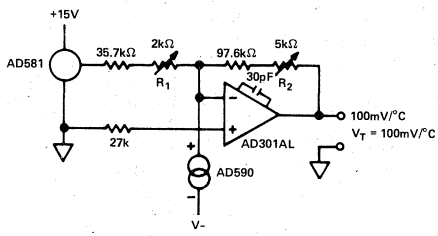


Figure 7A. Two Temperature Trim

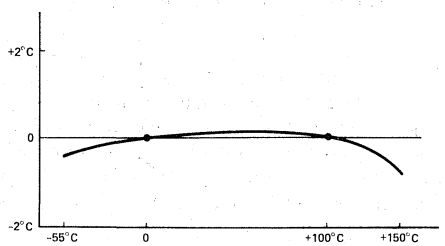


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

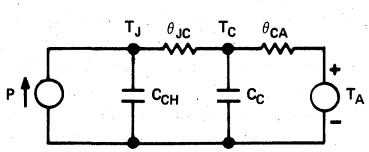


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table 1 gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heat-sink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$ (°C/watt)		τ (sec) (Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	–	5.0	–
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	–	108	–
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.

[2] Air velocity ≅ 9ft/sec.

[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table 1. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T (t). Table 1 shows the effective time constant, τ, for several media.

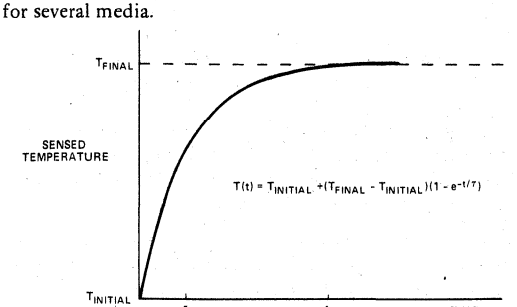


Figure 9. Time Response Curve

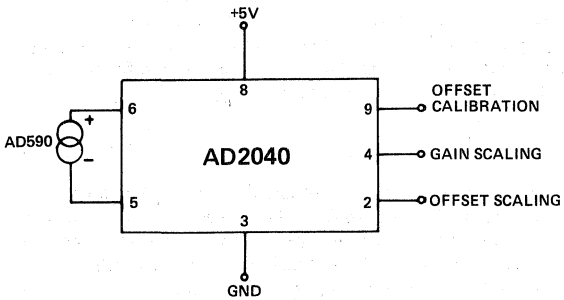


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

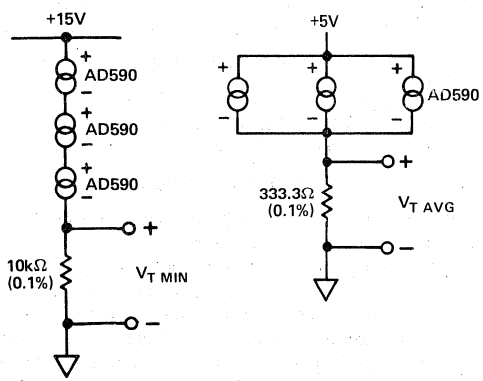


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate

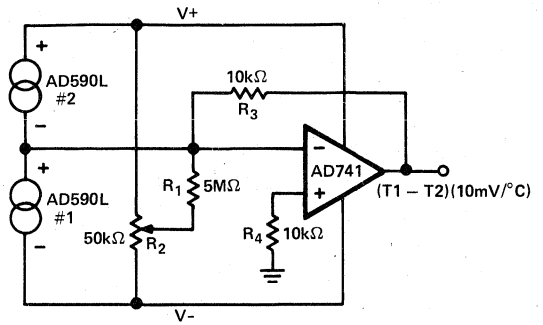


Figure 12. Differential Measurements

a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V– are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

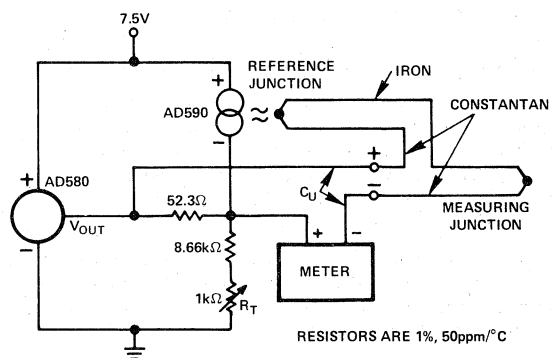


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

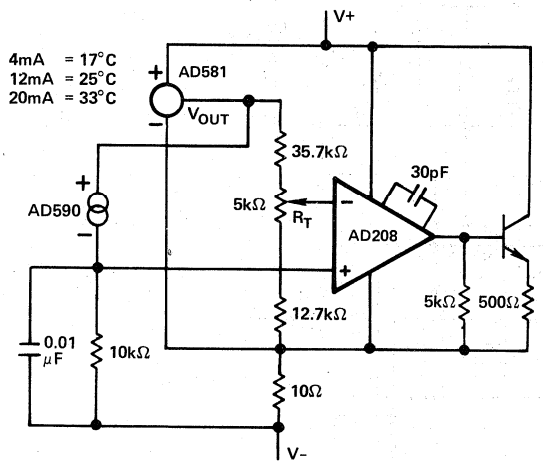


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/°K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

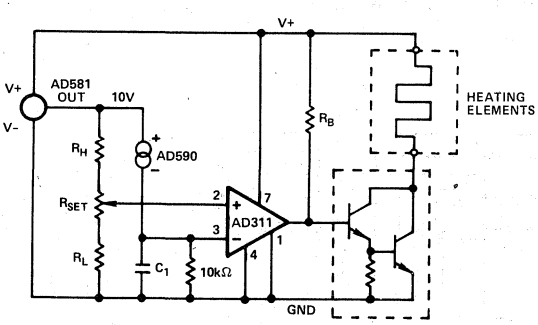


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8 bit DAC to produce a digitally controlled setpoint. This

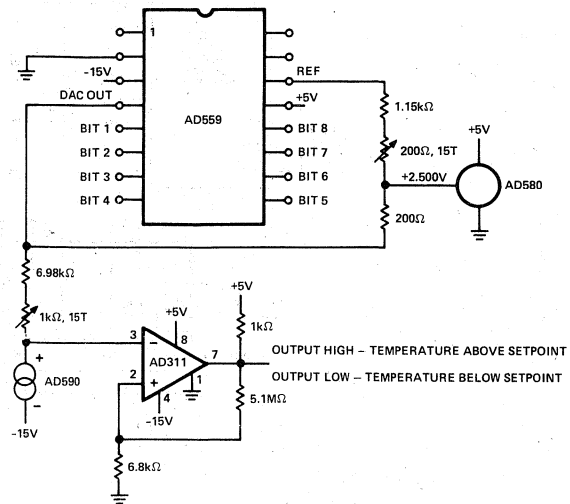


Figure 16. DAC Setpoint

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

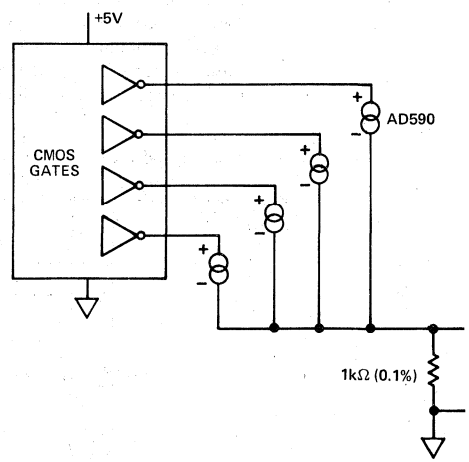


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

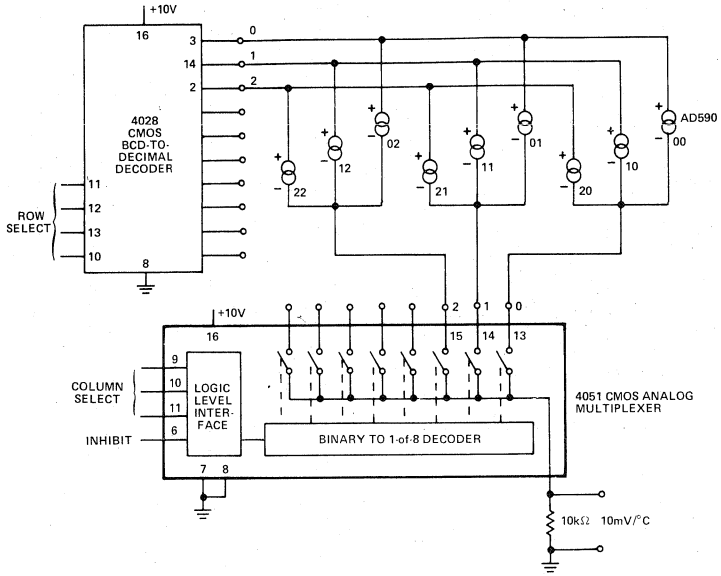


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

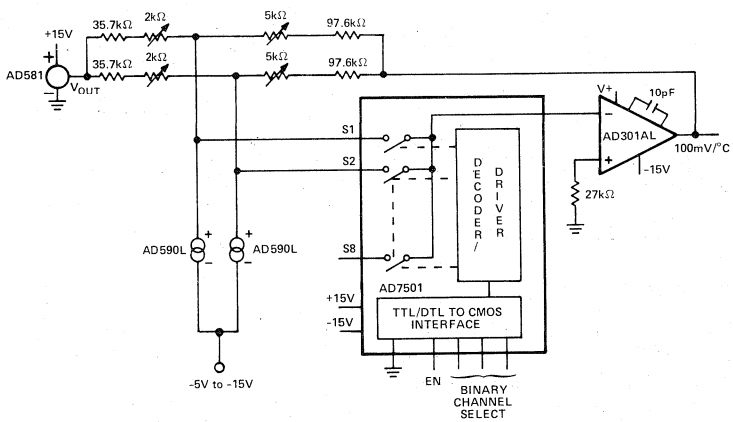


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of −55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

ANALOG DEVICES

6 Channel Scanning Digital Thermometer

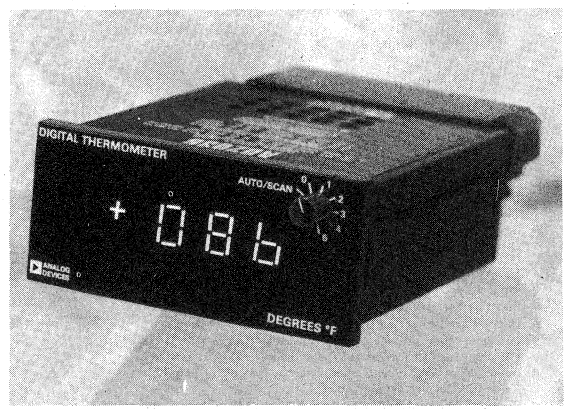
AD2036

FEATURES

Automatic Scan of 6 Thermocouples (TC's)
Manual Selection of Individual TC's
External Channel Selection by BCD Code
J, K, or T Thermocouple
°C or °F Readout
Self-Contained Linearization
Isolated Analog Input
Parallel BCD Output
1° Resolution
+5V dc at 10mA for External Logic

APPLICATIONS

Multi-Point Temperature Measurements for Remote Data Acquisition and Data Logging
Temperature Monitoring in Design, Laboratory, Manufacturing and Quality Control



GENERAL DESCRIPTION

The AD2036 is a low cost 3½ digit, ac line powered digital readout temperature meter. Inputs for six thermocouples of identical types, either J, K, or T and calibrated temperature ranges in °C or °F, make up a total of six available models.

Cycling on an internal clock, the AD2036 can continually scan 6 input channels. Individual channels can be manually selected via a small switch on the front. Channel selection can also be made via an external BCD input at the rear connector. A separate channel select output identifies the selected channel independent of selection mode. The channel select output together with the BCD Output provides complete information for automatic data collection. The Isolated Parallel BCD Output provides an easy interface to conventional recording and controlling instruments. For applications where there are high common mode voltages (CMV) present, the AD2036 has as a standard feature a floating opto isolated analog front end that will withstand CMV's up to 250V rms.

The AD2036 displays readings on large 0.5″ (13mm) high LED displays. Both (+) and (–) polarities are indicated. Controls are provided for blanking the display.

AUTO/SCAN

The AD2036, while in the Auto/Scan mode, will permit unattended scanning of all six input channels. The rate of the channel select is 3.2 seconds, 1.6 seconds or 0.8 seconds. The AD2036 can be used as a stand-alone instrument and with the Scan input held high will continually scan six channels. When the Scan input is brought low the AD2036 will continue to cycle and stop at channel 0. When used with a printer the channel select number in addition to the converted BCD value can be recorded.

MANUAL CHANNEL SELECTION

A switch on the front enables the user to manually select an individual thermocouple. As in the Auto/Scan mode, the BCD Output of the selected channel and the channel number are available. Selection of an individual TC channel automatically disables Scan and external channel selection is overridden. The Mode Output pin indicates when the switch is in this condition. On special order, meters can be supplied with card edge control for disabling the switch.

EXTERNAL CHANNEL SELECTION

For remote control of channel selection the AD2036 provides an input for an external BCD code selection. This feature enables external BCD switch, automatic microprocessor or computer control.

STANDARD PACKAGING

The AD2036 is packaged in Analog Devices' ac line powered DPM case which uses the same panel cutout as most other ac line powered DPMs from other manufacturers. In addition, the pin connections for the AD2036 converter board are the same as for the AD2022, AD2009, AD2016 and DPM's available from several other manufacturers.

SPECIFICATIONS (typical @ +25°C and nominal line voltage unless otherwise specified)

TYPES OF THERMOCOUPLE (TCs): J, K, or T

ACCURACY[1]

°C		Error ±½LSB	°F		Error ±½LSB
J	-60 to 0	±1.4	J	-76 to 32	±2.5
	0 to 500	±1.4		32 to 932	±2.5
	500 to 760	±2.2		932 to 1400	±4.0
K	-60 to 0	±1.4	K	-76 to 32	±2.5
	0 to 150	±1.4		32 to 302	±2.5
	150 to 1350	±2.6		302 to 2000	±4.7
T	-100 to 0	±1.3	T	-148 to 32	±2.3
	0 to 250	±1.5		32 to 450	±2.7
	250 to 400	±2.0		450 to 752	±3.6

DISPLAY OUTPUT
- Light emitting diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload >1999 indicated by flashing display, polarity remains valid. There is no overload indication for out of range readings.
- Decimal points (3) selectable at input connector.
- Display Blanking

SIGNAL INPUT
- Input Impedance: 100MΩ
- Bias Current: 10nA
- Overvoltage Protection Between Channels: ±18V peak max
- Common Mode Voltage: ±350V peak max
- CMV Between Channels: ±6V peak max
- Temperature Coefficient: Span: +temp, 100ppm; -temp, 120ppm Zero: 0.03degrees/degree C or F
- Settling Time to Rated Accuracy: 2.0 seconds (full span step input)
- Normal Mode Rejection: 60dB at 50 – 400Hz
- Common Mode Rejection: 120dB @ 250V rms max CMV (Between TC's and digital gnd), $dv_{cm}/dt < 10^6$ V/sec, 250Ω imbalance

CONVERSION RATE
- 5 conversions per second
- Hold and read on command

CONTROL INPUTS

Display Blanking (TTL Compatible, 3 LSTTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS, TTL Compatible, 1 LSTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated.

Data Hold (TTL Compatible, 1 TTL Load) - Logic "0" or grounding inhibits updating of latched parallel output data of AD2036. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on the normal conversion of the DPM and its display.

Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load) - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection.

Scan (Scan) (CMOS/TTL Compatible, 1 LSTTL Load) - A Logic "1" ("0") for <4 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan pulse while in the switch or external selection mode will initiate a sequence of six readings of the channel that is addressed then stop.

Channel BCD Input (CMOS/TTL Compatible 1 LSTTL Load) - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

Channel Increment (CMOS/TTL Compatible 1 LSTTL Load) - Positive going edge will initiate sequence to the next channel.

Spare Inverter Input (CMOS, TTL Compatible 1 LSTTL Load) - Spare inverter supplied for customer convenience.

DATA OUTPUTS

Isolated Parallel BCD Outputs - 3 BCD digits, Overrange, Overload and Data Ready Outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overload Output is Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity Output (TTL Compatible, 4 TTL Loads latched) indicates positive polarity when high (Logic "1"). Digital outputs are fully isolated from input circuitry; all logic levels are referenced to digital ground.

Channel BCD Outputs (CMOS/TTL Compatible 2 TTL Loads) - BCD Channel number data outputs are positive true.

Mode Output (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control, useful in microcomputer interface.

Data Ready (Data Ready) (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" ("0") indicates data from Temperature Card is ready. Data remains valid until next clock pulse (198ms).

Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads) - Spare inverter supplied for customer convenience.

Clock OUT (CMOS, TTL Compatible, 2 TTL Loads) - Indicates E.O.C. When Clock pulse is high latches are being updated, data is invalid. Data is valid on negative going edge. Clock OUT pulse is disabled when DATA HOLD line is low.

Analog Output - Nonlinear Error ±0.5% ±1mV

V_{OUT}, °C = (1.784mV/°C) Temperature

V_{OUT}, °F = (0.991mV/°F)(T-32)

TEMPERATURE RANGE[2]
- 0 to +50°C Operating
- -25°C to +85°C Storage

POWER OUTPUT
- +5V dc @ 10mA

POWER INPUT
- AC line 50 – 400Hz, See Voltage Options below
- Power Consumption - 5.8W @ 50 – 400Hz
- 12V dc +20% - 10%, 4.8W
- 5V dc ± 5%, 4W

CALIBRATION ADJUSTMENTS
- Span
- Zero
- Recommended Recalibration Interval: six months

SIZE
- 3.92" x 1.67"H x 5.80"D (100 x 42 x 147mm)
- Panel cutout 3.930" x 1.682" (99.8 x 42.7mm)

WEIGHT
- 1.25 pounds (0.568 kg)

DISPLAY LENS[4]

Lens 22-1: Red, °C with ADI Logo
Lens 22-2: Red, °F with ADI Logo

Lens 23-1: Red, °C without ADI Logo
Lens 23-2: Red, °F without ADI Logo

CONNECTORS(2)

2 each, 30 pin, 0.156" spacing card edge connector
Viking 2VK15D/1-2 or equivalent.
Optional: Order AC1501

ORDERING GUIDE

AD2036 □ – □ □ □ □

THERMOCOUPLE TYPE[3]
- J
- K
- T

– ENTER

POWER INPUT[3]
- 117V ac ±10% 1
- 220V ac ±10% 2
- 100V ac ±10% 3
- 240V ac ±10% 4
- 5V dc ±5% 5
- 12V dc +20%, -10% 6

SCAN RATE[3]
- 3.2sec 1
- 1.6sec 2
- 0.8sec 3

– ENTER#

DEGREE READOUT[3]
- °C 1
- °F 2

– ENTER#

RESOLUTION[3]
- 1.0° 1
- 0.1° 2

– ENTER#

NOTES
[1] For 0.1° resolution accuracy remains the same. Range is limited to 200.0°.
[2] Guaranteed
[3] Only one option may be specified.
[4] Lens 22 is supplied if no lens option is specified.

Specifications subject to change without notice.

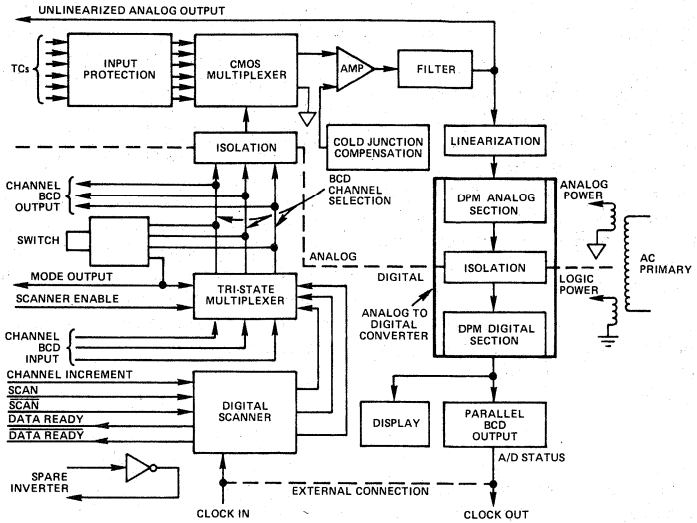


Figure 1. Block Diagram

DESIGNED AND BUILT FOR RELIABILITY

Even beyond the inherent advantages of the LSI IC design and LED displays, the AD2036 has had extreme care taken in its design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic equipment is used to test each DPM, both at the board level and at final assembly, to assure fault free performance. And, prior to shipment, each AD2036 must pass one full week of failure-free +50°C cycled power burn-in.

APPLYING THE AD2036

Description of Operation

The AD2036 Block Diagram is shown in Figure 1. Thermocouple selection is made by the CMOS Multiplexer which is comprised of two sets of six switches. The output of the Multiplexer is on two lines. One is connected to Analog Ground. The other is fed into an Amplifier that provides for Cold-Junction Compensation. The signal is then filtered and linearized and processed by the Analog to Digital Converter. The converter drives the Display and the Parallel BCD Output circuitry.

BCD Channel Selection is obtained from the Switch or the output of the Tri-State Multiplexer. In standard units, switch selection of individual TC Channels always takes precedence over the Tri-State Multiplexer. On special order, units can be wired for card edge enable/disable of the Switch. Under control of the Scanner Enable input, the Tri-State Multiplexer switches between channel selection from the Digital Scanner and the external Channel BCD Input. A logic low enables external selection. A logic high enables input from the Scanner.

As shown in the Timing Diagram of Figure 2, a Channel Scan is initiated by a logic high on the Scan input (pin S). The conclusion of the previous scan cycle will have resulted in Channel "0" already being selected. Conversions take place 5 times per second but 3.2 seconds are allowed to elapse before the Data Ready output indicates the data is valid. A minimum of 2 seconds is required for worst case settling

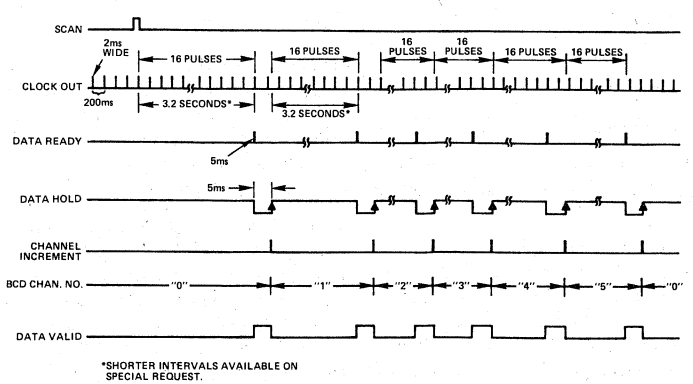


Figure 2. SCAN Timing Diagram

time of a full span step change as could take place in switching channel selection. Where conditions do not warrant the 3.2 second delay, units can be provided with Data Ready occurring after 1.6 seconds or 0.8 seconds. Data can actually be taken up to the maximum 5 per second conversion rate.

In the standard unit, the Data Ready line switches high 16 clock pulses after Scan initiation (approximately 3.2 seconds). The Data Hold input can then be switched low if it is desired to retain the data unchanged for more than the minimum interval of 200ms. Upon releasing the Hold, it is necessary to produce a positive going pulse change on the Channel Increment input in order to step the Channel Selection. In many cases the Data Hold and Channel Increment inputs can be tied together so that release of the Hold will automatically step the Channel Selection.

In this fashion (and as shown in Figure 2) a complete cycle of the six channels can be obtained with the AD2036 stopping on Channel "0" and awaiting another Scan input pulse to signal the start of another cycle.

Operation with Printer

Input and output connections for operating with a printer are shown in Figure 3. A scan of the channels is initiated via push button or other pulse source. When Data Ready goes high, Busy from the printer goes low. This "holds" the Data and Channel Number Outputs until the printer raises the $\overline{\text{Busy}}$. When $\overline{\text{Busy}}$ goes high the "hold" is released and the channel counter is incremented. After 3.2 seconds (in the standard unit), the Data Ready again goes high and the interlocking of signals repeat 5 times until data has been printed for all six channels. Each automatic or manual initiation of the scan causes the sequence to repeat.

To continuously scan all six channels with a printer, set up as in Figure 3 except $\overline{\text{Scan}}$ must be held at Logic "0".

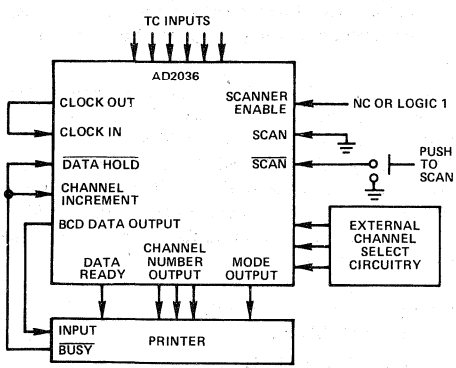


Figure 3. AD2036 with Printer

For continuous printing of a single channel set up as in Figure 3 except fix $\overline{\text{Scan}}$ at Logic "0". Channel can be selected by switch or externally.

For external Channel Selection, the Scanner Enable line should be held low. Under external BCD control, Channel Selection occurs immediately. If the Scan line is pulsed to a logic low, the printer will print the selected channel data 6 times and stop. If held low, a continuous printout of the selected channel will result. +5V power is provided at the rear connector to power external control logic.

Stand-Alone Operation

The AD2036 can at any time under switch control be operated so as to allow examination of individual channels. When used as a stand-alone instrument, it may also be desirable to be able to initiate a single scan of all six inputs. Figure 4 shows the necessary interconnections to obtain this operation. As before, the cycle is initiated via a pulse from a push button or other source. In this case, however, the Data Hold and Channel Increment inputs are controlled by the Data Ready. Each time Data Ready goes from low to high, the channel is incremented and conversions are made on the newly selected channel. The process continues until the meter is back on channel "0". The meter then waits for another scan initiation. During a scan each channel is displayed for 3.2 seconds (the whole scan takes approximately 20 seconds). Simultaneous display of channel number and converted value requires implementation of a separate display for channel number.

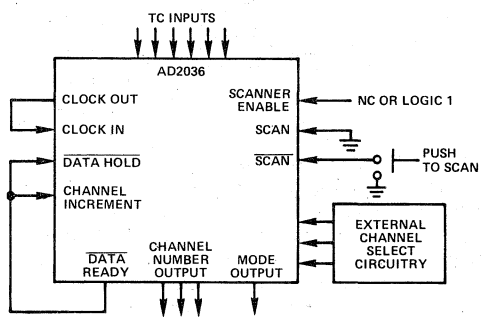


Figure 4. Stand-Alone Operation

To continuously scan, set up as per Figure 4 except fix the $\overline{\text{Scan}}$ input at Logic "0".

Opto Isolation

The AD2036 has as a standard feature Opto Isolation. This prevents external digital load currents from entering the analog circuitry via common ground paths and also enables safe temperature monitoring of equipment where there is no isolation from ac. As shown in the block diagram, Figure 1, digital and analog circuitry as well as the ac are isolated.

Wiring Connections

Power connections, thermocouple connections and control and digital connections are accessible at the rear. All but the thermocouple connections are via card edge (see Figures 6 and 7). Thermocouple wires are connected to a barrier strip on the top board (see Figure 5).

To install thermocouple wires, remove shroud from rear of unit by removing the screw. Feed thermocouple wires through slots in the shroud (see Figure 9). Thermocouple input wires are attached directly to the barrier strip. For easy access turn AD2036 upside down. (+) and (-) polarities are designated on the P.C.B. Care must be taken when connecting input wires to insure correct polarity. Figure 5 shows proper polarity and channel designations. Replace shroud after connecting TC's.

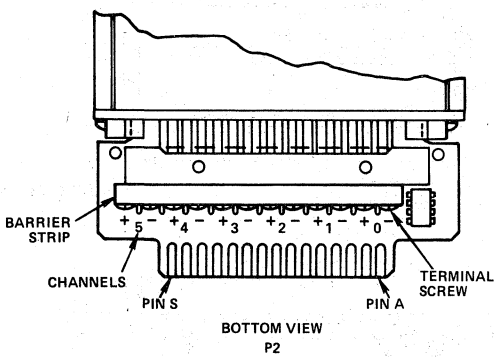


Figure 5. Thermocouple Connections

Power connections, control inputs and digital connections are contained in the pin out diagrams in Figures 6 and 7.

PIN REF	PIN FUNCTION
1	DATA HOLD
2	NC
3	CLOCK OUT
4	POLARITY
5	BCD 8
6	BCD 2
7	BCD 80
8	BCD 20
9	BCD 800
10	ANALOG GROUND
11	BCD 400
12	BCD 200
13	DISPLAY BLANK
14	OVERRANGE
15	AC LINE HIGH

PIN REF	PIN FUNCTION
A	NC (HOLE Y4)
B	NC (HOLE Y5)
C	OVERLOAD
D	CONVERTER HOLD
E	BCD 1
F	BCD 4
H	BCD 10
J	BCD 40
K	BCD 100
L	DP3 XX.X
M	DP2 X.XX
N	DIGITAL GROUND
P	DP1 .XXX
R	SHIELD (EARTH GROUND)
S	AC LINE LOW

KEY

Figure 6. Converter Card Pin Designations, P1

PIN REF	PIN FUNCTION
1	ANALOG GND
2	DATA READY
3	SPARE INVERTER OUTPUT
4	RESERVED FOR FUTURE FUNCTION
5	FACTORY USE
6	MODE OUTPUT
7	CHANNEL INPUT BCD 1
8	NC
9	NC
10	NC
11	NC
12	CLOCK IN
13	CHANNEL OUTPUT BCD 4
14	DIGITAL GND
15	FACTORY USE

PIN REF	PIN FUNCTION
A	ANALOG OUTPUT
B	DATA READY
C	CHANNEL INCREMENT
D	CHANNEL OUTPUT BCD 1
E	FACTORY USE
F	SPARE INVERTER INPUT
H	CHANNEL INPUT BCD 2
J	RESERVED FOR FUTURE FUNCTION
K	CHANNEL OUTPUT BCD 2
L	SCANNER ENABLE
M	RESERVED FOR FUTURE FUNCTION
N	CHANNEL INPUT BCD 4
P	SCAN
R	+5V dc (REF. TO DIG. GRD)
S	SCAN

KEY

Figure 7. Temperature Card Pin Designations, P2

Calibration Procedure

A precision voltage source and pure water Ice Bath are required. Location of the calibration adjusts are shown in Figure 8.

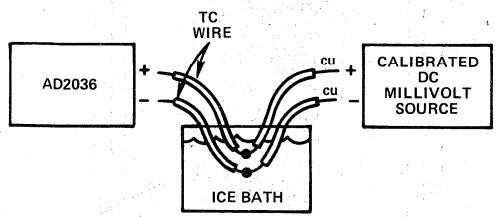


Figure 8. Calibration Diagram

With the voltage source set to zero, adjust the Zero control (top left) for a reading of 000 for Celsius or 032 for Fahrenheit units.

Using Table 1 for the proper thermocouple, set the calibrated voltage source to the appropriate number of millivolts and set span adjust (outer bottom right) for a correct reading.

				Zero Adjust		Span Adjust	
TC	Sensor Type	Color Code	Polarity	Input	Reading	Input/mV	Reading
J	Iron	White	+	0.0mV	0°C	41.013	730°C
	Constantan	Red	−	0.0mV	32°F	41.013	1346°F
K	Chromel	Yellow	+	0.0mV	0°C	52.049	1290°C
	Alumel	Red	−	0.0mV	32°F	42.303	1880°F
T	Copper	Blue	+	0.0mV	0°C	19.516	373°C
	Constantan	Red	−	0.0mV	32°F	19.536	713°F

Table 1. Calibration Chart

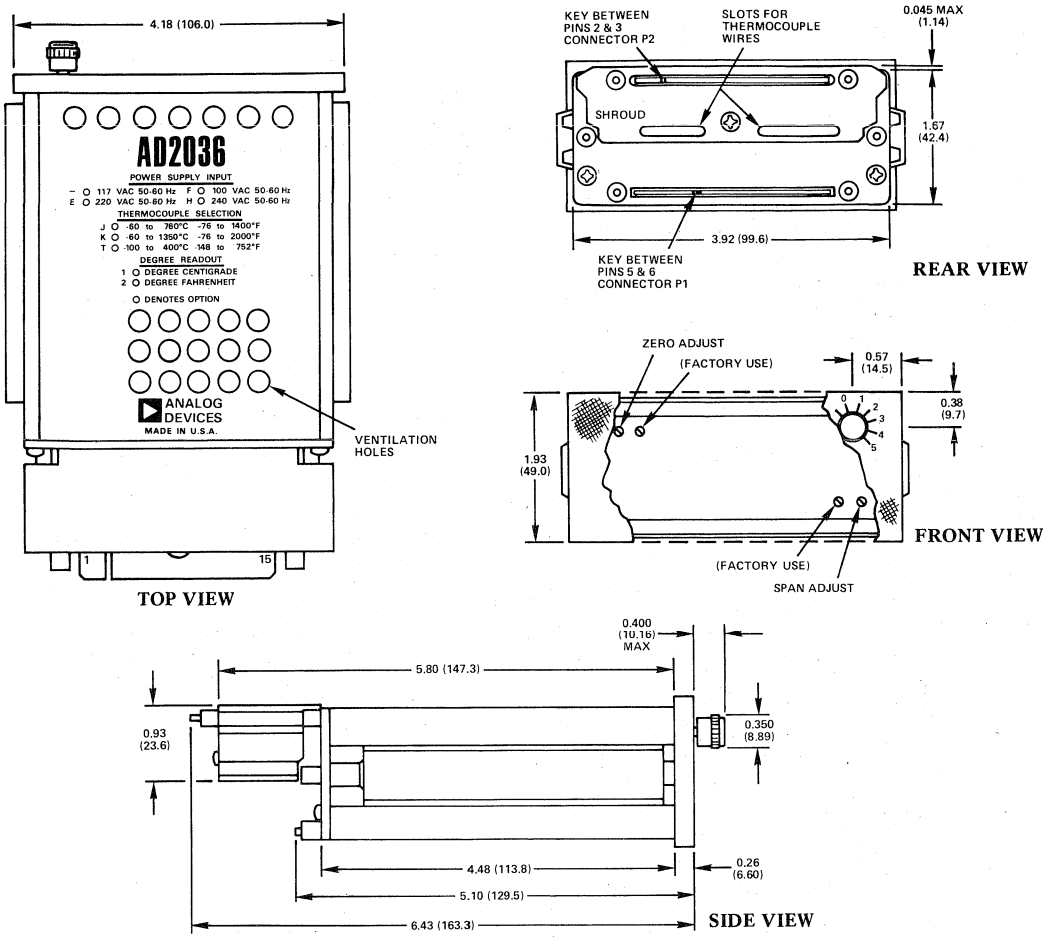


Figure 9. AD2036 Mechanical Outline
(Dimensions shown in inches and (mm))

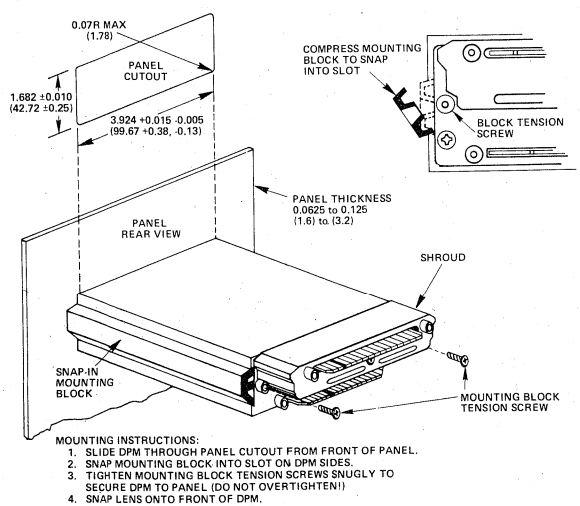


Figure 10. AD2036 Mounting Instructions
(Dimensions shown in inches and (mm))

ANALOG DEVICES

6 Channel Scanning Digital Voltmeter/ Thermometer

AD2037/AD2038

FEATURES

Automatic Scan of 6 Channel Inputs
Manual Selection of Individual Channel
External Channel Selection by BCD Code
±199.9mV or ±1.999V dc Full Scale Range
Isolated Analog Input
Parallel BCD Output
Accessible Gain Points for Implementation of Selectable Gain, to 6V dc F.S.
±12V dc and +5V dc for External Use
AD2038: High Accuracy Temperature Measurements Used with AD590 Transducer
0.1° Resolution; 6 Channels
-55.0°C to +150.0°C (-67.0°F to +199.9°F)

APPLICATIONS

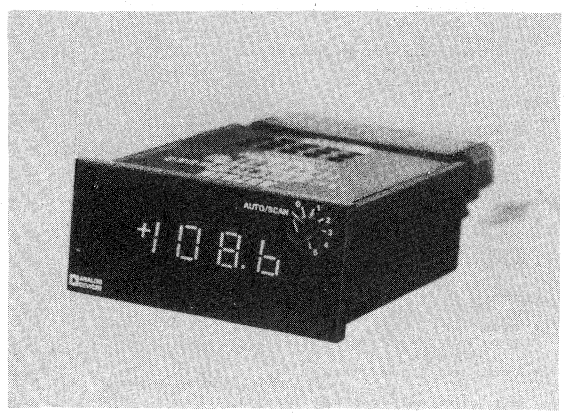
AD2037: Multi-point Measurements for Data Acquisition, Logging and Control
Data Processing from: Pressure and Flow Transducers; RTD and Thermistor Transducers; AD590 Temperature Transducers; LVDT and Level Transducers; Voltage and Current Sources.
AD2038: Temperature Monitoring in Laboratory, Manufacturing, and Quality Control

AD2037 GENERAL DESCRIPTION

The AD2037 is a low-cost 3 1/2 digit, ac line powered, 6 channel digital scanning voltmeter designed to interface to printers, computers, serial data transmitters, telephone lines, etc., for display, control, logging or transmission of multi-channel analog data. With appropriate external signal conditioning on each channel, the AD2037 becomes a versatile building block for a broad range of data acquisition, data logging, or control applications.

Channel selection is made via three methods: manual, using the switch provided on the front; Auto/Scan, where the AD2037 cycling on an internal clock can continually scan the 6 input channels; or External selection, where control inputs provided on the rear connector enables channel selection via external BCD code.

A separate channel select output identifies the selected channel independent of selection mode. The channel select output together with converted BCD output provides complete information for automatic data collection. For applications where there are high common mode voltages (CMV) present, the



AD2037 has as a standard feature, a floating opto isolated analog front end that will withstand CMV's up to 250V rms. The ±199.9mV full scale range or ±1.999V dc full scale range are user selectable via a jumper on the rear connector. Other full scale ranges, to 6V dc, are programmable, via one (1) external resistor.

AD2038 GENERAL DESCRIPTION

The AD2038 is a dedicated 6 channel digital scanning thermometer. Based on the AD2037 and designed to be used in conjunction with Analog Devices' AD590 Temperature Transducer, the AD2038 retains all of the input/output features of the AD2037 as well as the channel selection methods.

The AD2038 and AD590 will measure and display temperatures to ±1.3°C accuracy over the temperature range of -55.0°C to +150.0°C (-67.0°F to 200.0°F), over limited temperature ranges around a calibration point, accuracies approach a few tenths of a degree.

The AD590 is a laser trimmed, two terminal IC Temperature Sensor. Its output is a current (1μA per °K) linearly proportional to absolute temperature thus eliminating the need for

SPECIFICATIONS (typical @ +25°C and nominal power supply voltage)

DISPLAY OUTPUT
- Light emitting diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload indicated by flashing display, polarity remains valid. There is no indication of out of sensor range on AD2038.
- Decimal Points (3) Selectable at Input Connector
- Display Blanking
- Sensor Disconnect Indication same as overload.

ANALOG INPUT
- Opto/Transformer Isolated
- Configuration: Differential, isolated
- ±1.999V dc and ±199.9mV dc Full Scale Range
- Full Scale Range Programmable to 6V dc
- Input Impedance: 250MΩ
- Bias Current: 1.5nA
- Overvoltage Protection: (Continuous Without Damage)
  Normal Mode: ±30V pk
  Channel to Channel: ±30V pk

ACCURACY
AD2037
- ±0.05% Reading ±1 digit[1]
- Resolution: Programmable
- Temperature Range: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: 1.5μV/°C
- Warm-up Time to Rated Accuracy: Less than 5 minutes
- Settling Time to Rated Accuracy: 0.6 seconds (- full scale to + full scale)
- Max Voltage Between Channels: ±199.9mV FS; ±6.1V pk
  ±1.999V FS; ±2.5V pk

ACCURACY
AD2038
- Resolution 0.1°
- Range -55°C to +150°C
  -67°F to +200°F
- Accuracy: (±0.1° digitizing error)[2]

	AD590J	AD590K	AD590L
Sensor calibrated at +25°C (over range)	±2.2°C max	±1.2°C max	±1.2°C max
Uncalibrated Error at +25°C	±5.2°C max	±2.2°C max	±1.2°C max
Uncalibrated Error (over range)	±9.2°C max	±4.0°C max	±2.6°C max
Nonlinearity (over range)	±2.0°C max	±0.5°C max	±0.5°C max

- Temperature Coefficient: Span: 50ppm/°C
  Offset: 0.01 degrees/degree

NORMAL MODE REJECTION
- 50dB at 50 - 60Hz (Additional capacitor filtering may be added between pins A and 4 with degradation of response time)

COMMON MODE REJECTION
- Floated on Power Supply: 120dB at 250V rms max CMV, dV_{cm}/dt 10^6 V/sec max, 1kΩ Imbalance

CONVERSION RATE
- 5 Conversion/sec
- Hold and Read on Command

POWER INPUT
- AC Line 50 - 400Hz, see Voltage Options Below
- Power Consumption - 5.8W @ 50 - 400Hz

ANALOG OUTPUTS
- ±12V dc ±10% @ 10mA (Referenced to Isolation Analog Grd.)
- +5V dc ±5% @ 30mA
- Reference Voltage +6.4V ±1% (Referred to Analog Grd.) 25ppm/°C @ 50μA max output

DATA OUTPUTS

Isolated Parallel BCD Outputs - 3 BCD digits, overrange, overload outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overload output is Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity output (TTL compatible, 4 TTL Loads latched) indicates positive polarity when high (Logic "1"). Digital outputs are fully isolated from input circuitry; all Logic levels reference to digital ground.

Channel Address Outputs (CMOS/TTL Compatible 2 TTL Loads) - BCD Channel number data outputs are positive true.

Mode Output (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control, useful in Microcomputer Interface.

Data Ready (Data Ready) CMOS/TTL Compatible 2 TTL Loads) - Logic "1" ("0") indicates data from Scan Card is ready. Data remains valid until next clock pulse.

Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads) - Spare inverter supplied for customer convenience.

Clock Out (CMOS/TTL Compatible, 2 TTL Loads) - Indicates EOC. When clock pulse is high, latches are being updated, data is invalid. Data is valid on negative going edge for 198ms. Clock Out pulse is disabled when Data Hold line is low.

ANALOG OUTPUT (P2 Pin A): 1mA max output

AD2037: $V_O = K\ V_{IN}$
Where K is gain of programmable input amplifier. (K = 1 for 1.999V F.S. and K = 10 for 199.9mV)

AD2038: $V_O = (18.95mV/°C)T$ for T = °C
$V_O = (10.53mV/°F)(T-32)$ for T = °F
error = ±6mV

Notes:
[1] Guaranteed at 200mV full scale at +25°C and nominal power supply.
[2] Overall accuracy of meter plus sensor over entire sensor range (guaranteed max) Meter is factory calibrated for ideal sensor.
[3] Lens 22 (AD2038) Lens 28 (AD2037) supplied if no lens option is specified.
[4] Only one option may be specified.

Specifications subject to change without notice.

CONTROL INPUTS

Display Blanking (TTL Compatible, 3 LSTTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS/TTL Compatible, 1 LSTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated.

Data Hold (TTL Compatible, 1 TTL Load) - Logic "0" inhibits updating of latched parallel output data. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on normal conversion of the DPM and its display.

Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load) - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection.

Scan (Scan)(CMOS/TTL Compatible, 1 LSTTL Load) - A Logic "1" ("0") for <4 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan pulse while in the switch or external mode will initiate a sequence of six readings of the channel that is addressed then stop.

Channel Address Input (CMOS/TTL Compatible 1 LSTTL Load) - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

Channel Address Increment (CMOS/TTL Compatible 1 LSTTL Load) - Positive going edge will initiate sequence to the next channel.

Spare Inverter Input (CMOS/TTL Compatible 1 LSTTL Load) - Spare inverter supplied for customer convenience.

CALIBRATION ADJUSTMENTS
- Gain
- Offset, Course
- Offset, Fine
- Span/per Channel (AD2038 only)
- Recommended Recalibration Interval: Six Months

SIZE
- 3.92" x 1.67"H x 5.80"D (100 x 42 x 147mm)
- Panel Cutout 3.930" x 1.682" (99.8 x 42.7mm)

WEIGHT
- 1.25 pounds (0.563 kg)

OPTIONS[3]

AD2037	Lens: 28 Red with ADI Logo
	Lens: 27 Red without ADI Logo
AD2038	Lens 22-1, Red °C with ADI Logo
	Lens 22-2, Red °F with ADI Logo
	Lens 23-1, Red °C without ADI Logo
	Lens 23-2, Red °F without ADI Logo

CONNECTORS (2)
2 each, 30 pin, 0.156" Spacing Card Edge Connector
Viking 2Vk 15/1-2 or Equivalent
Optional: Order AC1501

ORDERING GUIDE

AD2037 or AD2038 -

POWER INPUT[4]
- 117V ac ±10% — 1
- 220V ac ±10% — 2
- 100V ac ±10% — 3
- 240V ac ±10% — 4

} Enter

SCAN RATE[4]
- 3.2 sec — 1
- 1.6 sec — 2
- 0.8 sec — 3

} Enter

TEMPERATURE SCALE READOUT (AD2038 Only)[4]
- °C — 1
- °F — 2

} Enter

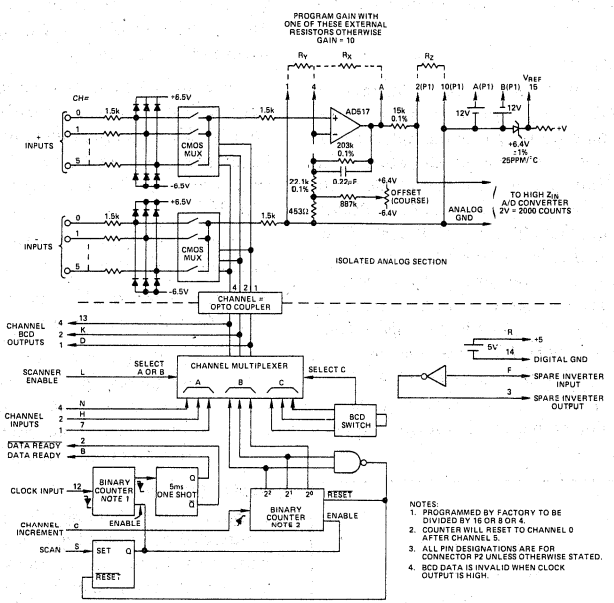


Figure 1. AD2037 Block Diagram

linearization and cold junction compensation. Just connect the sensors to the rear terminal block, calibrate them if necessary, and the AD2038 is ready to make measurements.

Due to the AD590's high impedance current output, it is insensitive to voltage drops over long lines thus enabling remote monitoring with no need for costly transmitters or special wire.

For normal applications the AD590J can be used and calibrated at a single temperature point. Where better linearity or sensor interchangeability is needed, the "K" and "L" versions are available. All versions are available to MIL-STD-883A Class B processing. In addition, the AC2626 (an AD590JF mounted in a 3/16 inch diameter, by 6 inch long stainless steel probe) will soon be available. The probe will be supplied with 3 feet of wire for easy interface to the AD2038.

AUTO/SCAN

The AD2037/38 while in the Auto/Scan mode, will permit unattended scanning of all six input channels. The rate of the channel select is 3.2 seconds, 1.6 seconds or 0.8 seconds per channel. The AD2037 or AD2038 can be used as a stand-alone instrument and with the Scan input held high will continually scan six channels. When the Scan input is brought low the AD2037/38 will continue to cycle and stop at Channel "0".

MANUAL CHANNEL SELECTION

A switch on the front enables the user to manually select an individual channel input. As in the Auto/Scan mode, the BCD output of the selected channel and the channel number are available. Selection of an individual channel automatically disables scan and external channel selection is overridden. The Mode Output pin indicates when the switch is in this condition. On special order, meters can be supplied with card edge control for disabling the switch.

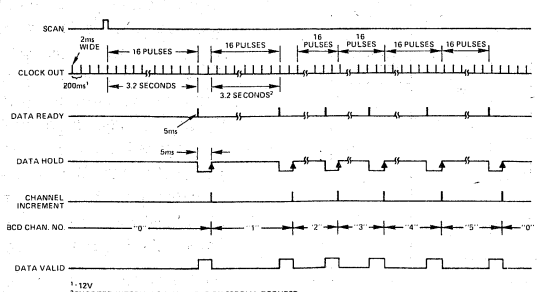


Figure 2. Scan Timing Diagram

EXTERNAL CHANNEL SELECTION

For remote control of channel selection, the AD2037/38 provides inputs for an external BCD code selection. This feature allows external switch, microprocessor or computer control.

CIRCUIT DESCRIPTION, AD2037

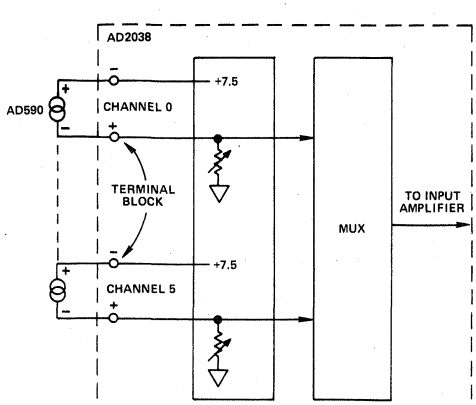
The AD2037 Block Diagram is shown in Figure 1. Channel selection is made by the CMOS Multiplexer which is comprised of two sets of six switches. The output of the multiplexer is on two lines. One is connected to Analog.Ground, the other is fed into an amplifier, where the Gain, when desirable, is selectable. The AD2037 is supplied from the factory with all Gain Points open and Gain equal to 10 (ten) for 199.9mV Full Scale. The 1.999V dc Full Scale (VFS) setting is accomplished via a jumper from Pin A to Pin 4 of P2. To select Full Scales less than 199.9mV (Gain >10) place a resistor, computed from formula in Table 1, between Pins 1 and 4 of P2. Similarly for Full Scale settings greater than 1.999V place the resistor between Pins 10 and 2 of P1 and jumper Pin A to Pin 4 of P2. In each case the signal is then filtered and processed by the Analog to Digital Converter. The converter drives the Display and the Parallel BCD Output.

FULL SCALE RANGE	
Less than 200mV	$R_y = \frac{203K}{\left(\frac{2}{VFS}\right) - 10}$
200mV to 2 Volts	$R_x = \frac{203K\ (2 - VFS)}{10VFS - 2}$
2 Volts to 6 Volts	$R_z = \frac{30K}{(VFS - 2)}$

Table 1.

CIRCUIT DESCRIPTION, AD2038

The AD2038 simplified Block Diagram is shown in Figure 3. The AD2037 together with a dedicated signal conditioning card, make up the AD2038. The selected sensor will transmit a current to the AD2038. The signal conditioning card converts the current from the appropriate AD590 to a voltage which is then measured and displayed. AD590 connection is accomplished at the terminal block on the rear.



NOTE: ATTACH SENSOR POLARITY INVERSELY TO THE METER, + OF SENSOR TO CHANNEL - INPUT; - OF SENSOR TO CHANNEL + INPUT.

Figure 3. AD2038 Diagram

CHANNEL SELECTION

As shown in Figure 1, Channel Selection is obtained by one of the three methods via the Channel Multiplexer. In method A, Channel selection is under external BCD logic control, in Method B, control is via the digital scanning circuitry. In Method C control is by the Front Panel Switch.

The method of channel selection is under control of the Scanner Enable input. A logic low enables external BCD logic control (Method A). A logic high enables internal scanning circuitry selection (Method B). In standard units, Front Panel switch selection (Method C) overrides selection by Methods A or B.

On special order, units can be wired for card edge enable/disable control of the switch.

The three methods allow the user to select his mode of operations: (See Figures 4 and 5).

- Continuous scan of 6 Channels
- Single scan of 6 Channels
- Continuous scan of an individual Channel
- Single scan of an individual Channel
- Individual Channel selection

SCAN TIMING

As shown in the Timing Diagram of Figure 2, a Channel Scan is initiated by a logic high on the Scan input (pin S). The conclusion of the previous scan cycle will have resulted in Channel "0" already being selected. Conversions take place 5 times per second but 3.2 seconds are allowed to elapse before the Data Ready output indicates the data is valid. 0.6 seconds is required for worst case settling time of a full span step change as could take place in switching channels. Where conditions do not warrant the 3.2 second delay, units can be provided with Data Ready occurring after 1.6 seconds or 0.8 seconds.

In the standard unit, the Data Ready line switches high 16 clock pulses after Scan initiation (approximately 3.2 seconds). The Data Hold input can then be switched low if it is desired to retain the data unchanged for more than the minimum interval of 198ms. Upon releasing the Hold, it is necessary to produce a positive going pulse change on the Channel Increment input in order to step the Channel Selection. In many cases the Data Hold and Channel Increment inputs can be tied together so that release of the Hold will automatically step the Channel Selection.

In this fashion (and as shown in Figure 2) a complete cycle of the six channels can be obtained with the AD2037/38 stopping on Channel "0" and awaiting another Scan input pulse to signal the start of another cycle.

OPERATION WITH PRINTER

Input and output connections for operating with a printer are shown in Figure 4. A scan of the channels is initiated via push *button* or other pulse source. When Data Ready goes high, $\overline{\text{Busy}}$ output from the printer goes low. This "holds" the Data and Channel Number Outputs until the printer raises the $\overline{\text{Busy}}$. When $\overline{\text{Busy}}$ goes high the "hold" is released and the channel counter is incremented. After 3.2 seconds (in the standard unit), the Data Ready again goes high and the interlocking of signals repeat 5 times until data has been printed for all six channels. Each automatic or manual initiation of the scan causes the sequence to repeat.

To continuously scan all six channels with a printer, set up as in Figure 4 except $\overline{\text{Scan}}$ must be held at Logic "0".

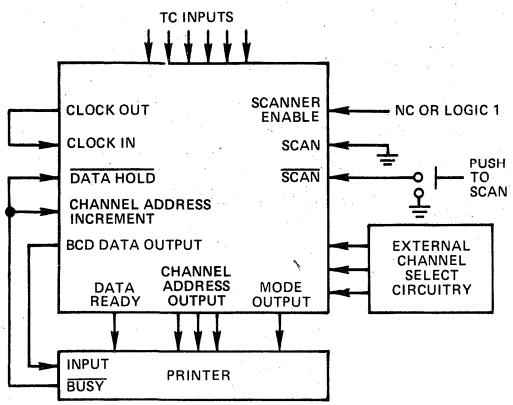


Figure 4. Operation with Printer

For continuous printing of a single channel set up as in Figure 4 except fix Scan at Logic "0". Channel can be selected by Front Panel switch or externally.

For external Channel Selection, the Scanner Enable line should be held low. Under external BCD control, Channel Selection occurs immediately. If the Scan line is pulsed to a logic low, the printer will print the selected channel data 6 times and stop. If held low, a continuous printout of the selected channel will result. +5V power is provided at the rear connector to power external control logic.

STAND-ALONE OPERATION

The AD2037/AD2038 can at any time, under Front Panel switch control, be operated so as to allow examination of individual channels. When used as a stand-alone instrument, it may also be desirable to initiate a single scan of all six inputs. Figure 5 shows the necessary interconnections to obtain this operation. As before, the cycle is initiated via a pulse from a

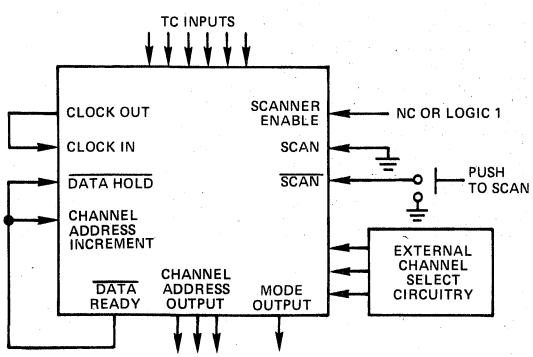


Figure 5. Stand-Alone Operation

push button or other source. In this case, however, the Data Hold and Channel Address Increment inputs are controlled by the Data Ready. Each time Data Ready goes from low to high, the channel is incremented and conversions are made on the newly selected channel. The process continues until the meter is back on Channel "0". The meter then waits for another scan initiation. During a scan each channel is displayed for 3.2 seconds (the whole scan takes approximately 20 seconds). Simultaneous display of channel number and converted value requires implementation of a separate display for channel number (see Figure 11).

To continuously scan, set up as per Figure 5 except fix the Scan input at Logic "0".

AD2037 CALIBRATION PROCEDURE

A precision voltage reference is needed for the calibration of the AD2037. The location of the calibration potentiometers is shown in Figure 14.

Offset adjustment – with Front Panel switch on Channel "0", short Channel "0" input and adjust offset potentiometer until the meter reads 000.

Gain adjustment – remove jumper from Channel "0" and apply an input of 0.9 times the programmed Full Scale Voltage. Vary gain adjust potentiometer until the meter reads 1800 exactly.

AD2038 CALIBRATION PROCEDURE

The AD2038 is factory calibrated in either °C or °F using an ideal sensor, and can be used directly if sensor accuracy is adequate. For maximum accuracy with any grade sensor, the calibration procedure is as follows:

Initial Calibration:

1. Attach sensors to Channel inputs. Polarity of the sensor must be connected inversely to the meter, + of sensor to Channel - input; - of sensor to Channel + input.
2. Set Front Panel Switch to Channel "0".
3. With sensor at a known temperature adjust the appropriate Span Adjust potentiometer on the rear (See Figure 14) for a reading on the AD2038 equal to the temperature.
4. Repeat step 3 for each sensor on each Channel making sure to turn Front Panel Switch to the appropriate Channel.

6 Month Calibration °C (°F)

A 4 1/2 Digit precision DVM and a resistance decade box are needed. The location of the calibration potentiometers are shown in Figure 14.

1. Set Front Panel Switch on Channel "Zero."
2. With sensor disconnected adjust Course Offset pot on the front for V_A = (between Pin A and Pin 1 of P2) = -5.1764 Volts.
3. Attach resistance decade box to sensor input (Channel "0").
4. Adjust resistance box until V_A = 0.000V (-0.3368V).
5. Adjust Fine Offset Adjust until the meter reading = 00.0.
6. Adjust resistance box until V_A = +3.6000V (+1.6632V).
7. Adjust Gain Adjust on the front until the meter reading = +190.0.
8. Attach AD590 Sensors. Polarity of the sensor must be connected inversely to the meter, + of sensor to Channel

- Input; - of sensor to Channel + Input.

9. With sensors at a known temperature (Front Panel Switch still on Channel "0"), adjust the appropriate Span Adjust on the rear for that temperature readout on the AD2038.
10. Repeat step 9 for each sensor on each Channel making sure to turn Front Panel Switch to the appropriate Channel.

WIRING CONNECTIONS

All connections are accessible at the read. All but the signal input connections are via card edge (see Figures 7 and 8). Signal Inputs are connected to a terminal block on the top board (see Figure 6).

Power connections, control inputs and digital connections are contained in the pin out diagrams in Figures 7 and 8.

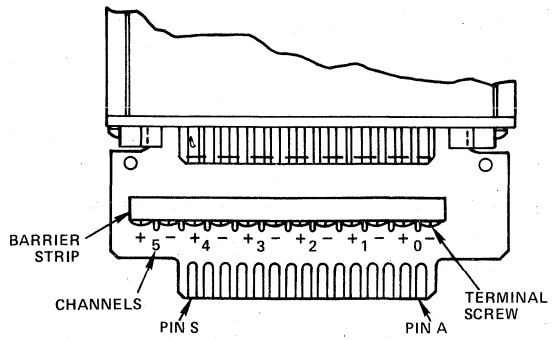


Figure 6.

PIN REF	PIN FUNCTION
1	$\overline{\text{DATA HOLD}}$
2	PROGRAMMABLE GAIN
3	CLOCK OUT
4	POLARITY
5	BCD 8
6	BCD 2
7	BCD 80
8	BCD 20
9	BCD 800
10	ANALOG GROUND
11	BCD 400
12	BCD 200
13	$\overline{\text{DISPLAY BLANK}}$
14	OVERRANGE
15	AC LINE HIGH

KEY

PIN REF	PIN FUNCTION
A	+12V dc (REF. TO ANALOG GRD)
B	-12V dc (REF. TO ANALOG GRD)
C	$\overline{\text{OVERLOAD}}$
D	$\overline{\text{CONVERTER HOLD}}$
E	BCD 1
F	BCD 4
H	BCD 10
J	BCD 40
K	BCD 100
L	DP3 XX.X
M	DP2 X.XX
N	DIGITAL GROUND
P	DP1 .XXX
R	SHIELD (EARTH GROUND)
S	AC LINE LOW

Figure 7. Converter Card Pin Designations, P1

PIN REF	PIN FUNCTION
1	ANALOG GND
2	$\overline{\text{DATA READY}}$
3	SPARE INVERTER OUTPUT
4	SELECTABLE GAIN AND OFFSET
5	FACTORY USE
6	MODE OUTPUT
7	CHANNEL ADDRESS INPUT BCD 1
8	NC
9	NC
10	NC
11	NC
12	CLOCK IN
13	CHANNEL ADDRESS OUTPUT BCD 4
14	DIGITAL GND
15	V_{REF}

KEY

KEY

PIN REF	PIN FUNCTION
A	ANALOG OUTPUT
B	DATA READY
C	CHANNEL ADDRESS INCREMENT
D	CHANNEL ADDRESS OUTPUT BCD 1
E	FACTORY USE
F	SPARE INVERTER INPUT
H	CHANNEL ADDRESS INPUT BCD 2
J	RESERVED FOR FUTURE FUNCTION
K	CHANNEL ADDRESS OUTPUT BCD 2
L	SCANNER ENABLE
M	RESERVED FOR FUTURE FUNCTION
N	CHANNEL ADDRESS INPUT BCD 4
P	$\overline{\text{SCAN}}$
R	+5V dc (REF. TO DIG. GRD)
S	SCAN

Figure 8. P2

PRESSURE METER

The pressure meter shown in Figure 9 is programmed for 0 - 100.0 PSI. The Programmable Gain and Offset features allow readout in any engineering units.

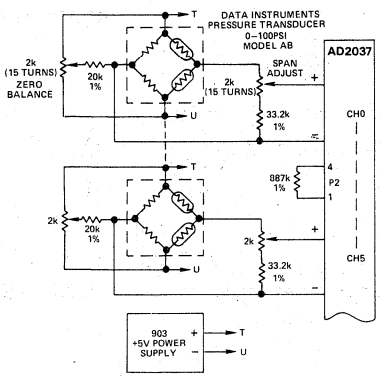


Figure 9. Pressure Meter

The signal voltage appearing across the output leads of the transducer is both a function of the applied pressure and the excitation voltage. At no load, a small residual output voltage will be present. This voltage can be nulled out using the Zero Balance potentiometer. Transducer span inaccuracies are calibrated via the Span Adjust potentiometer. The differential, isolated front end of the AD2037 rejects the 2.5V CMV of the strain gauge. At no time should the Analog Ground be connected to any portion of the pressure transducer circuitry.

RTD THERMOMETER

Figure 10 shows a 3 wire, 0.1° resolution, nonlinearized RTD circuit. For many applications where repeatability is required linearization is not necessary. The transistor, resistor (R1) and potentiometer on each Channel form a 1.5mA current source.

This current through the RTD resistive element is converted to a voltage which is proportional to absolute temperature and measured by the AD2037. Conversion from absolute temperature to °C or °F requires on offset which is produced by the reference of the AD2037 and R_O.

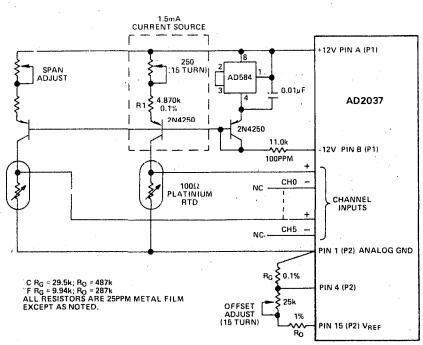


Figure 10. RTD Thermometer

NOTE: More detailed applications assistance available from factory.

REMOTE CHANNEL INDICATOR

The Channel number is displayed on a three tenth inch (0.3″) high efficiency, common cathode Hewlett Packard Display. The Channel BCD output feeds a seven segment decoder driver which in turn drives the LED. Power is supplied from Pin R (+5V) on P2.

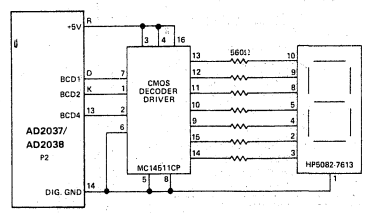


Figure 11. Remote Channel Indicator

LINEAR THERMISTOR THERMOMETER

For applications where the user is committed to or desires thermistor type sensors, the AD2037 is easily interfaced. The Linear Thermistor Thermometer, shown in Figure 12, uses the YSI42201. Linear Thermistors are available in various type probes for many medical, scientific and industrial applications.

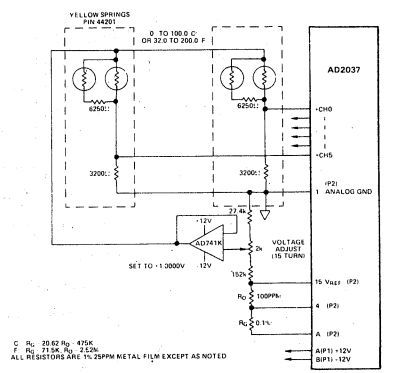


Figure 12. Linear Thermistor Thermometer

PROCESS MONITOR

As shown in Figure 13, the AD2037 provides scanning and digital readout for six (6) standard 4-20mA current loops. The AD2037 is programmed for 0-100.0% Readout. Other readout ranges can be accommodated by changing the Gain and Offset programming resistors.

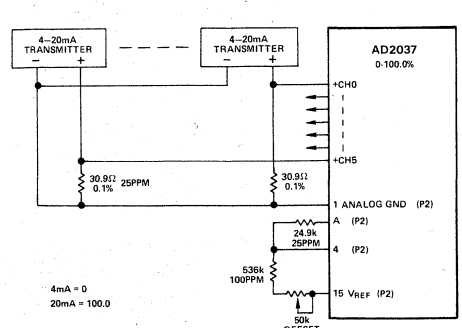


Figure 13. Process Monitor

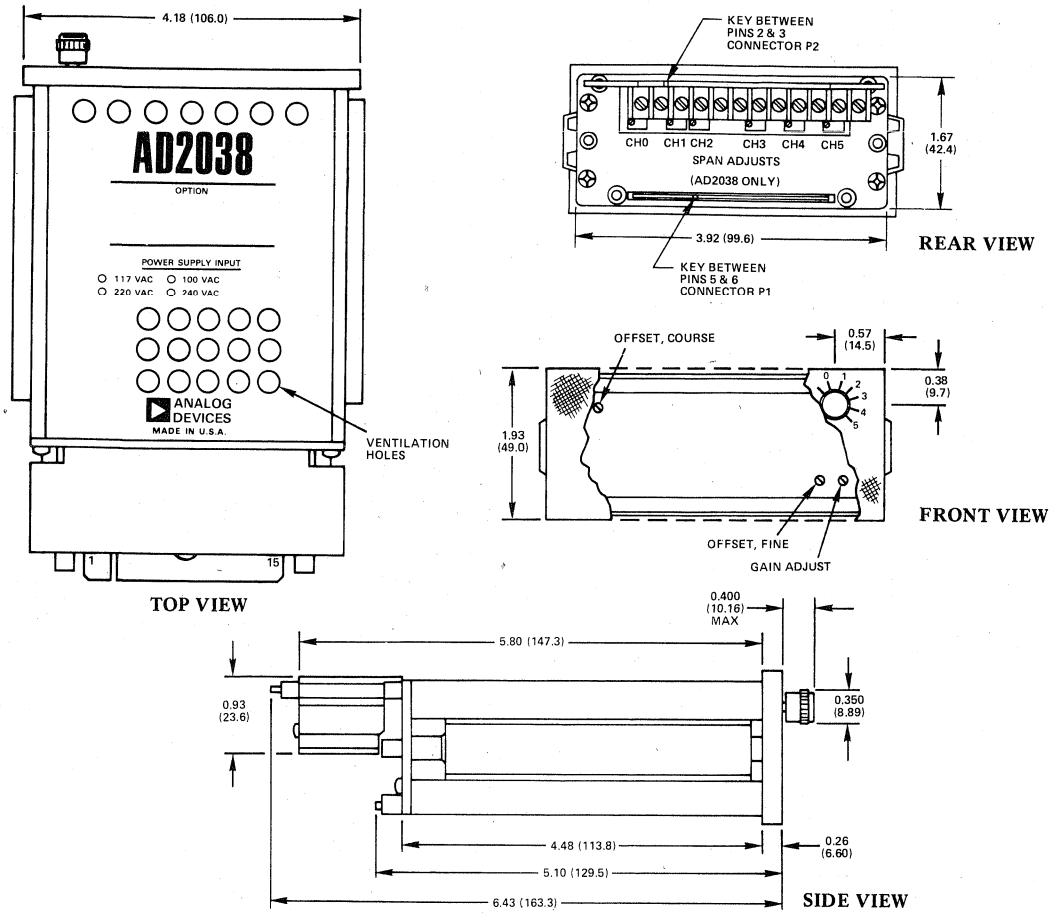
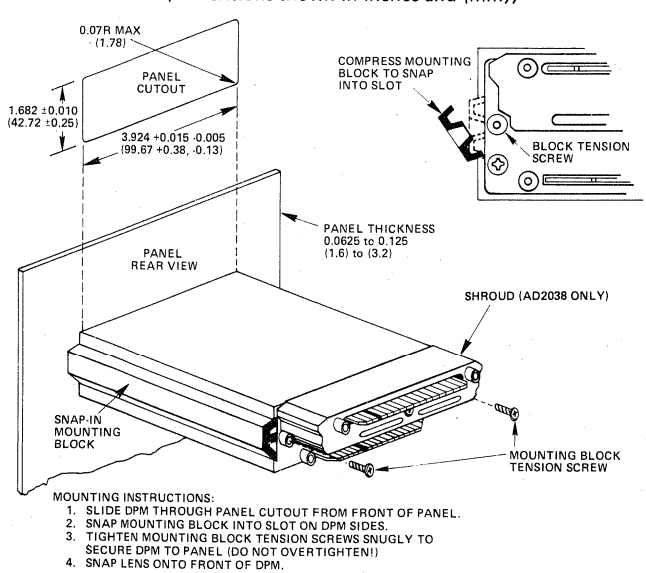


Figure 14. AD2037/38 Mechanical Outline
(Dimensions shown in inches and (mm))



MOUNTING INSTRUCTIONS:
1. SLIDE DPM THROUGH PANEL CUTOUT FROM FRONT OF PANEL.
2. SNAP MOUNTING BLOCK INTO SLOT ON DPM SIDES.
3. TIGHTEN MOUNTING BLOCK TENSION SCREWS SNUGLY TO SECURE DPM TO PANEL (DO NOT OVERTIGHTEN!)
4. SNAP LENS ONTO FRONT OF DPM.

Figure 15. AD2037/38 Mounting Instructions
(Dimensions shown in inches and (mm))

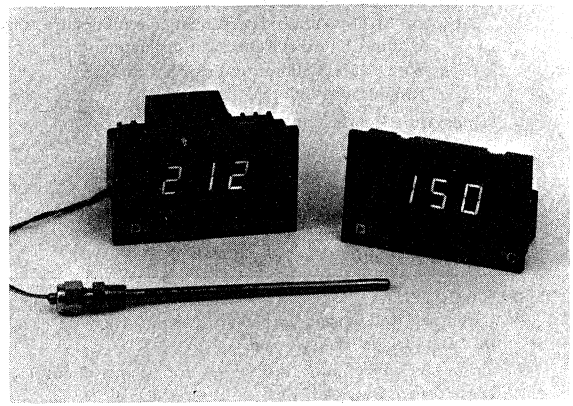
ANALOG DEVICES

Low Cost Temperature Indicator

AD2040

FEATURES
Low Cost
Direct Interface to AD590 or AC2626
Large 0.56″ Red Orange LED Display
Accuracy to ±1.0° ±1 Digit
Either ac Line or +5V dc Powered
Temperature Range: -55°C to +150°C
-67°F to +302°F
1000V rms Isolation (ac)
Terminal Block Interface
Small Size, Panel Mount

APPLICATIONS
Temperature Monitoring in Design, Laboratory, Manufacturing and Quality Control for Both +5V dc or Line Powered Applications



GENERAL DESCRIPTION

The AD2040 is a low-cost 3 digit temperature indicator. Based on the highly successful AD2026 low-cost DPM and designed to be used in conjunction with Analog Devices' AC2626 general purpose probe or the AD590 temperature transducer, the AD2040 is available in both 5V logic-powered, or ac line-powered versions.

The 5V AD2040 reads out directly in °C, °F, °R or K. A precision voltage reference, resistor network, and span and zero adjusts, needed to implement display of the different temperature scales, are all self-contained. User selectable degree readout, as well as all other connections, i.e., +5V power and sensor or probe interface, are all made via a terminal block on the rear.

For many stand-alone temperature measurement applications, i.e., in factories, labs, ovens, inspection stations, etc., +5V dc power is not available. For these applications, the AD2040 is available in an ac version. The ac-powered version retains all of the features of the 5V version, with exception of the user selectable degree readout. °C or °F must be specified when ordering (see Ordering Guide).

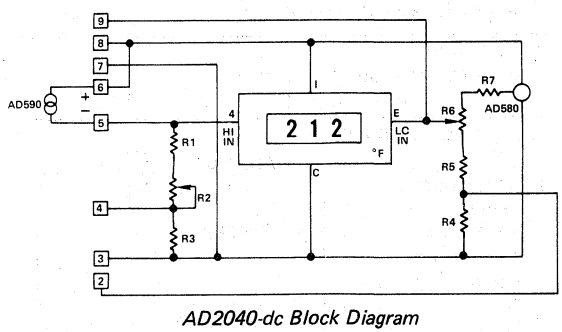
If required, calibration adjustments are easily accessible. No mounting hardware of any kind is used.

The AD2040 and AC2626 or AD590 will measure and display temperatures on large 0.56″ orange LED displays from -55°C to +150°C (-67°F to +302°F) with accuracy to ±1.0° ±1 digit. Reliability is assured with the inherent simplicity and accuracy of the sensor, combined with the highly efficient design of the AD2040.

THE SENSOR

The AD590 is a laser-calibrated, two terminal IC temperature transducer. Its output is a current (1μA per K) linearly proportional to absolute temperature, thus eliminating the need for costly linearization and cold junction compensation.

Due to the AD590's high impedance current output, it is insensitive to voltage drops over long lines thus enabling remote monitoring with no need for costly transmitters or special wire.



AD2040-dc Block Diagram

Above is a block diagram of the AD2040, showing the AD2026 DPM input, the current-to-voltage conversion resistors (R1, R2, R3), the offsetting resistance network (R4, R5, R6, R7), and the connections to the terminal strip. Attenuated voltage from the AD580, 2.5V reference, provides the offsets for readout on the F and C scales. On the AD2040 dc version, jumpers are connected by the user at the terminal strip to select the appropriate units of temperature for display. °C or °F must be specified when ordering the ac version (see Ordering Guide).

SPECIFICATIONS (typical @ +25°C and nominal supply unless otherwise specified)

ACCURACY

- Resolution: 1°
- Range: −55°C to +150°C
  −67°F to 302°F
  218K to 423K
  425°R to 793°R
- Accuracy: (±1 digit)[1]
  Calibration Error @ +25°C
  Absolute Error (overrated performance temperature range)
  Without External Calibration Adjustment
  With +25°C Calibration Error Set to Zero
  Nonlinearity
- Temperature Coefficient:
  Offset: 0.03 degrees/degree
  Span: 70ppm/°C
- Common Mode Rejection (ac)
  117dB, 1000V rms max Common Mode Voltage
- Normal Mode Rejection
  30dB @ 50-60Hz

	AD590J	AD590K	AD590L	AD590M
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error (overrated performance temperature range)	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
Without External Calibration Adjustment	±3.0°C	±2.0°C max	±1.6°C max	±1.0°C max
With +25°C Calibration Error Set to Zero	±1.5°C	±0.8°C max	±0.4°C max	±0.3°C max
Nonlinearity				

DISPLAY OUTPUT

- 7 Segment, Red Orange, LED 0.56″ (13mm) High for 3 Data Digits
- Sensor Disconnect Indication: ––– (for °C and °F only)
- DPM Positive Overload: EEE
- DPM Negative Overload: –––
- No Indication of Out of Sensor Range

INPUT IMPEDANCE

- °C, K: 1.0K
- °F, °C: 1.8K

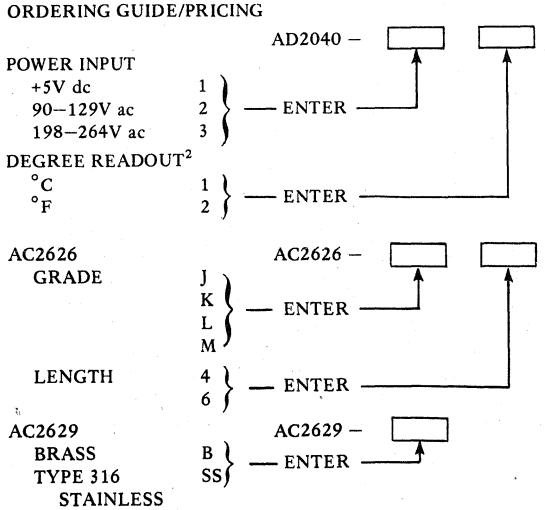
CONVERSION RATE

- 4 Conversions Per Second

POWER INPUT

- +5.0V ±5%; 160mA (dc version)
- AC Line 50-400Hz; See Voltage Options Below

ORDERING GUIDE/PRICING



POWER INPUT (ac Line Power)

- AC Line Power, 50-60Hz, 1.5 Watts

CALIBRATION ADJUSTMENT

- Span
- Gain
- Zero
- Offset
- Recommended Recalibration Interval: Six Months

SIZE

- 3.43″W × 2.0″H × 1.65″D (87 × 52 × 42mm)
- Panel Cutout Required: 3.175 ±0.015″ × 1.810 ±0.015″ (80.65 ±0.38 × 45.97 ±0.38mm)

WEIGHT

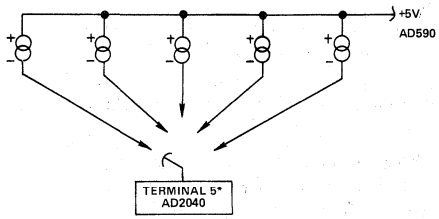
- 3 ounces (88 grams) (+5V dc)
- 7 ounces (198 grams) (ac Line Powered)

NOTES:

[1] Overall accuracy of meter plus sensor over entire range.

[2] +5V dc power input is calibrated in °F. Temperature scales are user selectable. Enter 2, e.g., AD2040-12.

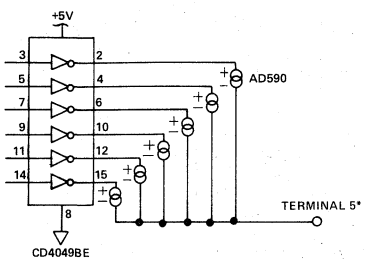
Specifications subject to change without notice.



*TERMINAL 5 IS -SENSOR INPUT ON THE +5V DC VERSION.
THIS TERMINAL IS TERMINAL #2 ON THE AC VERSION.

Figure 1. Manual Switching

Expansion to multiple sensors via manual switching is shown in Figure 1. The sensor selected will pass a signal current through the current measuring circuitry, internal to the AD2040. Similarly automatic switching, shown in Figure 2 is accomplished. A low level input on an inverter input will allow selection of the appropriate AD590.



*TERMINAL 5 IS -SENSOR INPUT ON THE +5V DC VERSION.
THIS TERMINAL IS TERMINAL #2 ON THE AC VERSION.

Figure 2. Automatic Switching

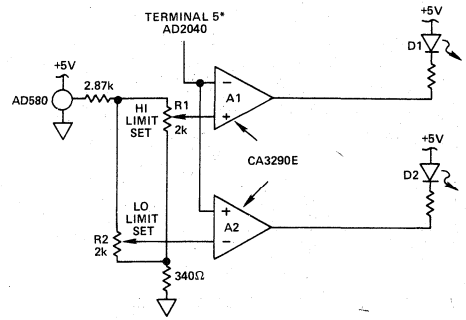
SCALE	TERMINAL 2	TERMINAL 3	TERMINAL 4	TERMINAL 9
°C	X	X	X	
°F				
K		X	X	X
°R		X		X

Table 1. Temperature Scale Selection (+5V dc Only)

As shown in Table 1 any of the standard temperature scales may be displayed.

The AD2040 dc version is factory calibrated in degrees Fahrenheit. Readout in degrees Celsius, Rankine or Kelvin are achieved via simple jumper connections on the terminal block, listed in the above table. (Connect terminals marked X.)

Figure 3 shows how the AD2040, in conjunction with 4 resistors, 2 trim pots, and a dual comparator, can be used to control as well as monitor particular applications via high and low set points. When the voltage at the AD590 sense terminal (terminal 5) goes higher than the Hi Limit Set Voltage, the



*TERMINAL 5 IS -SENSOR INPUT ON THE +5V DC VERSION.
THIS TERMINAL IS TERMINAL #2 ON THE AC VERSION.

Figure 3. Hi and Low Set Points

output of A1 goes low and D1 is illuminated. Similarly when the voltage at terminal 5 goes below the Lo Limit Set Voltage, the output of A2 goes low illuminating D2.

To set the high limit, replace the AD590 with a variable resistor. Adjust the resistor until the desired high temperature set point is displayed on the meter. Adjust R1 until D1 is just turning on. Repeat procedure for R2 (Lo Limit Set).

CALIBRATION PROCEDURE

The AD2040 is factory calibrated using an ideal sensor. The dc version is calibrated in °F and the ac version is calibrated to order. If sensor accuracy is adequate, no calibration is required (see note). If a lower grade sensor is used (i.e., J) and calibration is required, adjust Span Adjust on the rear with sensor at a known temperature for that temperature, e.g. for °F place sensor in Ice Bath at 32°F and adjust span for reading of 32.

Recalibration may be required after six (6) months; if so, proceed as follows:

1. With AD590 disconnected, short input of AD2040 (terminal 5 to 9 on dc version, or 1 to 3 on ac version). Remove AD2040 lens and adjust Front Panel Zero Adjust to display 000.
2. Attach AD590 sensor and stabilize at a known Reference Temperature; i.e., Ice Bath. Connect terminal 9 to terminal 3 (on dc version) or terminal 1 to access port (on ac version) and adjust Rear Span Adjust for a display of 273 plus Reference Temperature for °C or 460 plus Reference Temperature for °F.
3. Remove jumper between terminals 9 and 3 or 1 and access port. Adjust the Rear Offset Adjust for Reference Temperature. (For K or °R omit step 3.)

For optimum linearity calibration, for °C, repeat steps two (2) and three (3) with Reference Temperature at 0. Then with sensor at 100°C adjust Front Panel Gain Adjust for a meter display of 100. Other high end temperatures may be used with this procedure as long as they are known to be accurate.

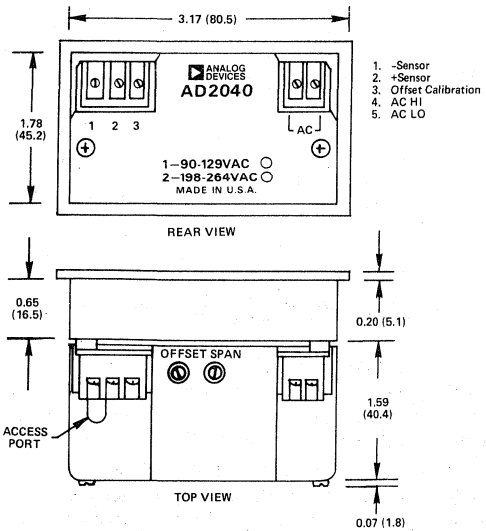
For °F repeat steps two and three with Reference Temperature at 32°F. Then with sensor at the high temperature, adjust Front Panel Gain. Adjust for readout equal to high temperature. The above temperature can be selected for optimum linearity over users temperature range.

NOTE: If other than °F readout on the dc version is desired, follow step 2 and 3 of Recalibration Procedure.

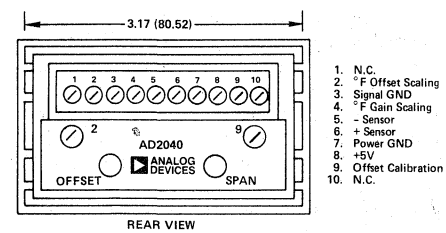
OUTLINE DIMENSIONS

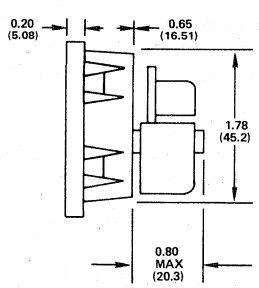
Dimensions shown in inches and (mm).

AD2040 (ac)



AD2040 (dc)





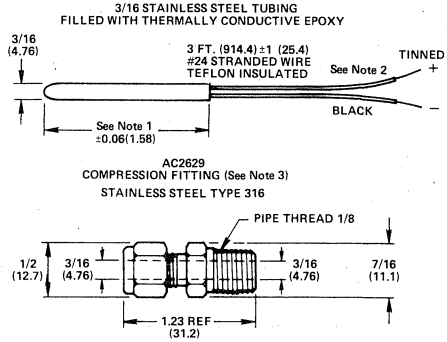
THE AC2626

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the new AD590F, the probe is available in linearity grades of 0.3°C. 0.4°C, 0.8°C or 1.5°C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AD2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

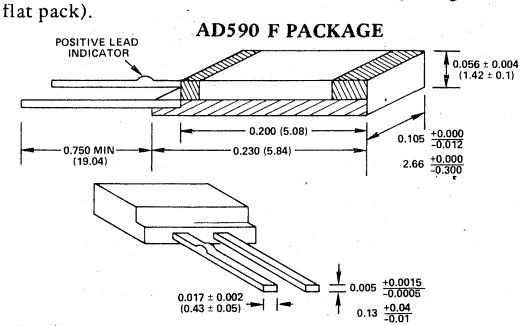
AC2626



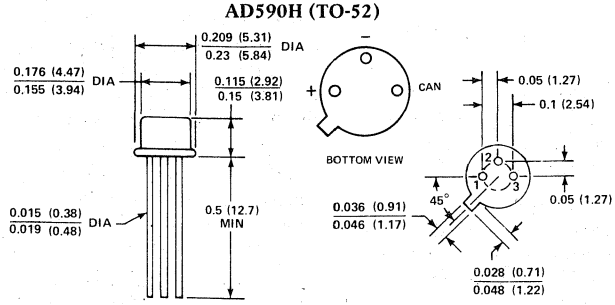
NOTE 1 Probes are available in 4-inch or 6-inch lengths.
NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue; M, green.
NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

The AD590 temperature transducer is available in two packages—the "H" package (TO-52) and the "F" package (ceramic flat pack).

AD590 F PACKAGE



AD590H (TO-52)



High Performance, 4-20mA Output Voltage-to-Current Converter

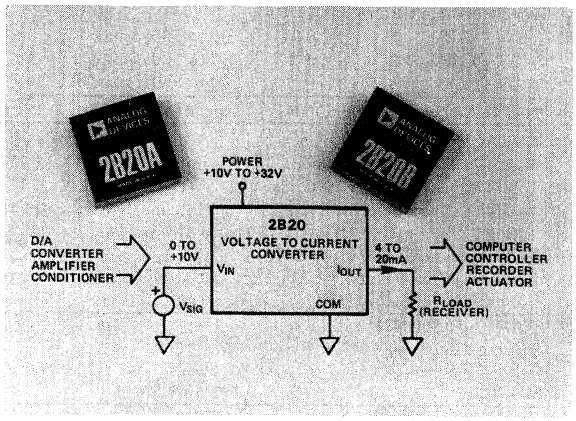
MODEL 2B20

FEATURES

- Complete, No External Components Needed
- Small Size: 1.1″ x 1.1″ x 0.4″ Module
- Input: 0 to +10V; Output: 4 to 20mA
- Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B)
- Wide Temperature Range: -25°C to +85°C
- Single Supply: +10V to +32V
- Meets ISA Std 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters
- Economical

APPLICATIONS

- Industrial Instrumentation and Control Systems
- D/A Converter — Current Loop Interface
- Analog Transmitters and Controllers
- Remote Data Acquisition Systems



GENERAL DESCRIPTION

Model 2B20 is a complete, modular voltage-to-current converter providing the user with a convenient way to produce a current output signal which is proportional to the voltage input. The nominal input voltage range is 0 to +10V. The output current range is 4 to 20mA into a grounded load.

Featuring low drift (0.005%/°C max, 2B20B) over the -25°C to +85°C temperature range and single supply operation (+10V to +32V), model 2B20 is available in two accuracy grades. The 2B20B offers precision performance with nonlinearity error of 0.005% (max) and guaranteed low offset error of ±0.1% max and span error of ±0.2% max, without external trims. The 2B20A is an economical solution for applications with lesser accuracy requirements, featuring nonlinearity error of 0.025% (max), offset error of ±0.4% (max), span error of ±0.6% (max), and span stability of 0.01%/°C max.

The 2B20 is contained in a small (1.1″ x 1.1″ x 0.4″), rugged, epoxy encapsulated package. For maximum versatility, two signal input (V_{IN1} and V_{IN2}) and two reference input (REF_{IN1} and REF_{IN2}) terminals are provided. Utilizing terminals V_{IN1} and REF_{IN1} eliminates the need for any external components, since offset and span are internally calibrated. If higher accuracy (up to ±0.01%) is required, inputs V_{IN2} and REF_{IN2} with series trim potentiometers may be utilized.

APPLICATIONS

Model 2B20 has been designed for applications in process control and monitoring systems to transmit information between subsystems or separated system elements. The 2B20 can serve as a transmission link between such elements of process control system as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners.

In a typical application, model 2B20 may act as an interface between the D/A converter output of a microcomputer based system and a process control device such as a variable position valve. Another typical application of the 2B20 may be as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

DESIGN FEATURES AND USER BENEFITS

Process Signal Compatibility: To provide output signal compatibility, the 2B20 meets the requirements of the Instrument Society of America Standard S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 3, Class L and U, nonisolated current loop transmitters.

External Reference Use: For increased flexibility, when ratiometric operation is desired, the 2B20 offers a capability of connecting an external reference (i.e., from multiplying D/A converter) to the REF_{IN2} terminal.

Wide Power Supply Range: A wide power supply range (+10V to +32V dc) allows for operation with either a +12V battery, a +15V powered data acquisition system, or a +24V powered process control instrumentation.

SPECIFICATIONS (typical @ +25°C and V_S = +15V, unless otherwise noted)

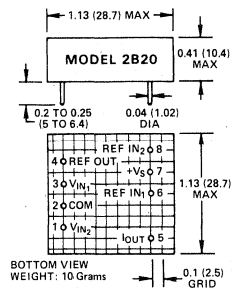
Model	2B20A	2B20B
INPUT SPECIFICATIONS		
Voltage Signal Range	0 to +10V	*
Input Impedance	10kΩ	*
OUTPUT SPECIFICATIONS		
Current Output Range[1]	4 to 20mA	*
Load Resistance Range[2]		
V_S = +12V	0 to 350Ω max	*
V_S = +15V	0 to 500Ω max	*
V_S = +24V	0 to 950Ω max	*
NONLINEARITY (% of Span)	±0.025% max	±0.005% max
ACCURACY[3]		
Warm-Up Time to Rated Specs	1 minute	*
Total Output Error @ +25°C[3,4]		
Offset (V_{IN} = 0 volts)	±0.4% max	±0.1% max
Span (V_{IN} = +10 volts)	±0.6% max	±0.2% max
vs. Temperature (-25°C to +85°C)		
Offset (V_{IN} = 0 volts)	±0.01%/°C max	±0.005%/°C max
Span (V_{IN} = +10 volts)	±0.01%/°C max	±0.005%/°C max
DYNAMIC RESPONSE		
Settling Time – to 0.1% of F.S. for 10V Step	25μs	*
Slew Rate	2.5mA/μs	*
REFERENCE INPUT[5]		
Voltage	+2.5V dc	*
Input Impedance	10kΩ	*
POWER SUPPLY		
Voltage, Rated Performance	+15V dc	*
Voltage, Operating	+10V to +32V dc max	*
Supply Change Effect (% of Span)[6]		
on Offset	±0.005%/V	*
on Span	±0.005%/V	*
Supply Current	6mA + I_{LOAD}	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Storage	-55°C to +125°C	*
CASE SIZE	1.125" X 1.125" X 0.4"	*

*Specifications same as 2B20A.
[1] Current output sourced into a grounded load over a supply voltage range of +10V to +32V.
[2] See Figure 1 for the maximum load resistance value over the power supply range.
[3] Accuracy is guaranteed with no external trim adjustments when REF_{IN} is connected to REF_{OUT}.
[4] All accuracy is specified as % of output span where output span is 16mA (±0.1%=±0.016mA output error).
[5] Reference input is normally connected to the reference output (+2.5V dc).
[6] Optional trim pots may be used for calibration at each supply voltage.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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LOAD RESISTANCE RANGE

The load resistance is the sum of the resistances of all connected receivers and the connection lines. The 2B20 operating load resistance is power supply dependent and will decrease by 50 ohms for each 1 volt reduction in the power supply. Similarly, it will increase by 50 ohms per volt increase in the power supply, but must not exceed the safe voltage capability of the unit.

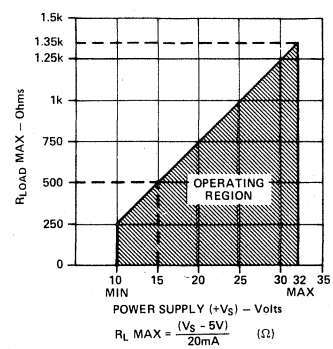


Figure 1. Maximum Load Resistance vs. Power Supply

PRINCIPLE OF OPERATION

The design of the 2B20 is comprised of high performance op amps, precision resistors and a high stability voltage reference to develop biasing and output drive capability. The 2B20 is designed to operate from a single positive power supply over a wide range of +10V to +32V dc and accepts a single ended, 0 to +10V voltage input. The internal reference has nominal output voltage of +2.5V (REF_{OUT}) and is used to develop 4mA output current for a zero volts input when REF_{IN} is connected to REF_{OUT}.

The output stage of the 2B20 utilizes a sensing resistor in the feedback loop, so the output current is linearly related to the voltage input and independent of the load resistance. There is no minimum resistance for the loads driven by the 2B20; it can drive even a short circuit with no damage to the unit. The maximum resistance of the load as seen by the unit (resistance of the load plus the resistance of the connecting wire) is limited. The maximum external loop resistance, R_L, is given by:

$$R_L\ (\Omega)\ \text{max} = \left(\frac{+V_S - 5V}{20mA}\right)$$

Figure 1 shows the operating region of the 2B20. The load must be returned to power supply common. The voltage appearing between I_{OUT} (pin 5) and COM (pin 2) should not exceed $V_{max} = +V_S - 5V$. Exceeding this value (up to +32V dc) will not damage the unit, but it will result in a loss of linearity.

The basic connections of the 2B20 are shown in Figure 2.

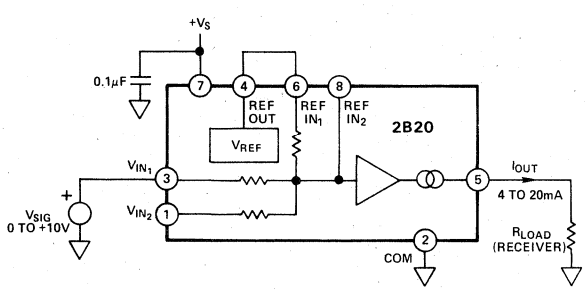


Figure 2. Basic Connections Diagram

OPTIONAL CALIBRATION AND TRIM PROCEDURE

Model 2B20's factory trimmed offset error is ±0.1% max and span error is ±0.2% max (2B20B). In most applications, further trimming will not be required. If it is necessary to obtain calibrated accuracy of up to ±0.01%, or, if a high signal source resistance (with respect to 10kΩ) introduces calibration error, inputs V_{IN2} and REF_{IN2} and optional trim pots should be used with V_{IN1} and REF_{IN1} open. To perform external trims, connect 500Ω potentiometers in series with V_{IN2} (span trim) and REF_{IN2} (offset trim) as shown in Figure 3. Adjust span pot, monitoring voltage drop across R_{LOAD}, to obtain an output voltage of 5.000V (I_{OUT} = 20mA) for a +10V input. Next, with 0 volts input, adjust offset pot to obtain 1.000V output (I_{OUT} = 4mA). Check both offset and span and retrim if necessary after each adjustment.

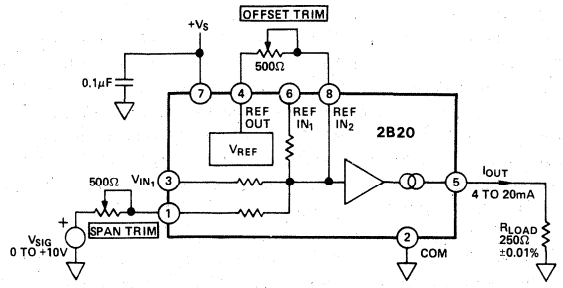


Figure 3. Model 2B20 Connections Using Optional Offset and Span Trims

CONNECTING THE 2B20 FOR 0 TO 10mA OUTPUT

The 2B20 may be utilized in applications requiring 0 to 10mA current output for a 0 to 10V input voltage range. To obtain 0mA output for 0V input, REF_{IN1} (pin 6) and REF_{IN2} (pin 8) terminals should be left open. A typical output current error for a zero volts input (without trimming) is 0.1mA. The 2B20 span calibration may be adjusted by a 1kΩ potentiometer in series with the V_{IN2} input. Basic connections of the 2B20 used to obtain a 0 to 10mA output are shown in Figure 4.

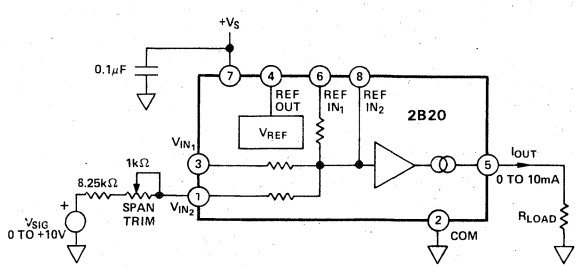


Figure 4. Model 2B20 Connected for 0 to 10mA Output Range

OUTPUT PROTECTION

In many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 5 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

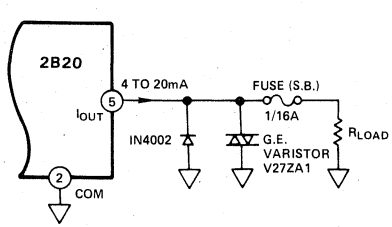


Figure 5. Output Protection Circuitry Connections

APPLICATIONS

Interfacing Voltage Output D/A Converters: The 2B20 is well suited in applications requiring 4 to 20mA output from D/A converters. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 6. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B20 (or the AD DAC80). First, a digital input code of all one's is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all 0's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA −1LSB = 19.9961mA.

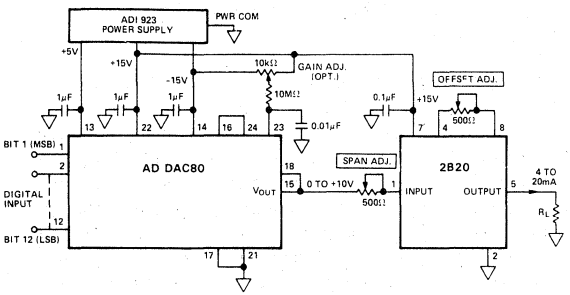


Figure 6. AD DAC80 – 4 to 20mA Current Loop Interface

Interfacing Current Output D/A Converters: To interface current output D/A converters, such as the AD562, a circuit configuration illustrated in Figure 7 should be used. Since the AD562 is designed to operate with an external +10V reference, the same external reference may be utilized by the 2B20 for ratiometric operation. The output of the AD562 is used to drive the summing junction of an operational amplifier to produce an output voltage. Using the internal feedback resistor of the AD562 provides a 0 to +10V output voltage range suitable to drive the 2B20.

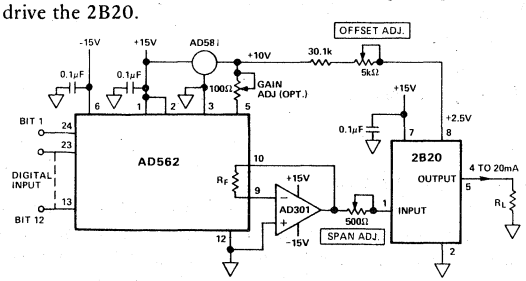


Figure 7. 12-Bit – 4 to 20mA Current Loop Interface

Microcomputer – Current Loop Interface: Figure 8 shows a typical application of the 2B20 in a multichannel microcomputer analog output system. When a microcomputer is to control a final control element, such as a valve positioner, servomechanism or motor, an analog output board with 4 to 20mA outputs is often necessary. The output boards typically have from one to eight channels, each with its own D/A converter. The 2B20, in a compact package, allows for an easy installation without any additional components and offers a 12-bit system compatible performance.

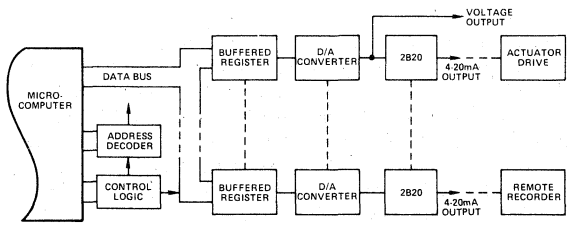


Figure 8. Microcomputer Analog Output Subsystem

Pressure Control System: In Figure 9, model 2B20 is used in a proportional pressure control system. The 3-15psi working pressure of a system is monitored with a pressure transducer interfaced by the model 2B31 signal conditioner. The high level voltage output of the 2B31 is converted to a 4 to 20mA to provide signal to the limit alarm and proportional control circuitry. A current-to-position converter controlling a motorized valve completes the pressure-control loop.

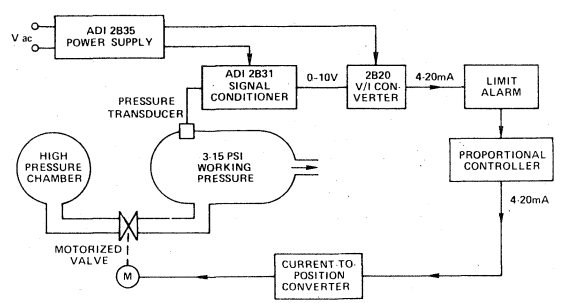


Figure 9. Proportional Pressure Control System

Isolated 4 to 20mA Output: For applications requiring up to ±1500V dc input to output isolation, consider using Analog Devices' model 2B22 isolated voltage-to-current converter.

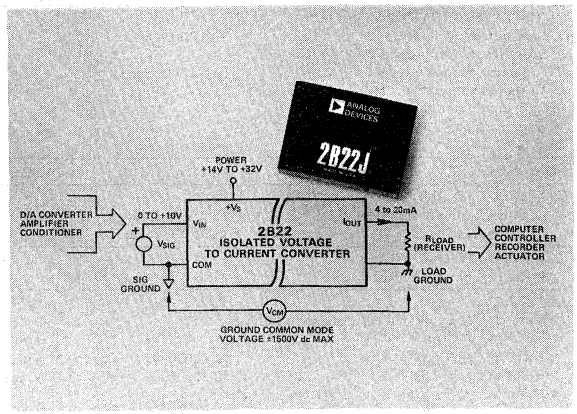
ANALOG DEVICES

High Performance, Isolated Voltage-to-Current Converter

MODEL 2B22

FEATURES
- Wide Input Range: 0 to +1V to 0 to +10V
- Standard Output Range: 4 to 20mA
- High CMV Input/Output Isolation: 1500V dc Continuous
- Low Nonlinearity: 0.05% max, 2B22L
- Low Span Drift: 0.005%/°C max, 2B22L
- Single Supply: +14V to +32V
- Meets IEEE Std 472: Transient Protection (SWC)
- Meets ISA Std 50.1: Isolated Current Loop Transmitters

APPLICATIONS
- Industrial Instrumentation and Process Control
  - Ground Loop Elimination
  - High Voltage Transient Protection
- D/A Converter – Current Loop Interface
- Analog Transmitters and Controllers
- Remote Data Acquisition Systems



GENERAL DESCRIPTION

Model 2B22 is a high performance, compact voltage-to-current converter offering 1500V dc input to output isolation in interfacing standard process signals. The input stage of the model 2B22 is single resistor programmable to accept voltage ranges from 0 to +1V to 0 to +10V. The isolated output current range is 4 to 20mA, and the 2B22 can be operated with 0 to 1000Ω grounded or floating loads.

Using modulation techniques with transformer isolation for reliable performance, the 2B22 is available in three accuracy selections offering guaranteed nonlinearity error (2B22L: ±0.05% max, 2B22K: ±0.1% max, and 2B22J: ±0.2% max) and guaranteed low span drift: ±0.005%/°C max, ±0.01%/°C max, and ±0.015%/°C max, respectively. The internally trimmed span and offset errors are ±0.1% max for the 2B22L and ±0.25% max for the 2B22J/2B22K. Both span and offset are adjustable by the optional external potentiometers.

Featuring a wide range, single supply operation (+14V to +32V), the 2B22 provides isolated +28V loop power and is capable of delivering rated current into an external 0 to 1000Ω load resistance. The unique output stage configuration also allows the user to utilize an optional external loop power supply to interface systems designed for a two-wire operation.

APPLICATIONS

Model 2B22 has been specifically designed for high accuracy applications in process control and monitoring systems to offer complete galvanic isolation and protection against damage from transients and fault voltages in transmitting information between subsystems or separated system elements. The 2B22 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 4, Class U isolated current loop transmitters.

In the industrial environment, model 2B22 can serve as a transmission link between such system elements as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners. In data acquisition and control systems, the 2B22 may act as an isolated interface between the D/A converter output of a microcomputer and standard 4 to 20mA analog loops.

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 2B22 is a conservatively designed, compact, epoxy encapsulated module capable of reliable operation in harsh environments. To assure high reliability, the 2B22 has been designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

Process Signal Compatibility: The versatile input stage design with a single resistor gain adjustment enables the 2B22 to accept any one of the standard inputs—0-1V, 0-10V, 1-5V; or 1-5mA, 4-20mA, 10-50mA; and provide standard, isolated 4-20mA output.

Isolated Loop Power: Internal 28V dc loop supply, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to drive 0 to 1000Ω loads and eliminates the need for an external dc/dc converter.

SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

Model	2B22J	2B22K	2B22L
INPUT SPECIFICATIONS			
Voltage Signal Range, G = 1.6mA/V	0 to +10V	*	*
G = 16mA/V	0 to +1V	*	*
Gain Range	1.6 to 16mA/V	*	*
Maximum Safe Input	+15V	*	*
Input Impedance	10MΩ	*	*
OUTPUT SPECIFICATIONS			
Current Output Range	4 to 20mA	*	*
Load Resistance Range, V_S = +14V to +32V, Internal Loop Power	0 to 1000Ω max	*	*
Maximum Output Current, @ Input Overload	25mA	*	*
Output Ripple, 100Hz Bandwidth G = 1.6mA/V	60μA pk-pk	*	*
NONLINEARITY (% of Span)	±0.2% max	±0.1% max	±0.05% max
CMV, INPUT TO OUTPUT			
ac, 60Hz, 1 Minute Duration	1500V rms	*	*
Continuous, ac or dc	±1500V pk max	*	*
CMR, INPUT TO OUTPUT			
60Hz, 1kΩ Source Imbalance	90dB	*	*
ACCURACY[1]			
Warm Up Time to Rated Performance 5 Minutes			
Total Output Error @ +25°C[1,2]			
Offset (V_{IN} = 0V)	±0.25% max	±0.25% max	±0.1% max
Span (V_{IN} = +10V)	±0.25% max	±0.25% max	±0.1% max
vs. Temperature (0 to +70°C, G = 1.6mA/V)			
Offset (V_{IN} = 0V)	±0.01%/°C max	±0.005%/°C max	±0.0025%/°C max
Span (V_{IN} = +10V)	±0.015%/°C max	±0.01%/°C max	±0.005%/°C max
vs. Temperature (0 to +70°C)			
Offset (V_{IN} = 0V, G = 1.6mA/V to 16mA/V)	±0.01%/°C	±0.005%/°C	±0.0025%/°C
Span (G = 1.6mA/V to 16mA/V)[3]	±0.015%/°C	±0.01%/°C	±0.005%/°C
DYNAMIC RESPONSE			
Settling Time — to 0.1% of F.S. for 10V Step	300μs	*	*
Slew Rate	0.06mA/μs	*	*
REFERENCE INPUT			
Voltage	+2.5V dc	*	*
Input Impedance	6kΩ	*	*
OSCILLATOR			
Frequency, Internal Oscillator	100kHz ± 10%	*	*
External Sync Input			
Frequency	100kHz ± 10% max	*	*
Waveform	Square wave, 50% duty cycle	*	*
Voltage	20V p-p	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15V dc	*	*
Voltage, Operating	+14V to +32V dc	*	*
Supply Current (at Full Scale Output)			
Using Internal Loop Power	100mA	*	*
Using External Loop Power	50mA	*	*
Suppiy Change Effect (% of Span)			
on Offset (V_{IN} = 0V)	±0.0005%/V	*	*
on Span (V_{IN} = +10V)	±0.0005%/V	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +75°C	*	*
Storage	-55°C to +85°C	*	*
CASE SIZE	2.2" X 3" X 0.6"	*	*

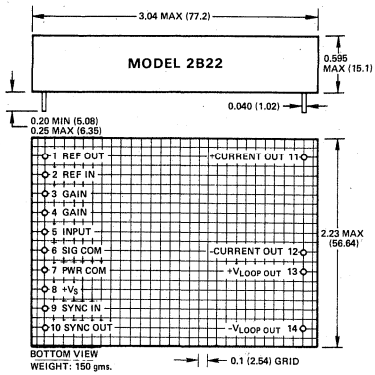
*Specifications same as 2B22J.

NOTES
[1] Accuracy is guaranteed at G = 1.6mA/V with no external trim adjustments when connected as shown in Figure 1.
[2] All accuracy is % of span where span is 16mA (±0.1% = ±0.016mA error).
[3] Span T.C. for gains higher than 1.6mA/V is R_G dependent — a low T.C. (±10ppm/°C) R_G is recommended for best performance.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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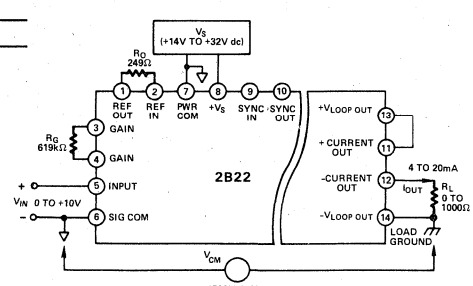
INTERCONNECTION DIAGRAM

Model 2B22 can be applied directly to achieve rated performance as shown in Figure 1 below. The input stage gain of 1.6mA/V, to convert a 0 to +10V signal into a 4 to 20mA output current, is obtained with the values shown. A single polarity power supply (+14V to +32V dc) should be connected to pin 8. To eliminate ground loops, the user should ensure that the signal return (common) lead does not carry the power supply current. Power common (pin 7) and signal common (pin 6) should be tied at the power supply common terminal. The voltage difference between pins 6 and 7 should not exceed 0.2V. An internal dc-dc converter provides isolated output loop power (pins 13 and 14), which is connected externally to the current output terminals (pins 11 and 12) and a load resistance. The standard 4 to 20mA current output signal is delivered into any external load between zero and 1000Ω.



NOTE: Resistors R_O and R_G are 1%, 50ppm/°C Metal Film Type. Values shown are for G = 1.6mA/V. For G = 16mA/V, use 10ppm/°C R_G and 50ppm/°C R_O.

Figure 1. Basic Connections

FUNCTIONAL DESCRIPTION

The high performance of model 2B22 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier, modulator section and the current output circuitry. The block diagram for model 2B22 is shown in Figure 2 below.

The 2B22 produces an isolated 4 to 20mA output current which is proportional to the voltage input and independent of the load resistance. The input amplifier operates single-ended and accepts a positive voltage within 0 to +10V range. Gain can be set from 1.6mA/V to 16mA/V by changing the gain resistor R_G to accommodate input ranges from 0 to +1V (G = 16mA/V) to 0 to +10V (G = 1.6mA/V). The transfer function is $I_{OUT} = (4mA + G \times V_{IN})$.

An internal, high stability reference has nominal output voltage of +2.5V (REF OUT) and is used to develop a 4mA output current for a 0 volts input. The terminals REF OUT (pin 1) and REF IN (pin 2) should be connected via the offset setting resistor R_O. For ratiometric operation, an external reference voltage can be connected to the REF IN terminal.

The 2B22 is designed to operate from a single positive power supply over a wide range of +14V to +32V dc. An internal dc-dc converter provides isolated +28V loop power which is independent of $+V_S$. The maximum resistance of the load R_L (resistance of the receivers plus the resistance of the connecting wire) is 1000Ω. Since the loop power is derived from the input side, the current capability of the power supply ($+V_S$) must be 100mA min to supply full output signal current.

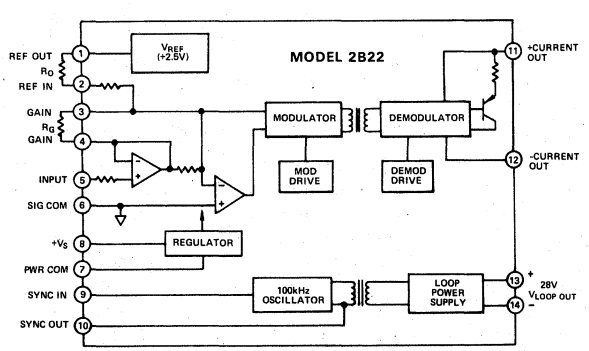


Figure 2. Block Diagram — Model 2B22

OPTIONAL TRIM ADJUSTMENTS

Model 2B22 is factory calibrated for a 0 to +10V input range (G = 1.6mA/V. As shipped, the 2B22 meets its listed specifications without use of any external trim potentiometers. Additional trim adjustment capability, to reduce span and offset errors to ±0.05% max, is easily provided as shown in Figure 3. The span and offset trim pots are adjusted while monitoring the voltage drop across a precision (or known) load resistor. The following trim procedure is recommended:

1. Connect model 2B22 as shown in Figure 3.
2. Apply V_{IN} = 0 volts and adjust R_O (Offset Adjust) for V_{OUT} = +2V ± 4mV.
3. Apply V_{IN} = +10.00V and adjust R_G (Span Adjust) for V_{OUT} = +10V ± 4mV.

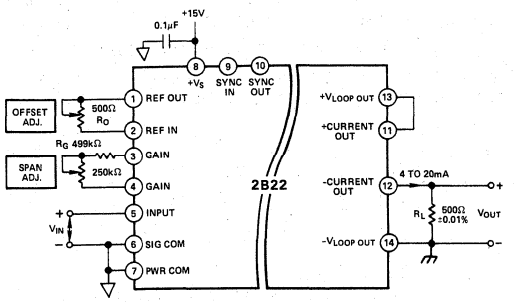


Figure 3. Optional Span and Offset Adjustment

GAIN AND OFFSET SETTING

The gain of the 2B22 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs (V_{IN}). The value of the gain setting resistor R_G is determined by: $R_G(k\Omega) = 6.314SF/(10.1 - SF)$ where SF is a scale factor equal to the value of V_{IN} F.S. Example: to convert a 0 to +1V input to the 4 to 20mA output, SF = 1 and R_G = 693Ω. Due to device tolerances, allowance should be made to vary R_G by ±5% using the potentiometer.

The value of the offset resistor R_O is independent from the gain setting and given by the relationship: $R_O\ (k\Omega) = 2.5\ (V_{REF} - 2.4)$ where V_{REF} is the reference voltage applied. For example, the reference provided by the 2B22 is +2.5V and therefore R_O = 250Ω. The accuracy of the R_O calculation from from the above formula is ±5%. When an external reference operation is desired (i.e. for ratiometric operation), connect the reference voltage via R_O to pin 2 and leave pin 1 open.

EXTERNAL LOOP POWER OPERATION

For maximum versatility, the 2B22's output stage is designed to operate from the optional, isolated external loop power supply. This feature allows the user to interface systems wired for a two-wire operation. As shown in Figure 4, the same wiring is used for loop power and output. The load resistance is connected in series with an external dc power supply (+6V to +32V), and the current drawn from the supply is the 4 to 20mA output signal. The input stage of the 2B22 still requires $+V_S$ power, but the current drain from $+V_S$ is limited to 50mA. Use of an external loop power may require gain and offset trimming to obtain specified accuracy. The maximum series load resistance depends on the loop supply voltage as shown in Figure 4.

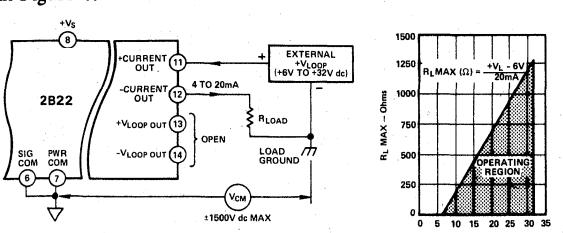


Figure 4. Optional External Loop Power Operation

SYNCHRONIZING MULTIPLE 2B22'S

In applications where multiple 2B22's are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by synchronizing multiple units by connecting the SYNC OUT (pin 10) terminal to the SYNC IN (pin 9) terminal of the adjacent 2B22. The SYNC OUT terminal of this "slaved" unit can be used to drive another adjacent 2B22 (Figure 5). For best accuracy, each 2B22 should be retrimmed when synchronizing connections are used.

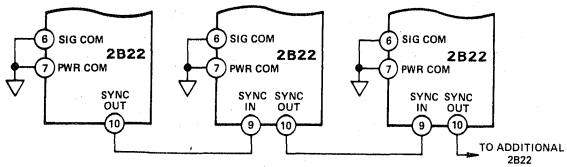


Figure 5. Multiple 2B22's Synchronization

OUTPUT PROTECTION

The current output terminals (pins 11 and 12) are protected from shorts up to +32V dc but in many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 6 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

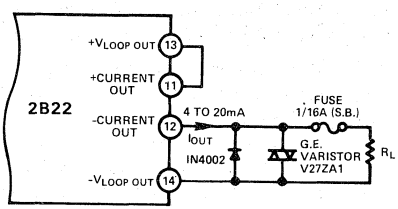


Figure 6. Output Protection Circuitry Connections

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Process Signal Isolator: In process control applications, model 2B22 can be applied to interface standard process signals (e.g. 1 to 5mA, 4 to 20mA, 10 to 50mA, 1 to 5V) and convert them to isolated 4 to 20mA output. A typical hook-up of model 2B22 is illustrated in Figure 7, showing input resistor R_C converting the current from a remote loop to a voltage input, and a span adjustment resistor R_G. A value of R_C should be selected to develop a minimum of +1V signal with full scale input current applied. For example, a 50Ω resistor converts the 4 to 20mA current input to a 200mV to 1V voltage input, which the 2B22 isolates and converts to a 4 to 20mA output. The reference input (pin 2) is not connected since the process signal provides a desired offset.

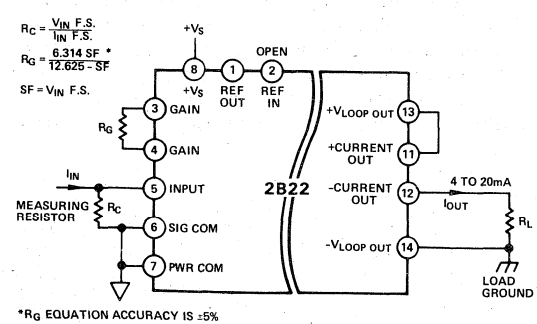


Figure 7. Process Signal Current Isolator

Isolated D/A Converter: Model 2B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20mA current loops. This requirement is common in a microcomputer-based control system. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the D/A converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 8. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B22. First, a digital input code of all one's is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all zero's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA less 1LSB (19.9961mA).

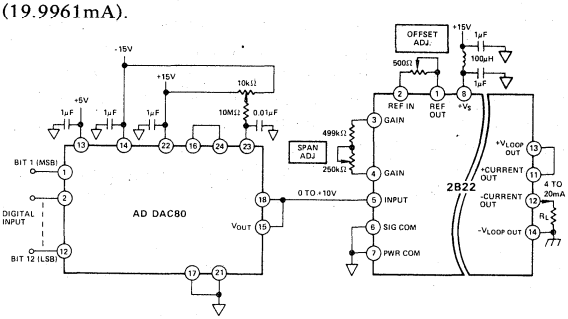


Figure 8. D/A Converter – Isolated 4 to 20mA Interface

Pressure Transmitter: In Figure 9, model 2B22 is used in a pressure transmitter application to provide complete input-output isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' model 2B30 transducer conditioner. The bridge excitation and system power is provided by the model 2B35 triple output power supply. The high level voltage output of the 2B30 is converted to the isolated 4 to 20mA current for transmission to a remote recorder or indicator.

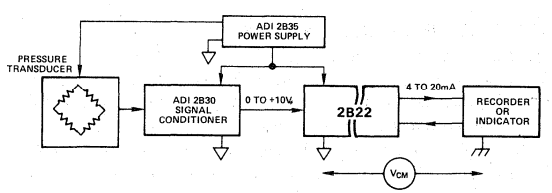


Figure 9. Isolated Pressure Transmitter

High Performance, Economy Strain Gage/RTD Conditioners

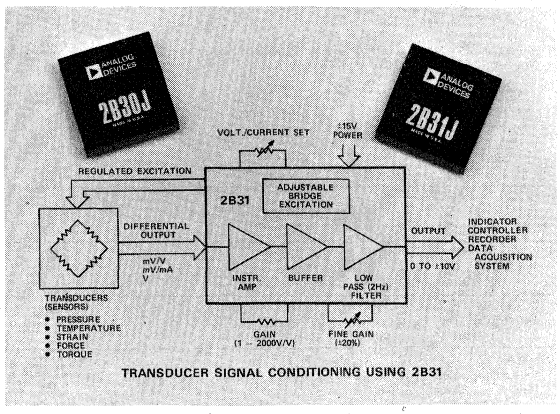
MODELS 2B30 AND 2B31

FEATURES

- Low Cost
- Complete Signal Conditioning Function
- Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
- Wide Gain Range: 1 to 2000V/V
- Low Nonlinearity: 0.0025% max ("L")
- High CMR: 140dB min (60Hz, G = 1000V/V)
- Input Protected to 130V rms
- Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)
- Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100μA to 10mA)

APPLICATIONS

- Measurement and Control of:
  - Pressure, Temperature, Strain/Stress, Force, Torque
- Instrumentation: Indicators, Recorders, Controllers
- Data Acquisition Systems
- Microcomputer Analog I/O



TRANSDUCER SIGNAL CONDITIONING USING 2B31

GENERAL DESCRIPTION

Models 2B30 and 2B31 are high performance, low cost, compact signal conditioning modules designed specifically for high accuracy interface to strain gage-type transducers and RTD's (resistance temperature detectors). The 2B31 consists of three basic sections: a high quality instrumentation amplifier; a three-pole low pass filter, and an adjustable transducer excitation. The 2B30 has the same amplifier and filter as the 2B31, but no excitation capability.

Available with low offset drift of 0.5μV/°C max (RTI, G = 1000V/V) and excellent linearity of 0.0025% max, both models feature guaranteed low noise performance 1μV p-p max, and outstanding 140dB common mode rejection (60Hz, CMV = ±10V, G = 1000V/V) enabling the 2B30/2B31 to maintain total amplifier errors below 0.1% over a 20°C temperature range. The low pass filter offers 60dB/decade roll-off from 2Hz to reduce normal-mode noise bandwidth and improve system signal-to-noise ratio. The 2B31's regulated transducer excitation stage features a low output drift (0.015%/°C max) and a capability of either constant voltage or constant current operation.

Gain, filter cutoff frequency, output offset level and bridge excitation (2B31) are all adjustable, making the 2B30/2B31 the industry's most versatile high-accuracy transducer-interface modules. Both models are offered in three accuracy selections, J/K/L, differing only in maximum nonlinearity and offset drift specifications.

APPLICATIONS

The 2B30/2B31 may be easily and directly interfaced to a wide variety of transducers for precise measurement and control of pressure, temperature, stress, force and torque. For applications in harsh industrial environments, such characteristics as high CMR, input protection, low noise, and excellent temperature stability make 2B30/2B31 ideally suited for use in indicators, recorders, and controllers.

The combination of low cost, small size and high performance of the 2B30/2B31 offers also exceptional quality and value to the data acquisition system designer, allowing him to assign a conditioner to each transducer channel. The advantages of this approach over low level multiplexers include significant improvements in system noise and resolution, and elimination of crosstalk and aliasing errors.

DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The true differential input circuitry with high CMR (140dB) eliminating common-mode noise pickup errors, input filtering minimizing RFI/EMI effects, output low pass filtering (f_c=2Hz) rejecting 50/60Hz line frequency pickup and series-mode noise.

Input and Output Protection: Input protected for shorts to power lines (130V rms), output protected for shorts to ground and either supply.

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

Programmable Transducer Excitation: User-programmable adjustable excitation source-constant voltage (4V to 15V @ 100mA) or constant current (100μA to 10mA) to optimize transducer performance.

Adjustable Low Pass Filter: The three-pole active filter (f_c=2Hz) reducing noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

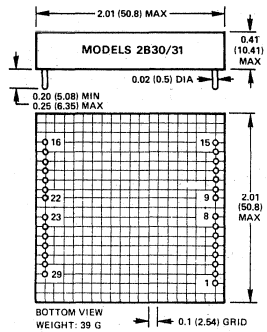
MODEL	2B30J 2B31J	2B30K 2B31K	2B30L 2B31L
GAIN[1]			
Gain Range	1 to 2000V/V	*	*
Gain Equation	$G = (1 + 94k\Omega/R_G)$ [$20k\Omega/(R_F + 16.2k\Omega)$]	*	*
Gain Equation Accuracy	±2%	*	*
Fine Gain (Span) Adjust. Range	±20%	*	*
Gain Temperature Coefficient	±25ppm/°C max (±10ppm/°C typ)	*	*
Gain Nonlinearity	±0.01% max	±0.005% max	±0.0025% max
OFFSET VOLTAGES[1]			
Total Offset Voltage, Referred to Input			
Initial, @ +25°C	Adjustable to Zero (±0.5mV typ)	*	*
Warm-Up Drift, 10 Min., G = 1000	±5μV RTI	*	*
vs. Temperature			
G = 1V/V	±150μV/°C max	±75μV/°C max	±50μV/°C max
G = 1000V/V	±3μV/°C max	±1μV/°C max	±0.5μV/°C max
At Other Gains	±(3 ± 150/G)μV/°C max	±(1 ± 75/G)μV/°C max	±(0.5 ± 50/G)μV/°C max
vs. Supply, G = 1000V/V	±25μV/V	*	*
vs. Time, G = 1000V/V	±3μV/month	*	*
Output Offset Adjust. Range	±10V	*	*
INPUT BIAS CURRENT			
Initial @ +25°C	+200nA max (100nA typ)	*	*
vs. Temperature (0 to +70°C)	-0.6nA/°C	*	*
INPUT DIFFERENCE CURRENT			
Initial @ +25°C	±5nA	*	*
vs. Temperature (0 to +70°C)	±40pA/°C	*	*
INPUT IMPEDANCE			
Differential	100MΩ‖47pF	*	*
Common Mode	100MΩ‖47pF	*	*
INPUT VOLTAGE RANGE			
Linear Differential Input	±10V	*	*
Maximum Differential or CMV Input Without Damage	130V rms	*	*
Common Mode Voltage	±10V	*	*
CMR, 1kΩ Source Imbalance			
G = 1V/V, dc to 60Hz[1]	90dB	*	*
G = 100V/V to 2000V/V, 60Hz[1] dc[2]	140dB min 90dB min (112 typ.)	*	*
INPUT NOISE			
Voltage, G = 1000V/V			
0.01Hz to 2Hz	1μV p-p max	*	*
10Hz to 100Hz[2]	1μV p-p	*	*
Current, G = 1000			
0.01Hz to 2Hz	70pA p-p	*	*
10Hz to 100Hz[2]	30pA rms	*	*
RATED OUTPUT[1]			
Voltage, 2kΩ Load[3]	±10V min	*	*
Current	±5mA min	*	*
Impedance, dc to 2Hz, G = 100V/V	0.1Ω	*	*
Load Capacitance	0.01μF max	*	*
DYNAMIC RESPONSE (Unfiltered)[2]			
Small Signal Bandwidth			
-3dB Gain Accuracy, G = 100V/V	30kHz	*	*
G = 1000V/V	5kHz	*	*
Slew Rate	1V/μs	*	*
Full Power	15kHz	*	*
Settling Time, G = 100, ±10V Output Step to ±0.1%	30μs	*	*
LOW PASS FILTER (Bessel)			
Number of Poles	3	*	*
Gain (Pass Band)	+1	*	*
Cutoff Frequency (-3dB Point)	2Hz	*	*
Roll-Off	60dB/decade	*	*
Offset (at 25°C)	±5mV	*	*
Settling Time, G = 100V/V, ±10V Output Step to ±0.1%	600ms	*	*
BRIDGE EXCITATION (See Table 1)			
POWER SUPPLY[4]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(12 to 18)V dc	*	*
Current, Quiescent	±15mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +125°C	*	*
CASE SIZE	2" x 2" x 0.4" (51 x 51 x 10.2mm)	*	*

*Specifications same as 2B30J/2B31J.
[1] Specifications referred to output at pin 7 with 3.75k, 1%, 25ppm/°C fine span resistor installed and internally set 2Hz filter cutoff frequency.
[2] Specifications referred to the unfiltered output at pin 1.
[3] Protected for shorts to ground and/or either supply voltage.
[4] Recommended power supply ADI model 902-2 or model 2B35 transducer power supply (for 2B30).

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

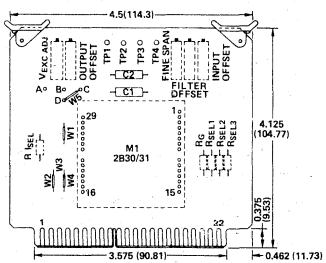


PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1 (UNFILTERED)	16	EXC SEL 1
2	FINE GAIN (SPAN) ADJ.	17	I SEL
3	FINE GAIN (SPAN) ADJ.	18	$V_{EXC\ OUT}$
4	FILTER OFFSET TRIM	19	$I_{EXC\ OUT}$
5	FILTER OFFSET TRIM	20	SENSE HIGH (+)
6	BANDWIDTH ADJ. 3	21	EXC SEL 2
7	OUTPUT 2 (FILTERED)	22	REF OUT
8	BANDWIDTH ADJ. 2	23	SENSE LOW (-)
9	BANDWIDTH ADJ. 1	24	REGULATOR $+V_{R\ IN}$
10	R_{GAIN}	25	REF IN
11	R_{GAIN}	26	$-V_S$
12	-INPUT	27	$+V_S$
13	INPUT OFFSET TRIM	28	COMMON
14	INPUT OFFSET TRIM	29	OUTPUT OFFSET TRIM
15	+INPUT		

Note: Pins 16 thru 25 are not connected in Model 2B30

MOUNTING CARDS AC1211, AC1213



AC1211/AC1213 CONNECTOR DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
A	REGULATOR $+V_{R\ IN}$	1	EXC SEL 1
B	SENSE LOW (-)	2	I SEL
C	REF OUT	3	$V_{EXC\ OUT}$
D	REF IN	4	$I_{EXC\ OUT}$
E		5	SENSE HIGH (+)
F		6	EXC SEL 2
H		7	OUTPUT OFFSET TRIM
J		8	
K	$-V_S$	9	$-V_S$
L	$+V_S$	10	$+V_S$
M		11	
N	COMMON	12	COMMON
P		13	
R	FINE GAIN ADJ.	14	
S	FINE GAIN ADJ.	15	
T	FILTER OFFSET TRIM	16	
U	FILTER OFFSET TRIM	17	R_{GAIN}
V	OUTPUT 2 (FILTERED)	18	R_{GAIN}
W	-INPUT	19	OUTPUT 1 (UNFILTERED)
X	INPUT OFFSET TRIM	20	BANDWIDTH ADJ. 1
Y	INPUT OFFSET TRIM	21	BANDWIDTH ADJ. 3
Z	+INPUT	22	BANDWIDTH ADJ. 2

The AC1211/AC1213 mounting card is available for the 2B30/2B31. The AC1211/AC1213 is an edge connector card with pin receptacles for plugging in the 2B30/2B31. In addition, it has provisions for installing the gain resistors and the bridge excitation, offset adjustment and filter cutoff programming components. The AC1211/AC1213 mates with a Cinch 251-22-30-160 (or equivalent) edge connector. The AC1213 includes the adjustment pots; no pots are provided with the AC1211.

FUNCTIONAL DESCRIPTION

Models 2B30 and 2B31 accept inputs from a variety of full bridge strain gage-type transducers or RTD sensors and convert the inputs to conditioned high level analog outputs. The primary transducers providing direct inputs may be 60Ω to 1000Ω strain gage bridges, four-wire RTD's or two- or three-wire RTD's in the bridge configuration.

The 2B30 and 2B31 employ a multi-stage design, shown in Figure 1, to provide excellent performance and maximum versatility. The input stage is a high input impedance ($10^8\Omega$), low offset and drift, low noise differential instrumentation amplifier. The design is optimized to accurately amplify low level (mV) transducer signals riding on high common mode voltages (±10V), with wide (1-2000V/V), single resistor (R_G), programmable gain to accommodate 0.5mV/V to 36mV/V transducer spans and 5Ω to 2000Ω RTD spans. The input stage contains protection circuitry for accidental shorts to power line voltage (130V rms) and RFI filtering circuitry.

The inverting buffer amplifier stage provides a convenient means of fine gain trim (0.8 to 1.2) by using a 10kΩ potentiometer (R_F); the buffer also allows the output to be offset by up to ±10V by applying a voltage to the noninverting input (pin 29). For dynamic, high bandwidth measurements—the buffer output (pin 1) should be used.

The three-pole active filter uses a unity-gain configuration and provides low-pass Bessel-type characteristics-minimum overshoot response to step inputs and a fast rise time. The cutoff frequency (-3dB) is factory set at 2Hz, but may be increased up to 5kHz by addition of three external resistors (R_{SEL_1} - R_{SEL_3}).

INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 illustrates the 2B31 wiring configuration when used in a typical bridge transducer signal conditioning application. A recommended shielding and grounding technique for preserving the excellent performance characteristics of the 2B30/2B31 is shown.

Because models 2B30/2B31 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and conditioner common (pin 28). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains. To avoid ground loops, signal return or cable shield should never be grounded at more than one point.

The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS

Models 2B30/2B31 have been conservatively specified using min-max values as well as typicals to allow the designer to develop accurate error budgets for predictable performance. The error calculations for a typical transducer application, shown in Figure 1 (350Ω bridge, 1mV/V F.S., 10V excitation), are illustrated below.

Assumptions: 2B31L is used, G = 1000, $\Delta T = \pm 10^\circ C$, source imbalance is 100Ω, common mode noise is 0.25V (60Hz) on the ground return.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources and their effect on system accuracy (worst case) as a % of Full Scale (10V) are listed:

Error Source	Effect on Absolute Accuracy % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.0025	±0.0025
Gain Drift	±0.025	
Voltage Offset Drift	±0.05	
Offset Current Drift	±0.004	
CMR	±0.00025	±0.00025
Noise (0.01 to 2Hz)	±0.01	±0.01
Total Amplifier Error	±0.09175 max	±0.01275 max
Excitation Drift	±0.15 (±0.03 typ)	
Total Output Error (Worst Case)	±0.24175 max (±0.1 typ)	±0.0127 max

The total worst case effect on absolute accuracy over ±10°C is less than ±0.25% and the 2B31 is capable of 1/2 LSB resolution in a 12 bit, low input level system. Since the 2B31 is conservatively specified, a typical overall accuracy error would be lower than ±0.1% of F.S.

In a computer or microprocessor based system, automatic recalibration can nullify gain and offset drifts leaving noise, nonlinearity and CMR as the only error sources. A transducer excitation drift error is frequently eliminated by a ratiometric operation with the system's A/D converter.

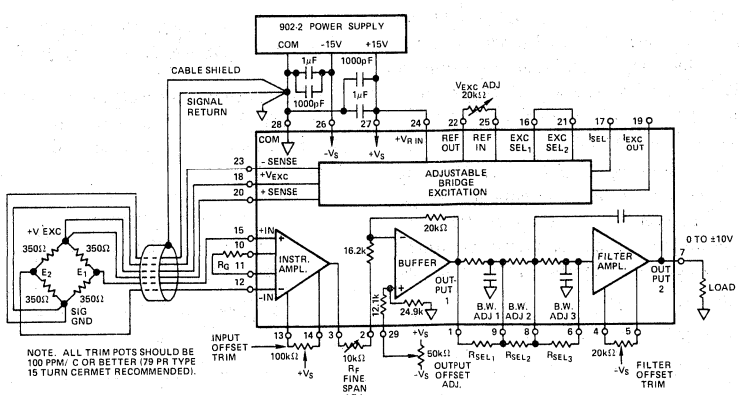


Figure 1. Typical Bridge Transducer Application Using 2B31

BRIDGE EXCITATION (2B31)

The bridge excitation stage of the model 2B31 is an adjustable output, short circuit protected, regulated supply with internally provided reference voltage (+7.15V). The remote sensing inputs are used in the voltage output mode to compensate for the voltage drop variations in long leads to the transducer. The regulator circuitry input (pin 24) may be connected to $+V_S$ or some other positive dc voltage (pin 28 referenced) within specified voltage level and load current range. User-programmable constant voltage or constant current excitation mode may be used. Specifications are listed below in Table 1.

MODEL	2B31J	2B31K	2B31L
Constant Voltage Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Voltage Range	+4V to +15V	*	*
Regulator Input/Output Voltage Differential	3V to 24V	*	*
Output Current[1]	0 to 100mA max	*	*
Regulation, Output Voltage vs. Supply	0.05%/V	*	*
Load Regulation, I_L = 1mA to I_L = 50mA	0.1%	*	
Output Voltage vs. Temperature (0 to +70°C)	0.015%/°C max 0.003%/°C typ	*	*
Output Noise	1mV rms	*	*
Reference Voltage (Internal)	7.15V ±3%	*	*
Constant Current Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Current Range	100µA to 10mA	*	*
Compliance Voltage	0 to 10V	*	*
Load Regulation	0.1%	*	*
Temperature Coefficient (0 to +70°C)	0.003%/°C	*	*
Output Noise	1µA rms	*	*

[1] Output Current derated to 33mA max for 24V regulator input/output voltage differential.

Table 1. Bridge Excitation Specifications

OPERATING INSTRUCTIONS

Gain Setting: The differential gain, G, is determined according to the equation:

$$G = (1 + 94k\Omega/R_G)\ [20k\Omega/(R_F + 16.2k\Omega)]$$

where R_G is the input stage resistor shown in Figure 1 and R_F is the variable 10kΩ resistor in the output stage. For best performance, the input stage gain should be made as large as possible, using a low temperature coefficient (10ppm/°C) R_G, and the output stage gain can then be used to make a ±20% linear gain adjustment by varying R_F.

Input Offset Adjustment: To null input offset voltage, an optional 100kΩ potentiometer connected between pins 13 and 14 (Figure 1) can be used. With gain set at the desired value, connect both inputs (pins 12 and 15) to the system common (pin 28), and adjust the 100kΩ potentiometer for zero volts at pin 3. The purpose of this adjustment is to null the internal amplifier offset and it is not intended to compensate for the transducer bridge unbalance.

Output Offset Adjustment: The output of the 2B30/2B31 can be intentionally offset from zero over the ±10V range by applying a voltage to pin 29, e.g., by using an external potentiometer or a fixed resistor. Pin 29 is normally grounded if output offsetting is not desired. The optional filter amplifier offset null capability is also provided as illustrated in Figure 1.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency may be increased from the internally set 2Hz by the addition of three external resistors connected as shown in Figure 1. The values of resistors required for a desired cutoff frequency, f_c, above 5Hz are obtained by the equation below:

$$R_{SEL_1} = 11.6 \times 10^6/(2.67f_c - 4.34);$$

$$R_{SEL_2} = 27.6 \times 10^6/(4.12f_c - 7)$$

$$R_{SEL_3} = 1.05 \times 10^6/(0.806f_c - 1.3)$$

where R_{SEL} is in ohms and f_c in Hz. Table 2 gives the nearest 1% R_{SEL} for several common filter cutoff (-3dB) frequencies.

f_c (Hz)	R_{SEL1} (kΩ) (Pin 1 to 9)	R_{SEL2} (kΩ) (Pin 9 to 8)	R_{SEL3} (kΩ) (Pin 8 to 6)
2	Open	Open	Open
5	1270.000	2050.00	383.000
10	523.000	806.00	154.000
50	90.000	137.00	26.700
100	44.200	68.10	13.300
500	8.660	13.30	2.610
1000	4.320	6.65	1.300
5000	0.866	1.33	0.261

Table 2. Filter Cutoff Frequency vs. R_{SEL}

Voltage Excitation Programming: Pin connections for a constant voltage output operation are shown in Figure 2. The bridge excitation voltage, V_{EXC}, is adjusted between +4V to +15V by the 20kΩ (50ppm/°C) R_{VSEL} potentiometer. For ratiometric operation, the bridge excitation can be adjusted by applying an external positive reference to pin 25 of the 2B31. The output voltage is given by: $V_{EXC\ OUT} = 3.265V_{REF\ IN}$. The remote sensing leads should be externally connected to the excitation leads at the transducer or jumpered as shown in Figure 2 if sensing is not required.

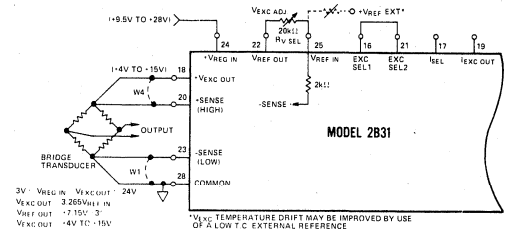


Figure 2. Constant Voltage Excitation Connections

Current Excitation Programming: The constant current excitation output can be adjusted between 100µA to 10mA by two methods with the 2B31. Figure 3 shows circuit configuration for a current output with the maximum voltage developed across the sensor (compliance voltage) constrained to +5V. The value of programming resistor R_{ISEL} may be calculated from the relationship: $R_{ISEL} = (V_{REG\ IN} - V_{REF\ IN})/I_{EXC\ OUT}$.

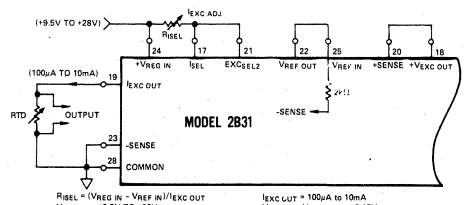


Figure 3. Constant Current Excitation Connections (V_{COMPL} = 0 to +5V)

A compliance voltage range of 0 to +10V can be obtained by connecting the 2B31 as shown in Figure 4. The 2kΩ potentiometer R_{ISEL} is adjusted for desired constant current excitation output.

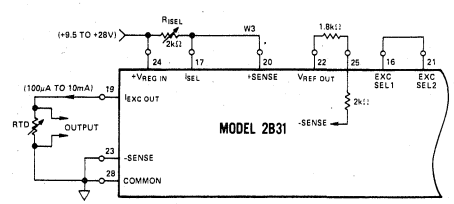


Figure 4. Constant Current Excitation Connections (V_{COMPL} = 0 to +10V)

APPLICATIONS

Strain Measurement: The 2B30 is shown in Figure 5 in a strain measurement system. A single active gage (120Ω, GF = 2) is used in a bridge configuration to detect small changes in gage resistance caused by strain. The temperature compensation is provided by an equivalent dummy gage and two high precision 120Ω resistors complete the bridge. The 2B35 adjustable power supply is set to a low +3V excitation voltage to avoid the self-heating error effects of the gage and bridge elements. System calibration produces a 1V output for an input of 1000 microstrains. The filter cutoff frequency is set at 100Hz.

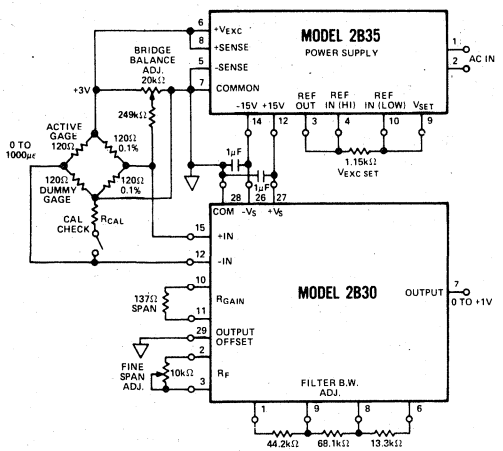


Figure 5. Interfacing Half-Bridge Strain Gage Circuit

Pressure Transducer Interface: A strain gage type pressure transducer (BLH Electronics, DHF Series) is interfaced by the 2B31 in Figure 6. The 2B31 supplies regulated excitation (+10V) to the transducer and operates at a gain of 333.3 to achieve 0-10V output for 0-10,000 p.s.i. at the pressure transducer. Bridge Balance potentiometer is used to cancel out any offset which may be present and the Fine Span potentiometer adjustment accurately sets the full scale output. Depressing the calibration check pushbutton switch shunts a system calibration resistor (R_{CAL}) across the transducer bridge to give an instant check on system calibration.

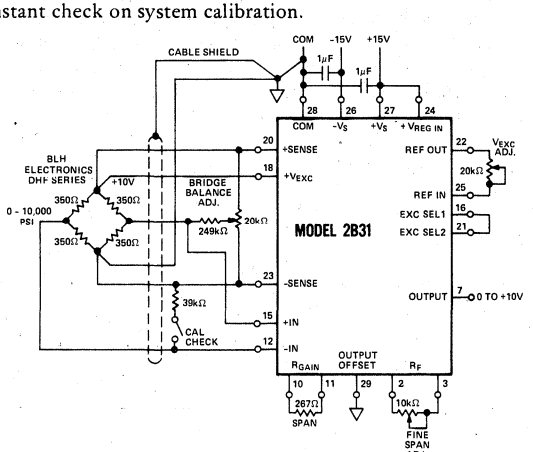


Figure 6. Pressure Transducer Interface Application

Platinum RTD Temperature Measurement: In Figure 7 model 2B31 provides complete convenient signal conditioning in a wide range (−100°C to +600°C) RTD temperature measurement system. YSI - Sostman four-wire, 100Ω platinum RTD (PT139AX) is used. The four wire sensor configuration, combined with a constant current excitation and a high input impedance offered by the 2B31, eliminates measurement errors resulting from voltage drops in the lead wires. Offsetting may be provided via the 2B31's offset terminal. The gain is set by the gain resistor for a +10V output at +600°C.

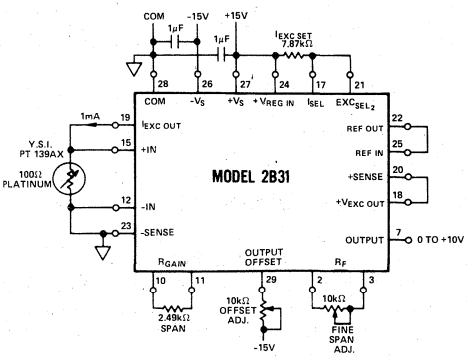


Figure 7. Platinum RTD Temperature Measurement

Interfacing Three-Wire Sensors: A bridge configuration is particularly useful to provide offset in interfacing to a platinum RTD and to detect small, fractional sensor resistance changes. Lead compensation is employed, as shown in Figure 8, to maintain high measurement accuracy when the lead lengths are so long that thermal gradients along the RTD leg may cause changes in line resistance. The two completion resistors (R1, R2) in the bridge should have a good ratio tracking (±5ppm/°C) to eliminate bridge error due to drift. The single resistor (R3) in series with the platinum sensor must, however, be of very high absolute stability. The adjustable excitation in the 2B31 controls the power dissipated by the RTD itself to avoid self-heating errors.

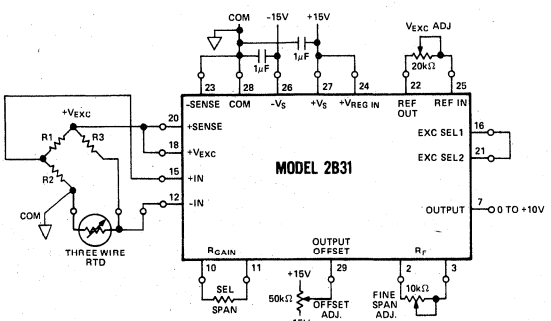


Figure 8. Three-Wire RTD Interface

Linearizing Transducer Output: To maximize overall system linearity and accuracy, some strain gage-type and RTD transducer analog outputs may require linearization. A simple circuit may be used with the 2B31 to correct for the curvature in the input signal. Consult factory for the application assistance.

Data Acquisition System: Figure 9 shows a typical application of the 2B30/2B31 in a low level, high speed microcomputer based data acquisition system. The advantages of this configuration are improvement in CMR enhanced by a low pass filter/channel provided by the 2B31, elimination of aliasing errors and crosstalk noise between input channels, improvement in system noise and resolution, and optimized, individual bridge excitation source for each channel.

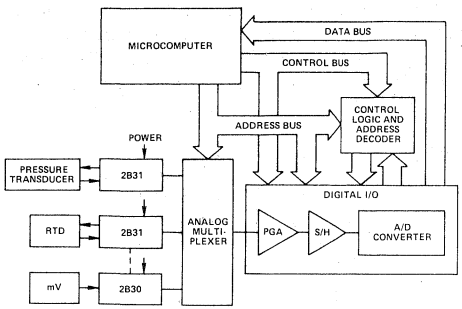


Figure 9. Use of the 2B30/2B31 in Data Acquisition System

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Models 2B30/2B31 are available in three drift selections: ±0.5, ±1 and ±3μV/°C (max, RTI, G = 1000V/V). Total input drift is composed of two sources (input and output stage drifts) and is gain dependent. Figure 10 is a graph of the worst case total voltage offset drift vs. gain for all versions.

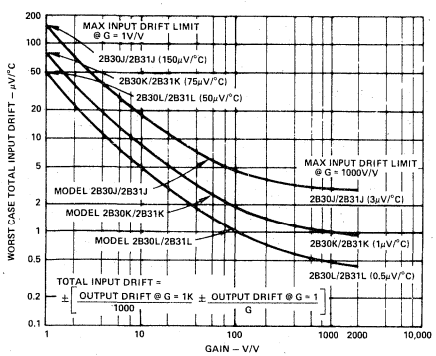


Figure 10. Total Input Offset Drift (Worst Case) vs. Gain

Gain Nonlinearity and Noise: Nonlinearity is specified as a percent of full scale (10V), e.g. 0.25mV RTO for 0.0025%. Three maximum nonlinearity selections offered are: ±0.0025%, ±0.005% and ±0.01% (G = 1 to 2000V/V). Models 2B30/2B31 offer also an excellent voltage noise performance by guaranteeing maximum RTI noise of 1μV p-p (G = 1000V/V, $R_S \leq 5k\Omega$) with noise bandwidth reduced to 2Hz by the low pass filter.

Low Pass Filter: The three pole Bessel-type active filter attenuates unwanted high-frequency components of the input signal above its cutoff frequency (–3dB) with 60dB/decade roll-off. With a 2Hz filter, attenuation of 70dB at 60Hz is obtained, settling time is 600ms to 0.1% of final value with less than 1% overshoot response to step inputs. Figure 11 shows the filter response.

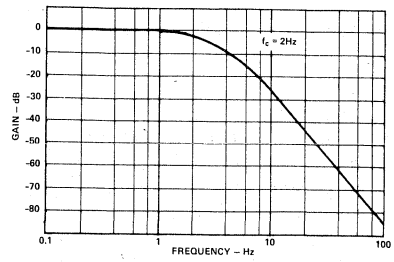


Figure 11. Filter Amplitude Response vs. Frequency

Common Mode Rejection: CMR is rated at ±10V CMV and 1kΩ source imbalance. The CMR improves with increasing gain. As a function of frequency, the CMR performance is enhanced by the incorporation of low pass filtering, adding to the 90dB minimum rejection ratio of the instrumentation amplifier. The effective CMR at 60Hz at the output of the filter (f_c = 2Hz) is 140dB min. Figure 12 illustrates a typical CMR vs. Frequency and Gain.

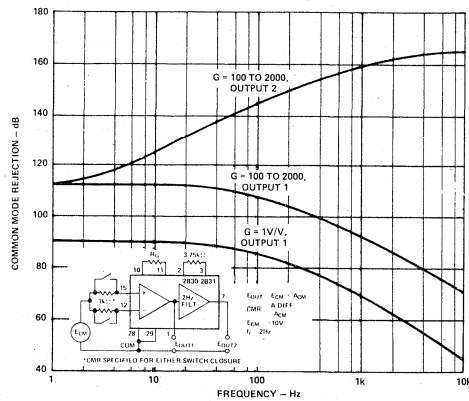


Figure 12. Common Mode Rejection vs. Frequency and Gain

Bridge Excitation (2B31): The adjustable bridge excitation is specified to operate over a wide regulator input voltage range (+9.5V to +28V). However, the maximum load current is a function of the regulator circuit input-output differential voltage, as shown in Figure 13. Voltage output is short circuit protected and its temperature coefficient is ±0.015% V_{OUT}/°C max (±0.003%/°C typ). Output temperature stability is directly dependent on a temperature coefficient of a reference and for higher stability requirements, a precision external reference may be used.

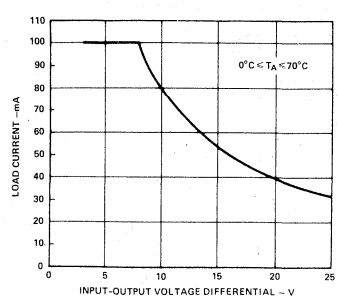


Figure 13. Maximum Load Current vs. Regulator Input-Output Voltage Differential

Precision, Triple Output Transducer Power Supply

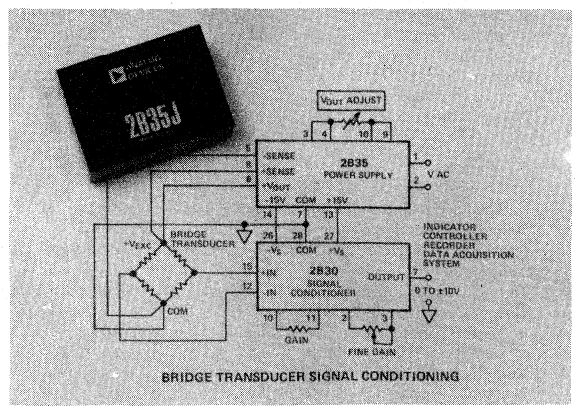
MODEL 2B35

FEATURES

- Resistor Programmable Voltage or Current Output
  - Voltage: +1V dc to +15V dc @ 125mA max
  - Current: 100μA to 10mA (V_{COMPL} = +10V)
- Dual Fixed Output: ±15V dc @ ±65mA max
- Excellent Regulation: Line ±0.01% max; Load ±0.02% max
- Low Drift: 0.006%/°C max (2B35K)
- No Derating Over -25°C to +71°C Operating Range

APPLICATIONS

- Measurement and Control Instruments and Systems
- Excitation Source For:
  - Strain Gages, Pressure Transducers, Load Cells, Torque Transducers, RTD's



BRIDGE TRANSDUCER SIGNAL CONDITIONING

GENERAL DESCRIPTION

The 2B35 is a triple output modular power supply designed to provide regulated excitation to a wide variety of transducers as well as ±15V power for amplifiers and other analog circuits of an instrumentation system. The single-resistor programmable transducer excitation output may be operated in two modes: constant voltage, providing a +1V to +15V output or a constant current, adjustable from 100μA to 10mA.

The programmable output in the voltage mode features current rating of 0 to 125mA, suitable to excite four 350Ω transducers at 10V. Current limiting protects the output against accidental overload and remote sensing corrects for the transducer cable resistance variations. In the constant current mode, externally set 100μA to 10mA output offers a 0 to +10V compliance voltage range. The ±15V outputs feature 0.5% tracking accuracy and current rating of 0 to ±65mA max.

Two accuracy selections are available offering guaranteed low temperature coefficient; 2B35K: 0.006%/°C max and 2B35J: 0.05%/°C max. Line and load regulation are also guaranteed; 2B35K: 0.01% and 0.02%, and 2B35J: 0.08% and 0.1%, max, respectively.

APPLICATIONS

The 2B35 is designed for ac powered signal conditioning instrumentation applications used for data acquisition, control, indication or recording. This compact module may be applied as a power source for the model 2B30 strain gage transducer/RTD signal conditioner in a high accuracy transducer interface application. Some typical applications involve strain gages for stress/strain measurements, pressure transducers, load cells, torque transducers and RTD's.

OPERATION

Figure 1 illustrates operation of the 2B35K providing an adjustable voltage output and dual 15V dc outputs. The resistor programmable output (+V_{OUT}) is set between +1V to +15V by the R_{TRIM}. R_{TRIM} may be determined by using either the table shown in Figure 1 or the graph shown in Figure 2. For example, to provide an adjustable range from +1V to +6V, R_{TRIM} should be a 5kΩ pot.

The remote sensing inputs (pins 5 and 8) are connected at the transducer (load) to the voltage output (SENSE HIGH to +V_{OUT} and SENSE LOW to COMMON).

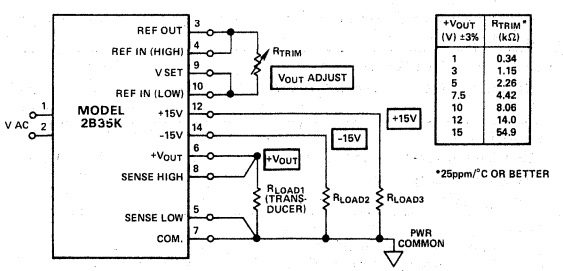


Figure 1. Model 2B35K Connection Diagram for Dual 15V dc and Adjustable +1V to +15V Output

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

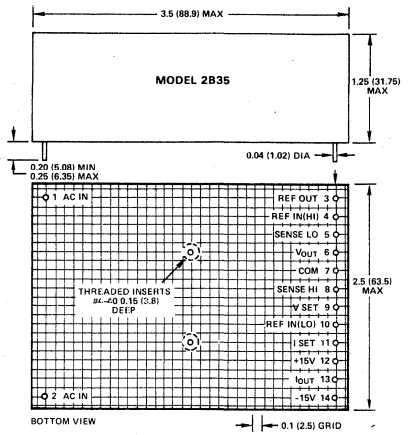
Model	2B35J	2B35K
INPUT		
Input Voltage Range[1]	105V ac to 125V ac	*
Input Frequency Range	50Hz to 400Hz	*
ADJUSTABLE OUTPUT		
Voltage Mode		
Output Voltage Range	+1V to +15V dc	*
Output Voltage Stability		
vs. Temperature – % V_{OUT}/°C max	±0.05	±0.006
vs. Time – % V_{OUT}/month	±0.01	*
Output Current (–25°C to +71°C)[2]	0 to 125mA max	*
Output Impedance – @ dc, max	0.1Ω	*
Noise and Ripple (dc to 1MHz) – mV p-p max	1	*
– mV rms max	0.25	*
Regulation		
Line (full range) – % V_{OUT} max	±0.08	±0.01
Load (no load to full load) – % V_{OUT} max	±0.1	±0.02
Remote Sensing Impedance	30kΩ	*
Short Circuit Current Limit[3] (–25°C to +71°C)	200mA	*
Current Mode		
Output Current Range	100µA to 10mA	*
Output Current Stability		
vs. Temperature – % I_{OUT}/°C max	±0.05	±0.006
vs. Time – % I_{OUT}/month	±0.01	*
Compliance Voltage Range	0 to +10V	*
Noise and Ripple (dc to 1MHz) –µA p-p	0.1	*
Line Regulation (full range) – % I_{OUT} max	±0.08	±0.01
DUAL FIXED OUTPUTS		
Output Voltage	±15V dc	*
Voltage Error – mV max	–0, +300	*
Accuracy Tracking (–15V Ref to +15V) – % max	±0.5	*
Stability vs. Temperature – %/°C max	±0.02	±0.006
Output Current[4]	0 to ±65mA max	*
Output Impedance – @ dc, max	0.1Ω	*
Noise and Ripple (dc to 1MHz) – mV p-p	1	*
– mV rms	0.25	*
Regulation		
Line (full range – % max	±0.08	±0.01
Load (no load to full load) – % max	±0.1	±0.02
Short Circuit Current Limit[3] (–25°C to +71°C)	±180mA	*
INPUT TO OUTPUT ISOLATION		
Breakdown Voltage – Continuous, ac or dc	±500V pk max	*
Isolation Resistance	50MΩ	*
TEMPERATURE RANGE		
Operating, Rated Performance	–25°C to +71°C	*
Storage	–25°C to +85°C	*
MECHANICAL		
Case Dimensions – Inches	2.5 x 3.5 x 1.25	*
Weight – Grams	550	*
Mating Socket	AC1212	*

NOTES
*Specifications same as model 2B35J.
[1] Optional input voltage ranges: "E" Option; 205-240V ac, 50 to 400Hz
"F" Option; 90-110V ac, 50 to 400Hz
"H" Option; 220-260V ac, 50 to 400Hz
Order option desired as a suffix to model number.
[2] Maximum output current available over the entire output voltage and temperature range without derating.
[3] Output protected for continuous short circuit over the temperature range.
[4] Unbalanced load operation is permissible for any combination of $+I_O$ and $|-I_O|$ which does not exceed a total of 130mA.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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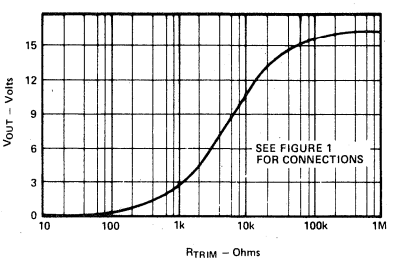


Figure 2. Voltage Output vs. R_{TRIM}

ADJUSTABLE CURRENT OUTPUT WITH DUAL 15V dc OUTPUTS

Pin connections to provide dual 15V dc and a constant current output are shown in Figure 3. The current output is adjusted from 100µA to 10mA via R_{TRIM}. The value of programming resistor R_{TRIM} may be calculated from the relationship: $R_{TRIM} = 2.46/I_{OUT}$ where R_{TRIM} is in kΩ and I_{OUT} in mA.

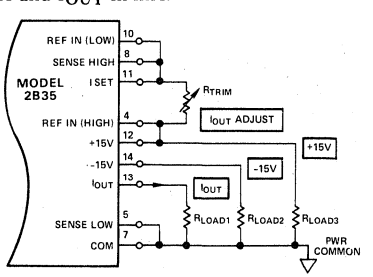


Figure 3. Model 2B35 Connection Diagram to Provide Dual 15V dc and Adjustable 100µA to 10mA Current Output

Four-Channel, Isolated Thermocouple/mV Conditioners

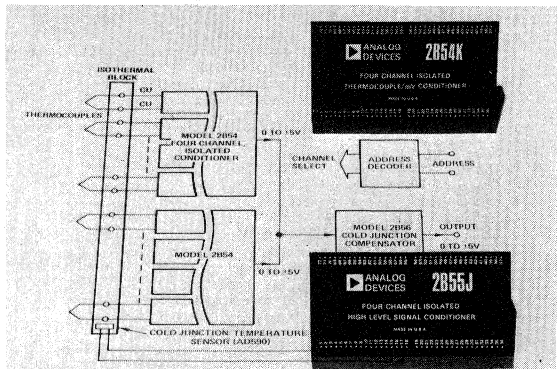
MODELS 2B54 AND 2B55

FEATURES

Low Cost
Wide Input Span Range: ±5mV to ±100mV (2B54)
±50mV to ±5V (2B55)
12-Bit Systems Compatible
High CMV Isolation: ±1000V dc; CMR = 156dB min @ 60Hz
Low Input Offset Voltage Drift: ±1μV/°C max (2B54B)
Low Gain Drift: ±25ppm/°C max (2B54B)
Low Nonlinearity: ±0.02% max (±0.012% typ)
Normal Mode Input Protection (130V rms) and Filtering
Channel Multiplexing: 400 chan/sec Scanning Speed
Solid State Reliability

APPLICATIONS

Multichannel Thermocouple Temperature Measurements
Low and High Level Data Acquisition Systems
Industrial Measurement and Control Systems



TEMPERATURE MEASUREMENT SYSTEM

GENERAL DESCRIPTION

Models 2B54 and 2B55 are low cost, high performance, four-channel signal conditioners. Both models are functionally complete, providing input protection, isolation and common mode rejection, multiplexing, filtering and amplification.

The 2B54 has been designed to condition low level signals (±5mV to ±100mV), like those generated by thermocouples or strain gages, in the presence of high common mode voltages. The 2B55 is optimized to condition ±50mV to ±5V or 4 to 20mA transmitter signals as inputs. The four-channel structure of both models results in significant cost and size reduction.

The high performance of the 2B54 and 2B55 is accomplished by the use of reliable transformer isolation techniques and an amplifier-per-channel architecture. Each of the input channels is galvanically isolated (±1000V dc) from the other input channels and from output ground. The amplifier-per-channel structure is used to obtain low input drift (±1μV/°C max, 2B54B), high common mode rejection (156dB @ 60Hz), and very stable gain (±25ppm/°C max). Other key features include low input noise (0.6μV p-p), low nonlinearity (±0.02% max) and open-thermocouple detection (2B54).

APPLICATIONS

Models 2B54 and 2B55 were designed to serve as a superior alternative to the relay multiplexing circuits used in multi-channel data acquisition systems, computer interface systems, process signal isolators, and temperature measurement and control instrumentation. Advantages over relay circuits include functional versatility, superior performance, and solid state reliability.

In thermocouple temperature measurement applications, outstanding low drift, high noise rejection, high throughput and 1000V isolation make the 2B54 a natural choice over flying capacitor multiplexers in conditioning any thermocouple type. When cold junction compensation is required in measurement of temperature with thermocouples, the 2B54 may be used directly with the model 2B56 Universal Cold Junction Compensator.

DESIGN FEATURES AND USER BENEFITS

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, reliable transformer isolation and solid state switching are used. Both models have been conservatively designed to meet the IEEE standard for Transient Voltage Protection (472-1974:SWC) and offer 130V rms normal mode input protection.

High Noise Rejection: To preserve high system accuracy in electrically noisy industrial environments, the 2B54 and 2B55 provide excellent common mode noise rejection, RFI/EMI immunity, and low pass filtering for rejection of series mode noise and 50Hz/60Hz pickup.

Ease of Use: The multichannel, functionally complete design in a compact (2″ X 4″ X 0.4″) module, assures ease of use, conserves board space and eliminates the need for a number of discrete components necessary in relay multiplexing circuits.

Low Cost: The 2B54 and 2B55 offer the lowest cost per channel for isolated, solid state, low level signal conditioners.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V and V_{OSC} = +15V, unless otherwise noted)

Model	2B54A	2B54B	2B55A
ANALOG INPUTS			
Number of Channels	4	*	*
Input Span Range	±5mV to ±100mV	*	±50mV to ±5V
Gain Equation	$G = 1 + 10k\Omega/R_G$	*	*
Gain Error	±0.2% max (G = 50 to 300)	*	±0.2% max (G = 1 to 100)
	±1% max (G = 1000)	*	NA
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max	±25ppm/°C max
Gain Nonlinearity[1]	±0.03% max (G = 50 to 300)	±0.02% max(±0.012% typ)	±0.02% max (G = 1 to 100)
	±0.03% (G = 1000)	*	NA
Offset Voltage			
Input Offset, Initial (Adj. to Zero)	±20µV max	*	±50µV max
vs. Temperature	±2.5µV/°C max	±1µV/°C max(±0.5µV/°C typ)	±5µV/°C max
vs. Time	±1.5µV/month	*	*
Output Offset (Adjustable to Zero)	±12mV max	*	*
vs. Temperature	±50µV/°C max	*	*
Total Offset Drift (RTI), max	$\pm\left(2.5+\frac{50}{G}\right)\mu V/°C$	$\pm\left(1+\frac{50}{G}\right)\mu V/°C$	$\pm\left(5\mu V+\frac{50}{G}\right)\mu V/°C$
Input Noise Voltage			
0.01Hz -100Hz, R_S = 1kΩ	0.6µV p-p	*	*
CMV, Channel-to-Channel or Channel-to-Ground			
Continuous, ac, 60Hz	750V rms	*	*
Continuous, ac or dc	±1000V pk max	*	*
Common Mode Rejection			
$R_S \leq 100\Omega, f \geq 50Hz$	156dB min (G = 1000)	*	145dB min (G = 100)
$R_S \leq 100\Omega, f \geq 50Hz$	128dB min (G = 50)	*	110dB min (G = 1)
Normal Mode Input, Without Damage	130V rms, 60Hz	*	*
Normal Mode Rejection, @ 60Hz	55dB min (G = 1000)	*	55dB min (G = 100)
Input Resistance, Power On	100MΩ	*	*
Power Off	35kΩ min	*	74kΩ min
Input Bias Current	+8nA max	*	*
Open Input Detection Time[2]	6 sec (G = 1000)	*	NA
	120 sec (G = 50)	*	NA
Open Input Response	Negative Overscale	*	NA
ANALOG OUTPUT			
Output Voltage Swing[3]	±5V @ ±5mA	*	*
Output Noise, dc - 100kHz	0.8mV p-p	*	*
Output Resistance			
Direct Output	0.1Ω	*	*
Switched Output	35Ω	*	*
CHANNEL SELECTION			
Channel Selection Time to ±0.01% FS	2.5ms max	*	*
Channel Scanning Speed	400 chan/sec min	*	*
Channel Select Input Reverse Voltage			
Rating	3V max	*	*
POWER SUPPLY			
Voltage			
Output ±V_S (Rated Performance)	±15V dc ±10%	*	*
(Operating)	±12V to ±18V dc max	*	*
Oscillator +V_{OSC}			
(Rated Performance)	+13.5V to +24V	*	*
Absolute max +V_{OSC}	+26V	*	*
Current			
Output ±V_S = ±15V	±4mA max	*	*
Oscillator +V_{OSC} = +15V	40mA max	*	*
Supply Effect on Offset			
Output ±V_S	100µV/V RTO	*	*
Oscillator +V_{OSC}	1µV/V RTI	*	*
ENVIRONMENTAL			
Temperature			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +85°C	*	*
Relative Humidity			
Non-Condensing to +40°C	0 to 85%	*	*
CASE SIZE	2" X 4" X 0.4"	*	*

*Specifications same as 2B54A.
[1] Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g. nonlinearity at an output span of 10V pk-pk (±5V) is ±0.02% or ±2mV.
[2] Response time can be reduced by addition of external resistors. More than one open input may cause output to saturate on all channels.
[3] Protected for shorts to ground and/or either supply voltage.

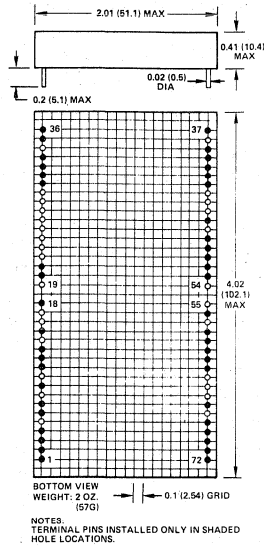
Specifications subject to change without notice.

MOUNTING CARDS
AC1215, AC1216

The AC1215 and AC1216 mounting cards are available to assist in evaluation of the 2B54 and 2B55. These 4 1/2" X 6" printed circuit edge connector cards have sockets that allow a 2B54/2B55 and 2B56 to be plugged directly onto them, as well as offset adjustment pots, and address decoding circuitry. The AC1215 and AC1216 differ only in input signal connections: the AC1215 includes a screw terminal block and AC1216 has an edge connector.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

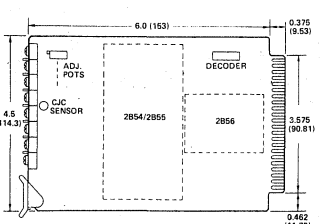


2B54/2B55 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	- } SELECT CH. D	37	HI
2	+ }	38	
3	SW'D OUTPUT ENABLE	39	R_G
4	SWITCHED	40	R_G/COM } CHANNEL A
5		41	LO/OFS
6	DIRECT	42	V-
7	SENSE	43	V+
8	} OUTPUT	44	
9	OFS. ADJ.	45	
10		46	
11	-V_S	47	HI
12	COM	48	
13	+V_S	49	R_G
14		50	R_G/COM } CHANNEL B
15	- }	51	LO/OFS
16	SELECT CH. C	52	V-
17		53	V+
18	+ }	54	
19		55	
20	- } SELECT CH. B	56	HI
21	+ }	57	
22		58	R_G
23		59	R_G/COM } CHANNEL C
24		60	LO/OFS
25		61	V-
26		62	V+
27		63	
28		64	
29		65	
30	+V_{OSC} } OSC. POWER	66	HI
31	COM }	67	
32	IN } SYNC	68	R_G
33	OUT }	69	R_G/COM } CHANNEL D
34		70	LO/OFS
35	- } SELECT CH. A	71	V-
36	+ }	72	V+

AC1215 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Mating Connector:
Cinch 251-22-30-160 or equivalent.

FUNCTIONAL DESCRIPTION

The internal structure of the 2B54/2B55 is shown in Figure 1. Four individually isolated input channels are multiplexed into a single output buffer, with the desired channel selected by control inputs SELECT A through SELECT D. Isolated power and timing signals for the input channels are provided by an internal oscillator.

Each channel contains an input protection and filtering network and a low-drift amplifier whose gain is set by a user-supplied resistor (R_G). Additional filtering is provided in the amplifier circuit. This structure preserves signal integrity by taking all signal gain ahead of the isolation and multiplexing circuits. The isolated power supply for each channel is brought out to permit convenient fine adjustment of the input offset voltage if desired.

Transformer coupling is used to achieve stable, reliable galvanic isolation of each channel from all other channels and from output ground. Although the bandwidth of the input channels is small (<2Hz at high gains) to provide immunity to normal-mode noise, the multiplexing technique allows the channels to be scanned at a high rate (400 channels/sec). Thus a high revisitation rate is maintained even in systems with a large number of input channels.

The output buffer amplifier operates at unity gain with feedback provided by an external connection from the DIRECT output to the SENSE input. The DIRECT output provides a ±5V swing with low source resistance to permit error-free operation with heavy loads. In addition, a separate series-switched output with an active-low enable control is provided so that multiple modules may be combined without the use of external analog multiplexers. An offset trim point which does not affect drift is also provided on the output channel.

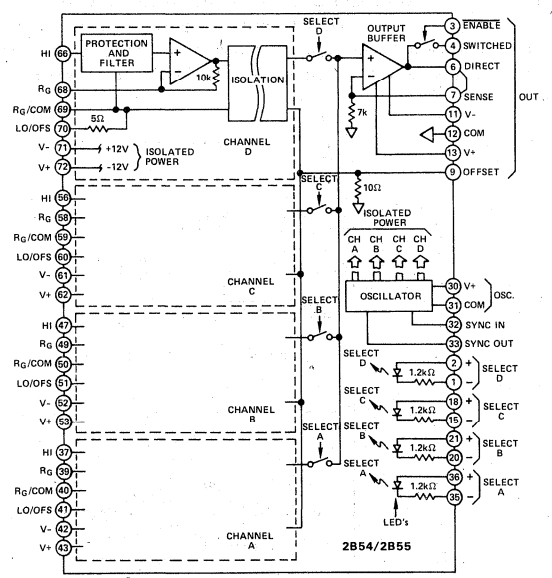


Figure 1. 2B54/2B55 Functional Diagram

The internal oscillator has its own power supply pins for enhanced application flexibility, and a sync mechanism is provided to eliminate beat-frequency errors when multiple 2B54/2B55's are used or when a system clock is present.

The 2B54 and 2B55 share the same design, differing only in input specifications and filter characteristics.

OPERATING INSTRUCTIONS

The connections shown in Figure 2 are common to most applications of the 2B54/2B55, and in many cases will be all that is required. The following sections describe this basic application and also detail some optional connections which enhance the module's utility in more complex applications.

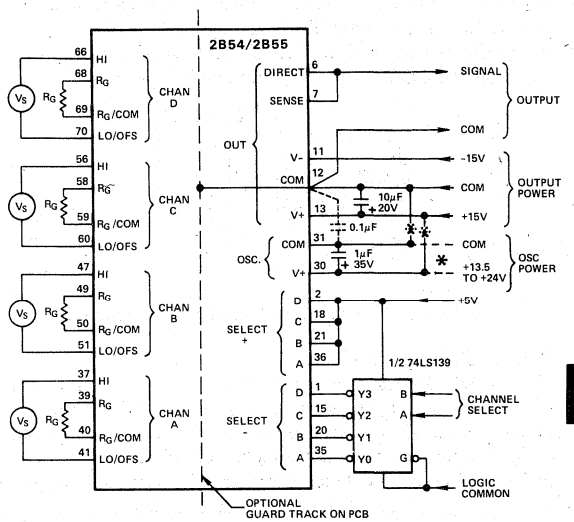


Figure 2. Basic 2B54/2B55 Application

Interconnection Guidelines

In any high accuracy isolator application it is important to minimize coupling between input and output, and the 2B54/2B55 pinout has been designed to make this easy to do. For best results, keep all leads associated with signals on the input edge as far as possible from signals on the output edge. This will minimize the effects of board leakage and capacitance. The use of a guard track on both sides of the board (Figure 2) can also be helpful.

The power supplies should be decoupled with tantalum capacitors as close to the unit as possible. For lowest noise, the output grounding scheme should be as shown in Figure 2. The output signal common is connected directly to pin 12, with power supply returns brought separately to that pin so that power supply currents do not flow in the low lead of the signal output.

Since most of the power taken by the 2B54/2B55 is supplied to the internal oscillator which requires only a positive supply and can accommodate a wide range of supply voltages, it is sometimes desirable to power the oscillator from a convenient source of unregulated power (such as +24V). The 0.1µF capacitor should be then connected directly from pin 12 to pin 31. Since the output and oscillator circuits are not fully isolated, a dc path must exist between the two power supply commons. A small one or two volts potential difference between OUT COM and OSC COM will not affect operation.

Gain Setting

The gain of each channel is independently set by a user-supplied resistor (R_G) connected as shown in Figure 2. Channel gain will normally be selected so that the maximum output of the signal source will result in a plus or minus full scale (±5V) output swing. The resistor value required is $R_G = 10k\Omega/(G-1)$. Thus if $R_G = 101\Omega$, the gain will be 100, and an input signal swing of ±50mV will yield an output span of ±5V.

A parallel trim on the gain-setting resistor can be used to trim out the resistor's tolerance and the module's gain error (Figure 3). Since a parallel trim will always increase the gain, the value of the gain-setting resistor should be chosen to give an untrimmed gain somewhat lower than the desired trimmed gain. Good quality metal-film resistors should be used for R_G since gain accuracy and drift are a direct function of R_G's characteristics. Cermet pots are suitable for the trim.

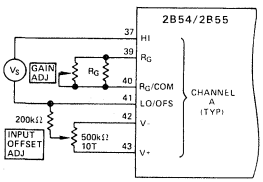


Figure 3. Input Offset and Gain Adjustments

Optional Offset Adjustment

The 2B54/2B55 has provision for fine adjustment of the input offset of each channel and the output offset of the entire module. None of the offset adjustments affect offset drift, and there is no need to make any adjustment unless the application calls for tighter offsets than those specified for the module type.

Connections for input offset adjustment are shown in Figure 3. This is a fine trim with a limited range (±250μV referred to the input), and in most applications can be used to adjust each channel for zero offset while operating at the desired gain. Since the range of the input offset trim is small, it will usually be necessary to adjust output offset first. This can be conveniently done by operating one channel with zero input at unity gain (by disconnecting the gain resistor) and adjusting the output offset control for zero output. Connections for output offset adjustment are shown in Figure 4.

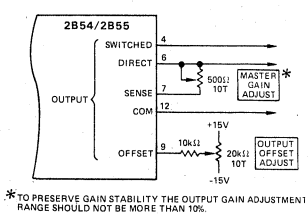


Figure 4. Output Offset and Master Gain Adjustments

An alternative offset adjustment procedure is appropriate in applications where the channel gains are field-selected by switching the gain-setting resistor. Here it is desirable to set the input offset so that there is no zero shift at the output when the gain is changed. To make the adjustment, switch back and forth from low to high gain with zero input and adjust the input offset control until no shift occurs at the output when changing gains. Then adjust the output offset control for zero output at the lower gain.

Stable components (a metal film resistor and a cermet pot) should be used for the input offset adjustment to avoid compromising drift. Output offset adjustment components are not critical and may be omitted altogether when a single 2B54/2B55 is followed by an A to D Converter that has a zero adjustment.

Channel Selection

Each channel in the 2B54/2B55 is turned on and off by a SELECT input. As indicated in Figure 1, each SELECT input consists of an LED in series with a resistor, and is not connected to any other circuits in the module. Turning the LED on ($I \geq 2.5mA$) turns the channel on, and turning the LED off ($I \leq 50\mu A$) turns the channel off. This allows considerable flexibility of connection, but the easiest way to use the SELECT inputs is to tie all four SELECT + pins to +5V and drive the SELECT—inputs from TTL logic (either open-collector or totem-pole outputs can be used), as shown in Figure 2.

It is also possible to use CMOS logic to drive the SELECT inputs (Figure 5). With a +15V logic supply a standard CMOS decoder or gate can supply enough current to drive the SELECT inputs directly, but at lower supply voltages it is advisable to use a buffer such as that shown in Figure 5b. The power taken by the SELECT inputs is small, since only one is on at a time, but at the higher CMOS supply voltages more current than the required 2.5mA will flow. This does not affect operation, but if desired the current can be brought back to the minimum value with series resistors as shown in Figure 5. Use 2kΩ for 10V operation, and 3.9kΩ at 15V.

The maximum reverse voltage applied to any SELECT input must be limited to 3V to avoid damage to the LED. Maximum forward current should be kept below 25mA. Each SELECT input is isolated from all other circuits in the module and may be operated up to ±50V away from output and power ground.

Channels may be selected in any order, and there are no restrictions on rate or duty cycle except the 2.5ms settling time for access to a channel. It should be noted, however, that selecting two or more channels simultaneously for more than a few microseconds will result in a very long settling time when the conflict is resolved. Timing overlaps should therefore be avoided.

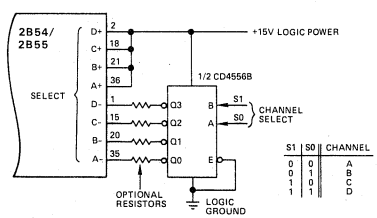


Figure 5a.

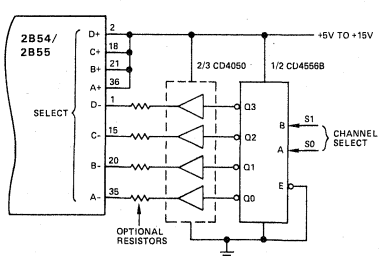


Figure 5b.

Figure 5. CMOS Channel Selection

Channel Expansion

The 2B54/2B55 has provision for directly interconnecting several modules when more than four channels are needed. The series-switched outputs of a group of modules are connected together, the SELECT inputs are driven in parallel, and the output of the desired module is selected using the Output Enable pin. This is shown in Figure 6. A single 74LS139 decoder is used to drive the SELECT inputs of up to four modules, and also provides address expansion so that the binary coded channel address word selects the appropriate module output via the Output Enable pins. The overall operation of the series-switched outputs is analogous to three-state logic, and the output rail is thus an analog bus.

It is possible to operate up to sixteen modules in parallel, for a total of 64 input channels. Note that it will be necessary to break up the SELECT inputs into several groups to avoid overloading the decoder when many modules are used. The settling time of the output switches is <50μs to ±0.01% and is thus negligible in comparison to the channel selection times.

The Output Enable signal is active low, and is compatible with both TTL and CMOS logic. The switching threshold is +1.8V; input current at 0V is typically -0.4mA.

The output resistance of the Switched Output (typically 35Ω +0.5%/°C) is low enough to provide fast switching times but will cause gain errors when driving a heavy load. A single buffer isolating the Switched Outputs from the load will solve this problem in an "analog bus" application (Figure 6). In single-module applications the DIRECT (low impedance) output should be used. Note that in all cases the SENSE pin *must* be connected to the DIRECT output to provide feedback for the output amplifier.

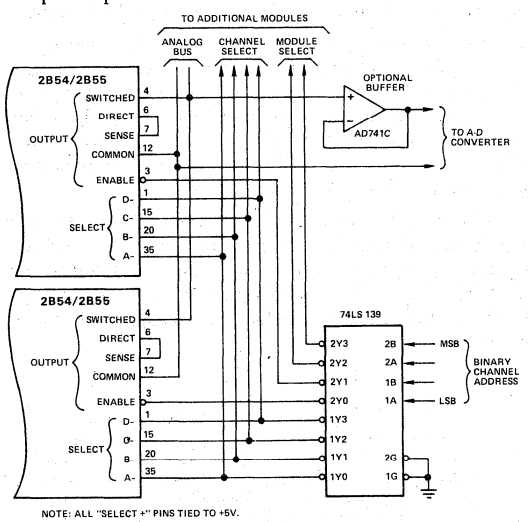


Figure 6. Expansion to More than Four Channels

Synchronization

In applications where multiple 2B54/2B55's are used in close proximity or when system clock signals are present near the isolator, differences in individual oscillator frequencies may cause "beat frequency" related output errors. To eliminate these errors, multiple units may be synchronized by connecting the SYNC OUT (pin 33) terminal to the SYNC IN (pin 32) terminal of the adjacent 2B54/2B55 (Figure 7). The first of a group of modules may be synchronized to an external source via the SYNC IN pin. To minimize noise pickup, sync wiring should be separated from analog signal runs.

The frequency of the external sync source, when used, will have a small effect on the gain and output offset of the 2B54/2B55. Thus any adjustments should be made with the module synchronized.

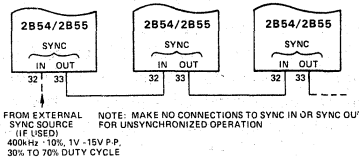


Figure 7. Synchronization

Open Input Detection

The 2B54 always responds to an open-circuit condition on a channel input by presenting a negative overscale (typically -7V) at the output when the affected channel is selected. The response time to detect an open input can be in the tens of seconds, since only a few nA of input bias current is available to charge the input filter. If shorter response times are desired, or if a positive overscale is the desired response, one of the circuits shown in Figure 8 can be used to augment or reverse the input bias current. Either circuit will produce a bias current of approximately 20nA which can be used to aid or oppose the 3nA typically supplied by the module, as shown. The circuit of Figure 8A has the advantage of simplicity, but the high-value resistor may not be readily available. Figure 8B shows how to solve the problem at the expense of complexity. The values shown may be modified to give an optimum trade of bias current for response time in a given application. A 2 to 5 second response is typical for the values shown.

The same circuits may be used to get open input detection with the 2B55, which is not specified for stand-alone open input response.

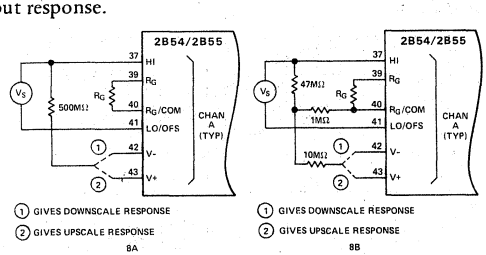


Figure 8. High Speed or Reversed Open Input Detection

Output Filtering

In most applications, no output filtering will be required since the effect of the small carrier-related noise spikes on the output (<1mV p-p, 100kHz B.W.) drops off rapidly as bandwidth decreases and in many cases will be negligible. In some applications (e.g., when driving a successive-approximation A to D) the effective system bandwidth may be large enough to pass the noise. To eliminate the carrier noise (without any effect on switching times), a simple R-C filter may be used at the output (Figure 9A). Only one filter is needed even when multiple modules are used, as shown in Figure 9B. If the load to be driven has an input resistance of less than 10MΩ, a buffer will be needed.

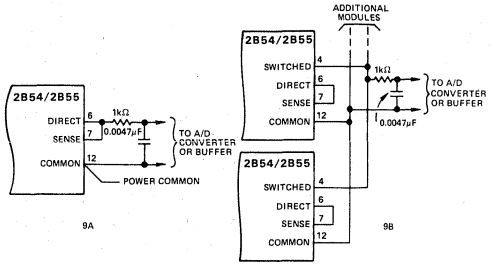


Figure 9. Output Filtering

CMR AND NMR PERFORMANCE

Common mode rejection is a result of both isolation and filtering and indicates ability to reject common mode inputs while amplifying differential signal inputs. CMR is dependent on source impedance imbalance, signal frequency and conditioner gain.

Normal mode rejection is also a function of the 2B54/2B55 gain. Figures 10 and 11 illustrate typical CMR and NMR performance. Note that any additional low pass filtering (e.g., an integrating A to D converter) at the output of the 2B54/2B55 will further improve both CMR and NMR performance.

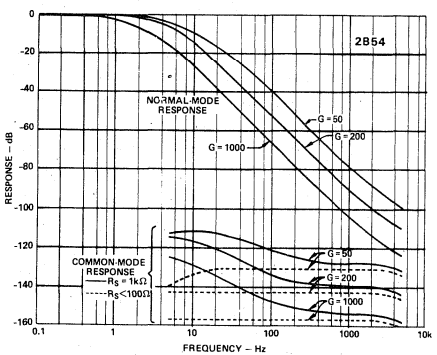


Figure 10. Common Mode and Normal Mode Response — Model 2B54

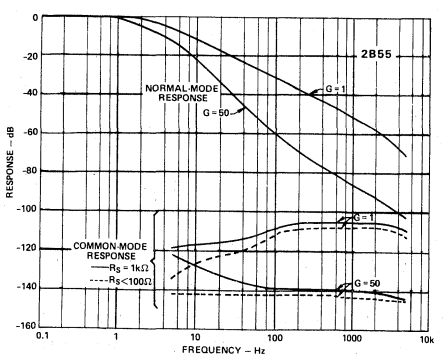


Figure 11. Common Mode and Normal Mode Response — Model 2B55

APPLICATIONS

Thermocouple Temperature Measurement: Figure 12 shows a four-channel thermocouple input system with isolation, amplification, and multiplexing provided by the 2B54. Several different thermocouple types are used, and the gain-setting resistors on each channel have been chosen to take the standard ANSI range for each type to a 5V output span. Since thermocouples must be compensated for the temperature of the reference junction which is formed where the thermocouple leads are terminated, the 2B56 Universal Cold Junction Compensator is used. The 2B56 monitors the temperature of the reference junction (terminal block) via an external sensor and corrects the signal at the output of the 2B54 for reference temperature. Compensation for several thermocouple types is selectable via digital control inputs. Thermocouple linearization, if needed, would be typically performed in system's software.

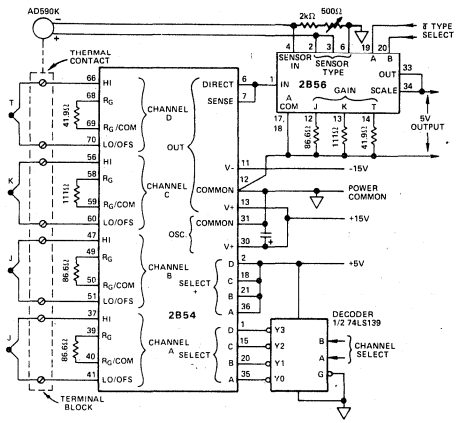


Figure 12. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

Process Signals Interface: In Figure 13, the 2B55 is used to provide floating inputs for four 4-20mA process signal loops. The use of floating inputs in this type of application gives protection from common-mode voltages and greatly simplifies system configuration, since additional loads in series with the loop can be connected on either side of the isolator input.

Each current input is converted into a 1 to 5 volt signal by a 250Ω resistor. The 2B55 is operated at unity gain (no gain-setting resistors) so that a 1 to 5 volt signal appears at the output. Since no gain-setting resistors are used, gain adjustment, if required, is done by connecting trims directly across the input resistors. Other current ranges can be accommodated by changing the value of the input resistors.

When there are several loads on the loop, compliance voltage at the transmitter may be at a premium. In this case it will be advantageous to reduce the voltage swing at the isolator inputs by using smaller resistors (perhaps 25Ω) and scaling the output back to a 5V span by taking an appropriate gain in the isolator.

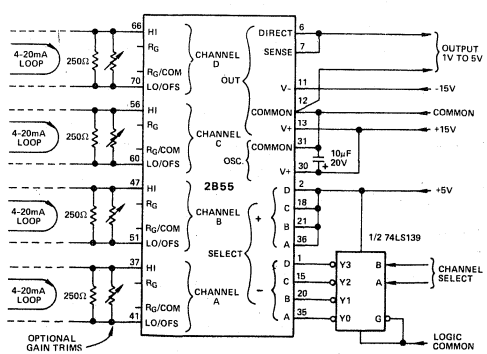


Figure 13. Isolated 4-20mA Loop Signals Interface

High Accuracy, Thermocouple Cold Junction Compensator

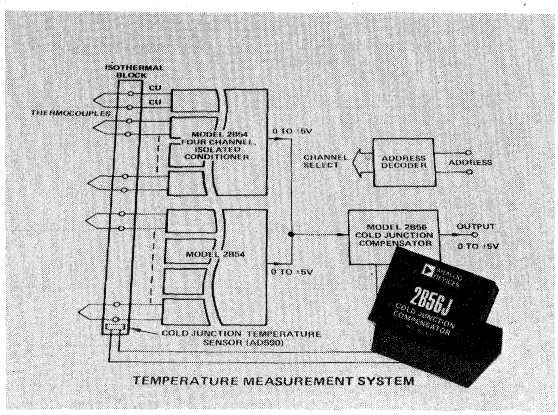
MODEL 2B56

FEATURES

- Universal Thermocouple Compensation:
  - Internally Provided: Types J, K, T
  - User Configurable: Types E, R, S, B
- Digitally Programmable
- High Accuracy: ±0.8°C max over +5°C to +45°C
- High Ambient Rejection: 50 to 1 min
- Low Cost
- Small Size: 1.5″ X 2″ X 0.4″

APPLICATIONS

- Thermocouple Signal Conditioning
- Temperature Measurement and Control Systems
- Temperature Data Acquisition and Logging
- Temperature Controllers



TEMPERATURE MEASUREMENT SYSTEM

GENERAL DESCRIPTION

Model 2B56 is a high accuracy, universal thermocouple cold junction compensator. Designed to operate with an external temperature sensor in thermal contact with the cold junction, the 2B56 provides an automatic compensation for amplified thermocouple signals over wide ambient temperature variations. The 2B56 is calibrated to compensate the cold junction to a reference temperature of 0°C. The total compensation error is ±0.8°C max over +5°C to +45°C.

Designed to compensate seven different thermocouple types, the 2B56 may be digitally programmed to select compensation for types J, K and T, and one user programmed type (E, R, S, B or none). This feature makes the 2B56 especially suitable for multichannel applications involving several thermocouple types.

COLD JUNCTION COMPENSATION PRINCIPLES

In thermocouple measurements, temperature is determined by measuring the potential difference between the measurement (hot) junction of two dissimilar metals and the reference (cold) junction which is formed when thermocouple leads are connected to a measuring circuit. Since this potential difference is proportional to the temperature difference between the measurement temperature and the temperature at the reference junction, the reference junction temperature must be known. Changes in reference junction temperature influence the output voltage and, therefore, cold junction compensation is required to eliminate measurement errors.

Two methods may be used to reduce errors introduced at the thermocouple connections: keep the reference junction at a known constant temperature, or measure the reference junction temperature and cancel the changes by the appropriate correction to the thermocouple output signal. The first method, accomplished by immersing the reference junction in an ice bath maintained at 0°C is not very practical. The 2B56 employs the second method and has been specifically designed to eliminate the need for ice baths by electronically simulating the desired reference point. Digital programmability, high accuracy and low cost make the 2B56 ideal for single or multichannel thermocouple temperature measurement, indication or control systems.

FUNCTIONAL DESCRIPTION

The 2B56 compensates for cold junction temperature by adding a correction signal at the output of the user's thermocouple amplifier, as shown in Figure 1. The value of the correction signal is determined by the cold junction temperature, as measured by a sensor, and the thermocouple type in use, as specified by two digital TYPE SELECT inputs. Since compensation is done at the output of the thermocouple amplifier it is also necessary to scale the correction signal for the gain of the amplifier. This is done by a scaling circuit which has provision for a user-supplied gain-setting resistor for each thermocouple type in use.

Compensating networks for thermocouple types J, K, and T are built into the 2B56. A fourth compensation (X) can be programmed with two external resistors for any other thermocouple type. The X compensation can also be used without programming resistors to obtain an uncompensated output when sensors other than thermocouples are in use.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V unless otherwise noted)

MODEL	2B56A
COLD JUNCTION COMPENSATION	
Thermocouple Types:	
Internally Compensated	J, K, T
Externally Programmable	B, E, R, S, None
Reference Temperature	0°C
Compensation Accuracy	
Total Output Error @ +25°C[1]	±0.2°C
vs. Ambient Temperature (+5°C to +45°C)[1]	±0.8°C max
Compensation Error	
vs. Sensor Temperature (+5°C to +45°C)[2]	±0.4°C max (±0.15°C typ)
vs. Compensator Module Temperature (0 to +70°C)[3]	±0.02°C/°C max (0.01°C/°C typ)
Cold Junction Temperature Sensing Element	AD590 or 2N2222
INPUT SPECIFICATIONS	
Voltage Signal Range	±10V
Input Impedance	100kΩ
Signal Gain[4]	+1V/V
vs. Temperature	±10ppm/°C
Input Offset Voltage	±1mV max
vs. Temperature	±15μV/°C max
OUTPUT SPECIFICATIONS[5]	
Output Voltage	±10V @±5mA
Output Impedance	0.1Ω
DYNAMIC RESPONSE	
Selection Settling Time	0.5ms
Signal Settling Time, to ±0.01%	50μs
DIGITAL INPUTS	
Select Inputs A & B	TTL, CMOS Compatible
POWER SUPPLY	
Analog, Rated Performance	±15V dc ±10% @ ±5mA
Operating	(±12V to ±18V dc)
Digital, V_{DD}	+5V to +15V dc @ 2mA max
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
CASE SIZE	1.5" X 2" X 0.4"

[1] Total compensation error composed of errors of temperature sensor and module at the same ambient temperature.
[2] Compensation error contributed by ambient temperature changes at temperature sensor.
[3] Compensation error contributed by ambient temperature changes at the module.
[4] Signal gain of 2 is also available by jumper selection.
[5] Protected for shorts to ground or either supply voltage.

Specifications subject to change without notice.

T Type	Max Gain for Sensor Temp to +45°C	to +70°C
J	1000	650
K, T	1300	820
E	870	550
R, S	9000	5500
B	Any	Any

Table I. Maximum Gain vs. Sensor Temperature and Thermocouple Type

T Type	RX1	RX2
E	412kΩ	1.43kΩ
R, S	412kΩ	121Ω

Table II. Resistor for Compensating Types E, R and S

Type Sel. Logic B	A	Compensation
0	0	J
0	1	K
1	0	T
1	1	X

Table III. Digital Selection of Compensation Type

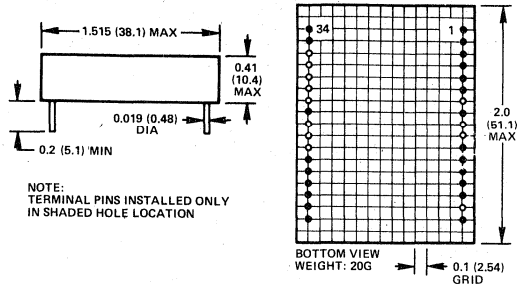
Sensor Temp (°C)	V_{CAL} (mV) 2N2222	AD590
5	616.5	634.5
10	604.9	645.9
15	593.3	657.3
20	581.6	668.7
25	570.0	680.1
30	558.4	691.5
35	546.8	702.9
40	535.1	714.3
45	523.5	725.7

Values may be interpolated

Table IV. Calibration Voltage vs. Sensor Temperature

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	SIGNAL INPUT	18	ANALOG COMMON
2	SENSOR SELECT	19	T TYPE SELECT
3	SENSOR SELECT	20	T TYPE SELECT
4	SENSOR INPUT	21	$+V_{DD}$
5	SENSOR SELECT	22	DIGITAL COMMON
6	SENSOR SELECT	23	$+V_S$
7		24	
8	V_{REF}	25	
9		26	
10		27	$-V_S$
11	"X" COMPENSATION	28	
12	TYPE J	29	
13	TYPE K (GAIN SELECT)	30	
14	TYPE T (GAIN SELECT)	31	
15	TYPE "X" (GAIN SELECT)	32	
16		33	OUTPUT
17	ANALOG COMMON	34	SCALE

MATING SOCKET: AC1217

A buffer amplifier is provided at the output of the 2B56 to preserve accuracy when driving heavy loads. The gain from V_{IN} to V_{OUT} will be +1 when SCALE is connected to V_{OUT} (see Figure 1). Input and output signal swings of up to ±10V can be accommodated with this connection. When the SCALE pin is left open, the gain from V_{IN} to V_{OUT} is +2. This is useful when interfacing a thermocouple amplifier with a ±5V output swing (such as the 2B54) to an A to D converter with a ±10V input range.

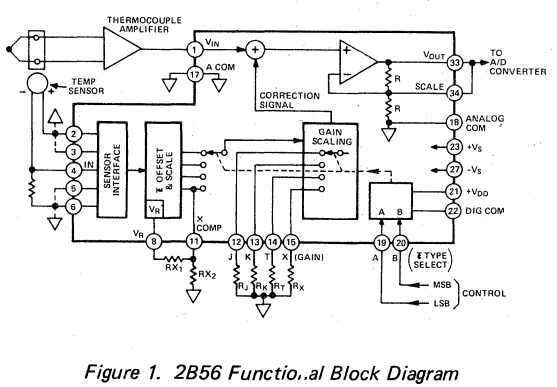


Figure 1. 2B56 Functional Block Diagram

It should be noted that the 2B56 is designed for use with noninverting thermocouple amplifiers. Thus a positive voltage change at the input of the 2B56 must indicate increasing temperature.

OPERATING INSTRUCTIONS

Temperature Sensors: The temperature sensor used with the 2B56 can be either the Analog Devices AD590 temperature transducer or the popular 2N2222 transistor. Either sensor type can be used without loss of accuracy, but each has advantages in different applications. The 2N2222 (the metal can version must be used) is widely available at very low cost. However, an adjustment must be made whenever the sensor is replaced. The AD590 is available in several precalibrated accuracy grades, but at somewhat higher cost.

Connections are shown for both sensor types in Figure 2. Resistor R_{CAL} is the calibration adjustment point. It is used only to adjust for unit-to-unit variations in the sensors. All other adjustments have been made internal to the 2B56.

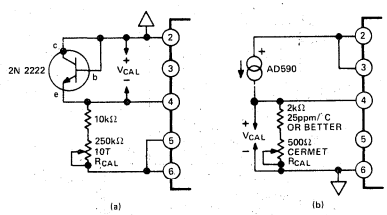


Figure 2. Sensor Connections and Calibration

With either sensor type, proper placement of the sensor is important. Close thermal contact of the sensor and the thermocouple termination point (reference junction) is necessary, particularly when nearby heat sources are present, since these could cause the sensor temperature to differ from the reference junction temperature. In multichannel applications, care should be taken to keep all input terminals at the same temperature to avoid channel-to-channel errors. The sensor may be placed at any distance from the 2B56. When the sensor leads are more than ten feet long, or where strong noise sources are present, shielded cable should be used with the 2N2222 sensor. The AD590 will operate properly with twisted-pair leads at distances up to a few hundred feet.

Gain Selection: Since the 2B56 performs cold junction compensation at the output of the user's thermocouple amplifier, it must take the gain of that amplifier into account. For this purpose, four gain-programming pins are provided: one each for the J, K, and T compensations and one for the X (user-selected) compensation. Thus the user's thermocouple amplifiers can have different gains for each thermocouple type in use, and the 2B56 gain will be selected automatically when the thermocouple type is selected at the digital TYPE SELECT inputs. Gain-programming resistors are connected as shown in Figure 1. The value of each resistor is $R = 10k\Omega/(G-1)$ where G is the gain of the user's thermocouple amplifier from the thermocouple terminals to the input of the 2B56. As an example, if the thermocouple amplifiers in use have a gain of 110 for type J, 90 for type K, and 220 for type T, then R_J = 91.7Ω, R_K = 112Ω, and R_T = 45.7Ω. Gain resistor pins for unused thermocouple types must be grounded. The resistors used to set gain should have a tolerance of 1% or better. A 1% error in setting gain will result in a 0.01°C/°C slope error.

The gain of the thermocouple amplifier will normally be determined by the thermocouple type, temperature measurement range, and A to D converter input range, but there are some practical limits imposed by the 2B56. The minimum allowable gain for proper operation is 40. The maximum gain which can be used is limited by the dynamic range of the compensation circuits in the 2B56, and is a function of thermocouple type and the temperature range (at the sensor) over which compensation is to be effective. Table I lists the maximum gain for each thermocouple type both for the specified +5°C to +45°C sensor temperature range and for a wider (reduced accuracy) 0 to +70°C range.

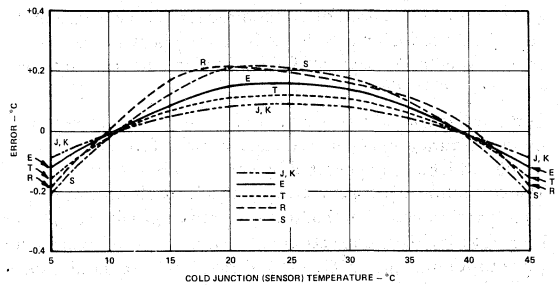


Figure 3. Error Due to Thermocouple Nonlinearity

Compensation of Other Thermocouple Types: Compensation for type J, K, and T thermocouples is built into the 2B56. A fourth compensation can be added by installing two resistors (R_{X1} and R_{X2}) as shown in Figure 1. Table II gives the values needed for proper compensation of type E, R, and S thermocouples. Type B thermocouples are a special case, in that they have almost no output in the +5°C to +45°C range, and therefore, do not need cold junction compensation at all. To accommodate a type B thermocouple, select No Compensation (described in the next section). Errors due to cold junction temperature will be less than ±1°C for any measurement temperature above 260°C. In the measurement range beyond 1000°C (where type B thermocouples are normally used) the error will be less than ±0.3°C.

No Compensation Operation: In some instances it may be desirable to disable the compensation function of the 2B56, so that it functions as a straight-through amplifier with a gain of one (or two, if the output scaling feature is used). This might be done, for example, in a multichannel system with a mixture of thermocouples and strain gage signals or other sources requiring no compensation. It is also necessary when using the type B thermocouple, as described above. The X compensation can be programmed to provide no compensation by grounding pin 11 (X COMP), Figure 1. A 200Ω resistor should be used for R_X (at any gain). Selecting X compensation with this connection will give an uncompensated output.

Digital Inputs: The TYPE SELECT inputs are compatible with TTL or CMOS logic, or may be used with jumpers or switches. Table III shows the truth table for these inputs. Each input has an internal 22kΩ pullup resistor to V_{DD} and drives a single CMOS gate. For use with TTL signals, V_{DD} should be connected to the +5V logic supply. When CMOS logic is used, connect V_{DD} to the CMOS logic power supply (which must be in the +5V to +15V range). If jumpers or switches are used, connect V_{DD} to the +15V analog power supply. Grounding a SELECT input will give a logic "0"; an open input will be at logic "1" due to the action of the internal pullups.

A separate pin is provided for logic ground to minimize ground loop problems. However, for proper operation logic ground at the module must be within ±0.3V of analog common. Failure to observe this restriction may result in damage to the module.

Calibration: Only one adjustment is necessary to get proper operation of the 2B56. This is shown in Figure 2 for both sensor types. R_{CAL} is adjusted to obtain the correct voltage at V_{CAL} for the appropriate sensor type and temperature, as listed in Table IV. Use a high-impedance voltmeter to measure V_{CAL} to prevent loading errors.

The tolerance to which the calibration adjustment must be made depends on the requirements of the application. For either sensor type, and for all thermocouple types, each millivolt of calibration error will result in a temperature offset error at the 2B56 output of 0.44°C, accompanied by a slope error of 0.0015°C/°C.

Curvature Error: The voltage output of thermocouples is a nonlinear function of temperature, so the reference junction output which is compensated by the 2B56 is also nonlinear. The correction signal generated by the 2B56, however, is approximately linear. The 2B56 is adjusted internally to give the best fit of its linear correction to the nonlinear reference junction output over the +5°C to +45°C range. The remaining error, which is included in the specifications given on page 2, is shown for each thermocouple type in Figure 3. Note that as a result of thermocouple nonlinearity the error at +25°C will not be zero after calibration is done. The error for a particular thermocouple type could be adjusted to zero at +25°C by appropriate adjustment of the thermocouple amplifier offset, but the improvement will be at the expense of increased errors over the +5°C to +45°C range.

APPLICATIONS

The application of the 2B56 to a single-channel system is shown in Figure 1. Because the 2B56 compensates at the output of the thermocouple amplifier, it is also very attractive for use in multiplexed multichannel systems. Three typical applications are shown in Figure 4. The amplifier-per-channel structure shown in Figure 4a is one example of a system which could have a different gain for each thermocouple type in use, with channels preassigned or switchable for thermocouple type. The model 2B30 may be used as an amplifier for applications not requiring isolation.

In systems of this type, it is important that the ON resistance of the multiplex switches be less than 100 ohms, since larger values can create slope errors in the 2B56. If switches with higher resistance are used, a unity-gain buffer should be placed between the multiplexer and the 2B56. An AD741 or AD301-type amplifier will suffice unless the system is very fast.

Figure 4b shows an input-multiplexed system. Different gains for different channels in this type of system are sometimes provided by software control of the amplifier gain. The 2B56 can also accommodate this situation, since it can accept a different gain for each thermocouple type.

Figure 4c shows a somewhat different application of the 2B56. Here the signal input is grounded, so that the output is simply the correction signal rather than a corrected version of the input. In this case the actual summation is done elsewhere, usually in the processor following the A to D converter. The advantage of such a structure is that it allows somewhat simpler calibration of the individual channels because the compensator can be bypassed.

There is no electrical limit to the number of channels that can be served by a single 2B56 in these applications or the

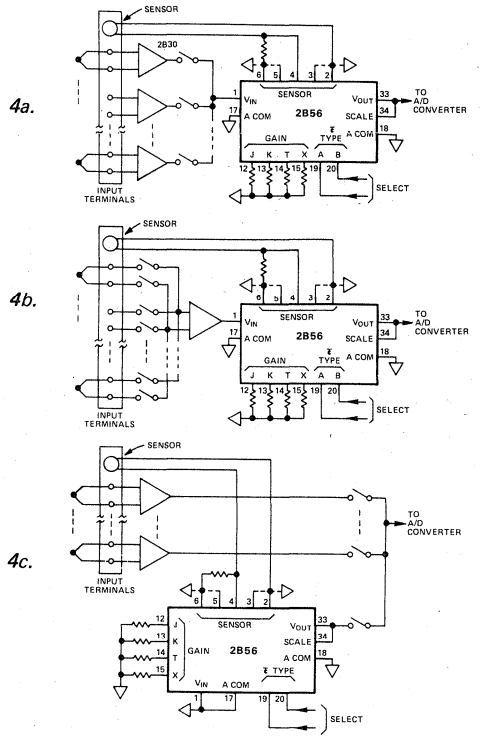


Figure 4. Model 2B56 in Various Multichannel Applications

many others that are possible. There is, however, a thermal limit in that a single temperature sensor must accurately monitor the temperature of a number of sets of input terminals. The actual channel limit will thus be determined by the allowable error and the degree to which all the inputs can be held at the same temperature.

Figure 5 shows the application of the 2B56 to the output of the 2B54 Four-Channel Isolator. More than one 2B54 can be served by the same 2B56 by using the built-in output switches of the 2B54 to connect several isolators to one output line. Note that the values of the gain-setting resistors for the 2B54 and 2B56 are the same, since both have the same gain formula. This permits very simple reconfiguration when the system must be tailored for new applications.

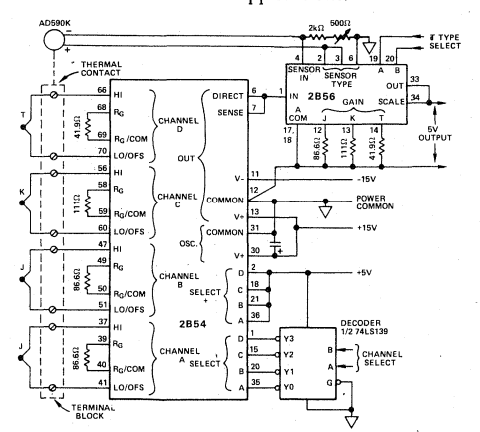


Figure 5. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

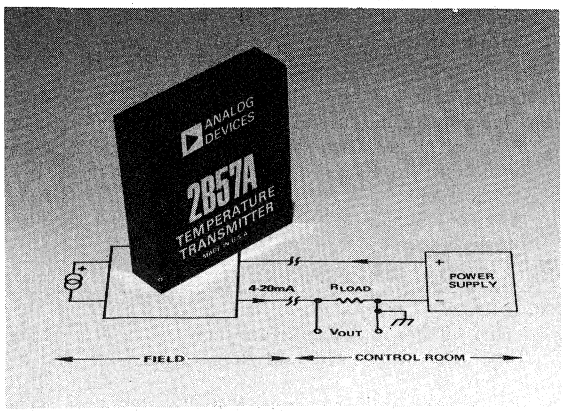
Low Cost, Two-Wire Temperature Transmitter

MODEL 2B57

PRELIMINARY TECHNICAL DATA

FEATURES
- Low Cost
- Compatible with Standard 4-20mA Loops
- Low Span Drift: ±0.005%/°C max
- Low Nonlinearity: ±0.05% max
- RFI Immunity
- Small Size: 1.5″ × 1.5″ × 0.4″

APPLICATIONS
- Temperature Monitoring and Control
- Remote Temperature Sensing
- Process Control Systems
- Energy Management Systems



GENERAL DESCRIPTION

The model 2B57 is a low cost, two-wire temperature transmitter designed to interface with Analog Devices' AD590 temperature transducer and produce a standard 4 to 20mA output current proportional to the measured temperature. The 2B57 features a low span drift of ±0.005%/°C max, a high linearity (±0.05% max) and high noise immunity to assure measurement accuracy in harsh industrial environments.

The transmitter accommodates the AD590 temperature measurement range of −55°C to +150°C. Both zero and span adjustments are provided to trim the range for input measurement spans between 20°C and 205°C. The transmitter output of 4 to 20mA and a wide range of power supply voltages make the 2B57 compatible with standard two-wire control loops.

The basic package is a small (1.5″ × 1.5″ × 0.4″), rugged, epoxy encapsulated module. For applications requiring protective housing, the 2B57 is available in a versatile metal case.

APPLICATIONS

The 2B57 has been specifically designed to provide low cost, accurate and reliable temperature measurement in any applications below +150°C in which conventional electrical temperature sensors and transmitters are currently employed.

Industrial applications in process control and monitoring systems include chemical, petroleum, food processing, power generation and a wide variety of other industries.

In multipoint energy management applications, low cost and small size combine to make the AD590 and 2B57 ideal for mounting in standard utility or thermostat boxes for remote temperature sensing.

DESIGN FEATURES AND USER BENEFITS

RFI Noise Immunity: The transmitter incorporates RFI filtering circuitry to assure protection against radio frequency interference.

Low Cost: The low cost of the 2B57 transmitter and two-wire operation reduce total system installation cost.

Linear Output: The transmitter output is linear with temperature, thus eliminating the need for linearizing circuitry.

Standard Loop Compatibility: The two-wire output structure conforms to the Instrument Society of America Standard ISA-S50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments."

SPECIFICATIONS (typical @ +25°C and V_S = +24V dc, unless otherwise noted)

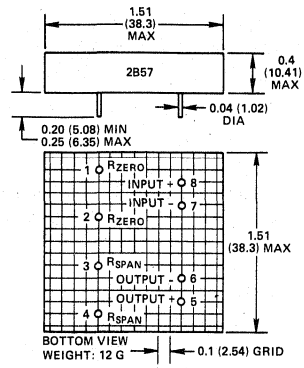
MODEL	2B57A
INPUT SPECIFICATIONS	
Sensor Type[1]	AD590
Maximum Temperature Measurement Range	-55°C to +150°C
Minimum Input Span (for a 4-20mA Output)	20°C
Zero Adjustment Range	-55°C to +60°C
Input Protection[2]	+50V dc
Open Input Detection	Upscale
OUTPUT SPECIFICATIONS	
Output Span	4 to 20mA
Minimum Output Current	2.5mA
Maximum Output Current	26mA
Load Resistance Range	
Equation	$R_{LMAX} = (V_{SUPPLY} - 12V)/20mA$
@ +24V Supply	0 to 600Ω max
Output Protection[2]	+50V dc
NONLINEARITY (% of Span)	±0.02% typ (±0.05% max)
ACCURACY	
Warm-Up Time to Rated Performance	1 min
Total Output Error, without External Trims[3]	
Zero	±0.2% typ (±0.5% max)
vs. Ambient Temperature (-30°C to +85°C)	±0.005%/°C typ (±0.01%/°C max)
Span	±0.2% typ (±0.5% max)
vs. Ambient Temperature (-30°C to +85°C)	±0.001%/°C typ (±0.005%/°C max)
RESPONSE TIME, to 90% of Span	0.15 sec
POWER SUPPLY	
Voltage, Rated Performance	+24V dc
Voltage, Operating	+12V to +50V dc
Supply Change Effect, % of Span	
on Zero	±0.005%/V
on Span	±0.001%/V
ENVIRONMENTAL	
Temperature Range, Rated Performance	-30°C to +85°C
Storage Temperature Range	-55°C to +100°C
Relative Humidity, to +40°C	0 to 90%
RFI Effect (5W @ 420MHz @ 3 ft)	
Error, % of Span	±0.5% max
CASE SIZE	1.5" X 1.5" X 0.4"

NOTES
[1] AD590 produces an output current proportional to absolute temperature (1μA/°K).
[2] Protected for any combination of input and output pins.
[3] Accuracy is specified as a percent of output span (16mA) for an input range of -55°C to +150°C. Accuracy spec includes combined effects of transmitter repeatability, hysteresis, and linearity. Does not include sensor error.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

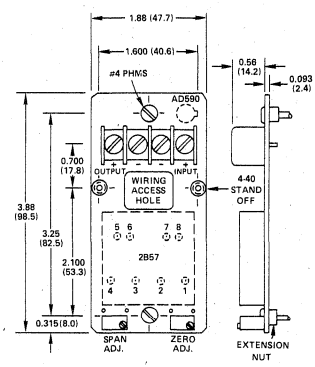
Dimensions shown in inches and (mm).



MOUNTING CARD AC1583

AC1583 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



The AC1583 mounting card is available to assist in applying the 2B57. The AC1583 is suitable for mounting in a standard 2" X 4" thermostat box. It includes screw terminals for field wiring, provisions for plugging in the 2B57 and AD590, and span and zero adjustment pots.

FUNCTIONAL DESCRIPTION

The 2B57 transmitter converts the output of an AD590 temperature transducer to a current output within a span of 4 to 20mA. The transmitter includes input protection and filtering circuitry, an amplifier, voltage regulator, precision voltage reference and an output current generator.

A precision voltage reference, resistor network, and span and zero adjusts are used in conjunction with a low current drain amplifier to scale output signal of the AD590. The amplifier drives a current generator which controls output current (Figure 1).

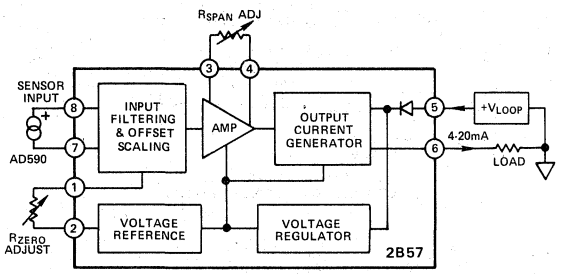


Figure 1. Model 2B57 Functional Block Diagram

Input power and output signal are transmitted over the same two leads. The load resistance is connected in series with a dc power supply, and the current drawn from the supply is the 4 to 20mA output signal. The maximum series load resistance depends on the supply voltage and is given by $R_{LMAX} = (+V_S - 12V)/20mA$. A wide range of power supply voltages may be used (see Figure 2).

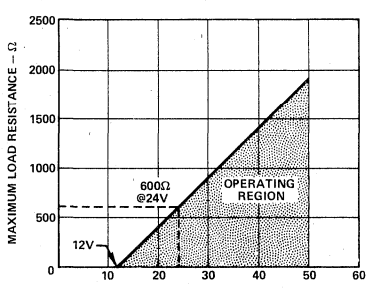


Figure 2. Maximum Load Resistance vs. Power Supply

THE SENSOR

The AD590 is a calibrated two terminal temperature sensor producing a current in microamperes (1μA/°K) that is linearly proportional to absolute temperature for temperatures from -55°C to +150°C. The AD590 sensor is available in a hermetically sealed TO-52 transistor package, a miniature flat-pack, chip form and stainless steel probes (AC2626). The sensor construction assures reliable isolation from ground.

The AD590 is available in several accuracy grades, as shown in Table 1. The grade selection will depend on whether the device is used uncalibrated or with calibration at a single value. For greater accuracy (in any grade), the device may be calibrated at two points.

TABLE 1. AD590 ACCURACY SPECIFICATIONS (MAX ERROR)

Conditions	Max Error (±°C)				
Grade	I	J	K	L	M
Error at 25°C, as delivered	10.0	5.0	2.5	1.0	0.5
Errors over the -55°C to +150°C range:					
Without external calibration	20.0	10.0	5.5	3.0	1.7
With error nulled at 25°C only	5.8	3.0	2.0	1.6	1.0
Nonlinearity	3.0	1.5	0.8	0.4	0.3

OPERATING INSTRUCTIONS

Model 2B57 is factory calibrated to ±0.5% accuracy for a maximum sensor measurement range of -55°C to +150°C (205°C span) with R_{SPAN} and R_{ZERO} resistor values as shown in Figure 3. For this input range 4mA output corresponds to an AD590 temperature of -55°C and 20mA to +150°C. The span and zero adjustments can be used to accommodate other input ranges.

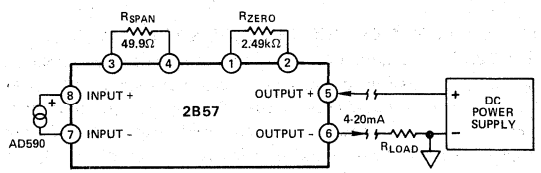


Figure 3. Model 2B57 Basic Application

Span Adjustment: The value of the span setting resistor R_{SPAN} is determined by:

$$R_{SPAN}\ (\Omega) = \left(\frac{1.2V}{10^{-6}\ A \times SPAN}\right) - 5810\Omega$$

where SPAN is a desired measurement span in °C. For example, for a measurement span of 100°C R_{SPAN} = $\left(\frac{1.2V}{10^{-6}\ A \times 100}\right) - 5810\Omega = 6.19k\Omega$. If a span accuracy of ±0.5% if desired, the value of the R_{SPAN} resistor should be accurate to ±0.1%.

Zero Adjustment: Zero adjustment must be performed after installation of the R_{SPAN} resistor. To select R_{ZERO} an AD590 or a calibrated current source may be used as an input to the 2B57. If an AD590 is used, it must be maintained at the desired reference temperature. A resistance decade box is inserted between pins 1 and 2 of the 2B57. The decade box is adjusted to produce an output corresponding to the selected reference temperature. For example, for a sensor measurement range of 0 to 100°C and an AD590 at 0°C, the R_{ZERO} is adjusted for an output current of 4mA. If a current source is used, its output must equal the AD590 output at the selected reference temperature. For example, at 0°C the current source output must equal 273.2μA.

Sensor Calibration Trim: The sensor calibration error is the major contributor to maximum total error in all AD590 grades. To trim this error the temperature of the AD590 is measured by a reference temperature sensor and R_{ZERO} is trimmed to the calculated value of the 2B57 output current at that temperature. A reference temperature at the midpoint in the span should be selected.

For best measurement accuracy over temperature, R_{ZERO} and R_{SPAN} should be trimmed with the AD590 at two known temperatures. For example, with the R_{SPAN} selected for a 100°C span and with the AD590 at 0°C R_{ZERO} is adjusted for a 4mA output. R_{SPAN} is then trimmed for a 20mA output with the sensor at 100°C. Figure 4 illustrates a typical two-trim system accuracy.

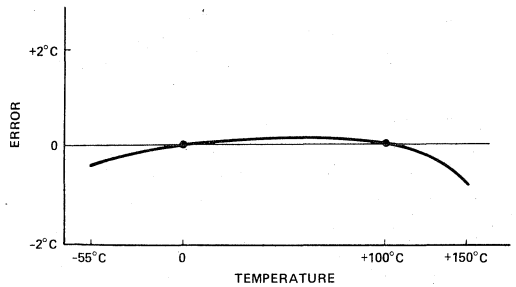


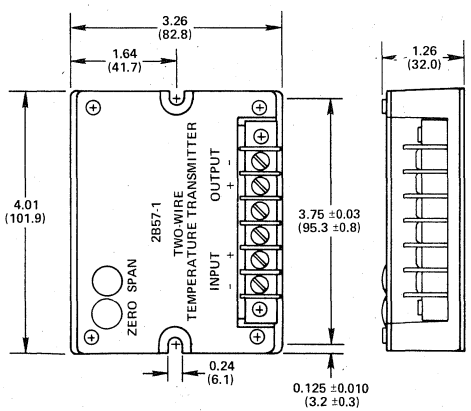
Figure 4. Typical Two-Trim Accuracy (AD590 and 2B57)

OPTIONAL PACKAGING CONFIGURATION (2B57A-1)

The 2B57 is available mounted in an aluminum case including screw terminals for connecting an external sensor and power. This versatile housing may be surface mounted in racks, cabinets, NEMA enclosures, etc., or snapped onto standard relay tracks. The 2B57 in a metal housing is calibrated for a -55°C to +150°C measurement range and may be ordered by specifying model 2B57A-1.

TRANSMITTER HOUSING OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



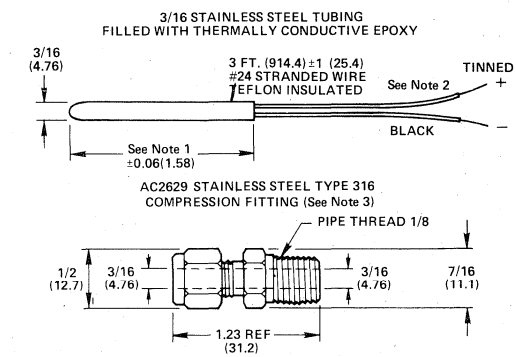
AC2626 PROBE (AD590 PACKAGING OPTION)

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the AD590F, the probe is available in linearity grades of 0.3°C, 0.4°C, 0.8°C or 1.5°C and is compatible with the 2B57 transmitter. The mechanical outline of the AC2626 is shown below.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring applications.

AC2626 MECHANICAL OUTLINE

Dimensions shown in inches and (mm).



NOTE 1 Probes are available in 4-inch or 6-inch lengths. Other lengths are available; consult factory for price and delivery.

NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue; M, green.

NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

Digital-to-Analog Converters

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●New product since the 1979 *Data Acquisition Products Catalog Supplement.*

Selection Guide
Digital-to-Analog Converters

The converter families catalogued in this section are divided into seven overlapping categories:

1. General Purpose, Low Cost
2. High Performance (Speed and Accuracy)
3. High Speed
4. High Resolution
5. Low Power and Multiplying
6. Digitally Buffered (Data-Bus Compatible)
7. Special-Purpose

The specifications and features are key for each device. Complete and detailed descriptions, specifications, and application information can be found on the data sheets. General information and definitions of important specifications can be found in the pages that follow.

In general, the devices catalogued here are available in various performance and temperature grades, and packages, as specified on the data sheets. All specifications are typical at rated supply voltage and $T_A = 25°C$, unless noted otherwise. Devices are listed in order of resolution.

1. GENERAL PURPOSE, LOW COST

Model	Resolution (Bits)	Features	Page
AD558 # ●	8	IC, complete, including μP-compatible digital buffering, on-chip voltage reference, and op amp (voltage output); Requires single supply, +5V to +15V, 75mW	9-13
AD7523 #	8	CMOS IC, 4-quadrant multiplying, low cost	9-75
AD1408 #	8	IC, replaces standard 1408/1508 directly	9-51
AD559 #	8	IC, high-performance alternative to 1408/1508	*
AD7524 #	8	CMOS IC, 4-quadrant multiplying with μP interface	9-79
AD DAC-08 #	8	IC, direct replacement for industry-standard DAC-08 85ns settling time, ±1/4LSB guaranteed linearity over temperature (A, H)	9-123
AD7533 #	10	CMOS IC, 4-quadrant multiplying, low cost	9-95
AD7530 #	10	CMOS IC, 4-quadrant multiplying	9-91
AD561 #	10	IC, internal reference, 250ns current settling	9-21
AD7531 #	12	CMOS IC, 4-quadrant multiplying, low cost	9-91
AD DAC80	12	IC, 3-chip improved replacement for standard DAC80, I and V versions	9-129
AD DAC85	12	IC, improved replacement for standard DAC85 over −55°C to +125°C	9-137
AD DAC87	12	IC, improved replacement for standard DAC87, monotonic over −55°C to +125°C temperature range	9-145
AD370 ●	12	Hybric IC, superior replacement for standard 370; ±10V output, low power — 150mW	9-9
AD371 ●	12	Hybrid IC, superior replacement for standard 371; 0 to +10V output	9-9

2. HIGH PERFORMANCE (SPEED AND ACCURACY)

Model	Resolution (Bits)	Features	Page
HDS-1250	12	24-pin DIP, 30ns current settling to 0.025%	9-171
MDS-1240	12	Module, TTL/ECL input, 40ns current settling to 0.025%	9-187
MDSL-1250	12	Module, 50ns current settling to 0.025%	9-187
AD565	12	IC, fast monolithic, current-output, internal reference, replacement for AD563, current settling time 200ns	9-35
AD566	12	IC, fast monolithic, current-output, multiplying; replacement for AD562, current settling time 200ns	9-43
MDH-1202	12	Module, 200ns voltage settling to 0.025%	9-187
HDH-1205	12	24-pin DIP, 500ns voltage settling to 0.025%	9-171
AD7541 #	12	CMOS IC, 4-quadrant multiplying, pretrimmed	9-101
AD563	12	High-performance, current output, internal reference	9-29
AD562	12	High-performance, current-output, multiplying capability	9-29

3. HIGH SPEED

Model	Resolution (Bits)	Features	Page
AD DAC-08	8	IC, 85ns current settling	9-123
AD561 #	10	IC, 250ns current settling, internal reference	9-21
HDS-E ●	10, 8	Hybrid ICs, ultra-high-speed ECL; Voltage settling 15/10ns to 0.1%/0.2%	9-177
HDS	12, 10, 8	24-pin DIP, 30/25/20ns current settling to 0.025%/0.1%/0.4%	9-171
DAC1108/1106	12, 10, 8	Module, 150/50/25ns current settling to 0.01%/0.05%/0.2%	9-149
MDSL	12, 10, 8	Module, 50/25/25ns current settling to 0.025%/0.1%/0.1%	9-187

MDS	12, 10, 8	Module, TTL/ECL input, 40/20/15ns current settling to 0.025%/0.1%/0.4%	9-187
MDD	10, 8	Module, deglitched, voltage output, 20MHz word rate	9-181
MDH	12, 10, 8	Module, 200/100/70ns voltage settling to 0.025%/0.1%/0.4%	9-187
HDH	12, 10, 8	24-pin DIP, 500/300/200ns voltage settling to 0.025%/0.1%/0.4%	9-171
AD565	12	IC, monolithic replacement for AD563, current settling time 200ns	9-35
AD566	12	IC, monolithic replacement for AD562, current settling time 200ns	9-43

4. HIGH RESOLUTION

Model	Resolution (Bits)	Features	Page
DAC1136†	16	Module, voltage or current output	9-153
DAC1137†	18 (16)	Module, voltage or current output	9-153
DAC1138†	18 (18)	Module, voltage or current output	9-153

5. LOW POWER AND MULTIPLYING §

Model	Resolution (Bits)	Features	Page
AD7523#	8	CMOS IC, 4-quadrant multiplying, low cost	9-75
AD7524#	8	CMOS IC, 4-quadrant multiplying, μP-compatible	9-79
AD558#●	8	IC, complete, including μP-compatible digital buffering, on-chip voltage reference, and op amp (voltage output); requires single supply +5V to +15V, 75mW	9-13
AD7533#	10	CMOS IC, 4-quadrant multiplying, low cost	9-95
AD7530#	10	CMOS IC, 4-quadrant multiplying	9-91
AD7520#	10	CMOS IC, 4-quadrant multiplying	9-61
AD7522#	10	CMOS IC, 4-quadrant multiplying, double-buffered serial-parallel, with μP interface	9-69
MDMS	11, 10, 8	Module, multiplying, 100ns current settling to ±0.1%	9-185
AD7525#	3 1/2	CMOS IC, multiplying (2-quadrant analog) "digital pot"	9-85
AD7542●	12	CMOS IC, 4-quadrant multiplying, 4- or 8-bit μP-compatible, double buffered, 3 4-bit nybbles	9-107
AD7543●	12	CMOS IC, 4-quadrant multiplying, double-buffered, serial loading	9-115
AD370/371	12	Hybrid IC, superior replacements for standard 370/371s, low power – 150mW	9-9
AD7531#	12	CMOS IC, 4-quadrant multiplying, low cost	9-91
AD7541#	12	CMOS IC, 4-quadrant multiplying	9-101
AD7521#	12	CMOS IC, 4-quadrant multiplying	9-61

6. DIGITALLY BUFFERED (DATA-BUS COMPATIBLE)

Model	Resolution (Bits)	Features	Page
AD558#●	8	IC, complete, including μP-compatible digital buffering, on-chip voltage reference, and op amp (voltage output); requires single supply, +5V to +15V, 75mW	9-13
AD7524#	8	CMOS IC, 4-quadrant multiplying, with μP interface	9-79
DAC1420●	8	Module, 4-to-20mA output, loop-powered, buffered digital input	1-161
MDD	10, 8	Module, deglitched, voltage output, 20MHz word rate	9-181
AD7522	10	CMOS IC, 4-quadrant multiplying, double-buffered	9-69
DAC1422	10	Module, 4-to-20mA output, loop-powered, buffered digital input	9-161
DAC1423●	10	Module, ISO-DAC™, 1500V dc isolation, 4-to-20mA output, loop-powered, buffered digital input	9-165
AD7542●	12	CMOS IC, 4-quadrant multiplying, 4- or 8-bit-μP-compatible, double-buffered 3 4-bit nybbles	9-107
AD7543●	12	CMOS IC, 4-quadrant multiplying, double buffered, serial loading	9-115

7. SPECIAL-PURPOSE

Model	Resolution (Bits)	Features	Page
DAC1420●	8	Module, 4-to-20mA output, loop-powered, buffered digital input	9-161
DAC1422	10	Module, 4-to-20mA output, loop-powered, buffered digital input	9-161
DAC1423●	10	Module, ISO-DAC™, 1500V dc isolation, 4-to-20mA output, loop-powered, buffered digital input	9-165
AD7525	3 1/2 BCD	CMOS IC, multiplying (2-quadrant analog), "digital pot", digitally controlled attenuator, can be manually operated with thumbwheel switches	9-85
AD7110●	14+	CMOS IC, digitally controlled audio attenuator with logarithmic taper, 59 1.5dB steps (= 88.5dB or 14.7 bits of gain range) and full muting; Includes swtiches for loudness compensation	9-55

†Card mounted assembly with deglitcher (Deglitcher IV) and high-performance output amplifier available. See data sheet.
§ All CMOS IC's have low power dissipation.
≠Monolithic chips available with guaranteed performance for precision hybrids; information available upon request.
All but AD558 can be found in the 1979 Chip Catalog, available upon request.
●New product since the 1979 *Data Acquisition Products Catalog Supplement.*
*Data sheet available upon request.

Orientation
Digital-to-Analog Converters

FACTORS IN CHOOSING A D/A CONVERTER

In the current issue of this catalog, there are listed some 32 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be more than 100 types to choose among. The reason for so many different types is the number of degrees of freedom in selection—technological, functional, and performance. Complete information on converters may be found in the 250-page book, ANALOG-DIGITAL CONVERSION NOTES, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood MA 02062.

TECHNOLOGICAL FACTORS

The technologies represented here include modules (cards and potted circuits) and integrated circuits—monolithic and hybrid. Modules historically have provided the extremes of performance and arbitrary levels of functional completeness (e.g., the 18-bit DAC1138, the 10-bit 20MHz-word-rate deglitched MDD-1020, and the isolated 10-bit DAC1423 loop DAC), although ICs are catching up rapidly. ICs are small and high in performance per dollar. IC technologies now make possible complete monolithic 12-bit current-output self-referenced DACs (AD565), complete monolithic 8-bit μP-compatible single-supply DACs including voltage reference, output amplifier and digital buffer on-chip (AD558), and wide-dynamic-range CMOS digital audio attenuators (AD7110: 88.5dB in 1.5dB steps). When combined with hybrid technologies, high-performance low-cost voltage-output (AD DAC85) and ultra-fast (10-bit 15ns HDS-E) DACs become available.

The three most-important IC technologies in current use at Analog Devices are thin-film-on-CMOS, thin-film on bipolar, and hybrid. *Hybrid* provides the most-complete high-performance devices. *Thin-film-on-bipolar* provides stable references, high-performance current switches, compatible I^2L logic, and laser-wafer-trimmed resistance networks; an outstanding example is the μP-compatible AD558, mentioned above. *Thin-film-on-CMOS* uses voltage switches in a current-steering mode for full four-quadrant multiplying operation. In addition, the inherent high-density logic-capability and low dissipation of CMOS make possible such devices as the 10-bit AD7542, a microprocessor-compatible double-buffered DAC that can also be used as a digital gain-control with very low analog feedthrough and high linearity for bipolar analog signals.

FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches, and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain output-conditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer-registers (single- or dual-rank), configuration conditioning, and even high-voltage isolation.

Basic DAC

This form, which supplies a current, and consequently a small voltage across its internal impedance or an external low-impedance load, is used principally for high speed, for example, the 10ns HDS-0810E. Basic current-output DACs, such as AD566, are inherently fast, but additional elements (such as an output op amp), furnished by the user to meet overall system specs, slow down the conversion. Some popular CMOS IC devices, such as the AD7523 and the AD7533, are quite simple (and correspondingly low in cost), but they usually require a buffering op amp.

While the basic DAC function is almost always linear, there are exceptions. For example, the AD7110 audio attenuator, which has linear two-quadrant analog response, has a digitally controlled exponential gain function, i.e., 1.5dB per bit; thus, its gain at the input code, 001000 (binary 8), is -12dB (8 X 1.5), and the analog output swing for 10V p-p input is 2.512V p-p (10 exp (10) (-12/20)).

Output Conditioning

The analog quantity that is the "output" of a DAC, representing the input digital data, may be a "gain" (multiplying DAC), a current, and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is generally provided on-board in modular and hybrid DACs (and in the monolithic AD558), but there are many ICs and other types that permit the user to choose an external op amp that will meet the particular needs of the application in stability, speed, and cost.

Almost all types of DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network, so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0–5V full-scale or 0–10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset output is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DACs reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In addition to the usual zero-based current and voltage outputs, DACs are available with 4-to-20mA ISA-standard loop-current outputs, both direct-coupled (DAC1420/22) and high-voltage-isolated (DAC1423), with some additional features that are specifically useful in digital control of analog processes.

In order to avoid difficulties, the user must pay especial attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

Reference Input
The reference may be specified as external or internal, fixed or variable, single-polarity or bipolar. If internal, it may be permanently connected (as in the AD561) or optionally connectible (as in the AD565). If the DAC is a 4-quadrant multiplying type, the reference (or "analog input") is external, variable, and bipolar (e.g., AD7533, 7541, etc.) The user should check a converter's specifications to determine whether the full-scale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

Digital Data
There are a number of ways in which converters differ in regard to the input data: First, the *coding* must be appropriate (binary, offset-binary, two's-complement, BCD, arbitrary, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the 2^n distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to 2^n output values in a monotonic progression at any temperature in the operating range, with sufficient accuracy. The *data levels* accepted by the converter must be checked (TTL, ECL, low-voltage CMOS, high-voltage CMOS), as must the input loading imposed by the converter, and the supply conditions under which the converter will respond to the data. Check the data notation (is the MSB Bit 1 or Bit (n-1)?)—misinterpretation can lead to connecting the data bits in backward order.

If *buffer registers* are desired, the converter should have an appropriate buffer configuration (for example, the AD558 has a set of TTL buffers, the AD7542 and AD7543 have two ranks of CMOS buffering). The 12-bit AD7542 is loaded via three 4-bit nybbles, and the AD7543 via a bit-serial input. The AD7522, also double-buffered, will accept either serial or parallel data, and the parallel data can be loaded in two bytes (2 MSBs and 8 LSBs). The data can be clocked in, while the DAC output remains unchanged.

Controls
If the DAC has external digital controls—for example, register strobes— their drive levels, digital sense (true or false), loading, and timing must be considered. The function and use of configuration controls (where present), such as serial/parallel, short-cycle, or chip-select decoding should be understood, and the appropriate ways of disabling them when not needed should be employed.

Power Supplies
Appropriate power supplies should be made available, considering the logic levels and analog output signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. Any recommended external protection circuitry (e.g., Schottky diodes, to ensure that V_{CC} is never more than 0.4V above V_{DD} in the AD7522) should be planned for. In many cases separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between the grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

SPECIFICATIONS AND TERMS
Definitions of the performance specifications, and related information, are provided on the next few pages, in alphabetical order.

Accuracy, Absolute
Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Error is usually commensurate with resolution, i.e., less than $2^{-(n+1)}$, or "½ LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative
Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative-accuracy error of a linear DAC can be interpreted as a measure of nonlinearity (see *Linearity*).

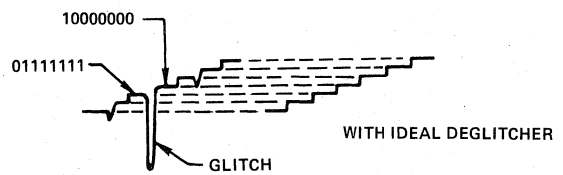
Compliance-Voltage Range
For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

Common-Mode Rejection (CMR)
The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio" e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10^6:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.

Common-Mode Voltage
An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Deglitcher
As the input code to a DAC is increased or decreased by small changes, it passes through what is known as major and minor transitions. The most major transition is at half-scale, when the DAC switches around the MSB, and all switches change state, i.e., 01111111 to 10000000. If, at major transitions, the

switches are faster (or slower) to switch off than on, this means that, for a short time, the D/A will give a zero (or full-scale) output, and then return to the required 1 LSB above the previous reading. Such large transient spikes which differ widely in amplitude and are extremely difficult to filter out, are commonly known as "glitches", hence, a deglitcher is a device which removes these glitches or reduces them to a set of small, uniform pulses. It normally consists of a fast sample-hold circuit, which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time-skew between 0-1 and 1-0 transitions.



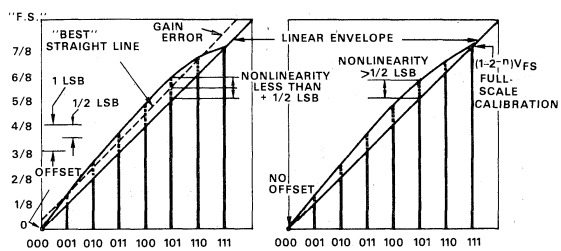
Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e,g,. *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

Four-Quadrant
In a multiplying DAC, "four quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

Gain
The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change, in a fixed-reference converter For fixed-reference converters where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain- and zero-adjustment are discussed under *Zero.*

Least-Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value, or weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost digit is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

Linearity
Linearity error of a converter (also, *integral nonlinearity*, see *Linearity, Differential*), expressed in % or ppm of full-scale range, or (sub)multiples of 1 LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is similar to *relative-accuracy* error.



a. ½LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line".

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Linearity, Differential
Any two adjacent digital codes should result in measured output values that are exactly 1 LSB apart (2^{-n} of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called *differential nonlinearity*, expressed in (sub)multiples of 1 LSB. It is an important specification, because a differential linearity error greater than 1 LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter (see *Differential Linearity* in the A/D converter section for an illustration).

Monotonic
A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a *differential nonlinearity* specification, since differential nonlinearity less than 1 LSB is a sufficient condition for monotonic behavior.

Most-Significant Bit (MSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB, with a weight of 2^{n-1}, or 8 LSBs. Its analog weight, relative to a DAC's full-

scale span, is ½. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

Multiplying DAC
A multiplying DAC differs from a fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see also *four-quadrant*).

Noise, Peak and rms
Internally generated random noise is not a major factor in D/A converters, except at extreme resolutions (e.g., DAC1138) and dynamic ranges (AD7110). Random noise is characterized by rms specifications for a given bandwidth, or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding 7x the rms value is less than 0.1% (see the waveform table in Section 6).

Of much greater importance in DACs is interference in the form of high-amplitude low-energy (hence low-rms) spikes appearing at the DAC's output, caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough, and by glitch-generation. Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing, and deglitching.

Offset
For almost all bipolar converters (e.g., ±10-volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1 MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the ½ scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

Power-Supply Sensitivity
The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (or fractions of 1 LSB) for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed ±½ LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code, usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of ±½ LSB, due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

Resolution
An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span. However, a nonlinear device, such as the AD7110 audio attenuator has a logarithmic gain resolution of 1.5/88.5dB = 1:59dB, which corresponds to a gain increment of 18.9%/step, or 26,600:1.

Settling Time
The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually ±½ LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Slew Rate (or Slewing Rate)
Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few V/μs are common, and moderate in cost. Slew rates greater than about 75 volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

Stability
Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

Staircase
A voltage or current, increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot), generated by applying a pulse train to a counter, and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1 LSB, the count is stopped, and the code corresponding to the count is the digital output.

Switching Time
In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10%-90%), but does not include settling time, e.g. to <½ LSB.

Temperature Coefficients

In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero*.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters the reference source will vary with temperature. For example, the tempco of an AD581L is generally less than 5ppm/°C

b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters (e.g. AD566K/T). High-resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior is achieved if the differential nonlinearity is less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range.

Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source

b) The voltage zero-stability of the output amplifier

c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op-amp (voltage-output DAC).

Zero- and Gain-Adjustment Principles

The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for F.S. $(1 - 2^{-n})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to -F.S. with all bits off, and the gain is set for +F.S. $(1 - 2^{-(n-1)})$ with all bits on. The data sheet instructions should be followed.

ANALOG DEVICES

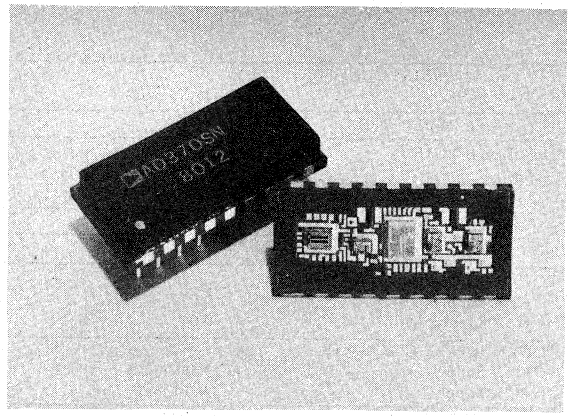
Complete-Low Power 12-Bit D/A Converter

AD370/AD371

PRELIMINARY TECHNICAL DATA

FEATURES

Bipolar Voltage Output: AD370
Unipolar Voltage Output: AD371
Low Power: 150mW max
Linearity: ±1/2LSB, -55°C to +125°C (S Version)
TTL/CMOS Compatible
Compatible with Standard 18-Pin DAC Configurations
Hermetic 18-Pin DIP
Factory Trimmed Gain and Offset
Guaranteed Monotonic Over Specified Temperature Range



PRODUCT DESCRIPTION

The AD370/AD371 is a complete 12-bit digital-to-analog converter fabricated with the most advanced monolithic and hybrid technologies. The design incorporates a low power monolithic CMOS DAC, precision high speed FET-input operational amplifiers and a low dirft reference available in a hermetically sealed package. This innovative design results in significant performance advantages over conventional designs. The integral package-substrate combined with a lower chip count improves reliability over the standard low power hybrids of this type.

The converters come in two versions: AD370 with a bipolar output voltage range (-10V to +10V) and AD371 with a unipolar output voltage range (0 to +10V). Each device is internally laser trimmed for gain and offset to provide adjustment free operation with only ±0.05% absolute error. The FET input operational amplifiers optimize the speed vs. power trade-off by settling to 1/2LSB from a full scale transition in 35μs with maximum total power dissipation of only 150mW. The low power monolithic CMOS DAC employs a current switched silicon-chromium R-2R ladder to ensure that monotonicity is maintained over the full temperature range.

The AD370/AD371 "K" and "S" features ±1/2LSB maximum nonlinearity error. Its rated temperature ranges are 0 to +70°C for the "J" and "K" versions and -55°C to +125°C for the "S" version.

PRODUCT HIGHLIGHTS

1. The AD370/AD371 directly replaces other devices of this type with significant increases in performance.
2. Reduced power consumption requirements (150mW max) result in improved stability and shorter warm-up time.
3. The precision output amplifiers and CMOS DAC have been optimized to settle within 1/2LSB for a full scale transition in 35μs.
4. Reduced chip count and integral package-subsrate improve reliability.
5. System performance upgrading is possible without redesign.
6. Internally laser trimmed—no gain or offset adjustments are required for specified accuracy.
7. The device is packaged in a hermetically-sealed ceramic 18 lead dual-in-line package. Processing to MIL-STD-883 Class B is available.
8. The AD370/AD371 is a second-source for 18-pin 12-bit DAC's of the same configuration.

SPECIFICATIONS (typical at T_A = +25°C, V = ±15 Volts unless otherwise noted)

Model	AD370J	AD370K	AD371J	AD371K	AD370S[1]	AD371S[1]	Units
RANGE	-10 to +10	*	0 to +10	**	*	**	Volts
CODE	OCBI	*	CBI	**	*	**	
LINEARITY ERROR							
+25°C	1	1/2	1	1/2	1/2	1/2	LSB[2] max
T_{min} - T_{max}	1	1/2	1	1/2	1/2	1/2	LSB[2] max
ABSOLUTE ACCURACY							
+25°C	0.05	*	*	*	*	*	% of FSR[3] max
T_{min} - T_{max}	0.2	*	*	*	0.3	0.3	% of FSR[3] max
FULL SCALE SETTLING TIME							
TO 1/2LSB	25(35 max)	*	*	*	*	*	μs
INTERNAL REFERENCE	+10.0	*	*	*	*	*	Volts
DIGITAL INPUTS							
V_{INH}	2.10	*	*	*	*	*	Volts min
V_{INL}	0.8	*	*	*	*	*	Volts max
INPUT LEAKAGE CURRENT	±1.0	*	*	*	*	*	μA
INPUT CAPACITANCE	8	*	*	*	*	*	pF
POWER SUPPLY REJECTION RATIO							
+15V Supply	0.01	*	*	*	*	*	% FSR[3]/% V_S max
-15V Supply	0.01	*	*	*	*	*	% FSR[3]/% V_S max
POWER SUPPLY CURRENTS							
+15V Supply	3.5(5 max)	*	*	*	*	*	mA max
-15V Supply	2.5(4 max)	*	*	*	*	*	mA max
POWER DISSIPATION	105(150 max)	*	*	*	*	*	mW
TEMPERATURE RANGE	0 to +70	*	*	*	-55 to +125	***	°C

NOTES
[1] Also available to MIL-STD-883, Level B.
[2] LSB: Least Significant Bit
[3] FSR: Full Scale Range
*Specifications same as AD370J.
**Specifications same as AD371J.
***Specifications same as AD370S.

Specifications subject to change without notice.

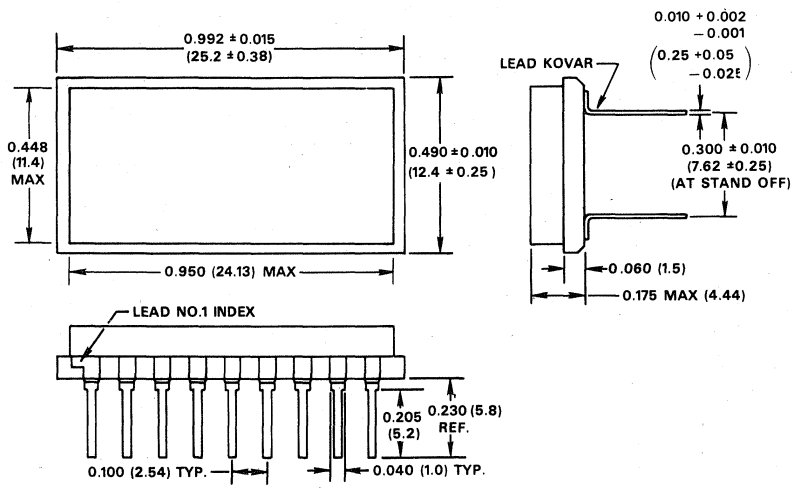


Figure 1. Hermetically-Sealed Ceramic Package Dimensions shown in inches and (mm).

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{EE} (to GND) . . . . . -17V
Digital Input Voltage Range . . . . . V_{DD} to GND
Storage Temperature . . . . . -65°C to +150°C

CAUTION – ELECTROSTATIC SENSITIVE DEVICES

The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

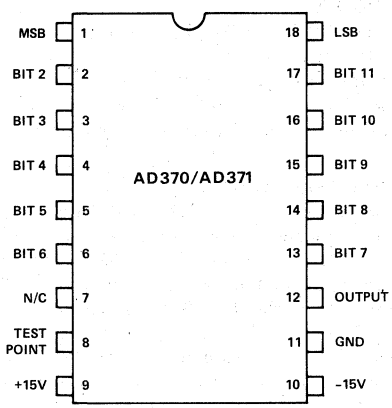


Figure 2. Pin Designations

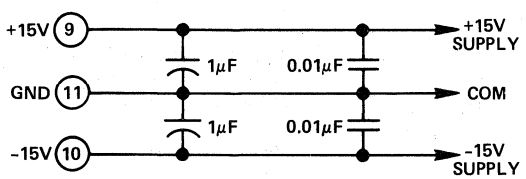


Figure 3. Power Supply Decoupling

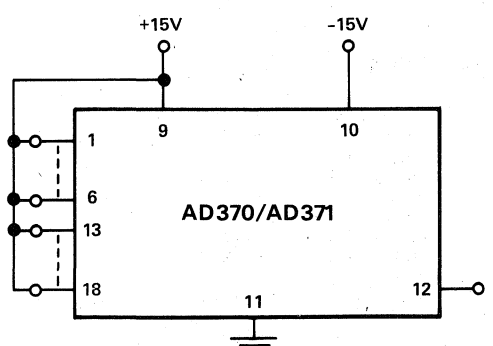


Figure 4. Burn-In Circuit

MIL-STD-883B

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD370/AD371 with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD370/AD371 is offered with 100% screening to MIL-STD-883, method 5008.

Table 1 details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to the following tests on a 100% basis.

TEST	METHOD
1. Internal Visual (Pre cap)	2017, Test Condition B
2. Stabilization Bake	Method 1008, 24 hours @ +150°C
3. Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4. Constant Acceleration	Method 2001, Test Condition B, Y1 plane, 10kg
5. Seal, Fine and Gross	Method 1014, Test Condition A and C
6. Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C
7. Final Electrical Tests	Performed 100% to all min and max dc specifications on data pages
8. External Visual	Method 2009

Table 1.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	0
100000000000	4.9975 Volts
011111111111	5.0000 Volts
000000000000	9.9975 Volts

Table 2. Code Table for the AD371 (CBI)

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-10.000 Volts
100000000001	-0.0097 Volt
100000000000	-0.0048 Volt
011111111111	0
000000000000	9.9952 Volts

Table 3. Code Table for the AD370 (OCBI)

ACCURACY

Accuracy error of a D/A converter is defined as the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error or linearity error. The initial accuracy of the AD370/AD371 is trimmed to within 0.05% of full scale by laser trimming the gain and zero errors. Of the error specifications, the linearity error specification is the most important since it cannot be corrected by the user. The linearity error of the AD370/AD371 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB maximum from an ideal straight line drawn between the end points (inputs all "1's" and all "0's") over the specified operating temperature range of of 0 to +70°C for the "K" version and -55°C to +125°C for the "S" version.

The absolute accuracy of the AD370/AD371 has been guaranteed to ±0.05% of full scale by internal factory trim of the gain and offset. External gain and offset adjustment terminals have been made available to allow fine adjustment to the ±0.012% accuracy level. The measurement system used to calibrate the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. The adjustment procedure, described below, should be carefully followed to assure optimum converter performance.

The proper connections for the offset and gain adjustments are shown in Figure 5. For the AD371, apply a digital input of all "1's" and adjust the offset potentiometer until a 0.000V output is obtained. For the full-scale calibration apply a digital input of all "1's" and adjust the gain potentiometer to +9.9975 volts (see Table 2).

The offset adjustment of the AD370 is made at the half-scale code. Adjust the offset potentiometer until 0.000V is obtained on the output. The full-scale adjustment is made at the negative endpoint or a code of all "1's". Adjust the gain potentiometer until -10.000 volts is obtained on the output.

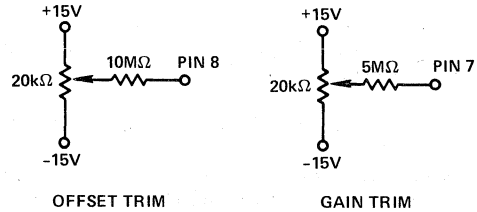


Figure 5. Optional External Trims

SETTLING TIME

Settling time for each AD370/AD371 model is the total time required for the output to settle within an 1/2LSB band around its final value after a change in input (including slew time). The settling time specification is given for a full scale step which is 20V for the AD370 and 10V for the AD371.

IMPROVED SECOND SOURCE

The substrate design of the AD370/AD371 provides for complete pin-for-pin compatibility with other 18-pin DAC's. The AD370/AD371 is a superior direct replacement for these devices where the function of pins 7 and 8 allow. The versatility designed into the AD370/AD371 allows the function of pin 7 and 8 to be modified to exactly second source each of the other units. Information on other second source devices with 4 quadrant multiplying capability is available from Analog Devices.

Analog Devices						
AD370KD	DAC346C-12BPG			MN360	MN370	MN3211
AD371KD	DAC346C-12VP			MN362	MN371	MN3210
AD370SD	DAC347LPC-12G	DAC356C-12	DAC356LPC-12	MN360H	MN370H	
AD370SD/883B	DAC347LPS-12G	DAC356B-12	DAC356LPB-12			
AD371SD	DAC347LPC-12U			MN362H	MN371H	
AD371SD/883B	DAC347LPB-12U					

Table 4. Cross Reference

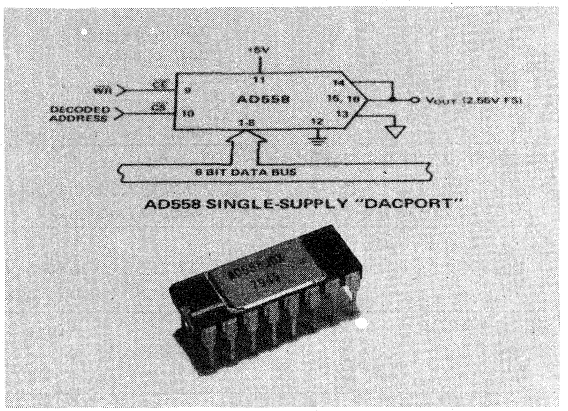
AD370/AD371 ORDERING GUIDE

Model	Package	Linearity	Output Voltage Range	Operating Temperature Range
AD370JN	Polymer Seal	1LSB	-10V to +10V	0 to +70°C
AD370JD	Hermetic	1LSB	-10V to +10V	0 to +70°C
AD371JN	Polymer Seal	1LSB	0 to +10V	0 to +70°C
AD371JD	Hermetic	1LSB	0 to +10V	0 to +70°C
AD370KN	Polymer Seal	1/2LSB	-10V to +10V	0 to +70°C
AD370KD	Hermetic	1/2LSB	-10V to +10V	0 to +70°C
AD371KN	Polymer Seal	1/2LSB	0 to +10V	0 to +70°C
AD371KD	Hermetic	1/2LSB	0 to +10V	0 to +70°C
AD370SD	Hermetic	1/2LSB	-10V to +10V	-55°C to +125°C
AD370SD/883B	Hermetic	1/2LSB	-10V to +10V	-55°C to +125°C
AD371SD	Hermetic	1/2LSB	0 to +10V	-55°C to +125°C
AD371SD/883B	Hermetic	1/2LSB	0 to +10V	-55°C to +125°C

ANALOG DEVICES

DACPORT™
Low Cost Complete μP-Compatible 8-Bit DAC
AD558

FEATURES
- Complete 8-Bit DAC
- Voltage Output — 2 Calibrated Ranges
- Internal Precision Band-Gap Reference
- Single-Supply Operation: +5V to +15V
- Full Microprocessor Interface
- Fast: 1μs Voltage Settling to ±1/2LSB
- Low Power: 75mW
- No User Trims
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_{min} to T_{max}
- Small 16-Pin DIP Package
- Single Laser-Wafer-Trimmed Chip for Hybrids
- Low Cost



PRODUCT DESCRIPTION

The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit* which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 1μs.

The AD558 is available in four performance grades and two package types. The AD558J and K are specified for use over the 0 to +70°C temperature range and are available in either a 16-pin hermetically-sealed side-brazed ceramic DIP or a lower-cost 16-pin plastic DIP. The AD558S and T grades are specified for −55°C to +125°C operation and the hermetically-sealed ceramic package is standard. Processing to MIL-STD-883, Class B is optional on S and T grades.

*Covered by U.S. Patent No. 3,887,863.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allows the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimmed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 700ns.
5. The AD558 is designed and specified to operate from a single +4.5V to +16.5V power supply.
6. Low digital input currents, 100μA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible over the entire operating V_{CC} range.

(continued on page 9-16)

SPECIFICATIONS (typical @ T_A = +25°C, V_{CC} = +5V to +15V unless otherwise specified)

MODEL	AD558J	AD558K	AD558S[1]	AD558T[1]
RESOLUTION	8 Bits	*	*	*
RELATIVE ACCURACY[2]				
0 to +70°C	±1/2LSB max	±1/4LSB max	*	**
-55°C to +125°C	—	—	±3/4LSB max	±3/8LSB max
OUTPUT				
Ranges	0V to +2.56V	*	*	*
	0V to +10V [3]	*	*	*
Current, Source	+5mA	*	+5mA min	***
Sink	Internal Passive Pull-Down to Ground[4]	*	*	*
OUTPUT SETTLING TIME[5]				
0 to 2.56 volt range	0.8μs (1.5μs max)	*	*	*
0 to 10 volt range[3]	2.0μs (3.0μs max)	*	*	*
FULL SCALE ACCURACY				
@ 25°C	±1.5LSB (±0.6%) max	±0.5LSB (±0.2%) max	*	**
T_{min} to T_{max}	±2.5LSB (±1.0%) max	±1LSB (±0.4%) max	*	**
ZERO ERROR				
@ 25°C	±1LSB max	±1/2LSB max	*	**
T_{min} to T_{max}	±2LSB max	±1LSB max	*	**
MONOTONICITY[6]				
T_{min} to T_{max}	Guaranteed	*	*	*
DIGITAL INPUTS				
T_{min} to T_{max}				
Input Current	±100μA max	*	*	*
Data Inputs, Voltage				
Bit On — Logic "1"	2.0V min	*	*	*
Bit Off — Logic "0"	0.8V max	*	*	*
Control Inputs, Voltage				
On — Logic "1"	2.0V min	*	*	*
Off — Logic "0"	0.8V max	*	*	*
TIMING[7]				
T_{min} to T_{max}				
t_W (Strobe Pulse Width)	100ns min	*	*	*
t_{DH} (Data Hold Time)	10ns max	*	*	*
t_{DS} (Data Set-Up Time)	100ns min	*	*	*
POWER SUPPLY				
Operating Voltage Range (V_{CC})				
2.56 Volt Range	+4.5V to +16.5V	*	*	*
10 Volt Range	+11.4V to +16.5V	*	*	*
Current (I_{CC})	15mA typ, 25mA max	*	*	*
Rejection Ratio	0.03%/% max	*	*	*
POWER DISSIPATION, V_{CC} = 5V	75mW (125mW max)	*	*	*
V_{CC} = 15V	225mW (375mW max)	*	*	*
OPERATING TEMPERATURE RANGE				
T_{min}	0°C	*	-55°C	***
T_{max}	+70°C	*	+125°C	***

NOTES

[1] The AD558S and AD558T are available fully processed and screened to the requirements of MIL-STD-883, Class B. A complete description is given on page 9-16 of this data sheet. Order AD558SD/883B or AD558TD/883B.

[2] Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4] Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.

[5] Settling time is specified for a positive-going full-scale step. Negative-going steps to zero are slower, but can be improved with an external pull-down. See page 9-19 of this data sheet for details.

[6] A monotonic converter has a maximum differential linearity error of ±1LSB.

[7] See Figure 8, page 9-18.

*Specifications same as AD558J.
**Specifications same as AD558K.
***Specifications same as AD558S.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Ground . . . . . .0V to +18V
Digital Inputs (Pins 1-10) . . . . . .0 to V_{CC}
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N (plastic) Package . . . . . -25°C to +100°C
D (ceramic) Package. . . . . -55°C to +150°C
Lead Temperature (soldering, 10 second). . . . . 300°C
Thermal Resistance
Junction to Ambient (Junction to Case)
N (plastic) Package . . . . . .140(55)°C/W
D (ceramic) Package. . . . . .100(30)°C/W

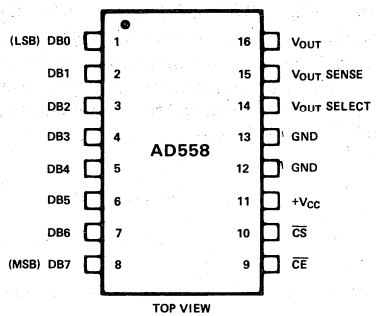


Figure 1. AD558 Pin Configuration

CHIP AVAILABILITY

The AD558 is available in laser-trimmed, passivated chip form. Figure 2 shows the AD558 metalization pattern bonding pads and dimensions. All four grades are available with guaranteed temperature specifications from +25°C to T_{max}. Consult the factory for details.

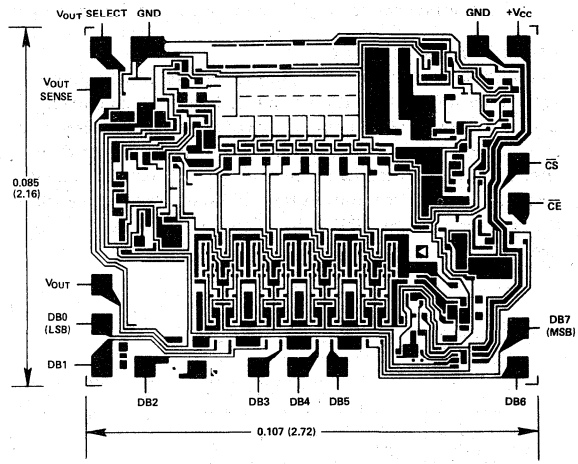
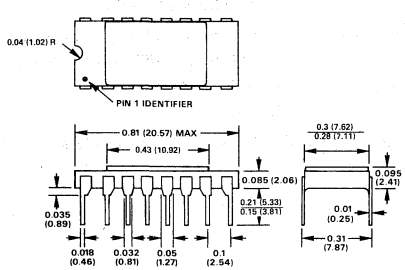


Figure 2. AD558 Chip Bonding Diagram (Dimensions shown in inches and (mm))

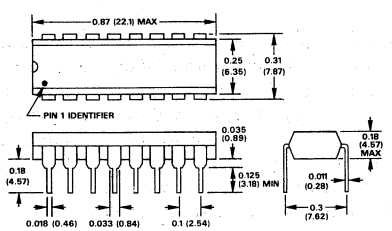
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

D (CERAMIC) PACKAGE



N (PLASTIC) PACKAGE



AD558 ORDERING GUIDE

Model	Package	Temperature	Relative Accuracy Error Max T_{min} to T_{max}	Full-Scale Error, Max T_{min} to T_{max}
AD558JN	Plastic	0 to +70°C	±1/2LSB	±2.5LSB
AD558KN	Plastic	0 to +70°C	±1/4LSB	±1LSB
AD558JD	Ceramic	0 to +70°C	±1/2LSB	±2.5LSB
AD558KD	Ceramic	0 to +70°C	±1/4LSB	±1LSB
AD558SD	Ceramic	-55°C to +125°C	±3/4LSB	±2.5LSB
AD558SD/883B	Ceramic	-55°C to +125°C	±3/4LSB	±2.5LSB
AD558TD	Ceramic	-55°C to +125°C	±3/8LSB	±1LSB
AD558TD/883B	Ceramic	-55°C to +125°C	±3/8LSB	±1LSB

(continued from page 9-13)

7. The single-chip, low power I^2L design of the AD558 is inherently more reliable than hybrid multi-chip or conventional single-chip bipolar designs. The AD558S and T grades, which are specified over the -55°C to +125°C temperature range, are available fully processed to MIL-STD-883, Class B.
8. All AD558 grades are available in chip form with guaranteed specifications from +25°C to T_{max}. MIL-STD-883, Class B processing is standard on Analog Devices bipolar chips. Contact the factory for additional chip information.

CIRCUIT DESCRIPTION

The AD588 consists of four major functional blocks, fabricated on a single monolithic chip (see Figure 3). The main D to A converter section uses eight equally-weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

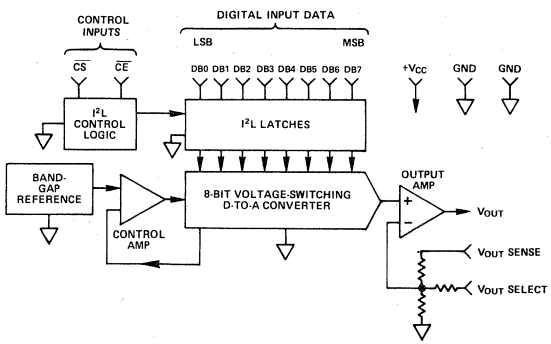


Figure 3. AD558 Functional Block Diagram

The high-speed output buffer amplifier is operated in the non-inverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed to match and track the DAC resistors and to assure precise initial calibration of the two output ranges, 0V to 2.56V and 0V to 10V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2 volts and thus, unlike 6.3 volt temperature-compensated zeners, may be operated from a single, low-voltage logic power supply.

The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low-power, small geometry and high-speed are advantages of the I^2L design as applied to this section. I^2L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a μP or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD558, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The available hermetically-sealed, low profile DIP package ("D" suffix) takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further ensure reliability, military-temperature range AD558 grades S and T are available 100% screened to MIL-STD-883, Class B, method 5004. Table 1 details the test procedure.

TEST	METHOD
1) Internal Visual (Pre cap)	Method 2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1014, Test Condition B, 160 hours @ +125°C min
7) Final Electrical Tests	Performed 100% to all min and max dc specifications on data pages.
8) External Visual	Method 2009

Table 1. MIL-STD-883, Class B Test Procedures

CONNECTING THE AD558

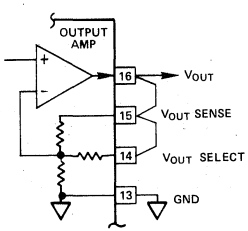
The AD558 has been configured for ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision that must be made by the user is a single jumper to select output voltage range. Clean circuit-board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

Figure 4 shows the two alternative output range connections. The 0V to 2.56V range may be selected for use with any power supply between +4.5V and +16.5V. The 0V to 10V range requires a power supply of +11.4V to +16.5V.

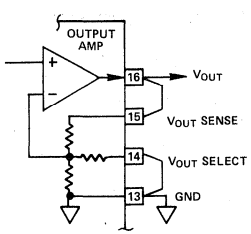
Because of its precise factory calibration, the AD558 is intended to be operated without user trims for gain and offset; therefore no provisions have been made for such user-trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with V_{OUT} SENSE will increase the output range.

For example if a 0V to 10.24V output range is desired (40mV = 1LSB), a nominal resistance of 850Ω is required. It must be remembered that, although the internal resistors all ratio-match and track, the *absolute* tolerance of these resistors is typically ±20% and the *absolute* TC is typically −50ppm/°C (0 to −100ppm/°C). That must be considered when re-scaling is performed. Figure 5 shows the recommended circuitry for a full-scale output range of 10.24 volts. Internal resistance values shown are nominal.

NOTE: Decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.



a. 0V to 2.56V Output Range



b. 0V to 10V Output Range

Figure 4. Connection Diagrams

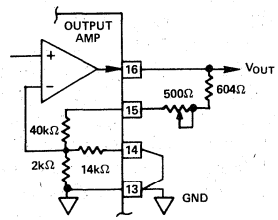


Figure 5. 10.24V Full-Scale Connection

GROUNDING AND BYPASSING*

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD558 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD558 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 6 shows how the ground connections should be made.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD558, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD558, it is recommended that analog common be selected.

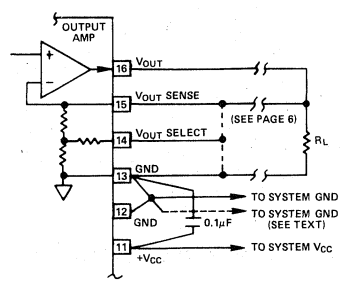


Figure 6. Recommended Grounding and Bypassing

POWER SUPPLY CONSIDERATIONS

The AD558 is designed to operate from a single positive power supply voltage. Specified performance is achieved for any supply voltage between +4.5V and +16.5V. This makes the AD558 ideal for battery-operated, portable, automotive or digital main-frame applications.

The only consideration in selecting a supply voltage is that, in order to be able to use the 0V to 10V output range, the power supply voltage must be between +11.4V and +16.5V. If, however, the 0V to 2.56V range is to be used, power consumption will be minimized by utilizing the lowest available supply voltage (above +4.5V).

*For additional insight, "An IC Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right For A Change", is available at no charge from any Analog Devices Sales Office.

TIMING AND CONTROL

The AD558 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs, pins 9 and 10 respectively. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1", the input data is latched into the registers and held until both $\overline{CE}$ and $\overline{CS}$ return to "0". (Unused $\overline{CE}$ or $\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table II. The logic function is also shown in Figure 7.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	∫	0	0	latching
1	∫	0	1	latching
0	0	∫	0	latching
1	0	∫	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
∫ = Logic Threshold at Positive-Going Transition

Table II. AD558 Control Logic Truth Table

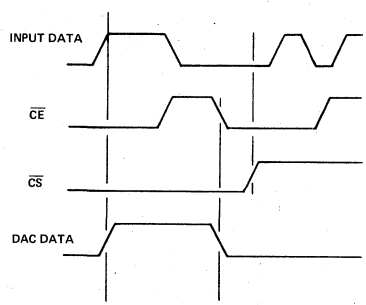


Figure 7. AD558 Control Logic Function

Figure 8 shows the timing for the data and control signals; $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

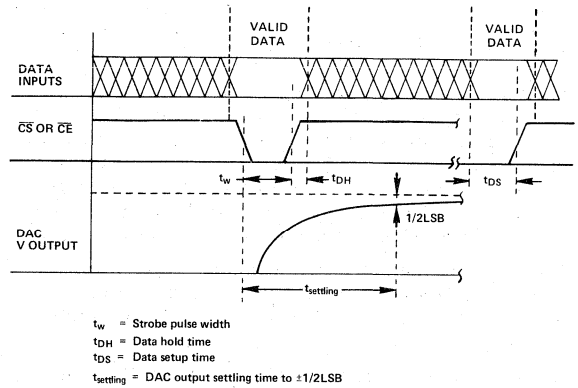
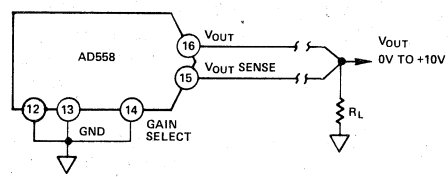


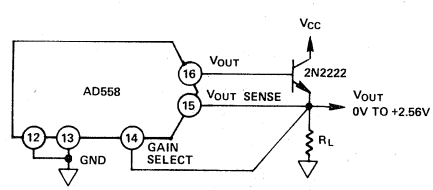
Figure 8. AD558 Timing

USE OF V_{OUT} SENSE

Separate access to the feedback resistor of the output amplifier allows additional application versatility. Figure 9a shows how I X R drops in long lines to remote loads may be cancelled by putting the drops "inside the loop". Figure 9b shows how the separate sense may be used to provide a higher output current by feeding back around a simple current booster.



a. Compensation for I x R Drops in Output Lines



b. Output Current Booster

Figure 9. Use of V_{OUT} sense

OPTIMIZING SETTLING TIME

In order to provide single-supply operation and zero-based output voltage ranges, the AD558 output stage has a passive "pull-down" to ground. As a result, settling time for negative-going output steps may be longer than for positive-going output steps. The relative difference depends on load resistance and capacitance. If a negative power supply is available, the negative-going settling time may be improved by adding a pull-down resistor from the output to the negative supply as shown in Figure 10. The value of the resistor should be such that, at zero voltage out, current through that resistor is 0.5mA max.

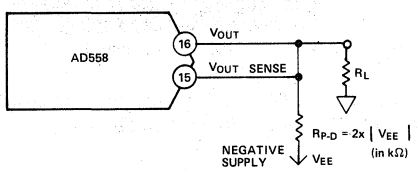


Figure 10. Improved Settling Time

BIPOLAR OUTPUT RANGES

The AD558 was designed for operation from a single power supply and is thus capable of providing only unipolar (0V to +2.56 and 0V to 10V) output ranges. If a negative supply is available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 11 shows how a ±1.28 volt output range may be achieved when a −5 volt power supply is available. The offset is provided by the AD589 precision 1.2 volt reference which will operate from a +5 volt supply. The AD544 output amplifier can provide the necessary ±1.28 volt output swing from ±5 volt supplies. Coding is complementary offset binary.

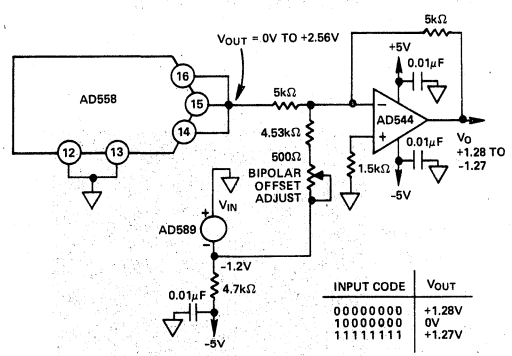
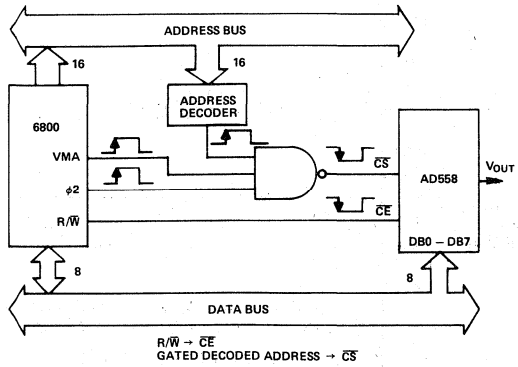


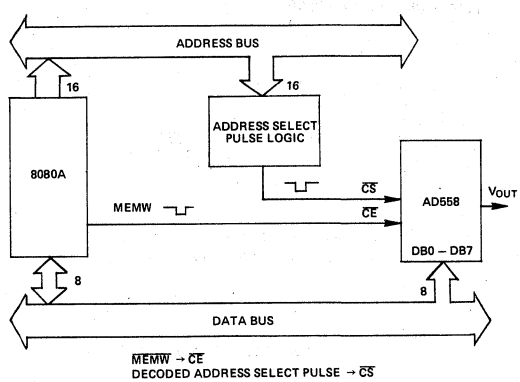
Figure 11. Bipolar Operation of AD558 from ±5V Supplies

INTERFACING THE AD558 TO MICROPROCESSOR DATA BUSES*

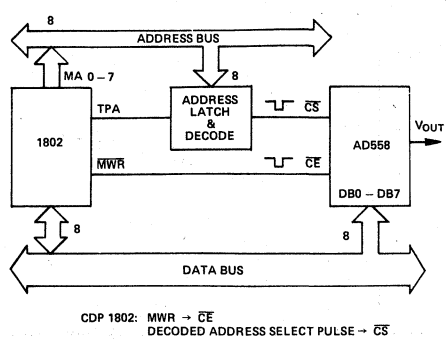
The AD558 is configured to act like a "write only" location in memory that may be made to coincide with a read only memory location or with a RAM location. The latter case allows data previously written into the DAC to be read back later via the RAM. Address decoding is partially complete for either ROM or RAM. Figure 12 shows interfaces for three popular microprocessor systems.



a. 6800/AD558 Interface



b. 8080A/AD558 Interface



c. 1802/AD558 Interface

Figure 12. Interfacing the AD558 to Microprocessors

*The microprocessor-interface capbilities of the AD558 are extensive. A comprehensive application note, "Interfacing the AD558 8-Bit DAC to Microprocessors" is available from any Analog Devices Sales Office upon request, free of charge. (Available Spring of 1980).

AD558 Performance (typical @ +25°C, V_{CC} = +5V to +15V unless otherwise noted)

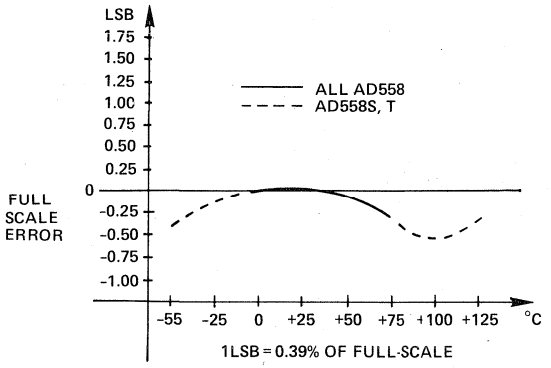


Figure 13. Full Scale Accuracy vs. Temperature Performance of AD558

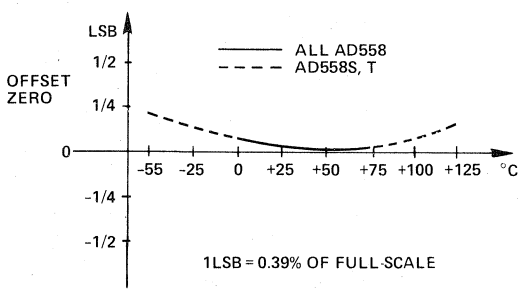


Figure 14. Zero Drift vs. Temperature Performance of AD558

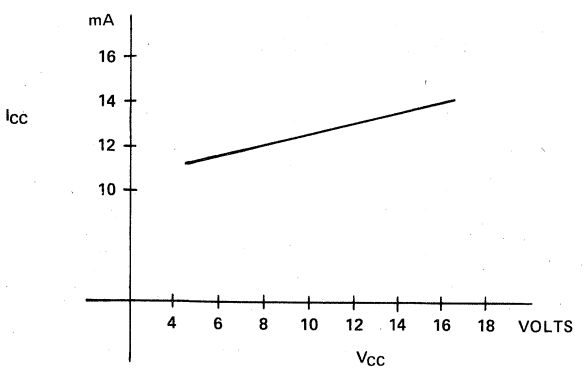


Figure 15. Quiescent Current vs. Power Supply Voltage for AD558

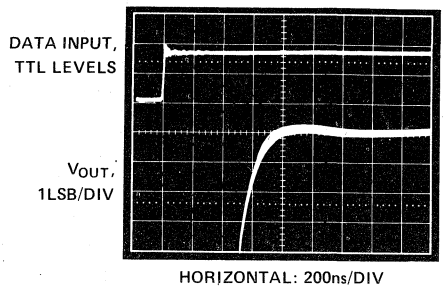


Figure 16. AD558 Settling Characteristic Detail 0V to 2.56V Output Range Full-Scale Step

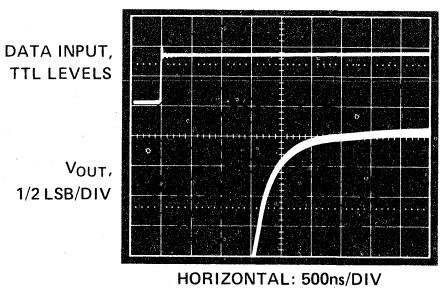


Figure 17. AD558 Settling Characteristic Detail 0V to 10V Output Range Full-Scale Step

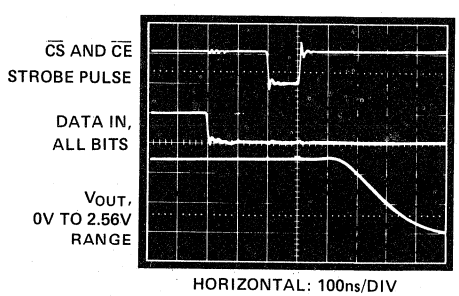


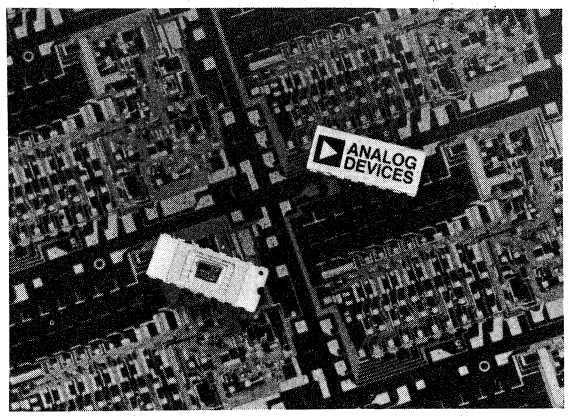
Figure 18. AD558 Logic Timing

Low Cost 10-Bit Monolithic D/A Converter

AD561

FEATURES

- Low Cost
- Complete Current Output Converter
- High Stability Buried Zener Reference
- Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)
- Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
- Fast Settling – 250ns to 1/2LSB
- Guaranteed Monotonicity Over Full Operating Temperature Range
- TTL/DTL and CMOS Compatible (Positive True Logic)
- Single Chip Monolithic Construction
- Hermetically-Sealed Ceramic DIP (All Grades)



PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/°C; the T.C. is tested and guaranteed to 30ppm/°C max for the K and T versions, 60ppm/°C max for the S, and 80ppm/°C for the J.

All grades are packaged in a 16-pin hermetically-sealed ceramic dual-in-line package. The AD561J and K versions are specified for operation over the 0 to +70°C temperature range, the AD561S and T for operation over the full military temperature range from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25μA.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5μs range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40MΩ open collector output impedance results in negligible errors due to output leakage currents.
5. Every AD561 is subjected to a 24 hour stabilization bake at 150°C, a gross leak test and a 24 hour burn-in at 125°C to ensure reliability and long term stability.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +5V, V_{EE} = -15V, unless otherwise specified)

MODEL	AD561J MIN	AD561J TYP	AD561J MAX	AD561K MIN	AD561K TYP	AD561K MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			*			V
Bit OFF Logic "0"			+0.8			*	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			*			V
Bit OFF Logic "0"			30% V_{CC}			*	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		*	*	nA
Bit OFF Logic "0"		-5	-25		*	*	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	*	*	*	mA
Bipolar	±0.75	±1.0	±1.2	*	*	*	mA
Resistance (Exclusive of Application Resistors)		40M			*		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		*	*	% of F.S.
Capacitance		25			*		pF
Compliance Voltage	-2	-3	+10	*	*	*	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			*		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		*	*	mA
V_{EE}, -10.8V dc to -16.5V dc		12	16		*	*	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		*	*	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		*	*	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			*	*	°C
Storage		-65 to +150			*	*	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	80		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			*		V
RANGES (See Figs. 5, 6)		-5 to +5			*		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			*		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			*		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			*		% of F.S.
Bipolar Zero (With 20Ω Trimmer)		±0.2			*		% of F.S.

***Specifications same as AD561J specs.**
Specifications subject to change without notice.

MODEL	AD561S MIN	AD561S TYP	AD561S MAX	AD561T MIN	AD561T TYP	AD561T MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		-25	-100		**	**	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of Application Resistors)		40M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of F.S.
Capacitance		25			**		pF
Compliance Voltage	-2	-3	+10	**	**	**	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		6	10		**	**	mA
V_{EE}, -10.8V dc to -16.5V dc		11	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		**	**	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		**	**	ppm of F.S./%
TEMPERATURE RANGE							
Operating		-55 to +125			**	**	°C
Storage		-65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	60		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT RANGES (See Figs. 5, 6)		0 to +10 -5 to +5			** **		V V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			**		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			**		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			**		% of F.S.
Bipolar Zero (With 20Ω Trimmer)		±0.2			**		% of F.S.

****Specifications same as AD561S specs.**
Specifications subject to change without notice.

DIGITAL LOGIC INTERFACE

All standard positive supply logic families interface easily with the AD561. The digital code is positive true binary (all bits high, Logic "1", gives positive full scale output). The logic input load factor (100nA max at Logic "1", -25μA max at Logic "0", 3pF capacitance), is less than one equivalent digital load for all logic families, including unbuffered CMOS. The digital threshold is set internally as a function of the positive supply, as shown in Figure 1. For most applications, connecting V_{CC} to the positive logic supply will set the threshold at the proper level for maximum noise immunity. For nonstandard applications, refer to Figure 1 for threshold levels. Uncommitted bit input lines will assume a "1" state (similar to TTL), but they are high impedance and subject to noise pickup. Unused digital inputs should be connected directly to ground or V_{CC}, as desired.

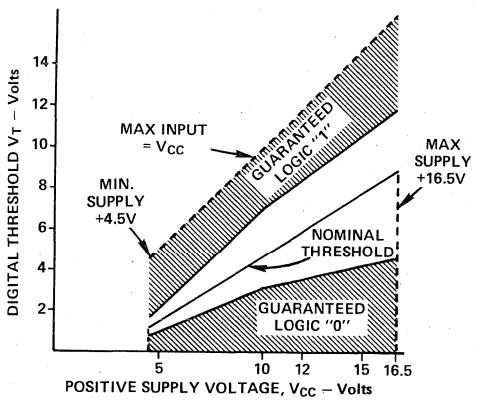
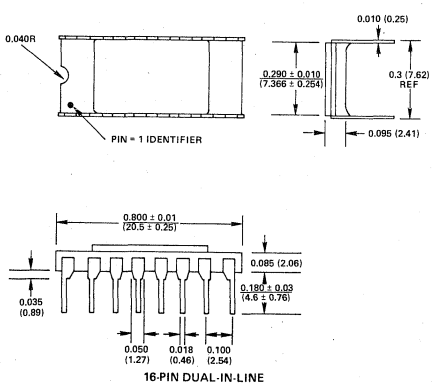


Figure 1. Digital Threshold Vs. Positive Supply



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Figure 2.

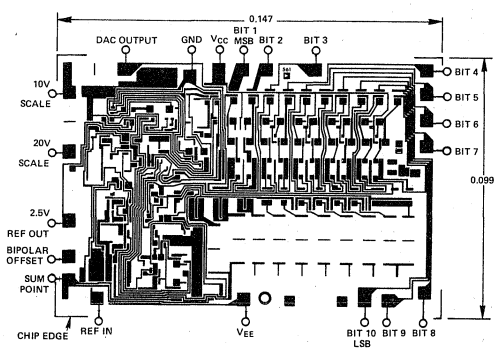
THE AD561 OFFERS TRUE 10-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see following page) from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD561 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T versions – 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD561 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 9.8mV change in the analog output (1LSB = 10V x 1/1024 = 9.8mV). If in actual use, however, a 1LSB change in the input code results in a change of only 2.45mV (1/4LSB) in analog output, the differential nonlinearity error would be 7.35mV, or 3/4LSB. The AD561K and T have a max differential linearity error of 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 2.5ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.025% (100 x 2.5ppm/°C of error). The resulting error could then be as much as 0.025% + 0.025% = 0.05% of F.S. (1/2LSB represents 0.05% of F.S.). To be sure of accurate performance all versions of the AD561 are therefore 100% tested to be monotonic over the full operating temperature range.



THE AD561 IS AVAILABLE IN A LASER TRIMMED CHIP FORM. THE CHIP OFFERS MORE APPLICATION FLEXIBILITY THAN THE 16-PIN PACKAGED DEVICE. PLEASE CONSULT CHIP CATALOG FOR APPLICATION DETAILS.

Figure 3. Chip Bonding Diagram

AD561 ORDERING GUIDE

MODEL	TEMP RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)
AD561J	0 to +70°C	±½LSB max	80ppm max
AD561K	0 to +70°C	±¼LSB max	30ppm max
AD561S	-55 to +125°C	±½LSB max	60ppm max
AD561S/883B*	-55 to +125°C	±½LSB max	60ppm max
AD561T	-55 to +125°C	±¼LSB max	30ppm max
AD561T/883B*	-55 to +125°C	±¼LSB max	30ppm max

*The AD561S/883B and AD561T/883B are fully processed to MIL-STD-883A, Method 5004, Class B. The complete procedure list is available on request.

CONNECTING THE AD561 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to 1/2LSB on a 10 volt scale). If a 25Ω fixed resistor is substituted for the 50Ω trimmer, unipolar zero will typically be within ±1/10LSB (plus op amp offset), and full scale accuracy will be within ±1LSB. Substituting a 10Ω resistor for the 20Ω bipolar offset trimmer will give a bipolar zero error typically within ±1LSB.

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25picofarad DAC output capacitance.

FIGURE 5. UNIPOLAR CONFIGURATION
This configuration will provide a unipolar 0 to +10 volt output range.

STEP I . . . ZERO ADJUST
Turn all bits OFF and adjust op amp trimmer, R_1, until the output reads 0.000 volts (1LSB = 9.76mV).

STEP II . . . GAIN ADJUST
Turn all bits ON and adjust 50Ω gain trimmer, R_2, until the output is 9.990 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.23V full scale is desired (exactly 10mV/bit), insert a 120Ω resistor in series with R_2.

FIGURE 6. BIPOLAR CONFIGURATION
This configuration will provide a bipolar output voltage from -5.000 to +4.990 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . ZERO ADJUST
Turn ON MSB only, turn OFF all other bits. Adjust 20Ω trimmer R_3, to give 0.000 output volts.

STEP II . . . GAIN ADJUST
Turn OFF all bits, adjust 50Ω gain trimmer to give a reading of -5.000 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 7. ±10 VOLT BUFFERED BIPOLAR OUTPUT
The AD561 can also be connected for a ±10 volt bipolar range with an additional external resistor as shown in Figure 7. A larger value trimmer is required to compensate for tolerance in the thin film resistors (which are trimmed to match the full scale current). For best full scale temperature coefficient performance, the external resistors should have a T.C. of -50ppm/°C. For applications requiring optimum performance, a ±10 volt bonding option is available on special order.

PIN CONFIGURATION
TOP VIEW

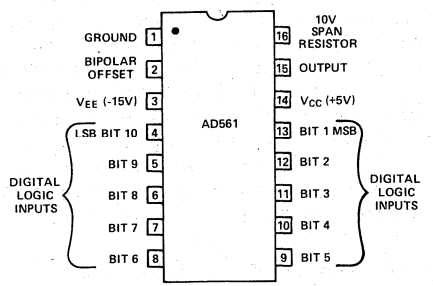


Figure 4.

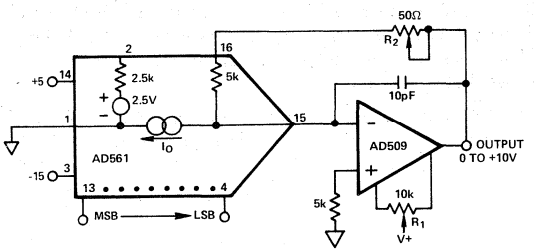


Figure 5. 0 to +10V Unipolar Voltage Output

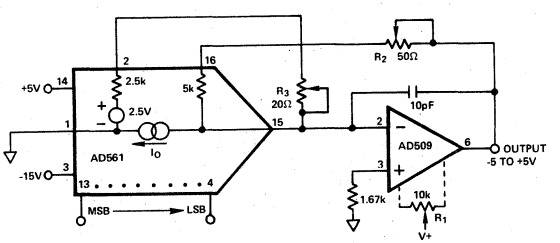


Figure 6. ±5V Buffered Bipolar Voltage Output

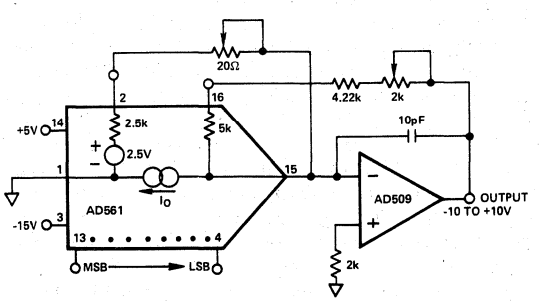


Figure 7. ±10V Buffered Voltage Output

CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 8. The voltage reference, CR1, is a buried zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to ±15ppm/°C.

The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5kΩ bipolar offset resistor; it can still be used as a voltage reference as shown below in Figure 9.

The 2.5kΩ scaling resistor and control amplifier A_2 then force a 1mA reference current to flow through reference transistor Q1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and have equal 5kΩ emitter resistors, Q_2 also carries 1mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5mA; Q_8 carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing 120μA through the 150Ω interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than 1/4LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly but is not switched to the output; thus full scale is 1023/1024 x 2mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

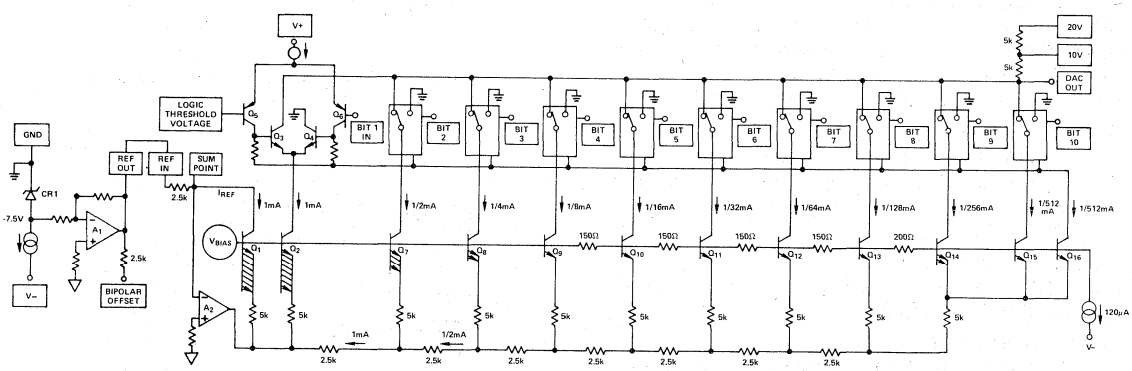


Figure 8. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

PRECISION LOW-NOISE REFERENCE

The precision reference of the AD561 can be brought out separately from the DAC to serve as a master system reference. Since the reference is connected through the 2.5kΩ bipolar offset resistor, it must be buffered externally, as shown here in Figure 9. The DAC section can still be operated independently in a unipolar mode, but internal thermal and ground loop effects will create crosstalk of about 0.01% with an ideal ground. The long term stability of this reference will be especially good, typically ±0.01% per year or better. If the filter capacitor, C is not used, wideband output noise will be about 120ppm p-p (1.2mV p-p for 10 volts). If C is 4.7μF, wideband noise will be about 25μV p-p (10 volts out) and 15μV p-p from 0.1 to 10Hz.

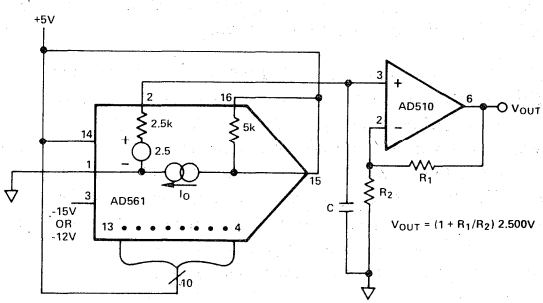


Figure 9. Precision Ultra Low Noise Reference

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD561 are specifically designed for fast settling operation. The typical settling time to ±0.05% (1/2LSB) for the worst case transition (major carry, 0111111111 to 1000000000) is less than 250ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB.) But full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD561 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. This form of conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 12. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD561 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.05% of full scale (for a full scale transition) requires 7.6 time constants. This effect is important for $R > 1k\Omega$.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits using the fast settling AD509. The circuits shown settle to ±1/2LSB in 600ns unipolar and 1.1μs bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1μF will be sufficient since the AD561 runs at constant supply current regardless of input code.

POWER SUPPLY SELECTION

The AD561 will operate over a wide range of power supply voltages, with a total supply from 15.3 to 33 volts. Symmetrical supplies are not required, and in many applications not recommended.

The positive supply level determines the digital threshold level, as explained previously and shown in Figure 1. It is therefore recommended that V_{CC} be connected directly to the digital supply for best threshold match.

Positive output voltage compliance range is unaffected by the positive supply level because of the open collector output stage design; thus the full +10 volt compliance is available even with a +5 volt V_{CC} level. Power supply rejection is excellent, so that digital supply noise will not be reflected to the output. but use of a 0.1μF bypass capacitor near the AD561 is recommended for decoupling.

The nominal negative supply level is -15 volts, with an allowable range of -10.8 to -16.5 volts. The negative supply level affects the negative compliance range, as shown in Figure 10.

OUTPUT VOLTAGE COMPLIANCE

The AD561 has a typical output compliance range from -3 to +10 volts. The output current is unaffected by changes in the output terminal voltage over that range. This results from the use of open collector output switching stages in a cascode configuration, and gives an output impedance of 40MΩ. Positive compliance range is limited only by collector breakdown (and is independent of positive supply level), but the negative range is limited by the required bias levels and resistor ladder voltage. Negative compliance varies with negative supply, as shown in Figure 10. The compliance range is guaranteed to be -2 to +10 volts with V_{EE} = -15 volts.

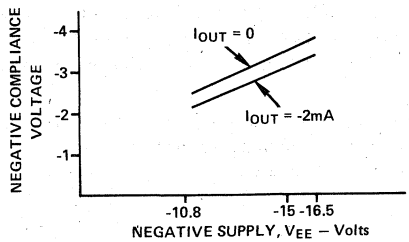


Figure 10. Typical Negative Compliance Range Vs. Negative Supply.

DIRECT UNBUFFERED VOLTAGE OUTPUT

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 1 shows a connection using the gain and bipolar output resistors to give a ±1.66 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 2.5 volt reference voltage for bipolar offset. For example, setting R_X = 2.5kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance. A 0 to +10 volt output can be obtained by connecting the 5kΩ gain resistor to 9.99 volts; again the digital code is complementary binary.

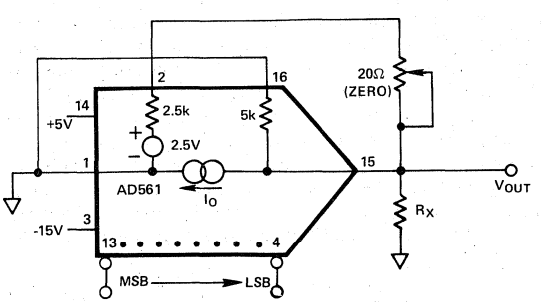


Figure 11. Unbuffered Bipolar Voltage Output

HIGH SPEED 10-BIT A/D CONVERTERS

The fast settling characteristics of the AD561 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 10-bit converter system to be constructed with a minimum parts count. Shown here is a configuration using standard components; this system completes a full 10-bit conversion in 5.5μs unipolar or 12μs bipolar. This converter will be accurate to ±1/2LSB of 10 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.99 volts, with each bit having a value of 9.76mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +4.9mV; trim R_1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9985 volts (10 volts − 1LSB − 1/2LSB); then trim R_2 again until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.99 volts. Bipolar offset trimming is done by applying a +4.9mV input signal and trimming R_1 for the LSB transition (MSB "1", all other bits "0"). Full scale is set by applying -4.995 volts and trimming R_2 for the LSB transition (all other bits "0"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 10-bit ±1/2LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance of 1kΩ, 1LSB = 2mV) to the point that comparator performance will be sacrificed. A 1kΩ resistor is the optimum value for this application for 10-bit accuracy. The chart shown in the figure gives the speed of the ADC for ±1/2LSB accuracy (and no missing codes) for 6, 8 and 10-bit resolution.

A much faster converter can be constructed by using higher performance external components. Each individual high-order bit settles in less than 250ns; the low-order bits less than 200ns. Because of this, a staged clock which speeds up for lower bits will improve the speed. Also, a faster comparator and Schottky TTL or ECL logic would be necessary. 10-bit converters in the 3 to 5μs range could be built around the AD561 with these techniques.

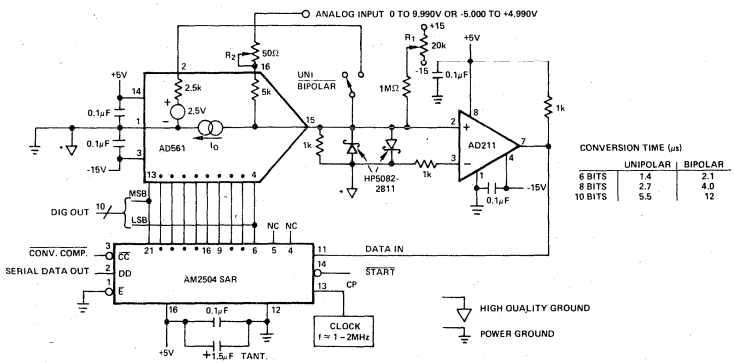


Figure 12. Fast Precision Analog to Digital Converter

DIGITAL 4 TO 20mA OR 1 TO 5 VOLT CONVERTER

A direct digital 4 to 20mA or 1 to 5 volt line driver can be built with the AD561 as shown in Figure 13. The 2.5 volt reference is divided to provide 1 volt at the op amp noninverting input − thus a zero input code results in a 1 volt output at the Darlington emitter (V_{OUT}). The 2k feedback resistance converts the nominal 2mA (±20%) full scale output from the AD561 to 4 volts, for a total output of 5 volts F.S. The voltage at the emitter forces a proportional current through the 250Ω (which appears at the collector as I_{OUT}). The AD561 current is added to the 4−20mA line; thus 5 volts full scale gives 22mA in the current loop. For exactly 20mA, trim the 1k pot for 4.5V F.S. (A single op amp circuit will not produce both 1 to 5 volt and 4 to 20mA outputs simultaneously.)

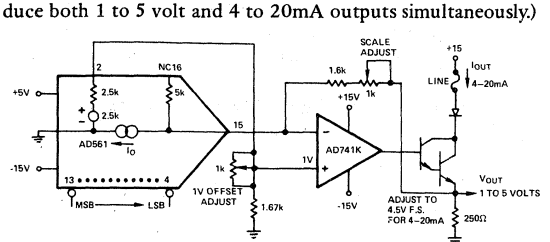


Figure 13. Digital 4 to 20mA or 1 to 5 Volt Line Driver

DIGITALLY PROGRAMMABLE SETPOINT COMPARATOR

Figure 15 demonstrates a high accuracy systems-oriented setpoint comparator. The 2.5 volt reference is buffered and amplified by the AD741K to produce an exact 10.000 volt reference which could be used as a primary system reference for several such circuits. The +10 volt compliance of the AD561 then allows it to generate a zero to +10 volt output swing through the 5kΩ application resistor without an additional op amp. The digital code for this system will be complementary binary (all 1's give 0.00 volts out).

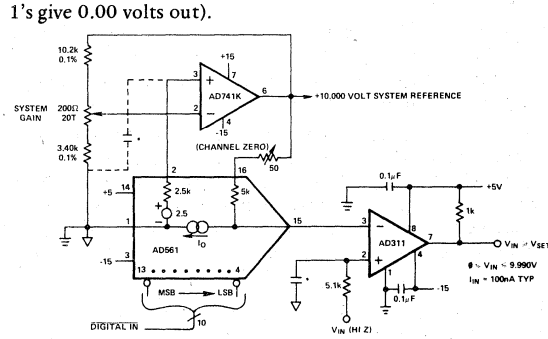


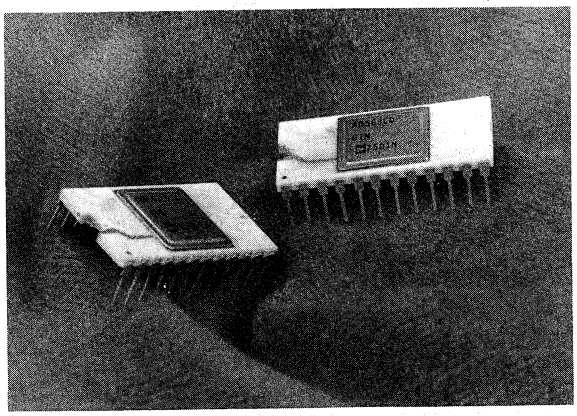
Figure 14. Digitally Programmable Set Point Comparator

ANALOG DEVICES

IC 12-Bit D/A Converter

AD562/AD563

FEATURES
Low Cost
True 12-Bit Accuracy
Guaranteed Monotonicity Over Full Temperature Range
Hermetic 24-Pin DIP
TTL/DTL and CMOS Compatibility
Positive True Logic



PRODUCT DESCRIPTION

The AD562/AD563 are integrated circuit 12-bit digital-to-analog converters consisting of a specially designed precision bipolar switch and control amplifier chip and a compatible high stability silicon chromium thin film resistor chip. The AD563 also includes its own internal voltage reference chip. All chips are internally connected and mounted in a hermetically sealed ceramic 24 lead dual-in-line package to produce a self-contained current output DAC.

A unique combination of advanced circuit design, high stability SiCr thin film resistor processing and laser trimming technology provide the AD562/AD563 with true 12-bit accuracy. The maximum error at +25°C is limited to ±½LSB on all versions and monotonicity is guaranteed over the full operating temperature range.

The AD562 and AD563 are recommended for high accuracy 12-bit D/A converter applications where true 12-bit performance is required, but low cost and small size are considerations. Both devices are also ideal for use in constructing A/D conversion systems and as building blocks for higher resolution D/A systems. J and K versions are specified for operation over the 0 to +70°C temperature range, the S and T for operation over the military temperature range, −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD562 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, the AD563 is recommended with its internal low drift voltage reference.
2. True 12-bit resolution is achieved with guaranteed monotonicity over the full operating temperature range. Voltage outputs are easily implemented by using an external operational amplifier and the AD562/AD563's internally provided feedback resistors.
3. The devices incorporate a newly developed and fully differential, non-saturating precision current switching cell structure which provides increased immunity to supply voltage variation and also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation.
4. The thin film resistor network contains gain, range, and bipolar offset resistors so that various output voltage ranges can be programmed by changing connections to the device terminal leads. Thin film resistors are laser trimmed while the device is powered to accurately calibrate all scale factors. The scale factors are dependent upon the tracking coefficient (<±2ppm/°C) of these resistors, rather than upon their absolute temperature coefficients.
5. TTL or CMOS inputs can be accommodated for supply voltages from +5V to +15V.
6. Positive true logic eliminates the need for additional inverter components.

SPECIFICATIONS (T_A = +25°C, unless otherwise specified)

MODEL	AD562KD/BIN AD562KD/BCD	AD562AD/BIN AD562AD/BCD	AD562SD/BIN AD562SD/BCD
DATA INPUTS (positive True, Binary (BCD) and Offset Binary (BCD))			
TTL, V_{CC} = +5V, Pin 2 Open Circuit			
Bit ON Logic "1"	+2.0V	*	*
Bit OFF Logic "0"	+0.8V max	*	*
CMOS, 4.75 ≤ V_{CC} ≤ 15.8, Pin 2 Tied to Pin 1			
Bit ON Logic "1"	70%V_{CC} min	*	*
Bit OFF Logic "0"	30%V_{CC} max	*	*
Logic Current (Each Bit)			
Bit ON Logic "1"	+20nA typ, +100nA max	*	*
Bit OFF Logic "0"	−50μA typ, −100μA max	*	*
OUTPUT			
Current			
Unipolar	−1.6mA min, −2.0mA typ, −2.4mA max	*	*
Bipolar	±0.8mA min, ±1.0mA typ, ±1.2mA max	*	*
Resistance (Exclusive of Span Resistors)	5.3kΩ min, 6.6kΩ typ, 7.9kΩ max	*	*
Unipolar Zero (All Bits OFF)	0.01% of F.S. typ, 0.05% of F.S. max	*	*
Capacitance	33pF typ	*	*
Compliance Voltage	−1.5V to +10V typ	*	*
RESOLUTION			
Binary	12 Bits	*	*
BCD	3 Digits	*	*
ACCURACY (Error Relative to Full Scale)			
Binary	±1/2LSB max	*	±1/4LSB
BCD	±1/2LSB max	*	±1/10LSB
DIFFERENTIAL NONLINEARITY	±1/2LSB max	*	*
SETTLING TIME TO 1/2LSB			
All Bits ON-to-OFF or OFF-to-ON	1.5μs typ	*	*
POWER REQUIREMENTS			
V_{CC}, +4.75 to +15.8V dc	15mA typ, 18mA max	*	*
V_{EE}, −15V dc ±5%	20mA typ, 25mA max	*	*
POWER SUPPLY GAIN SENSITIVITY			
V_{CC} @ +5V dc	2ppm of F.S./% max	*	*
V_{CC} @ +15V dc	2ppm of F.S./% max	*	*
V_{EE} @ −15V dc	6ppm of F.S./% max	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C typ	−25°C to +85°C	−55°C to +125°C
Storage	−65°C to +150°C typ	*	*
TEMPERATURE COEFFICIENT			
Unipolar Zero	1ppm of F.S./°C max	*	2ppm of F.S./°C
Bipolar Zero	4ppm of F.S./°C max	*	*
Gain	3ppm of F.S./°C max	*	*
Differential Nonlinearity	2ppm of F.S./°C	*	1ppm of F.S./°C
MONOTONICITY	Guaranteed Over Full Operating Temperature Range	*	*
EXTERNAL ADJUSTMENTS[1]			
Gain Error with Fixed 50Ω Resistor	±0.2% of F.S. typ	*	*
Bipolar Zero Error with Fixed 10Ω Resistor	±0.1% of F.S. typ	*	*
Gain Adjustment Range	±0.25% of F.S. typ	*	*
Binary Bipolar Zero Adjustments Range	±0.25% of F.S. typ	*	*
BCD Bipolar Offset Adjustment Range	±0.17% of F.S. typ	*	*
PROGRAMMABLE OUTPUT RANGES (See Figs. 1a, 1b)	0 to +5V typ	*	*
	−2.5V to +2.5V typ	*	*
	0V to +10V typ	*	*
	−5V to +5V typ	*	*
	−10V to +10V typ	*	*
REFERENCE INPUT			
Input Impedance	20kΩ typ	*	*

*Specifications same as AD562KD. **Specifications same as AD563KD. ***Specifications same as AD563JD. [1]Device calibrated with internal reference.

AD563JD/BIN AD563JD/BCD	AD563KD/BIN AD563KD/BCD	AD563SD/BIN AD563SD/BCD	AD563TD/BIN AD563TD/BCD
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	±1/4LSB	**	**
*	±1/4LSB	**	**
*	*	*	*
*	*	*	*
15mA typ, 20mA max	***	***	***
*	*	*	*
3ppm of F.S./% typ, 10ppm of F.S./% max	***	***	***
3ppm of F.S./% typ, 10ppm of F.S./% max	***	***	***
14ppm of F.S./% typ, 25ppm of F.S./% max	***	***	***
*	*	-25°C to +85°C	-55°C to +125°C
*	*	*	*
With Internal Reference			
1ppm of F.S./°C typ, 2ppm of F.S./°C max	***	***	***
10ppm of F.S./°C max	***	***	***
50ppm of F.S./°C max	20ppm of F.S./°C max	30ppm of F.S./°C max	10ppm of F.S./°C max
*	*	*	*
*	*	*	*
*	*	*	*
With Fixed 10Ω Resistor			
±0.2% of F.S. typ	***	***	***
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
5kΩ typ	***	***	***

THE AD562/AD563 OFFERS TRUE 12-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

Accuracy: Analog Devices defines accuracy as the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) *for any bit combination.* The AD563, for example, is laser trimmed to ¼LSB (0.006% of F.S.) maximum error at +25°C for K, S and T versions . . . ½LSB for the J version.

Monotonicity: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD562/AD563 are monotonic over their full operating temperature range.

Differential Nonlinearity: Monotonic behavior requires that the differential nonlinearity error be <1LSB both at 25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a one LSB change in digital input code. For example, for a 10V full-scale output, a change of one LSB in the digital input code should result in a 2.4mV change in the analog output (10V x 1/4096 = 2.4mV). If in actual use, however, a one LSB change in the input code results in a change of 1.3mV in analog output, the differential nonlinearity would be 1.1mV, or 0.011% of F.S. The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1ppm/°C) of error. The resulting error could then be as much as 0.006% + 0.01% = 0.016% of F.S. (1LSB represents 0.024% of F.S.). All versions of the AD563 are 100% tested to be monotonic over the full operating temperature range.

UNIPOLAR DAC's

STEP I . . . OUTPUT RANGE

Determine the output range required. For +10V F.S., connect the external operational amplifier output to Pin 10 and leave Pin 11 unconnected. For +5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . ZERO ADJUST

Turn all bits OFF and adjust R_1 until op amp output is 0 volts.

STEP III . . . GAIN ADJUST

Turn all bits ON for binary DAC's (bits 1, 4, 5, 8, 9 and 12 ON for BCD DAC's). Adjust R_2 until op amp output is:

BINARY	BCD
4.9988V for +5V Range	4.9950 for +5V Range
9.9976 for +10V Range	9.9900 for +10V Range

BIPOLAR DAC's

Figure 1b is a typical connection scheme for the AD563 used in bipolar operation.

STEP I . . . OUTPUT RANGE

Determine the output range required. For ±10V F.S., connect the external op amp output to Pin 11 and leave Pin 10 unconnected. For ±5V F.S., connect the external op amp output to Pin 10 and leave Pin 11 unconnected. For ±2.5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . OFFSET ADJUST

Turn all bits OFF and adjust R_3 until op amp output is:

−2.5000V for ±2.5V Range
−5.0000V for ±5V Range
−10.0000V for ±10V Range

STEP III . . . GAIN ADJUST (Bipolar Zero)

Turn bit 1 ON for Binary DAC's (bits 2 and 4 ON for BCD DAC's). Adjust R_2 until op amp output is 0 volts.

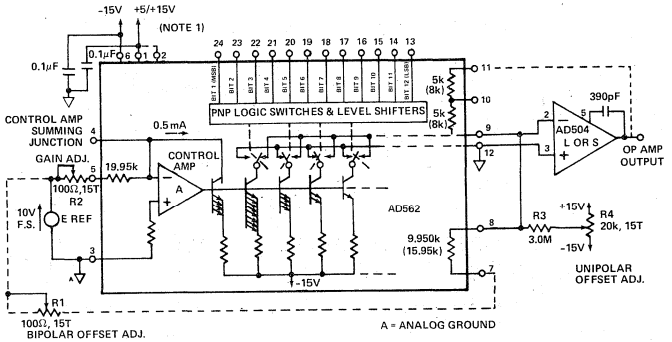
MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD563, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the switch, resistor and reference chips from hazardous environments. To further ensure reliability, the AD563 is offered with 100% screening to MIL-STD-883, method 5004.

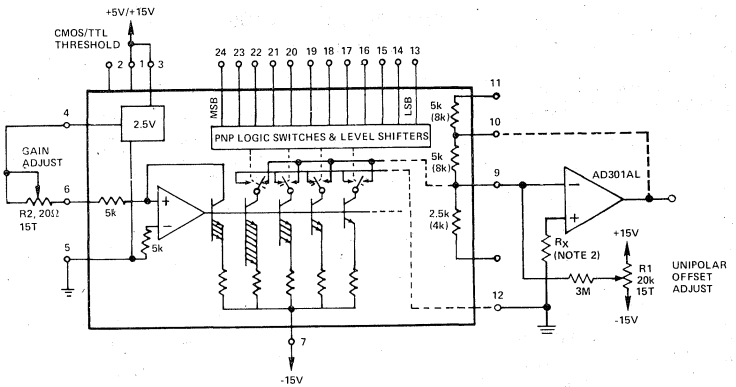
Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to these tests on a 100% basis.

TABLE I

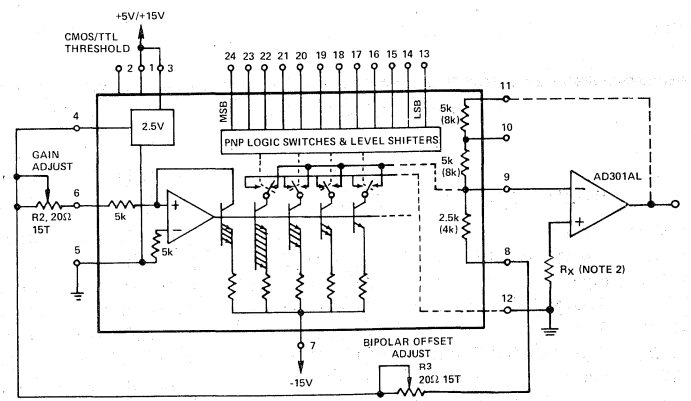
TEST	METHOD	PURPOSE
1) Internal Visual (Pre cap)	2010, Test Condition B	Removes potentially defective parts with respect to bonding, metalization, etc.
2) Stabilization Bake	Method 1008, 24 hours @ +150°C	Stabilizes circuit elements, thin film resistors.
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C	Removes potential failures due to weak wire or chip bonding.
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg	Removes potential failures due to weak wire or chip bonding.
5) Seal, Fine and Gross	Method 1014, Test Condition A and C	Verifies integrity of hermetic package.
6) Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C	Removes potential electrical failures
7) Final Electrical Tests	Performed at maximum and minimum operating temperatures	Removes any failures from the above tests and verifies electrical specifications.
8) External Visual	Method 2009	Insures physical condition of package and branding.



AD562 in Typical Unipolar and Bipolar Connection Scheme



AD563 in Typical Unipolar Connection Scheme



NOTE 1.
- A. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND LEAVE PIN 2 OPEN.
- B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.
- C. FOR HIGH VOLTAGE CMOS COMPATIBILITY, CONNECT +15 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

NOTE 2. IN UNIPOLAR OPERATION, R_X SHOULD BE MADE EQUAL TO THE PARALLEL COMBINATION OF THE INTERNAL FEEDBACK RESISTOR AND 6.6k. IN BIPOLAR, R_X EQUALS THE FEEDBACK RESISTOR IN PARALLEL WITH 1.8k.

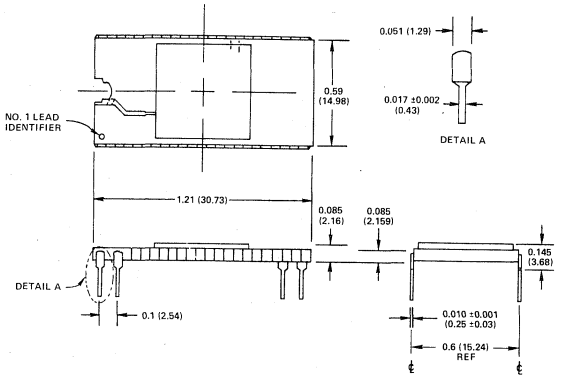
NOTE 3. RESISTOR VALUES IN PARENTHES ARE FOR BCD MODEL.

NOTE 4. SUPPLIES MAY BE BYPASSED WITH 0.1μF CAPACITORS.

AD563 in Typical Bipolar Connection Scheme

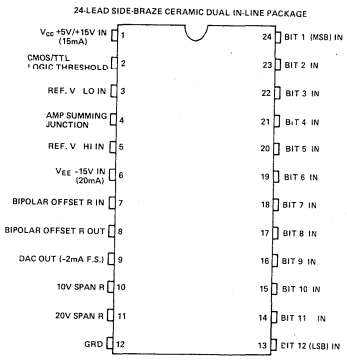
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

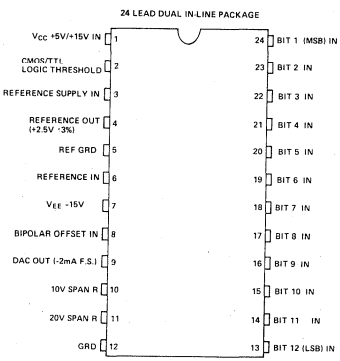


24 Lead Dual-in-Line Package

PIN CONFIGURATIONS
TOP VIEW



AD562



AD563

ORDERING GUIDE

MODEL	INPUT CODE	TEMP. RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)
AD562KD/BIN	Binary	0 to +70°C	±1/2LSB max	3ppm max
AD562KD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	3ppm max
AD562AD/BIN	Binary	-25°C to +85°C	±1/2LSB max	3ppm max
AD562AD/BCD	Binary Coded Decimal	-25°C to +85°C	±1/2LSB max	3ppm max
AD562SD/BIN	Binary	-55°C to +125°C	±1/4LSB max	3ppm max
AD562SD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/10LSB max	3ppm max
AD563J/BIN	Binary	0 to +70°C	±1/2LSB max	30ppm max
AD563J/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	30ppm max
AD563K/BIN	Binary	0 to +70°C	±1/4LSB max	20ppm max
AD563K/BCD	Binary Coded Decimal	0 to +70°C	±1/4LSB max	20ppm max
AD563S/BIN	Binary	-55°C to +125°C	±1/4LSB max	30ppm max
AD563S/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	30ppm max
AD563T/BIN	Binary	-55°C to +125°C	±1/4LSB max	10ppm max
AD563T/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	10ppm max

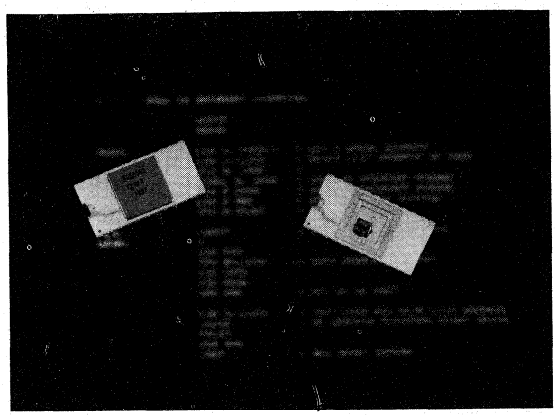
ANALOG DEVICES

Complete High Speed 12-Bit Monolithic D/A Converter

AD565

FEATURES

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 200ns
Full Scale Switching Time: 30ns
High Stability Buried Zener Reference on Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD565K, T)
Low Power: 225mW Including Reference
Pin-Out Compatible with AD563
Low Cost



PRODUCT DESCRIPTION

The AD565 is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The AD565 chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried Zener voltage reference to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD565 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565 has a 10 – 90% full scale transition time under 35 nanoseconds and settles to within ±1/2LSB in 200 nanoseconds. AD565 chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. This high speed and accuracy make the AD565 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD565 is thus well suited for wide temperature range performance with maximum linearity error ±1/2LSB and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD565 is available in four performance grades and two package types. The AD565J and K are specified for use over the 0 to 70°C temperature range and are both available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP, or a 24 pin plastic DIP. The AD565S and T grades are specified for the −55°C to +125°C range and are available in the ceramic package.

***Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.**

PRODUCT HIGHLIGHTS

1. The AD565 is a self-contained current output DAC and voltage reference fabricated on a single IC chip.
2. The device incorporates a newly developed* fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset resistors.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The pin-out of the AD565 is compatible with the industry-standard AD563 so that a system can easily be upgraded to higher speed performance without board changes.
6. The single-chip construction makes the AD565 inherently more reliable than hybrid multi-chip designs. The AD565S and T grades with guaranteed linearity and monotonicity over the −55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available fully processed to MIL-STD-883, Level B.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified)

MODEL	AD565J MIN	AD565J TYP	AD565J MAX	AD565K MIN	AD565K TYP	AD565K MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 5, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage (D Package)	-65		+150	-65		+150	°C
Storage (N Package)	-25		+100	-25		+100	°C
POWER REQUIREMENTS							
V_{CC}, +13.5 to +16.5V dc		3	5		3	5	mA
V_{EE}, -13.5 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +15V, ±10%		3	10		3	10	ppm of F.S./%
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 4,5,6)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 4)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 5)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 4)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications subject to change without notice.

MODEL	AD565S MIN	AD565S TYP	AD565S MAX	AD565T MIN	AD565T TYP	AD565T MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 5, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage (D Package)	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +13.5 to +16.5V dc		3	5		3	5	mA
V_{EE}, -13.5 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +15V, ±10%		3	10		3	10	ppm of F.S./%
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 4,5,6)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 4)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 5)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 4)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . .0V to +18V
V_{EE} to Power Ground . . . . . .0V to −18V
Voltage on DAC Output (Pin 9) . . . . . .−3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . .±12V
Bipolar Offset to Reference Ground . . . . . .±12V
10V Span R to Reference Ground . . . . . .±12V
20V Span R to Reference Ground . . . . . .±24V
Ref Out. . . . . .Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

THE AD565 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see next page) from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD565 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and T Versions—1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD565 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD565K and T have a max differential linearity error of 1/2LSB, which is a tighter specification than to simply guarantee monotonicity.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.01% (100 x 1.0ppm/°C of error). The resulting error could then be as much as 0.01% + 0.006% = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD565 are therefore 100% tested for monotonicity over the full operating temperature range.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

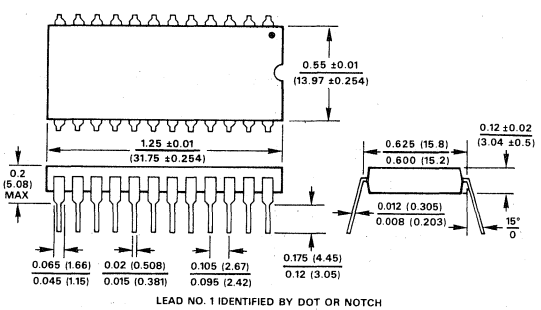


Figure 1. Molded Plastic Package (Type N) 24-Lead Dual-In-Line

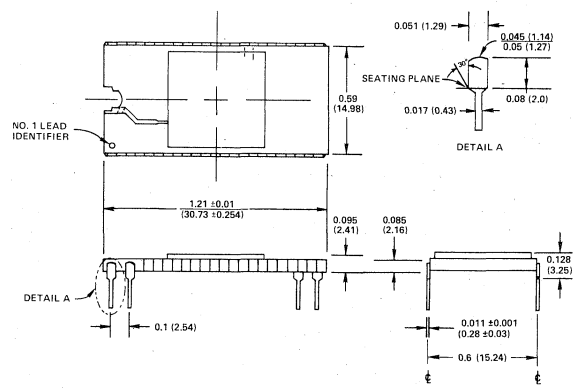


Figure 2. Hermetically-Sealed Ceramic Side-Brazed Package (Type D) 24-Lead Dual-In-Line

AD565 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	MAX GAIN T.C. (ppm of F.S./°C)
AD565JN/BIN	Plastic	0 to +70°C	±1/2LSB	30
AD565JD/BIN	Ceramic	0 to +70°C	±1/2LSB	30
AD565KN/BIN	Plastic	0 to +70°C	±1/4LSB	20
AD565KD/BIN	Ceramic	0 to +70°C	±1/4LSB	20
AD565SD/BIN	Ceramic	−55°C to +125°C	±1/2LSB	30
AD565SD/BIN/883B	Ceramic	−55°C to +125°C	±1/2LSB	30
AD565TD/BIN	Ceramic	−55°C to +125°C	±1/4LSB	15
AD565TD/BIN/883B	Ceramic	−55°C to +125°C	±1/4LSB	15

CONNECTING THE AD565 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 6. OTHER VOLTAGE RANGES

The AD565 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 6.

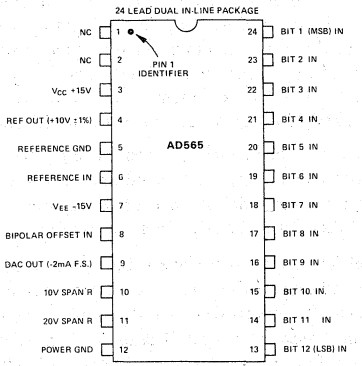


Figure 3.

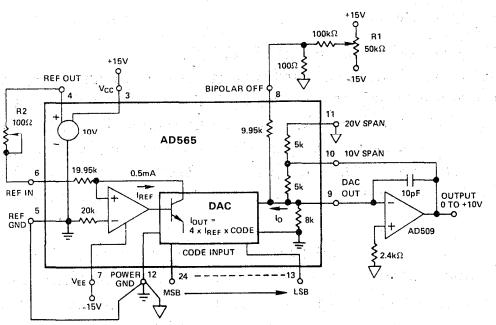


Figure 4. 0 to +10V Unipolar Voltage Output

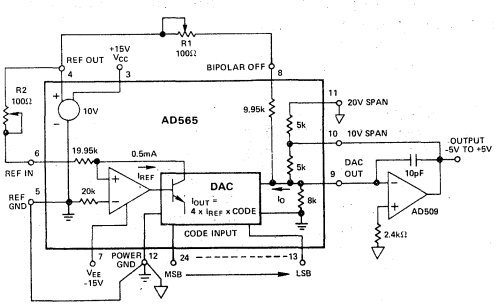


Figure 5. ±5V Bipolar Voltage Output

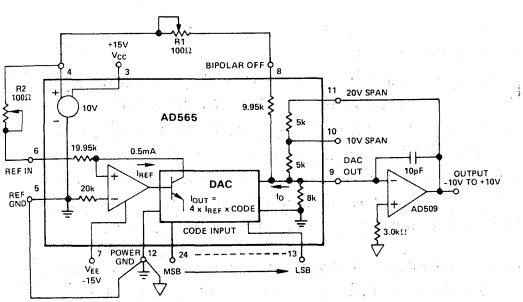


Figure 6. ±10V Voltage Output

INTERNAL/EXTERNAL REFERENCE USE

The AD565 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD565 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale and bipolar) is done in this configuration.

The AD565 can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference. For external reference applications, the AD566 series is recommended.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset, if used). A minimum of 1.5mA is available for driving external circuits. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

DIGITAL INPUT CONSIDERATIONS

The AD565 uses a standard positive true straight binary code for unipolar outputs (all 1's give full scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0's on the inputs, the output will go to negative full scale; with 100. . . 00 (only the MSB on), the output will be 0.00 volts; with all 1's, the output will go to positive full scale.

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 7. The input line can be modeled as a 30kΩ resistance connected to a -0.7V rail.

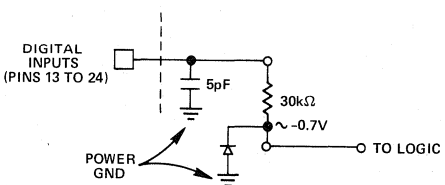


Figure 7. Equivalent Digital Input Circuit

GROUNDING RULES

The AD565 brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

The reference ground at pin 5 is the ground point for the internal reference and is thus the "high quality" ground for the AD565; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

OUTPUT VOLTAGE COMPLIANCE

The AD565 has a typical output compliance range from -2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 8.

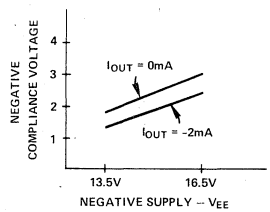


Figure 8. Typical Negative Compliance Range vs. Negative Supply

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD565, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD565 is offered with 100% screening to MIL-STD-883, method 5004, Class B.

Table 1 details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	Method 2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C min
7) Final Electrical Tests	Performed 100% to all min and max dc specifications on data pages
8) External Visual	Method 2009

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD565 are specifically designed for fast settling operation. The typical settling time to ±0.01% (1/2LSB) for the worst case transition (major carry or full scale step) is about 200ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB).

The excellent high speed performance of the AD565 is demonstrated in these oscilloscope photographs. The measurements are made with the AD565 driving directly into an equivalent 50Ω load, and amplified with a low capacitance MOS-input, UHF amplifier. Both figures show the worst case situation, which is full scale transition from switching all bits OFF to ON.

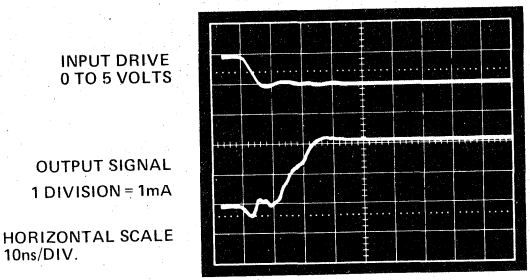


Figure 9. Full Scale Transition

The full transition characteristic is shown in Figure 9. There is about a 6-8ns delay, followed by a 10ns rise time and minimal overshoot. The transition in the other direction shows approximately a 20ns delay prior to a 10ns rise time. The slewing characteristics for smaller transitions show a similar characteristic.

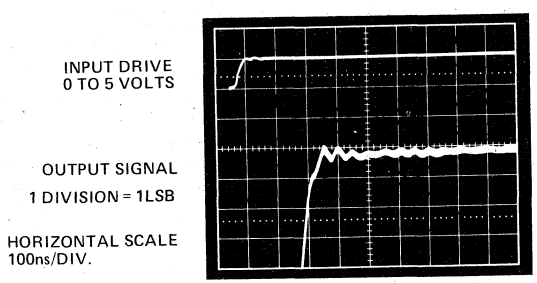


Figure 10. Settling Characteristic Detail

The fine detail of the full scale settling characteristic is shown in Figure 10. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance. The final portion of the signal slews to within 10LSB's in less than 150ns, reaches and stays within 1/2LSB in about 200ns, and shows less than 1/2LSB overshoot. The characteristic is completely settled out in less than 400ns.

HIGH SPEED SYSTEM DESIGN

Full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD565 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see the next page), or in many display applications. This form of current-to-voltage conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 11. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD565 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over 1kΩ.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits using the fast settling AD509. The circuits shown settle to ±1/2LSB in 1μs unipolar or bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1μF will be sufficient since the AD565 runs at constant supply current regardless of input code.

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 11 shows a connection using the gain and bipolar output resistors to give a ±1.60 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting R_X = 2.67kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50mV full scale swing. Settling time would be very fast, as discussed in the section above.

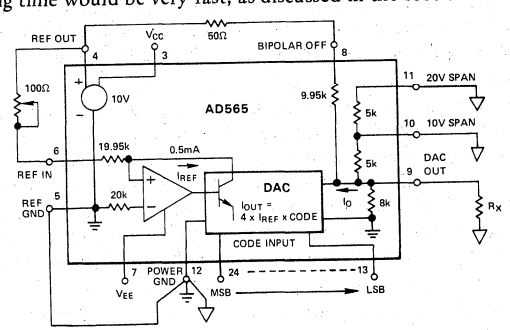


Figure 11. Unbuffered Bipolar Voltage Output

HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the AD565 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 12-bit converter system to be constructed with a minimum parts count. Shown in Figure 12 is a configuration using standard components; this system completes a full 12-bit conversion in 10μs unipolar or bipolar. This converter will be accurate to ±1/2LSB of 12 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.9976 volts, with each bit having a value of 2.44mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +1.22mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9963 volts (10 volts − 1LSB − 1/2LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0 to +4.9976 volts. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R1 for the LSB transition (all other bits "0").

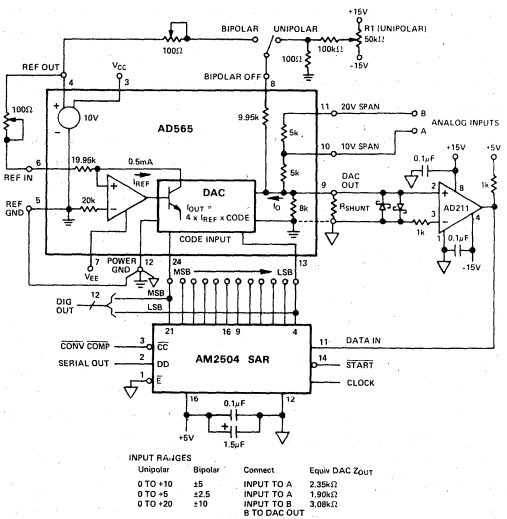


Figure 12. Fast Precision Analog to Digital Converter

Full scale is set by applying +4.9963 volts and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±1/2LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1kΩ, 1LSB = 0.5mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration, as shown in the input range table.

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the AD509 high speed op amp.

HIGH-RESOLUTION CIRCUITS

16-bit resolution digital-to-analog converters can be built by cascading an AD565 12-bit DAC with an AD559 or AD1408 8-bit DAC. This technique can be used either to provide a 16-bit binary DAC or a 4-digit BCD DAC. By using an AD565K with ±1/8LSB typical linearity to 12 bits, the total circuit will typically achieve ±1/2LSB accuracy for 14 binary bits, and ±1/2 least significant digit to 4 digits BCD. The binary configuration is shown in Figure 13. The AD559, with its thin film ladder network similar to the AD565, is preferred for good performance over temperature.

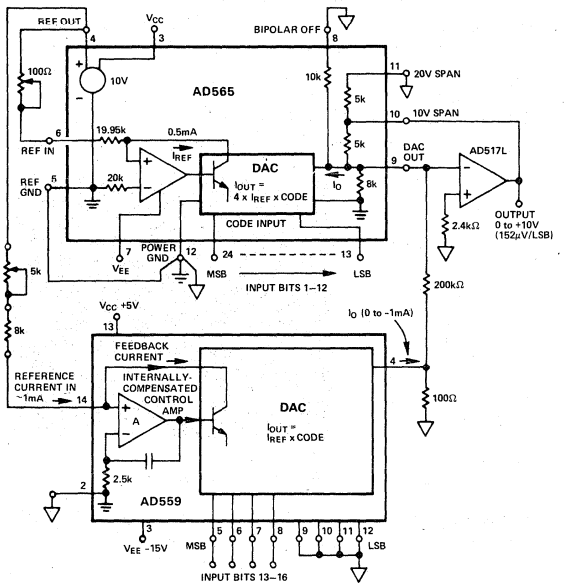


Figure 13. 16-Bit Binary DAC

COMPLEMENTARY BINARY CODE CIRCUITS

The AD565 can be used in circuits where only a complementary binary code is available. This is done by connecting the 10 volt span resistor to the 10 volt reference and connecting the DAC output to a noninverting amplifier as shown in Figure 14. The 8kΩ DAC output impedance and the 5kΩ span resistor will form a divider which will give a full scale output voltage (with all bits off) to the amplifier of about 6.15 volts. To obtain a 10 volt full scale, the amplifier is shown with a gain network back to the inverting input.

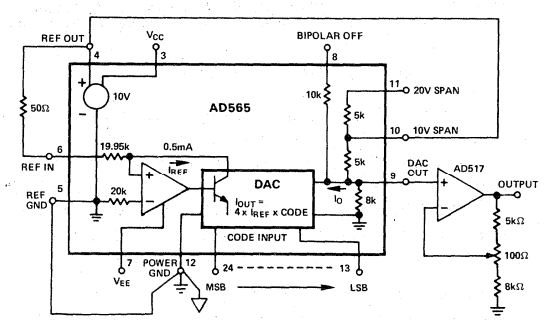


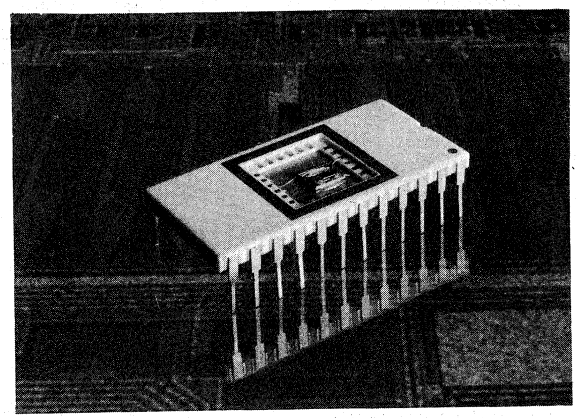
Figure 14. Complementary Output DAC

ANALOG DEVICES

Low Cost High Speed 12-Bit Monolithic D/A Converter

AD566

FEATURES
Single Chip Construction
Very High Speed: Settles to 1/2LSB in 200ns
Full Scale Switching Time: 30ns
Single Supply Operation
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD566K, T)
Low Power: 180mW
Pin-Out Compatible with AD562
Low Cost



PRODUCT DESCRIPTION

The AD566 is a fast 12-bit digital-to-analog converter which incorporates the latest advances in analog circuit design into a low power monolithic chip.

The AD566 chip uses 12 precision, high speed bipolar current steering switches, control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD566 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD566 has a 10–90% full scale transition time less than 35 nanoseconds and settles to within ±1/2LSB in 200 nanoseconds. AD566 chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD566 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The AD566 is available in four performance grades and two package types. The AD566J and K are specified for use over the 0 to +70°C temperature range and are available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP, or a 24-pin plastic DIP. The AD566S and T grades are specified for the −55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. The combination of single supply operation with wide output compliance range is idealy suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The device incorporates a newly developed*, fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The chip also contains SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
4. The pin-out of the AD566 is compatible with the industry-standard AD562 so that a system can easily be upgraded to provide higher speed performance.
5. The single-chip construction makes the AD566 inherently more reliable than hybrid multi-chip designs. The AD566S and T grades, with guaranteed linearity and monotonicity over the −55°C to +125°C range, are especially recommended for high reliability needs in harsh environments. These units are available fully processed to MIL-STD-883, Level B.

***Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.**

SPECIFICATIONS (T_A = +25°C, V_{EE} = -15V, unless otherwise specified)

MODEL	AD566J MIN	AD566J TYP	AD566J MAX	AD566K MIN	AD566K TYP	AD566K MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 5)		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 6 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -13.5 to -16.5V dc		-12	-20		-12	-20	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 5, 6, 7)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 5)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 6)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 5)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		+1V to +10V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage					
Reference Feedthrough (unipolar mode, all bits OFF, and 0 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%-90%		5mA/μs					
90%-10%		1mA/μs					
Output Settling Time (all bits on and a 0-10V step change in reference voltage)		1.5μs to 0.01% F.S.					
CONTROL AMPLIFIER							
Full Power Bandwidth		300kHz					
Small-Signal Closed-Loop Bandwidth		1.8MHz					

Specifications subject to change without notice.

MODEL	AD566S MIN	AD566S TYP	AD566S MAX	AD566T MIN	AD566T TYP	AD566T MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 5)		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 6 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -13.5 to -16.5V dc		-12	-20		-12	-20	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 5, 6, 7)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 5)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 6)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 5)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 0 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%-90%	5mA/μs
90%-10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.

CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

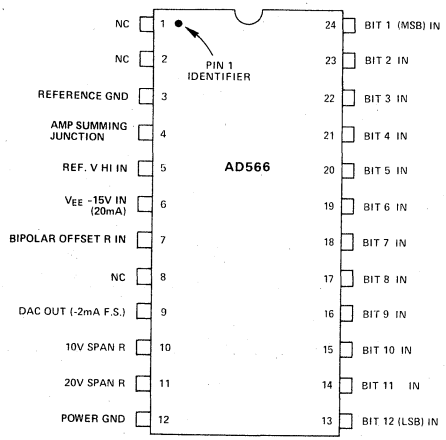
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Power Ground . . . . . 0V to −18V
Voltage on DAC Output (Pin 9) . . . . . −3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Power Dissipation 1000mW

PIN CONFIGURATION

TOP VIEW



MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmos in electronic circuits. The AD566, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD566 is offered with 100% screening to MIL-STD-883, method 5004.

Table 1 details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	Method 2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C min
7) Final Electrical Tests	Performed 100% to all min and max dc specifications on data pages.
8) External Visual	Method 2009

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

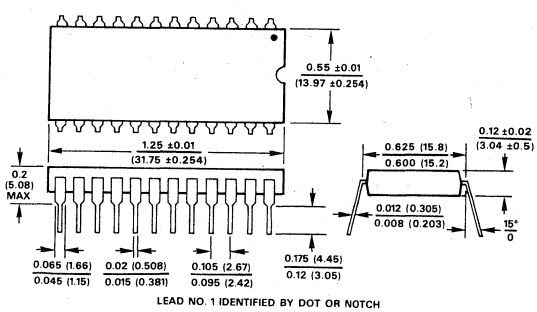


Figure 1. Molded Plastic Package (Type N) 24-Lead Dual-In-Line

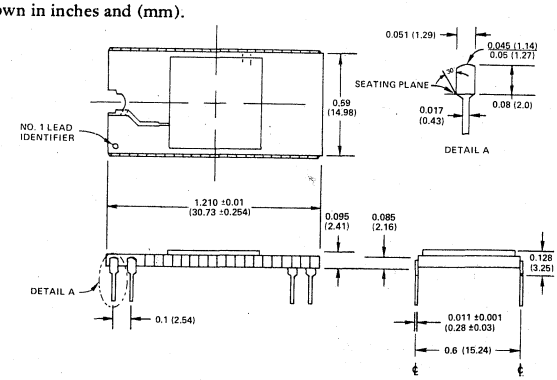


Figure 2. Hermetically-Sealed Ceramic Side-Brazed Package (Type D) 24-Lead Dual-In-Line

AD566 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	MAX GAIN T.C. (ppm of F.S./°C)
AD566JN/BIN	Plastic	0 to +70°C	±1/2LSB	10
AD566JD/BIN	Ceramic	0 to +70°C	±1/2LSB	10
AD566KN/BIN	Plastic	0 to +70°C	±1/4LSB	3
AD566KD/BIN	Ceramic	0 to +70°C	±1/4LSB	3
AD566SD/BIN	Ceramic	-55°C to +125°C	±1/2LSB	10
AD566SD/BIN/883B	Ceramic	-55°C to +125°C	±1/2LSB	10
AD566TD/BIN	Ceramic	-55°C to +125°C	±1/4LSB	3
AD566TD/BIN/883B	Ceramic	-55°C to +125°C	±1/4LSB	3

THE AD566 OFFERS TRUE 12-BIT PERFORMANCE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see the next page) from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD566 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T version and to 1/2LSB for the J and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD566 are monotonic over their entire operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, if a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be 1.83mV, or 3/4LSB. The AD566K and T have a max differential linearity error of 1/2LSB, which is a tighter specification than simply guaranteed monotonicity.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 3.

The input reference current to the DAC, I_{REF}, is developed from the external reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC} which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

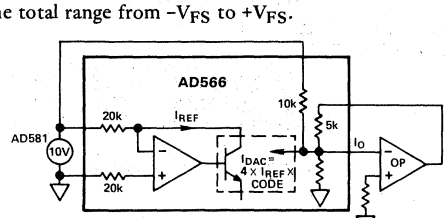


Figure 3. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ±1/2LSB max and the differential linearity error of ±3/4LSB max guarantee monotonic performance over the range of −55°C to +125°C. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of 2ppm/°C max (which comes from leakage currents) causes a linear shift in the transfer curve as shown in Figure 4. The gain drift causes a change in the slope of the curve which results from reference drift and the device gain drift. The device gain drift is the DAC drift and drift in R_{GAIN} relative to the DAC resistors for a total of 3ppm/°C max (AD566K, T). Total absolute error due to all of these effects is guaranteed to be less than ±0.05% of full scale from −55°C to +125°C.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to V_{REF} (see Figure 3) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 4. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD566 this error is held to 10ppm max. The total of all these errors is held to ±0.15% of full scale from −55°C to +125°C (AD566T). Note that, in the bipolar ranges, full scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

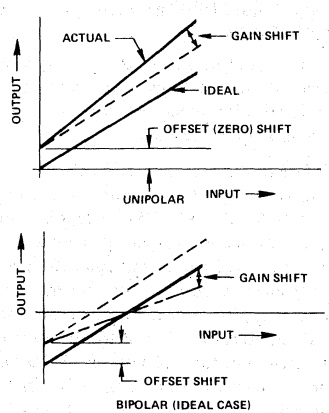


Figure 4. Unipolar and Bipolar Drifts

CONNECTING THE AD566 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 5 UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 6. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 7. OTHER VOLTAGE RANGES

The AD566 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or +2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 7.

DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*
000000000000		Zero	-Full Scale	Zero
011111111111		Mid Scale -1LSB	FS -1LSB	+FS -1LSB
100000000000		+1/2 FS	Zero	-FS
111111111111		+FS -1LSB	+ Full Scale -1LSB	+FS -1LSB

*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

Table 2. Digital Input Codes

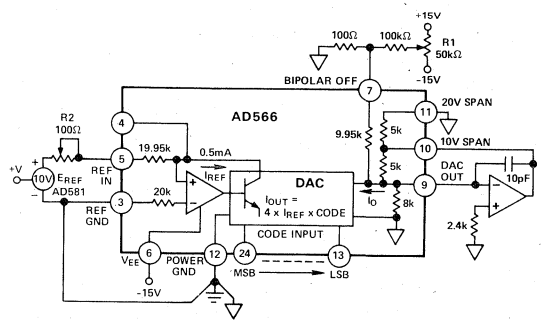


Figure 5. 0 to +10V Unipolar Voltage Output

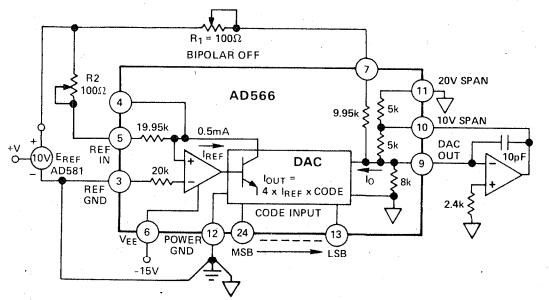
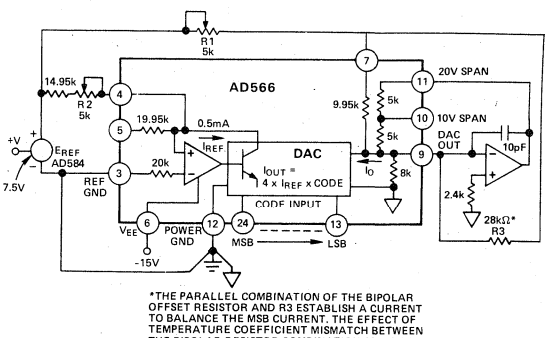


Figure 6. ±5V Bipolar Voltage Output



*THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE.

Figure 7. ±10V Voltage Output

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 2.0 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 8. The input line can be modelled as a 30kΩ resistance connected to a –0.7V rail.

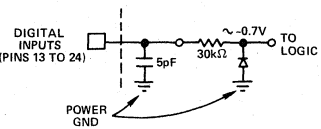


Figure 8. Equivalent Digital Input Circuit

GROUNDING RULES

The AD566 brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds must be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize the current flow in low-level signal paths. In this way, logic gate return currents are not summed into the same return path with analog signals.

The reference ground at pin 3 is the ground point for the internal reference and is thus the "high quality" ground for the AD566; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground point; analog power return is preferred. If the power ground contains high frequency noise in excess of 200mV; this noise may feed through to the output of the converter, thus some caution is required in applying these grounds.

OUTPUT VOLTAGE COMPLIANCE

The AD566 has a typical output compliance range of –2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8kΩ in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are a function of output current and negative supply, as shown in Figure 9.

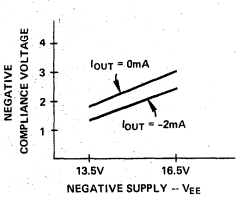


Figure 9. Typical Neg. Compliance Range vs. Neg. Supply

HIGH SPEED SYSTEM DESIGN

Full realization of the AD566 high speed capabilities requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD566 is specified for the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. With proper design this form of current-to-voltage conversion can give very fast operation. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 10. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD566 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over 1kΩ.

If an op amp is used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits, based on the fast settling AD509 are shown in the applications circuits on Performance page. The unipolar or bipolar circuits shown settle to ±1/2LSB in 1μs. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. The supply should be bypassed near the device; 0.1μF will be sufficient since the AD566 runs at constant supply current regardless of input code. Output capacitance effects can be minimized by grounding pin 11 in 10V span applications.

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 10 shows a connection using the gain and bipolar output resistors to give a ±1.60 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting R_X = 2.67kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. A 50Ω R_X resistor drives a 50Ω cable with a ±50mV full scale swing; settling time is very fast as discussed in the section above.

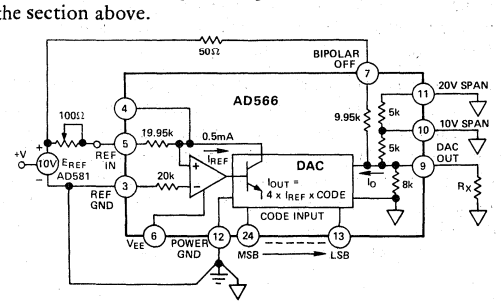


Figure 10. Unbuffered Bipolar Voltage Output

MICROPROCESSOR CONTROL FOR A 12-BIT DAC

A common I/O interface is the Digital-to-Analog Converter output, which provides a voltage corresponding to a data word from a microprocessor.

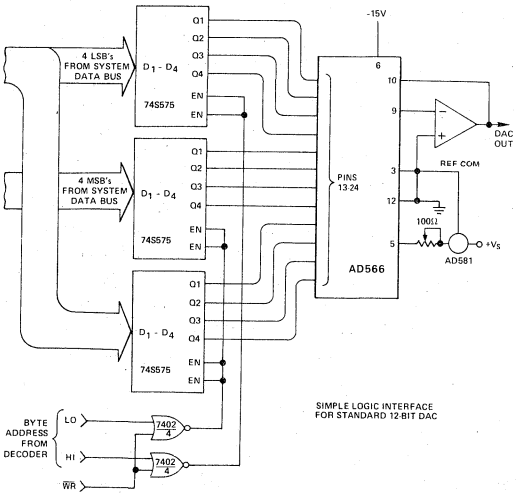


Figure 11.

Interfacing is more complex when the DAC needs more bits of resolution than the system data bus can carry in 1 byte. For example, applications using an 8-bit microprocessor to drive a 12-bit DAC are common. Several hardware formats are possible; the most convenient one depends on the desired data format. If the least significant 8 bits are in one byte of memory, they can be transferred into an 8-bit latch in one memory-or I/O-write cycle. An adjacent cycle can be used to transfer the 4 least-significant bits of another data word into a latch controlling the 4 most-significant bits of the DAC. The least-significant bits of the data bus drive two 4-bit latches which are controlled by two separate addresses. The Hi Byte address allows the microprocessor to write in the 4 most significant data bits and the Lo Byte address allows the microprocessor to write in the 8 remaining bits. When all 12 bits are latched, the DAC output will assume its proper new value. An intermediate value will be momentarily present at the DAC terminals between Hi and Lo Byte write cycles. For applications such as CRT displays where this intermediate value cannot be tolerated, double buffering can be effectively employed. This could be implemented with a separately-controlled 12-bit latch at the DAC inputs.

D/A CONVERTERS IN DISPLAYS

In Figure 12, a counter-driven AD566 is shown as a sawtooth sweep generator. When used for displays, this scheme provides a highly-repeatable, controllable linear sweep.

Raster displays are usually generated by a fast horizontal scan and a slower vertical scan which is derived from the horizontal scan. Intensity modulation during each horizontal scan provides the pictorial information. The picture resolution is expressed in terms of the number of discernible data points per line multiplied by the number of lines. The minimum frame period is the time allowed for the horizontal scan-plus-retrace multiplied by the number of lines, plus vertical retrace time.

A family of monolithic D/A converters is available from Analog Devices that are suitable for vertical sweeps. The line-spacing uniformity depends on linearity while maximum number of lines depends on DAC resolution. A display of 1024 lines would require 10 bits of resolution and 12 bits of linearity (0.012% of linearity provides less than 12% of spacing error). Switching transients created within the vertical sweep DAC are blanked because they occur during the horizontal retrace interval.

For horizontal sweeps, the DAC requirements are more severe. For example, to resolve 500 points per line, at 500 lines per frame, at a 30Hz frame rate, requires that each digital horizontal step settle within 100ns (typical full scale settling time is 200ns), and that there be no "glitches". Even if the display is blanked between horizontal steps, large glitches at major carries can cause deflection-amplifier transients, which distort the pattern.

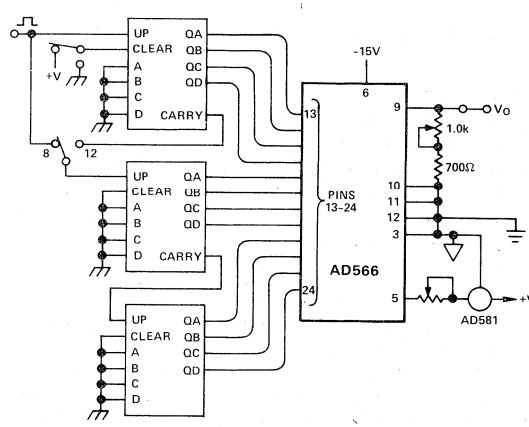


Figure 12.

The excellent high speed performance of the AD566 is demonstrated in the oscilloscope photograph of Figure 13. This measurement is made with the AD566 driving directly into an equivalent 50Ω load, amplified with a low capacitance MOS-input, UHF amplifier. The figure shows the worst case situation, which is full scale transition from switching all bits OFF to ON. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance.

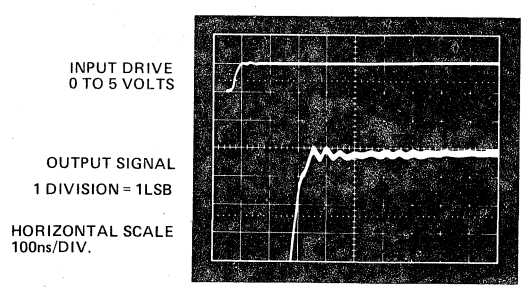


Figure 13. Settling Characteristic Detail

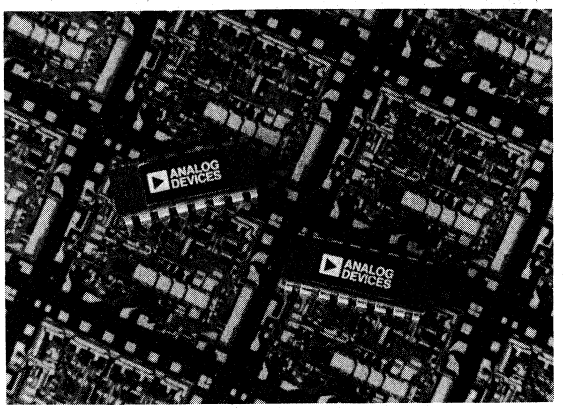
ANALOG DEVICES

8-Bit Monolithic Multiplying D/A Converter

AD1408/AD1508

FEATURES

- Improved Replacement for Industry Standard 1408/1508
- Improved Settling Time: 250ns typ
- Improved Linearity: ±0.1% Accuracy Guaranteed Over Temperature Range (-9 Grade)
- High Output Voltage Compliance: +0.5V to -5.0V
- Low Power Consumption: 157mW typ
- High Speed 2-Quadrant Multiplying Input: 4.0mA/μs Slew Rate
- Single Chip Monolithic Construction
- Hermetic 16-Pin Ceramic DIP
- Low Cost



PRODUCT DESCRIPTION

The AD1408 and AD1508 are low cost monolithic integrated circuit 8-bit multiplying digital-to-analog converters, consisting of matched bipolar switches, a precision resistor network and a control amplifier. The single chip is mounted in a hermetically sealed ceramic 16 lead dual-in-line package.

Advanced circuit design and precision processing techniques result in significant performance advantages over older industry standard 1408/1508 devices. The maximum linearity error over the specified operating temperature range is guaranteed to be less than ±¼LSB (-9 grade) while settling time to ±½LSB is reduced to 250ns typ. The temperature coefficient of gain is typically 20ppm/°C and monotonicity is guaranteed over the entire operating temperature range.

The AD1408/AD1508 is recommended for all low-cost 8-bit DAC requirements; it is also suitable for upgrading overall performance where older, less accurate and slower 1408/1508 devices have been designed in. The AD1408 series is specified for operation over the 0 to +75°C temperature range, the AD1508 series for operation over the entire military temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monolithic IC construction makes the AD1408/AD1508 an optimum choice for applications where low cost is a major consideration.
2. The AD1408/AD1508 directly replaces other devices of this type.
3. Versatile design configuration allows voltage or current outputs, variable or fixed reference inputs, CMOS or TTL logic compatibility and a wide choice of accuracy and temperature range specifications.
4. Accuracies within ±¼LSB allow performance improvement of older applications without redesign.
5. Faster settling time (250ns typ) permits use in higher speed applications.
6. Low power consumption improves stability and reduces warm-up time.
7. The AD1408/AD1508 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, a fixed reference is used.
8. The AD1408/AD1508 is available in chip form; please consult factory for details.
9. The device is packaged in a hermetically-sealed ceramic 16 lead dual-in-line package. Processing to MIL-STD-883 level B is available.

SPECIFICATIONS (typical @ +25°C and V_{CC} = +5.0V dc, V_{EE} = -15V dc unless otherwise noted)

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
POWER SUPPLY VOLTAGE	V_{CC}	+5.5	V dc
	V_{EE}	-16.5	V dc
DIGITAL INPUT VOLTAGE	V_5 thru V_{12}	+5.5, 0	V dc
APPLIED OUTPUT VOLTAGE	V_0	+0.5, -5.2	V dc
REFERENCE CURRENT	I_{14}	5.0	mA
REFERENCE AMPLIFIER INPUTS	V_{14}, V_{15}	V_{CC}, V_{EE}	V dc
POWER DISSIPATION			
(Package Limitation)		1000	mW
Derate above T_A = +25°C	P_D	6.7	mW/°C
OPERATING TEMPERATURE RANGE			
AD1408 Series	T_A	0 to +75	°C
AD1508 Series	T_A	-55 to +125	°C
STORAGE TEMPERATURE RANGE	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V dc, V_{EE} = -15V dc, $\frac{V_{REF}}{R14}$ = 2.0mA, **AD1508 Series:** T_A = -55°C to +125°C
AD1408 Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
RELATIVE ACCURACY					
(Error Relative to Full Scale I_O)					
AD1508-9, AD1408-9	E_r	–	–	±0.10	%
AD1508-8, AD1408-8	E_r	–	–	±0.19	%
AD1408-7	E_r	–	–	±0.39	%
SETTLING TIME					
to Within 1/2LSB [Includes t_{PLH}]					
(T_A = +25°C)	t_S	–	250	–	ns
PROPAGATION DELAY TIME					
T_A = +25°C	t_{PLH}, t_{PHL}	–	30	100	ns
OUTPUT FULL SCALE CURRENT DRIFT	TCI_O	–	-20	–	ppm/°C
DIGITAL INPUT LOGIC LEVELS (MSB)					
High Level, Logic "1"	V_{IH}	2.0	–	–	V dc
Low Level, Logic "0"	V_{IL}	–	–	0.8	V dc
DIGITAL INPUT CURRENT (MSB)					
High Level, V_{IN} = 5.0V	I_{IH}	–	0	0.04	mA
Low Level, V_{IL} = 0.8V	I_{IL}	–	-0.4	-0.8	mA
REFERENCE INPUT BIAS CURRENT					
(Pin 15)	I_{15}	–	-1.0	-3.0	μA
OUTPUT CURRENT RANGE					
V_{EE} = -5.0V	I_{OR}	0	2.0	2.1	mA
V_{EE} = -6.0V to -15V	I_{OR}	0	2.0	4.2	mA
OUTPUT CURRENT					
V_{REF} = 2.000V, R14 = 1000Ω	I_O	1.9	1.99	2.1	mA
OUTPUT CURRENT					
(All Bits Low)	I_O (min)	–	0	4.0	μA
OUTPUT VOLTAGE COMPLIANCE					
($E_I \leq$ 0.19% at T_A = +25°C)					
V_{EE} = -5V	V_O	–	–	-0.6, +0.5	V dc
V_{EE} below -10V	V_O	–	–	-5.0, +0.5	V dc
REFERENCE CURRENT SLEW RATE	SRI_{REF}	–	4.0	–	mA/μs
OUTPUT CURRENT POWER SUPPLY					
SENSITIVITY	$PSSI_O$	–	0.5	2.7	μA/V
POWER SUPPLY CURRENT					
(All Bits Low)	I_{CC}	–	+9	+14	mA
	I_{EE}	–	-7.5	-13	mA
POWER SUPPLY VOLTAGE RANGE					
(T_A = +25°C)	V_{CCR}	+4.5	+5.0	+5.5	V dc
	V_{EER}	-4.5	-15	-16.5	V dc
POWER DISSIPATION					
All Bits Low					
V_{EE} = -5.0V dc	P_D	–	82	135	mW
V_{EE} = -15V dc	P_D	–	157	265	mW
All Bits High					
V_{EE} = -5.0V dc	P_D	–	70	–	mW
V_{EE} = -15V dc	P_D	–	132	–	mW

Specifications subject to change without notice.

APPLYING THE AD1408/1508

Reference Amplifier Drive and Compensation

Figures 2a and 2b are the connection diagrams for using the AD1408/AD1508 in basic voltage output modes. In Figure 2a, a positive reference voltage, V_{REF}, is converted to a current by resistor R14. This reference current determines the scale factor for the output current such that the full scale output is 1LSB (1/256) less than the reference current. R15 provides bias current compensation to the reference control amplifier to minimize temperature drift; it is nominally equal to R14 although it needn't be a stable precision resistor. This configuration develops a negative output voltage across R_L and requires a positive V_{REF}.

If a negative V_{REF} is to be used, connections to the reference control amplifier must be reversed as shown in Figure 2b. This circuit also delivers a negative output voltage, but presents a high impedance to the reference source. The negative V_{REF} must be at least 4 volts above the V_{EE} supply.

Two quadrant multiplication may be performed by applying a bipolar ac signal as the reference as long as pin 14 is positive relative to pin 15 (reference current must flow into pin 14). If the ac reference is applied to pin 14 through R14, a negative voltage equal to the negative peak of the ac reference must be applied through R15 to pin 15; if the ac reference is applied to pin 15 through R15, a positive voltage equal to the positive peak of the ac reference must be applied through R14 to pin 14.

When a dc reference is used, capacitive bypass from reference to ground will improve noise rejection.

The compensation capacitor, C, provides proper phase margin for the reference control amplifier. As R14 is increased, the closed-loop gain of the amplifier is decreased, therefore C must be increased. For R14 = 1.0kΩ, 2.5kΩ and 5.0kΩ, minimum values of capacitance are 15pF, 37pF and 75pF respectively. C may be tied to either V_{EE} or ground, but tying it to V_{EE} increases negative supply noise rejection. If the reference is driven by a high-impedance current source, heavy compensation of the amplifier is required; this causes a reduction in overall bandwidth.

Output Current Range

The nominal value for output current range is 0 to 1.992mA as determined by a 2mA reference current. If V_{EE} is more negative than -7.0 volts, this range may be increased to a maximum of 0 to 4.2mA. An increase in speed may be realized at increased output current levels, but power consumption will increase, possibly causing small shifts in linearity.

Pin 1, range control, may be grounded or unconnected. Although other older devices of this type require different terminations for various applications, the AD1408/AD1508 compensates automatically. This pin is not connected internally, therefore any previously installed connections will be tolerated.

Output Voltage Range

The voltage on pin 4 is restricted to a +0.5 to -0.6 volt range when V_{EE} = -5V. When V_{EE} is more negative than -10 volts, this range is extended to +0.5 to -5.0 volts. If the current into pin 14 is 2mA (full-scale output current = 1.992mA), a 2.5kΩ resistor between the output, pin 4, and ground will provide a 0 to -4.980 volt full-scale. If R_L exceeds 500Ω however, the settling time of the device is increased.

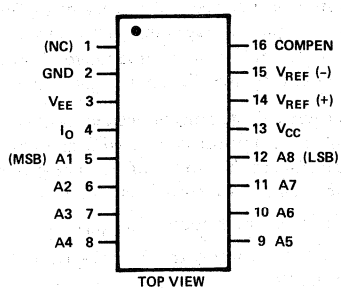
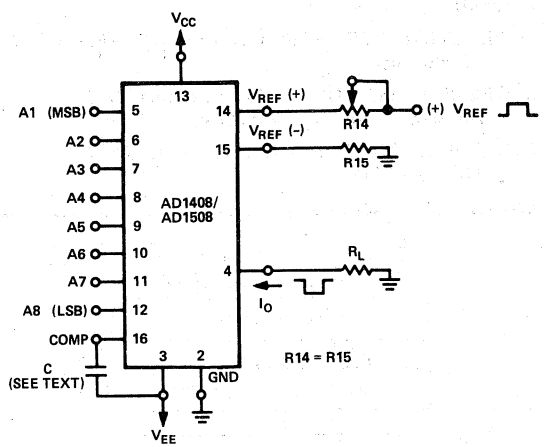
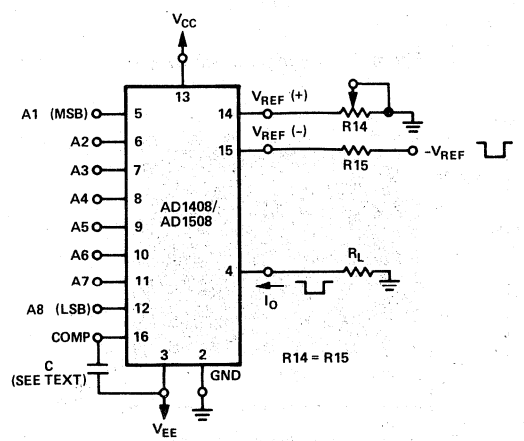


Figure 1. Pin Connections



a. Connections for Use with Positive Reference



b. Connections for Use with Negative Reference

Figure 2. Basic Connections

Voltage Output

A low impedance voltage output may be derived from the output current of the AD1408/AD1508 by using an output amplifier as shown in Figure 3. The output current I_O flows in R_O to create a positive-going voltage range at the output of amplifier A1. R_O may be chosen for the desired range of output voltage; the complete circuit transfer function is given in Figure 3.

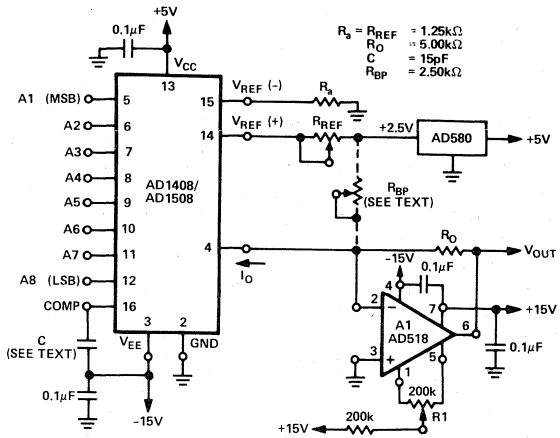
If a bipolar output voltage range is desired, R_{BP}, shown dotted, must be installed. Its purpose is to provide an offset equal to one-half of full-scale at the output of A1. The procedure for calibrating the circuit of Figure 3 is as follows:

Calibration for Unipolar Outputs (No R_{BP})

1. With all bits "OFF", adjust the A1 null-pot, R1, for V_{OUT} = 0.00V.
2. With all bits "ON", adjust R_{REF} for V_{OUT} = (Nominal Full Scale) − 1LSB = +9.961 volts

Calibration for Bipolar Outputs (R_{BP} installed, R1 not required)

1. With all bits "OFF", adjust R_{BP} for V_{OUT} = -F.S. = -5.000 volts
2. With Bit 1 (MSB) "ON", and all other Bits "OFF", adjust R_{REF} for V_{OUT} = 0.000V.
3. With all bits "ON", verify that E_{OUT} = +5.000V− 1LSB = 4.961V.



$$V_{OUT} = \frac{V_{REF}}{R_{REF}}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

ADJUST V_{REF}, R_{REF} OR R_O SO THAT WITH ALL DIGITAL INPUTS AT LOGIC "1", V_{OUT} = 9.961 VOLTS:

$$V_{OUT} = \frac{2.5}{1.25k\Omega}(5k\Omega)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right] = 9.961 \text{ VOLTS}$$

Figure 3. Typical Connection Diagram, AD1408/AD1508, Voltage Output, Fixed Reference

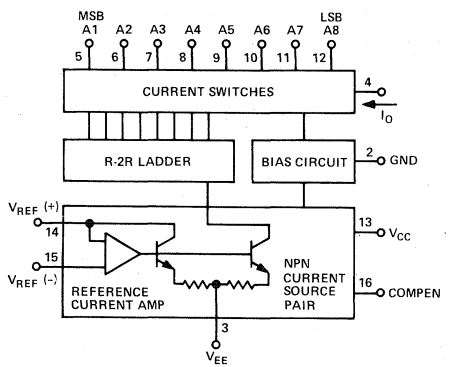
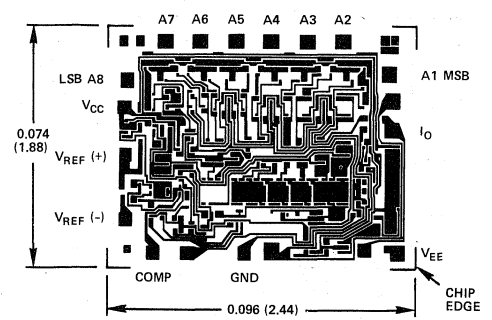


Figure 4. Simplified Block Diagram



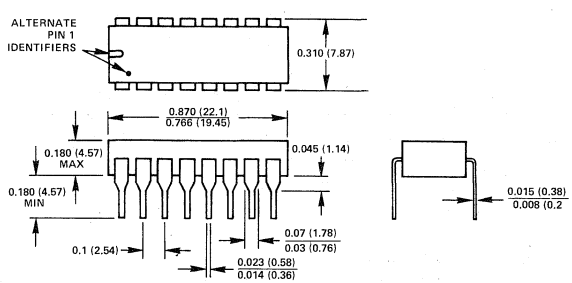
THE AD1408/AD1508 IS AVAILABLE IN CHIP FORM; CONSULT CHIP CATALOG FOR APPLICATION DETAILS.

Figure 5. Chip Dimensions and Pad Layout. Dimensions shown in inches and (mm).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN DUAL-IN-LINE



AD1408/AD1508 ORDERING GUIDE

MODEL	ACCURACY (±% F.S.)	TEMP. RANGE (°C)
AD1408-7D	0.39	0 to +75
AD1408-8D	0.19	0 to +75
AD1408-9D	0.10	0 to +75
AD1508-8D	0.19	-55 to +125
AD1508-9D	0.10	-55 to +125
AD1508-8D/883B	0.19	-55 to +125
AD1508-9D/883B	0.10	-55 to +125

ANALOG DEVICES

CMOS
Digitally Controlled Audio Attenuator
AD7110 *

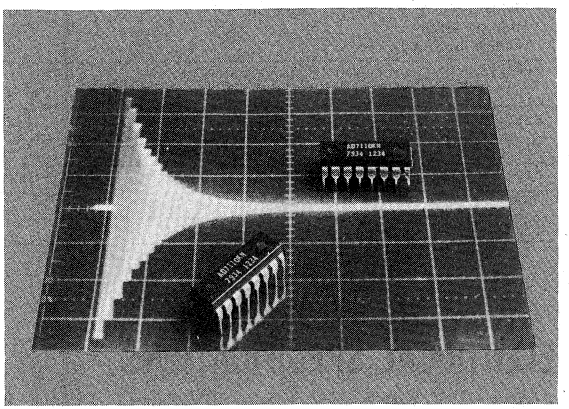
PRELIMINARY TECHNICAL DATA

FEATURES

Attenuation Range: 0 to 88.5dB Plus Full Muting
Resolution: 1.5dB
Low Distortion: THD Better Than -98dB
IMD Better Than -92dB
Includes Switches for Loudness Compensation
Low Power Consumption
Excellent S/N Ratio: 100dB (20Hz – 20kHz)
Low Cost
Complies with DIN 45403 and DIN 45405
Latch-Proof Operation

APPLICATIONS

Digitally Controlled Audio Gain
Wide Dynamic Range D/A Converters

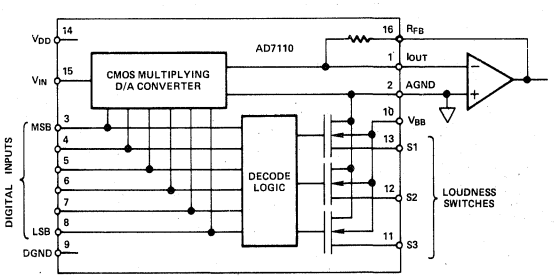


GENERAL DESCRIPTION

The AD7110 is a monolithic CMOS digitally controlled audio attenuator (patent pending). With the addition of an external operational amplifier it provides 0 to 88.5dB of attenuation in 1.5dB steps, plus full muting of the audio input signal for digital input code 1111XX, where X can be 1 or 0. The audio input is applied to the V_{IN} pin and the device delivers a logarithmically related output current which is determined by a 6-bit binary input code. Loudness compensation switches are provided on the device to enable additional bass boost at low volume settings.

The device is manufactured using an advanced thin-film on CMOS monolithic wafer fabrication process and is packaged in a 16-pin DIP.

FUNCTIONAL DIAGRAM

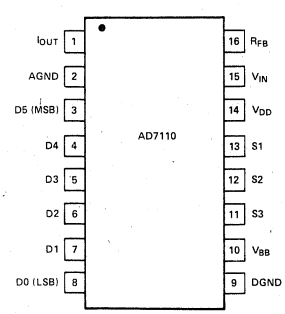


AD7110 AUDIO ATTENUATOR

ORDERING INFORMATION

Model	Package	Operating Temperature Range
AD7110KN	16-Pin Plastic Dip	0 to +50°C

PIN CONFIGURATION



*PATENT PENDING

AUDIO SPECIFICATIONS

(V_{DD} = +5 to +12V, V_{BB} = 0 to -12V, Pins 11–13 Open, T_A = 0 to +50°C unless otherwise noted)

PARAMETER	AD7110 WITH "IDEAL OP AMP"	AD7110 WITH TL071 OP-AMP (FIG. 1)	UNITS	TEST CONDITIONS/COMMENTS
ATTENUATION RANGE	0 to -88.5	0 to -88.5	dB	V_{IN} = 10V rms @ 1kHz
RESOLUTION	1.5 max	1.5 max	dB	Frequency Range: 20Hz to 20kHz
ATTENUATION ACCURACY (Absolute) 0dB to -48dB -48dB to -88.5dB	 ±0.7 max Monotonic	 ±0.7 max Monotonic	 dB	The AD7110 is guaranteed monotonic for all attenuation settings between 0 and -88.5dB
TOTAL HARMONIC DISTORTION (THD)	-98 max	-85 typ	dB	per DIN 45403, BLATT 2 (with input level of 1V rms)
INTERMODULATION DISTORTION (IMD)	-92 max	-79 typ	dB	per DIN 45403, BLATT 4
V_{IN}	30 max	10 max	V peak	for <1% (max) THD (Note 1)
FEEDTHROUGH ERROR	Better than -85dB @ 1kHz. Feedthrough is primarily dependent upon printed circuit board layout.			
OUTPUT NOISE VOLTAGE DENSITY	30 max	70 typ	nV/√Hz	20Hz to 20kHz (Note 2)
BANDWIDTH	D.C. to 150 min	D.C. to 250 typ	kHz	0dB Attenuation

ELECTRICAL SPECIFICATIONS

(V_{DD} = +12V, V_{BB} = -12V, V_{IN} = -10V, Pins 11–13 open, T_A = 0 to +50°C unless otherwise noted)

PARAMETER	LIMIT	TEST CONDITIONS/COMMENTS
ANALOG INPUT		Input resistance for a given unit is constant for all input conditions.
Input Resistance of V_{IN} (pin 15)	18kΩ max 9kΩ min	 V_{OUT} = 0V
LOUDNESS SWITCHES		
Switch ON Resistance R_{ON}	 600Ω max	 Switch Current = 1mA
Switch OFF Leakage Current	1μA max	V_{switch} = +12V
Switch Coding	See Table 1	
DIGITAL INPUTS		
V_{INH}	11.5V min	
V_{INL}	0.5V max	
I_{INH}	1μA max	
I_{INL}	1μA max	
C_{IN}	5pF typ	
POWER REQUIREMENTS		
V_{DD}	+12V nom	
V_{BB}	-12V nom	
I_{DD}	1mA max	Digital Inputs = V_{INL} or V_{INH}
I_{BB}	100μA max	
Total Power Dissipation	5mW typ	

NOTES:
[1] Output amplifier (and, amplifier supplies) must be capable of 30V peak output.
[2] Output noise voltage density includes op amp noise.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

*V_{DD} (to GND)	+14V
*V_{BB} (to GND)	-14V
Voltage (pins 11, 12, 13) to GND	V_{BB}, +14V
V_{IN} (to GND)	±35V
Digital Input Voltage to GND	-0.3V to V_{DD}
Output Voltage (Pin 1) to GND	-100mV to VDD
Power Dissipation (Package)	670mW
Operating Temperature	0 to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

*If Loudness Compensation Switches (S1, S2, S3) are not used, the negative power supply may be omitted and V_{BB} (Pin 10) connected instead to DGND (Pin 9). In this case the absolute maximum rating of V_{DD} is +17V.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent binary codes. The AD7110 resolution is 1.5dB.

MONOTONICITY: The AD7110 digitally controlled audio attenuator is monotonic if the analog output decreases (or remains constant) as the digital input code (attenuation setting) increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when the digital input code is set to mute the input signal.

ANALOG CIRCUIT PERFORMANCE:

Table I gives the nominal attenuation in dB for the AD7110 for all digital input codes. It also shows the Loudness Switch states and the nominal output voltage when using an external operational amplifier (as shown in Figure 1) and a fixed -10 volt reference applied to V_{IN} (pin 15). It may be seen that the transfer function for the circuit of Figure 1 is given by

$$V_{OUT} = -V_{IN}\ 10^{-\left(\frac{1.5N}{20}\right)}$$

where N is the binary input for values 0 to 59. For N = 60 through 63 the input is fully muted, that is, the attenuation is infinite.

HIGH FREQUENCY AMPLIFIERS

R_{FB} and the output capacitance of the AD7110 create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 30–50pF of feedback capacitance (C1) ensures stability.

DC PERFORMANCE OF AD7110

For fixed-reference applications, an output amplifier with low offset voltage (less than 50μV) is required, e.g. the AD517L. This combination will provide the utmost stability at the expense of slow settling times.

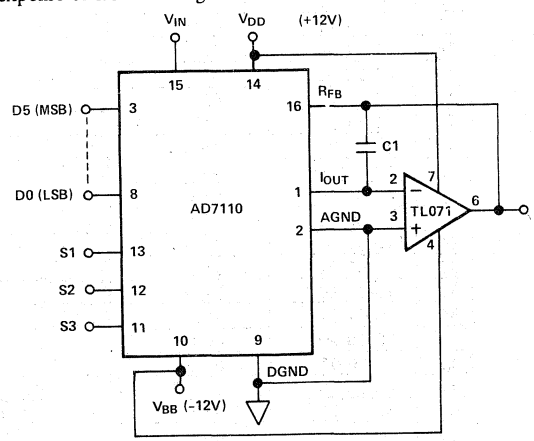


Figure 1.

Table I

N	Digital Input D5 D0	Attenuation dB	Switches[1] S1	S2	S3	V_{OUT}[2]
0	00 00 00	0.0				10.00
1	00 00 01	1.5				8.414
2	00 00 10	3.0				7.079
3	00 00 11	4.5				5.597
4	00 01 00	6.0				5.012
5	00 01 01	7.5				4.217
6	00 01 10	9.0				3.548
7	00 01 11	10.5				2.985
8	00 10 00	12.0				2.512
9	00 10 01	13.5				2.113
10	00 10 10	15.0				1.778
11	00 10 11	16.5				1.496
12	00 11 00	18.0				1.259
13	00 11 01	19.5				1.059
14	00 11 10	21.0				0.891
15	00 11 11	22.5				0.750
16	01 00 00	24.0				0.631
17	01 00 01	25.5				0.531
18	01 00 10	27.0				0.447
19	01 00 11	28.5				0.376
20	01 01 00	30.0				0.316
21	01 01 01	31.5				0.266
22	01 01 10	33.0				0.224
23	01 01 11	34.5				0.188
24	01 10 00	36.0				0.158
25	01 10 01	37.5				0.133
26	01 10 10	39.0				0.112
27	01 10 11	40.5				0.0944
28	01 11 00	42.0				0.0794
29	01 11 01	43.5				0.0668
30	01 11 10	45.0				0.0562
31	01 11 11	46.5				0.0473
32	10 00 00	48.0	■			0.0398
33	10 00 01	49.5	■			0.0335
34	10 00 10	51.0	■			0.0282
35	10 00 11	52.5	■			0.0237
36	10 01 00	54.0	■			0.0200
37	10 01 01	55.5	■			0.0168
38	10 01 10	57.0	■			0.0141
39	10 01 11	58.5	■			0.0119
40	10 10 00	60.0		■		0.0100
41	10 10 01	61.5		■		0.00841
42	10 10 10	63.0		■		0.00708
43	10 10 11	64.5		■		0.00596
44	10 11 00	66.0		■		0.00501
45	10 11 01	67.5		■		0.00422
46	10 11 10	69.0		■		0.00355
47	10 11 11	70.5		■		0.00299
48	11 00 00	72.0		■		0.00251
49	11 00 01	73.5		■		0.00211
50	11 00 10	75.0		■		0.00178
51	11 00 11	76.5		■		0.00150
52	11 01 00	78.0		■		0.00126
53	11 01 01	79.5		■		0.00106
54	11 01 10	81.0		■		0.000891
55	11 01 11	82.5		■		0.000750
56	11 10 00	84.0		■		0.000631
57	11 10 01	85.5		■		0.000531
58	11 10 10	87.0		■		0.000447
59	11 10 11	88.5		■		0.000376
60	11 11 XX[3]	∞		■	■	

NOTES:
[1] Switch closed in shaded area.
[2] V_{IN} = -10V dc
[3] X = 1 or 0. Output is fully muted for N≥60.

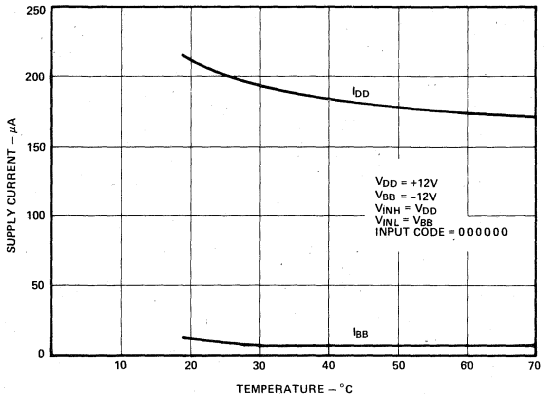


Figure 2. Power Supply Current vs. Temperature

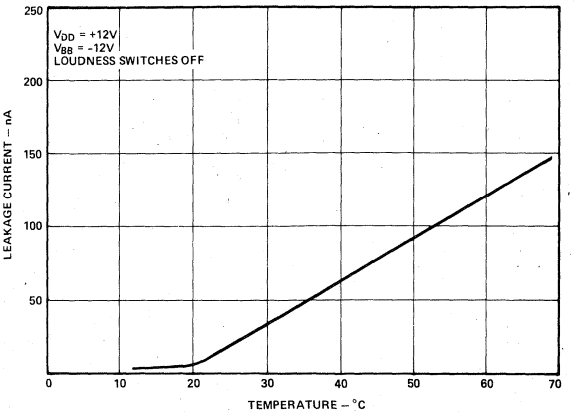


Figure 5. Loudness Switch Leakage Current vs. Temperature

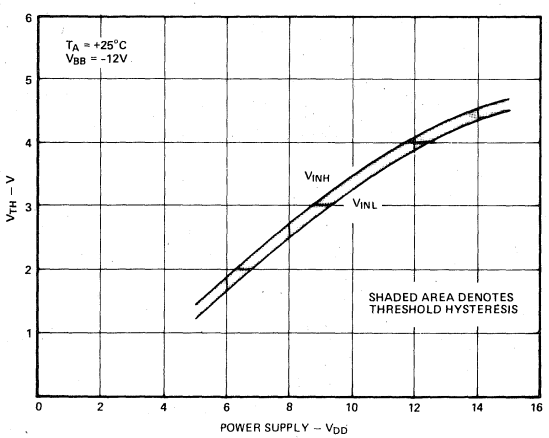


Figure 3. Digital Threshold Voltage vs. Power Supply Voltage

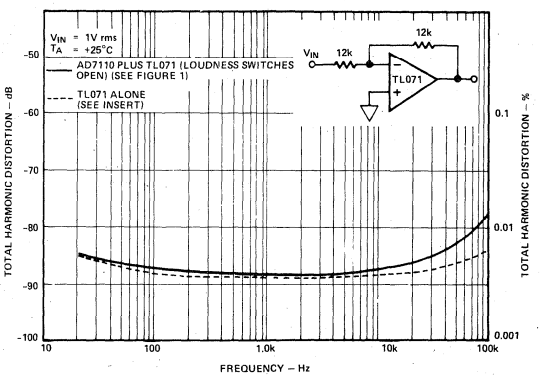


Figure 6. Total Harmonic Distortion vs. Frequency

Figure 6 shows that the total harmonic distortion of the attenuator circuit of Figure 1 is almost totally dependent on the characteristics of the operational amplifier used.

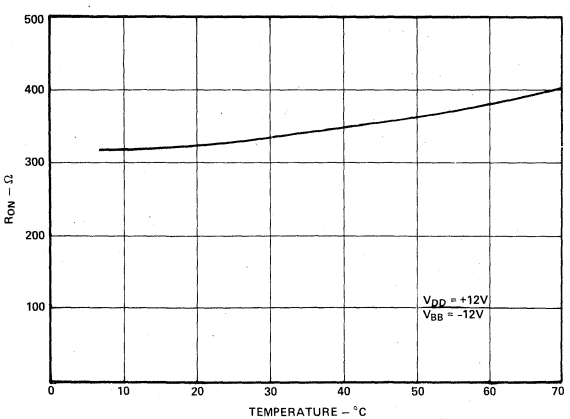


Figure 4. Loudness Switch On Resistance vs. Temperature

Applications Information

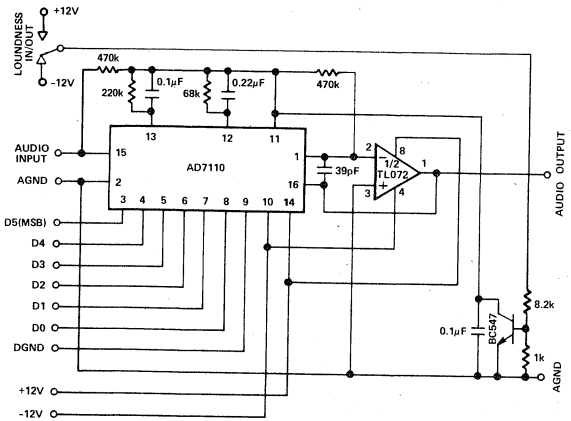


Figure 7. Single Channel Audio Attenuator with Loudness Compensation

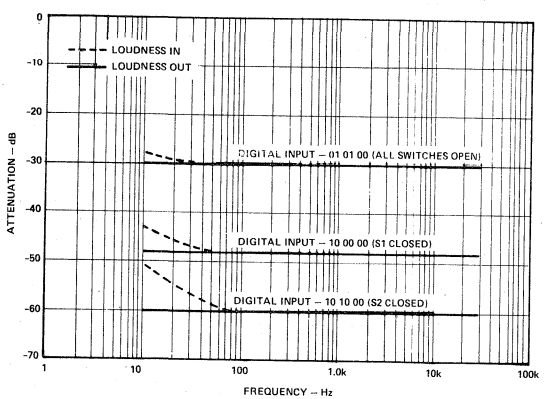


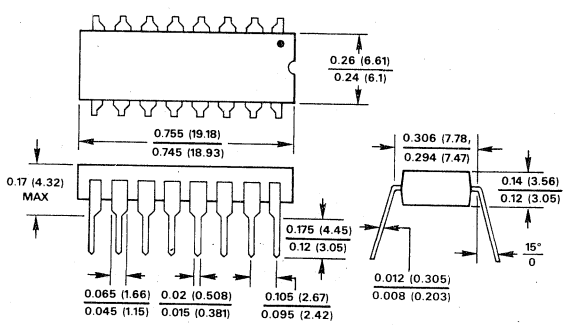
Figure 8.

Figure 8 shows the Attenuation vs. Frequency for the circuit of Figure 7. The attenuation is plotted against frequency for the two digital input codes at which the loudness compensation switches S1 and S2 are activated.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN PLASTIC DIP



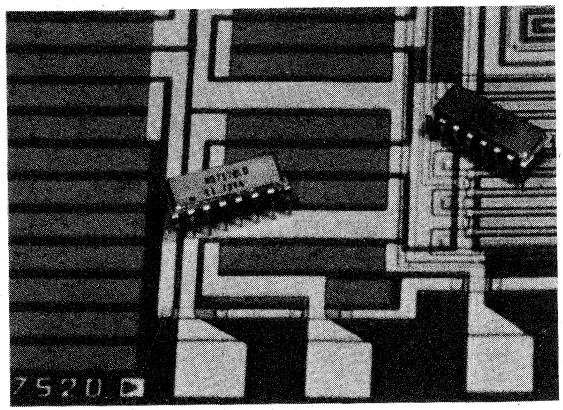
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. LEADS ARE SOLDER-PLATED KOVAR

CMOS 10-& 12-Bit Monolithic Multiplying D/A Converters

AD7520, AD7521

FEATURES
- AD7520: 10-Bit Resolution
- AD7521: 12-Bit Resolution
- Linearity: 8-, 9- and 10-Bit
- Nonlinearity Tempco: 2ppm of FSR/°C
- Low Power Dissipation: 20mW
- Current Settling Time: 500ns
- Feedthrough Error: 1/2LSB @ 100kHz
- TTL/DTL/CMOS Compatible

Note: AD7533 is recommended for new 10-bit designs.
AD7541, AD7542 or AD7543 is recommended for new 12-bit designs.



GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin wilm technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

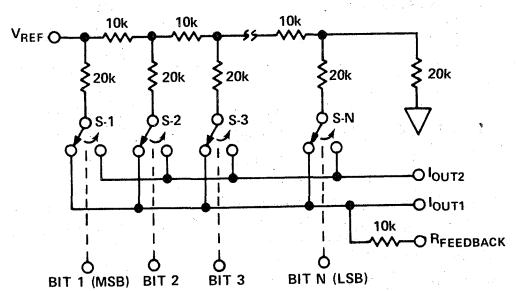
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7521JN	AD7520JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7521KN	AD7520KD AD7521KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7521LN	AD7520LD AD7521LD	AD7520UD AD7521UD

PACKAGE IDENTIFICATION

Suffix D: Ceramic DIP package
Suffix N: Plastic DIP package

FUNCTIONAL DIAGRAM

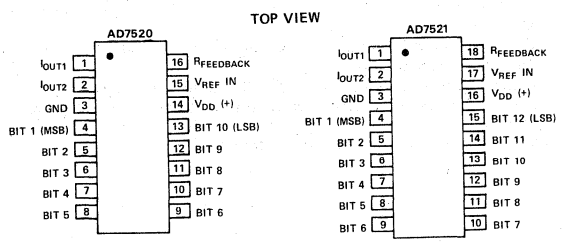


DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7520: N=10
AD7521: N=12
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

PIN CONFIGURATION

TOP VIEW



SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER	AD7520	AD7521	TEST CONDITIONS
DC ACCURACY[1]			
Resolution	10 Bits	12 Bits	
Nonlinearity (See Figure 5)			
	J, 0.2% of FSR max (8 Bit)	*	S,T,U: over -55°C to +125°C
	S, 0.2% of FSR max (8 Bit)	*	$-10V \leq V_{REF} \leq +10V$
	K, 0.1% of FSR max (9 Bit)	*	
	T, 0.1% of FSR max (9 Bit)	*	
	L, 0.05% of FSR max (10 Bit)	*	
	U, 0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco	2ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Gain Error[2]	0.3% of FSR typ	*	$-10V \leq V_{REF} \leq +10V$
Gain Error Tempco[2]	10ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Output Leakage Current (either output)	200nA max	*	Over specified temperature range
Power Supply Rejection (See Figure 6)	50ppm of FSR%/°C typ	*	
AC ACCURACY			To 0.05% of FSR
Output Current Settling Time (See Figure 10)	500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error (See Figure 9)	10mV p-p max		V_{REF} = 20V p-p, 100kHz
		*	All digital inputs low
REFERENCE INPUT			
Input Resistance[3]	5kΩ min	*	
	10kΩ typ	*	
	20kΩ max	*	
ANALOG OUTPUT			
Output Capacitance I_{OUT1}	120pF typ	*	All digital inputs high
(See Figure 8) I_{OUT2}	37pF typ	*	All digital inputs high
I_{OUT1}	37pF typ	*	All digital inputs low
I_{OUT2}	120pF typ	*	All digital inputs low
Output Noise (both outputs) (See Figure 7)	Equivalent to 10kΩ typ Johnson noise	*	
DIGITAL INPUTS[4]			
Low State Threshold	0.8V max	*	Over specified temperature range
High State Threshold	2.4V min	*	Over specified temperature range
Input Current (low to high state)	1μA typ	*	Over specified temperature range
Input Coding	Binary	*	See Tables 1 & 2 under Applications
POWER REQUIREMENTS			
Power Supply Voltage Range	+5V to +15V	*	
I_{DD}	5nA typ	*	All digital inputs at GND
	2mA max	*	All digital inputs high or low
Total Dissipation (Including ladder)	20mW typ	*	

NOTES:
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Using the internal $R_{FEEDBACK}$
[3] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
[4] Ladder and feedback resistor tempco is approximately -150ppm/°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . -100mV to V_{DD}
Power Dissipation (package)
  up to +75°C 450mW
  derates above +75°C by . . . . . 6mW/°C
Operating Temperature
  JN, KN, LN Versions . . . . . 0 to +70°C
  JD, KD, LD Versions . . . . . -25°C to +85°C
  SD, TD, UD Versions . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted

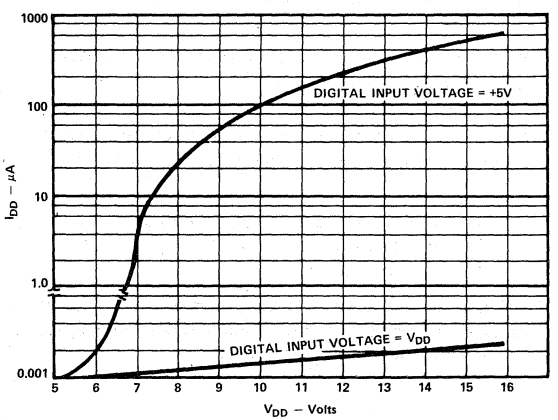


Figure 1. Supply Current vs. Supply Voltage

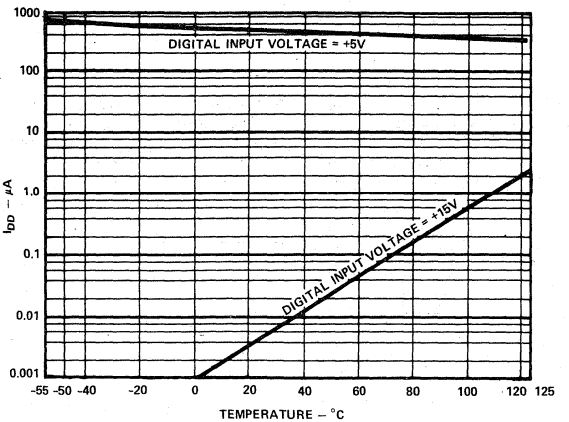


Figure 2. Supply Current vs. Temperature

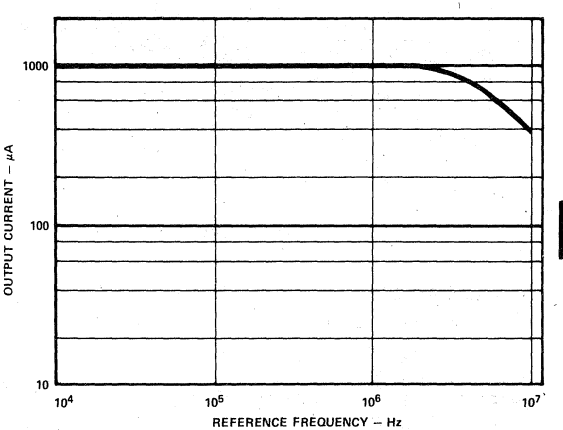


Figure 3. Output Current Bandwidth

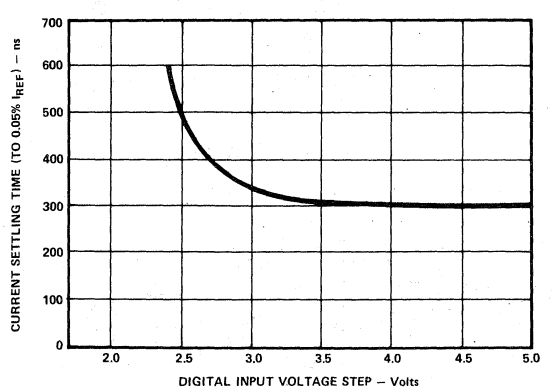


Figure 4. Output Current Settling Time vs. Digital Input Voltage

TEST CIRCUITS

Note: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7521.

DC PARAMETERS

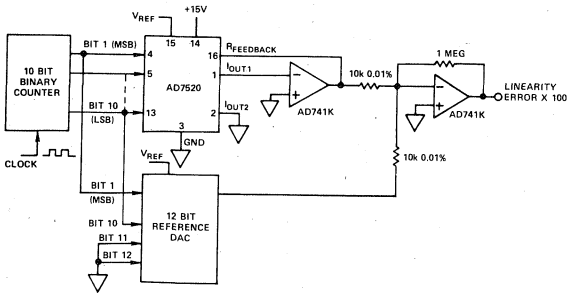


Figure 5. Nonlinearity

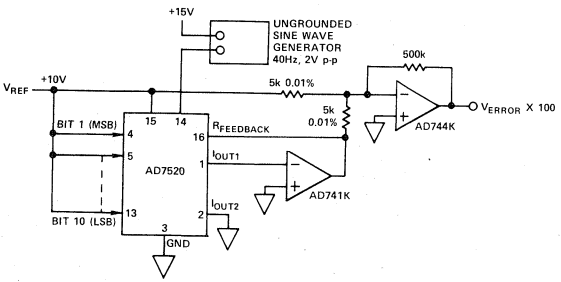


Figure 6. Power Supply Rejection

AC PARAMETERS

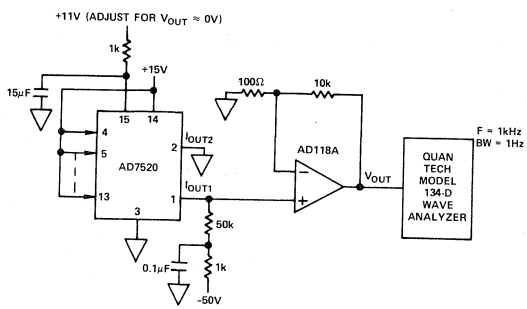


Figure 7. Noise

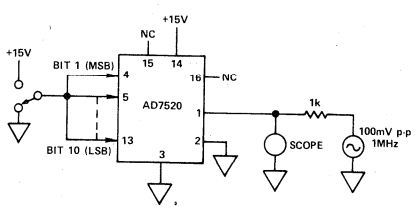


Figure 8. Output Capacitance

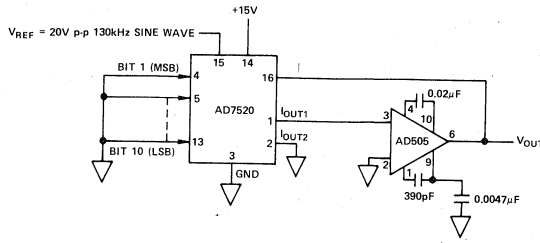


Figure 9. Feedthrough Error

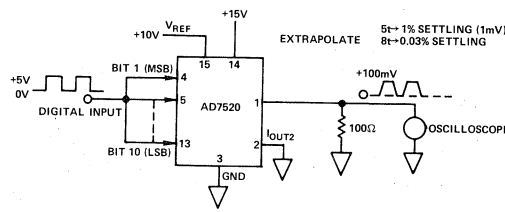


Figure 10. Output Current Settling Time

TERMINOLOGY

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7521), a 10-bit (12-bit) multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten (twelve) CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 11. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

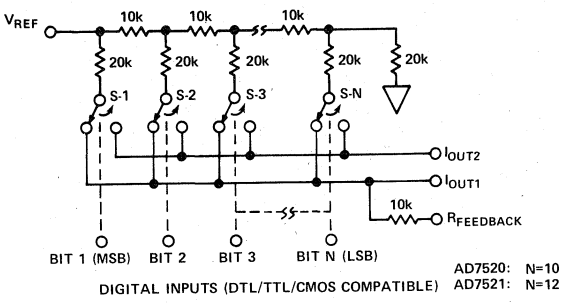


Figure 11. AD7520 (AD7521) Functional Diagram

One of the CMOS current switches is shown in Figure 12. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch-1 of Figure 12 was designed for an "ON" resistance of 20 ohms, switch-2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

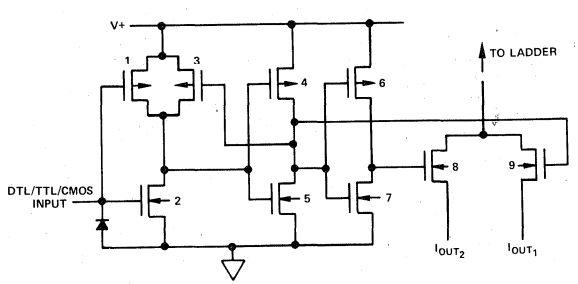


Figure 12. CMOS Switch

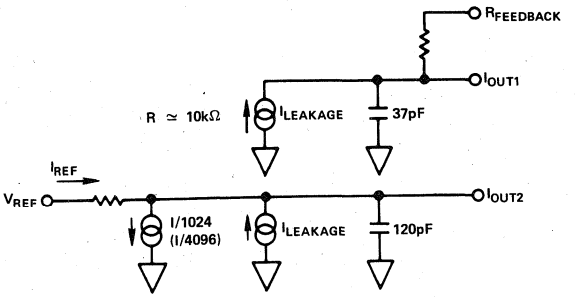


Figure 13. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 13 and 14. In Figure 13 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}\left(\frac{I}{4096}\right)$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 37pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 14 is similar to Figure 13; however, the "ON" switches are now on terminal I_{OUT1}, hence the 120pF at that terminal.

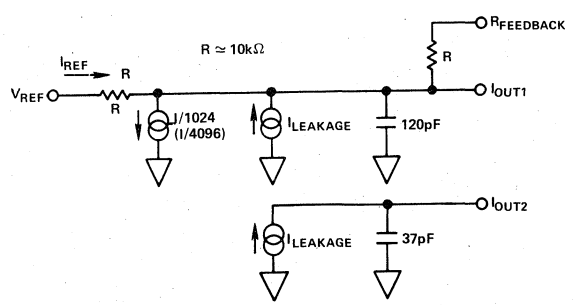


Figure 14. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs High

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 15 shows the circuit connections required for unipolar operation using the AD7520. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1.

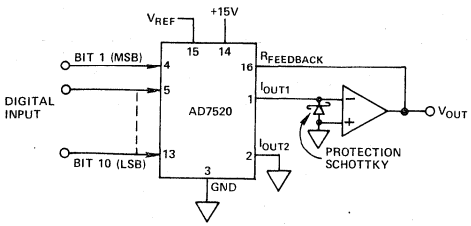


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

(Note: Protection Schottky not required with TRIFET output amplifier such as AD542 or AD544).

Zero Offset Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to GND potential.
2. Adjust the offset trimpot on the output operational amplifier for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to the +15V supply.
2. To increase V_{OUT}, place a resistor R in series with the amplifier output terminal and $R_{FEEDBACK}$ of the AD7520 (AD7521) (R = 0 to 500Ω)
3. To decrease V_{OUT}, place a resistor R in series with V_{REF}. (R = 0 to 500Ω)

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-10})$
1000000001	$-V_{REF}\ (1/2 + 2^{-10})$
1000000000	$\frac{-V_{REF}}{2}$
0111111111	$-V_{REF}\ (1/2 - 2^{-10})$
0000000001	$-V_{REF}\ (2^{-10})$
0000000000	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table 1. Code Table — Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 16 illustrates the AD7520 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-9})$
1000000001	$-V_{REF}\ (2^{-9})$
1000000000	0
0111111111	$V_{REF}\ (2^{-9})$
0000000001	$V_{REF}\ (1 - 2^{-9})$
0000000000	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table 2. Code Table — Bipolar (Offset Binary) Operation

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})\ (10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal.

Offset Adjustment

1. Make V_{REF} approximately +10V.
2. Tie all digital inputs to +15V (Logic "1").
3. Adjust amplifier #2 offset trimpot for 0V ±1mV at amplifier #2 output.
4. Tie MSB (Bit 1) to +15V, all other bits to ground.
5. Adjust amplifier #1 offset trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

Gain adjustment is the same as for unipolar operation.

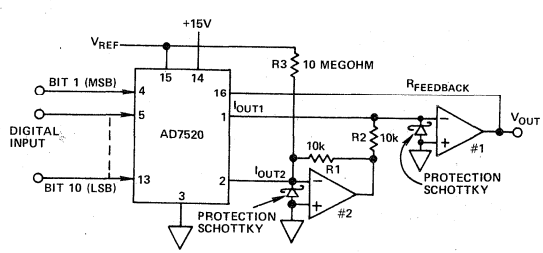


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

(Note: Protection Schottky not required with TRIFET output amplifier such as AD542 or AD544).

DYNAMIC PERFORMANCE CHARACTERISTICS

The following circuits and associated waveforms illustrate the dynamic performance which can be expected using some commonly available IC amplifiers. All settling times are to 0.05% of 10V.

AD741J

Small Signal Bandwidth: 180kHz
Settling Time: 20μs

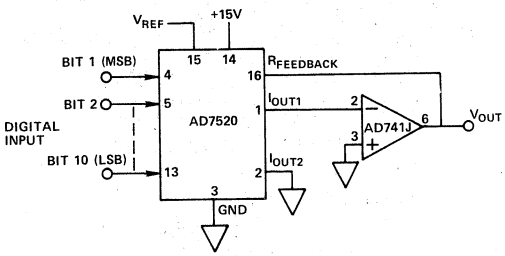


Figure 17. DAC Circuit Using AD741J

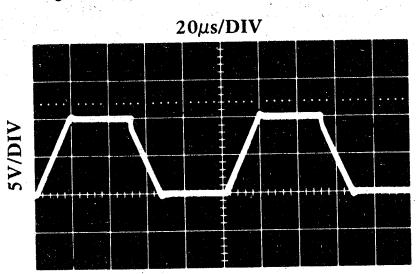


Figure 18. Output Waveform

AD518K

Small Signal Bandwidth: 1.0MHz
Settling Time: 6.0μs

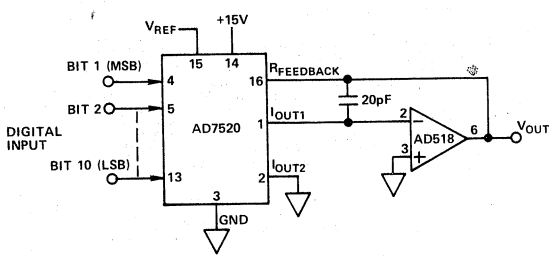


Figure 19. DAC Circuit Using AD518K

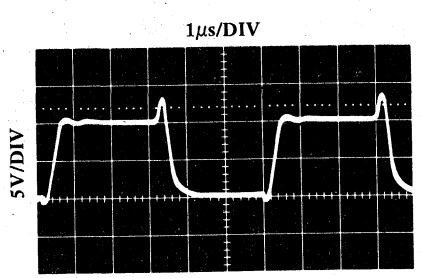


Figure 20. Output Waveform

AD505J

Small Signal Bandwidth: 1.0MHz
Settling Time: 2.5μs

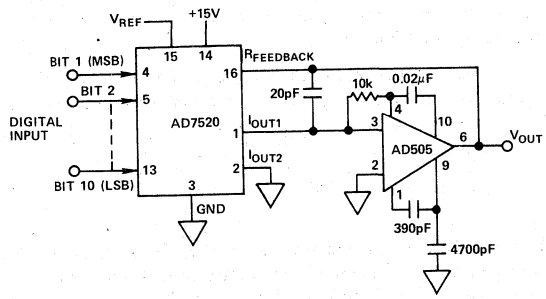


Figure 21. DAC Circuit Using AD505J

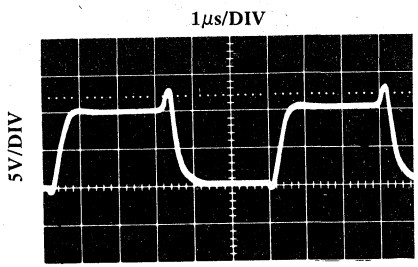


Figure 22. Output Waveform

AD509K

Small Signal Bandwidth: 1.6MHz
Settling Time: 2.0μs

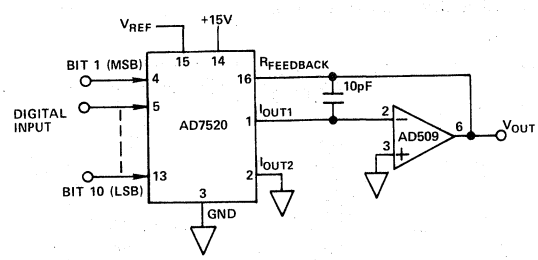


Figure 23. DAC Circuit Using AD509K

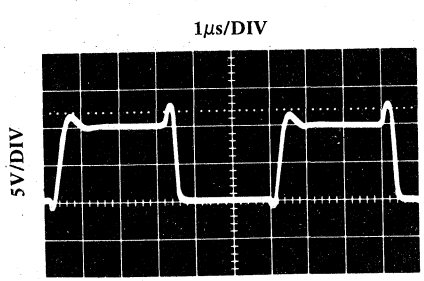


Figure 24. Output Waveform

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_0 = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 25, the transfer function becomes

$$V_0 = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit 10) ON, the gain is 1024. With all bits ON, the gain is 1 (±1 LSB).

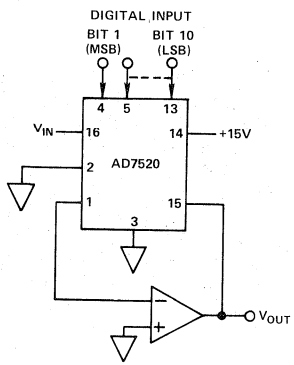
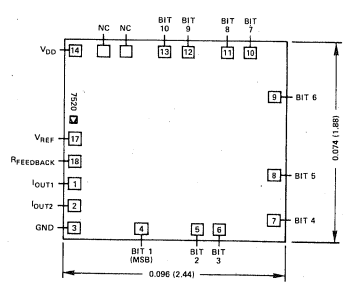


Figure 25. Analog/Digital Divider

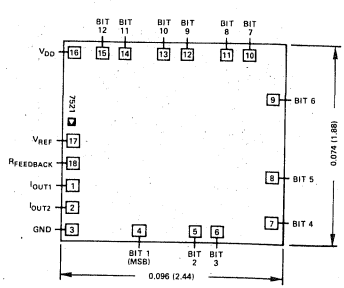
BONDING DIAGRAMS

Dimensions shown in inches and (mm).

AD7520



AD7521

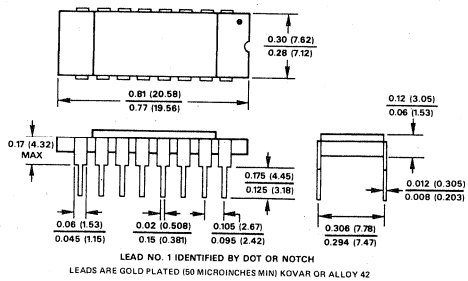


OUTLINE DIMENSIONS

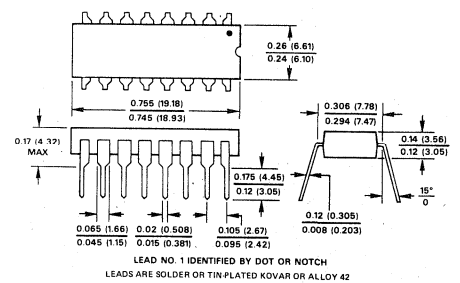
Dimensions shown in inches and (mm).

AD7520

16 PIN CERAMIC DIP

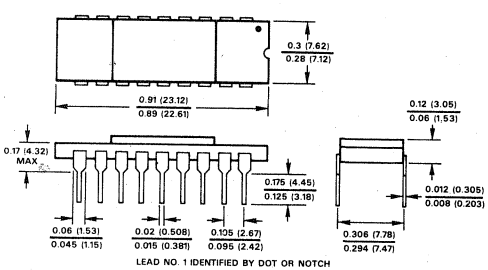


16 PIN PLASTIC DIP

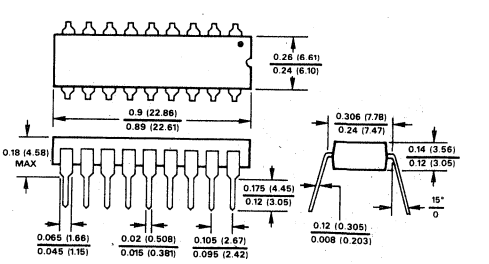


AD7521

18 PIN CERAMIC DIP



18 PIN PLASTIC DIP

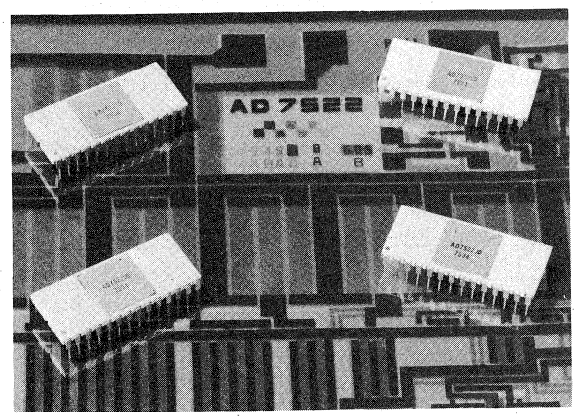


CMOS 10-Bit, Buffered Multiplying D/A Converter

AD7522

FEATURES

- 10-Bit Resolution
- 8-, 9- & 10-Bit Linearity
- Microprocessor Compatible
- Double Buffered Inputs
- Serial or Parallel Loading
- DTL/TTL/CMOS Direct Interface
- Nonlinearity Tempco: 2ppm of FSR/°C
- Gain Tempco: 10ppm of FSR/°C
- Very Low Power Dissipation
- Very Low Feedthrough



GENERAL DESCRIPTION

The AD7522 is a monolithic CMOS 10-bit multiplying D/A converter, with an input buffer and a holding register, allowing direct interface with microprocessors. Most applications require the addition of only an operational amplifier and a reference voltage.

The key to easy interface to a data bus is the AD7522's ability to load the input buffer in two bytes (an 8-bit and a 2-bit byte), and subsequently move this data to a holding register, where the digital word is converted into an analog current or voltage (with external operational amplifier). The input loading of either 8 or 10 bits can be done in a parallel or serial mode.

The AD7522 is packaged in a 28-pin DIP, and operates with a +15V main supply at 2mA max, and a logic supply of +5V for TTL interface, or +10 to +15V for CMOS interface.

A thin film on high density CMOS process, using silicon nitride passivation, ensures high reliability and excellent stability.

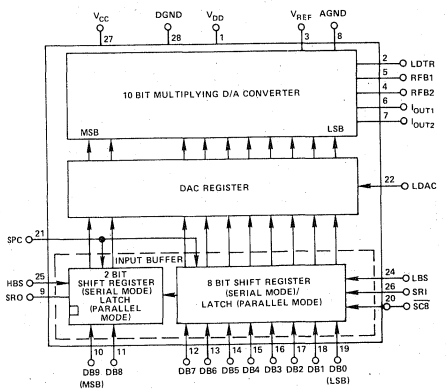
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7522JN	AD7522JD	AD7522SD
0.1% (9-Bit)	AD7522KN	AD7522KD	AD7522TD
0.05% (10-Bit)	AD7522LN	AD7522LD	AD7522UD

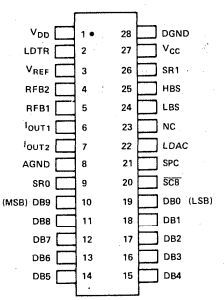
PACKAGE IDENTIFICATION

Suffix "D": Ceramic DIP Package
Suffix "N": Plastic DIP Package

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V, TA = +25°C unless otherwise noted)

PARAMETER		TA = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
STATIC ACCURACY				
Resolution	All	10 Bits min	10 Bits min	$\overline{SC8}$ = "1"
Nonlinearity	AD7522J	±0.2% FSR max		
	AD7522S	±0.2% FSR max	±0.2% FSR max	
	AD7522K	±0.1% FSR max		
	AD7522T	±0.1% FSR max	±0.1% FSR max	
	AD7522L	±0.05% FSR max		
	AD7522U	±0.05% FSR max	±0.05% FSR max	-10V≤V_{REF}≤+10V
Nonlinearity Tempco[1]	AD7522J,K,L	±1ppm FSR/°C typ	±2ppm FSR/°C max	
	AD7522S,T,U		±2ppm FSR/°C max	
Gain Error	AD7522J,K,L	±0.3% Reading typ		
Gain Error Tempco[1]	AD7522J,K,L	±5ppm of Reading/°C typ	±10ppm of Reading/°C max	
	AD7522S,T,U		±10ppm of Reading/°C max	
Output Leakage Current at I_{OUT1} or I_{OUT2}	All		200nA max	I_{OUT1}: DB0 through DB9 = 0 I_{OUT2}: DB0 through DB9 = 1
Power Supply Rejection	AD7522J,K,L	50ppm of Reading/% typ		
AC ACCURACY				
Feedthrough Error[1]	All	1mV p-p typ, 10mV p-p max		V_{REF}= 20V p-p; 10kHz
Output Current Settling Time	AD7522J,K,L	500ns typ		To 0.05% of FSR for a FSR Step. HBS and LBS Low to High LDAC = 1
REFERENCE INPUT				
Input Resistance	All	5kΩ min	20kΩ max	
ANALOG OUTPUT				
Output Capacitance				
C_{OUT1}	AD7522J,K,L	120pF typ		All Data Input High
C_{OUT2}	AD7522J,K,L	40pF typ		
C_{OUT1}	AD7522J,K,L	40pF typ		All Data Inputs Low
C_{OUT2}	AD7522J,K,L	120pF typ		
DIGITAL INPUTS				
Low State Threshold	All	0.8V max	0.8V max	V_{CC} = +5V
	All	1.5V max	1.5V max	V_{CC} = +15V
High State Threshold	All	2.4V min	2.4V min	V_{CC} = +5V
	All	13.5V min	13.5V min	V_{CC} = +15V
Input Current	AD7522J,K,L	1μA typ		
LDAC Pulse Width[1]	All	500ns min	500ns min	LDAC: 0 to +3V
HBS, LBS Pulse Width[1]	All	500ns min	500ns min	HBS, LBS: 0 to +3V
Serial Clock Frequency[1]	All	1MHz max	1MHz max	
HBS, LBS Data Set Up[2]	All	250ns min	250ns min	
Data Hold Time[3]	All	500ns min, 200ns typ	500ns min	
POWER REQUIREMENTS				
I_{DD}	All	2mA max		In Quiescent State
I_{CC}	All	2mA max		

Notes

[1] Guaranteed by design. Not tested.
[2] Data setup time is the minimum amount of time required for DB0 - DB9 to be stable prior to strobing HBS, LBS.
[3] Data hold time is the minimum amount of time required for DB0 - DB9 to be stable after strobing HBS, LBS.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{REF} to GND . . . . . ±25V
V_{DD} to GND . . . . . +17V
V_{CC} to GND . . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
I_{OUT1}, I_{OUT2} . . . . . −0.3V to V_{DD}
Operating Temperature
JN, KN, LN versions . . . . . 0 to +70°C
JD, KD, LD versions . . . . . −25°C to +85°C
SD, TD, UD versions . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation (Package)
Up to +50°C:
Plastic (Suffix N) 1200mW
Ceramic (Suffix D) 1000mW
Derate Above +50°C by
Plastic (Suffix N) . . . . . 12mW/°C
Ceramic (Suffix D) . . . . . 10mW/°C
Digital Input Voltage Range . . . . . V_{DD} to GND

CAUTION:

1. Do not apply voltages higher than V_{CC} to SRO.
2. Do not apply voltages higher than V_{DD} or less than GND to any other input/output terminal except V_{REF}, R_{FB1} or R_{FB2}.
3. The digital control inputs are zener protected, however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
4. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

TERMINOLOGY

RESOLUTION

Value of the LSB. For example, a unipolar n-bit converter has a resolution of (2^{-n}) (V_{REF}). A bipolar n-bit converter has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

GAIN

The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is a linear error which can be externally adjusted (see gain adjustment on next page).

OUTPUT LEAKAGE CURRENT

Current which appears on the OUT1 terminal when the DAC register is loaded with all "0's" or on the OUT2 terminal when the DAC register is loaded with all "1's."

DAC CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7522's DAC functional block consists of a highly stable Silicon Chromium thin film R-2R ladder, and ten SPDT N-channel current steering switches. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

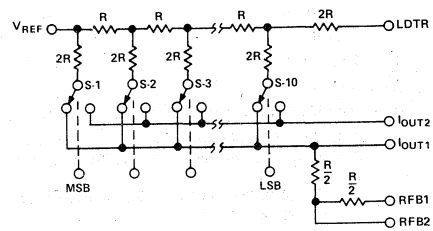


Figure 1. DAC Functional Diagram

EQUIVALENT CIRCUIT

The DAC equivalent circuit is shown in Figure 2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $I_{REF}/1024$ current source represents the 1LSB of current lost through the ladder termination resistor to ground. The C_{OUT1} and C_{OUT2} output capacitances are as shown when the DAC latches feed the DAC with all "1's." If the DAC latches are loaded with all "0's," C_{OUT1} is 37pF, while C_{OUT2} is 120pF. In addition, C_{SD} is shunted by 10 ohms, and the 10 ohm R_{ON} in I_{OUT1} is replaced by a C_{SD} of 10pF. When fast amplifiers are used, it will be necessary to provide phase compensation (in the form of feedback capacitance) to cancel the pole formed by $R_{FEEDBACK}$ and C_{OUT} if stability is to be maintained.

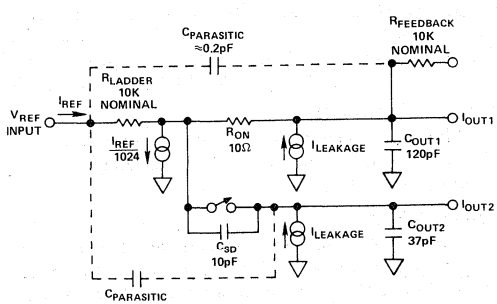


Figure 2. Equivalent Circuit (Shown for all Digital Inputs High)

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{DD}	+15V (nominal) Main Supply.
2	LDTR	R-2R Ladder Termination Resistor. Normally grounded for unipolar operation or terminated at I_{OUT2} for bipolar operation.
3	V_{REF}	Reference Voltage Input. Since the AD7522 is a multiplying DAC, V_{REF} may vary over the range of ±10V.
4	RFB2	$R_{FEEDBACK} \div 2$; gives full scale equal to $V_{REF}/2$.
5	RFB1	$R_{FEEDBACK}$, used for normal unity gain (at full scale) D/A conversion.
6	I_{OUT1}	DAC Current OUT1 Bus. Normally terminated at virtual ground of output amplifier.
7	I_{OUT2}	DAC Current OUT2 Bus, terminated at ground for unipolar operation, or virtual ground of op amp for bipolar operation.
8	AGND	Analog Ground. Back gate of DAC N-channel SPDT current steering switches.
9	SRO	Serial Output. An auxiliary output for recovering data in the input buffer.
10	DB9	Data Bit 9. Most significant parallel data input.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.
18	DB1	Data Bit 1.
19	DB0	Data Bit 0. Least significant parallel data input.
20	$\overline{SC8}$	8-Bit Short Cycle Control. When in serial mode, if $\overline{SC8}$ is held to Logic "0", the two least significant input latches in the input buffer are bypassed to provide proper serial loading of 8-bit serial words. If $\overline{SC8}$ is held to Logic "1", the AD7522 will accept a 10-bit serial word. Data bits 0 (LSB) and DB1 are in a parallel load mode when $\overline{SC8}$ = 0 and should be tied to a logic low state to prevent false data from being loaded.
21	SPC	Serial/Parallel Control. If SPC is a Logic "0", the AD7522 will load parallel data appearing on DB0 through DB9 into the input buffer when the appropriate strobe inputs are exercised (see HBS and LBS). If SPC is a Logic "1", the AD7522 will load serial data appearing on Pin 26 into the input buffers. Each serial data bit must be "strobed" into the buffer with the HBS and LBS.
22	LDAC	Load DAC: When LDAC is a Logic "0", the AD7522 is in the "hold" mode, and digital activity in the input buffer is locked out. When LDAC is a Logic "1", the AD7522 is in the "load" mode, and data in the input buffer loads the DAC register.
23	NC	No Connection.
24	LBS	Low Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB0 (LSB) through DB7 inputs will be "clocked" into the input buffer on the positive going edge of the LBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edge of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
25	HBS	High Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB9 (MSB) and DB8 data inputs will be "clocked" into the input buffer on the positive going edge of HBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edges of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
26	SRI	Serial Input.
27	V_{CC}	Logic Supply. If +5V is applied, all digital inputs/outputs are TTL compatible. If +10V to +15V is applied, digital inputs/outputs are CMOS compatible.
28	DGND	Digital Ground

Note 1

Note 1: Logic "1" applied to a data bit steers that bit's current to the $I_{OUT}1$ terminal.

APPLICATIONS

(Note: Protection Schottky CR3 in Figure 3 and CR3, CR4 in Figure 4 are not required when using TRI-FET amps such as the AD542 or AD544).

UNIPOLAR OPERATION

Figure 3 shows the analog circuit connections required for unipolar operation. The input code/output voltage relationship is shown in Table 1.

Zero Offset Adjustment

1. Adjust the op amp's offset potentiometer for <1mV on the amplifier junction. (Each millivolt of amplifier V_{OS} causes ±0.66mV of differential nonlinearity which adds to the ladder nonlinearity.)

Gain Adjustment

1. Set R1 and R2 to 0Ω. Load the DAC register with all "1's."
2. If analog out is greater than $-V_{REF}$, increase R1 for required full scale output. If analog out is less than $-V_{REF}$, increase R2 for required full scale output.

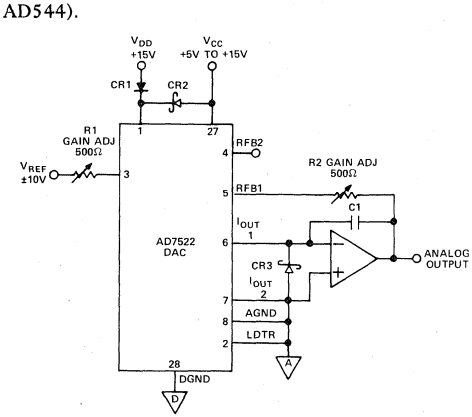


Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-10})$
1000000001	$-V_{REF}\ (1/2 + 2^{-10})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}\ (1/2 - 2^{-10})$
0000000001	$-V_{REF}\ (2^{-10})$
0000000000	0

Table 1. Unipolar Code Table

BIPOLAR OPERATION

Figure 4 shows the analog circuit connections required for bipolar operation. The input code/output voltage relationship is shown in Table 2.

Zero Offset Adjustment

1. Adjust the offset potentiometer of amplifier A1 and A2 for <1mV on the respective summing junctions. If the analog out for code 1000000000 is not zero, sum current into or out of the summing junction of A1 for 0V at analog out.

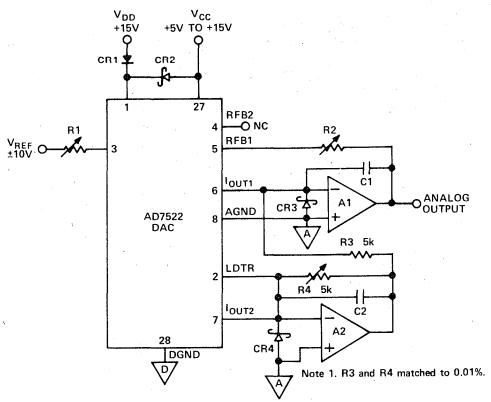


Figure 4. Bipolar Operation

Gain Adjustment

1. Load the DAC register with all "0's." Set R1 and R2 to 0Ω.
2. If analog out is greater than $+V_{REF}$, increase R2 until it reads precisely $+V_{REF}$. If analog out is less than $+V_{REF}$, increase R1 until it reads precisely V_{REF}.

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-9})$
1000000001	$-V_{REF}\ (2^{-9})$
1000000000	0
0111111111	$V_{REF}\ (2^{-9})$
0000000001	$V_{REF}\ (1 - 2^{-9})$
0000000000	V_{REF}

Table 2. Bipolar Code Table

SINGLE BYTE PARALLEL LOADING

Figure 5 illustrates the logic connections for loading single byte parallel data into the input buffer. DB0 should be grounded on "K" and "T" versions, and DB0 and DB1 should be grounded on "J" and "S" versions for monotonic operation of the DAC. DB9 is always the MSB, whether 8-bit, 9-bit, or 10-bit linear AD7522's are used.

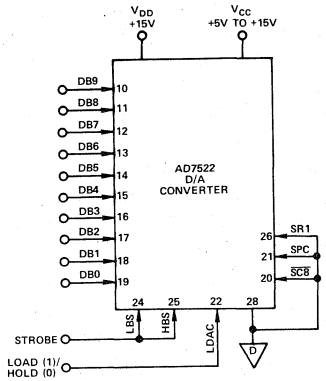


Figure 5. Single Byte Parallel Loading

When data is stable on the parallel inputs (DB0-DB9), it can be transferred into the input buffer on the positive edge of the strobe pulse.

Data is transferred from the input buffer to the DAC register when LDAC is a Logic "1." LDAC is a level-actuated (versus edge-triggered) function and must be held "high" at least 0.5μs for data transfer to occur.

TWO BYTE PARALLEL LOADING

Figures 6 and 7 show the logic connections and timing requirements for interfacing the AD7522 to an 8-bit data bus for two byte loading of a 10-bit word.

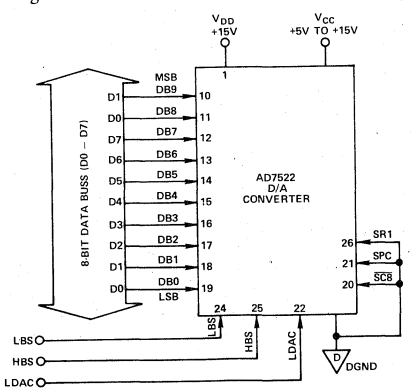


Figure 6. Two Byte Parallel Loading

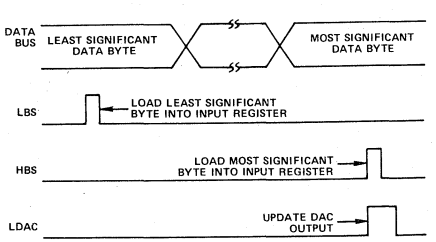


Figure 7. Timing Diagram

First, the least significant data byte (DB0 through DB7) is loaded into the input buffer on the positive edge of LBS. Subsequently, the data bus is used for status indication and

instruction fetching by the CPU. When the most significant data byte (DB8 and DB9) is available on the bus, the input buffer is loaded on the positive edge of HBS. The DAC register updates to the new 10-bit word when LDAC is "high." LDAC may be exercised coincident with, or at any time after HBS loads the second byte of data into the input buffer.

SERIAL LOADING

Figure 8 and Figure 9 show the connections and timing diagram for serial loading.

To load a 10-bit word ($\overline{SC8}$ = 1), HBS and LBS must be strobed simultaneously with exactly 10 positive edges to clock the serial data into the input buffer. For 8-bit words (SC8 = 0), only 8 positive edges are required.

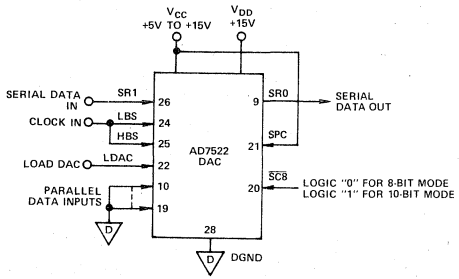


Figure 8. Serial 8- and 10-Bit Loading (Analog Outputs Not Shown for Clarity)

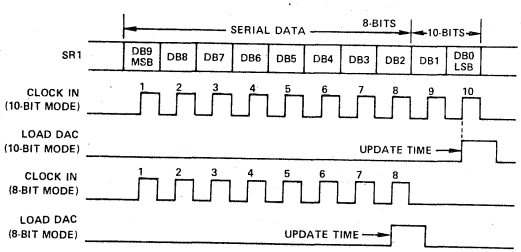


Figure 9. Timing Diagram for Serial 8- and 10-Bit Loading

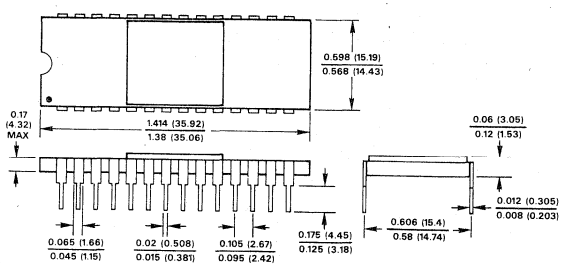
APPLICATION HINTS

1. CR1 and CR2 on Figures 3 and 4 protect the AD7522 against latch-up V_{CC} exceeds V_{DD}, and may be omitted if V_{DD} and V_{CC} are driven from the same voltage.
2. Diodes CR3 on Figure 3 and CR3 and CR4 on Figure 4 clamp the amplifier junction to -300mV if they attempt to swing negative during power up or power down. The input structures of some high-speed op amps can supply substantial current under the transient conditions encountered during power sequencing. It is recommended that the PC layout be able to accommodate the diodes.
3. Fast op amps will require phase compensation for stability due to the pole formed by C_{OUT1} or C_{OUT2} and $R_{FEEDBACK}$.
4. During serial loading, all data inputs (DB0 through BD9), should be grounded.

OUTLINE DIMENSIONS

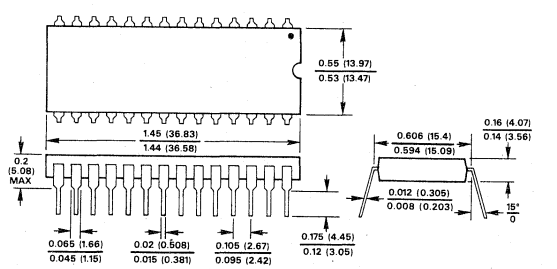
Dimensions shown in inches and (mm).

28 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

28 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

ANALOG DEVICES

CMOS 8-Bit Multiplying D/A Converter

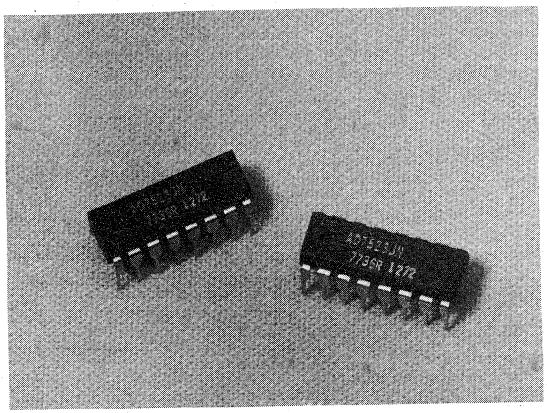
AD7523

FEATURES

- Low Cost
- Fast Settling: 100ns
- Low Power Dissipation
- Low Feedthrough: ½LSB @ 200kHz
- Full Four-Quadrant Multiplying

APPLICATIONS

- Battery Operated Equipment
- Low Power, Ratiometric A/D Converters
- Digitally Controlled Gain Circuits
- Digitally Controlled Attenuators
- CRT Character Generation
- Low Noise Audio Gain Control

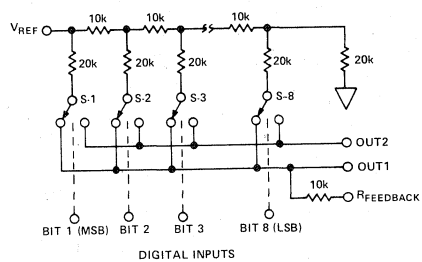


GENERAL DESCRIPTION

The AD7523 is a low cost, monolithic multiplying digital-to-analog converter packaged in a 16-pin DIP. The device uses an advanced monolithic, thin-film-on-CMOS technology to provide 8-bit resolution with accuracy to 10-bits and very low power dissipation.

The AD7523's excellent multiplying characteristics and low cost allow it to be used in a wide ranging field of applications such as: low noise audio gain control, CRT character generation, motor speed control, digitally controlled attenuators, etc.

FUNCTIONAL DIAGRAM

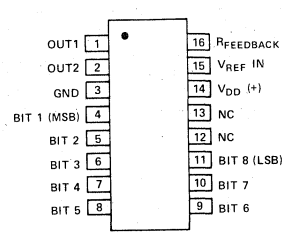


ORDERING INFORMATION

Model	Linearity	Package	Operating Temperature Range
AD7523JN	±1/2LSB	16 pin Plastic	0 to +70°C
AD7523KN	±1/4LSB		
AD7523LN	±1/8LSB		
AD7523AD	±1/2LSB	16 pin Ceramic	-25°C to +85°C
AD7523BD	±1/4LSB		
AD7523CD	±1/8LSB		
AD7523SD	±1/2LSB	16 pin Ceramic	-55°C to +125°C

Ceramic versions are available 100% screened to MIL-STD-883 Class B. To order add "/883" to part number shown above. Example: AD7523AD/883B.

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = T_{min} to T_{max}	TEST CONDITION
STATIC ACCURACY			
Resolution	8 Bits min	8 Bits min	
Nonlinearity[1]			
AD7523JN, AD, SD	±1/2LSB max (±0.2% FSR max)	±1/2LSB max (±0.2% FSR max)	V_{OUT1} = V_{OUT2} = 0V
AD7523KN, BD	±1/4LSB max (±0.1% FSR max)	±1/4LSB max (±0.1% FSR max)	
AD7523LN, CD	±1/8LSB max (±0.05% FSR max)	±1/8LSB max (±0.05% FSR max)	
Monotonicity	Guaranteed over T_{min} to T_{max}		V_{OUT1} = V_{OUT2} = 0V
Gain Error[1,2,3]	-1.5% of FSR min, +1.5% of FSR max	-1.8% of FSR min, +1.8% of FSR max	Digital Inputs = V_{INH}
Power Supply Rejection (Gain)[1,2]	0.02% per % max	0.03% per % max	V_{DD} = +14V to +15V Digital Inputs = V_{INH}
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INL}
I_{OUT2} (pin 2)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INH}
DYNAMIC PERFORMANCE			
Output Current			
Settling Time[4]	150ns max	200ns max	To 0.2% FSR, Load = 100Ω Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error[4]	±1/2LSB max	±1LSB max	Digital Inputs = V_{INL} V_{REF} = 20V p-p, 200kHz sinewave
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max		V_{OUT1} = V_{OUT2} = 0V
Temperature Coefficient		-500ppm/°C max	
ANALOG OUTPUTS[4]			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max	100pF max	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	30pF max	30pF max	
C_{OUT1} (pin 1)	30pF max	30pF max	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max	100pF max	
DIGITAL INPUTS			
Logic Thresholds			
V_{INH}	+14.5V min	+14.5V min	
V_{INL}	+0.5V max	+0.5V max	
Input Leakage Current			
I_{IN} (per input)	±1μA max	±1μA max	V_{IN} = 0V or +15V
Input Capacitance			
C_{IN}[4]	4pF max	4pF max	
Input Coding	Unipolar Binary of Offset Binary (see next page)		
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Device Functionality. Accuracy is tested and guaranteed only at
I_{DD} S and all /883B versions	200μA max	500μA max	V_{DD} = +15V
I_{DD} J, K, L, A, B, C versions	100μA max	100μA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:
[1] FSR is Full Scale Range.
[2] Using internal feedback resistor, Full Scale Range (FSR) is equal to (V_{REF} - 1LSB) in the unipolar circuit on the next page.
[3] Max gain change from +25°C to T_{min} or T_{max} is ±0.3% FSR.
[4] Guaranteed by design. Not subject to test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0V, +17V
V_{REF} to GND . . . . . ±25V
Digital Input Voltage (V_{IN}) to GND . . . . . -0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND . . . . . -0.3V to V_{DD}

Power Dissipation (package)
To +70°C 670mW
Derate Above +70°C by . . . . . .8.3mW/°C
Operating Temperature . . . . . 0 to +70°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher the V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V^- during power-up or power-down sequencing. To prevent the AD7523 OUT1 or OUT2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figure 1 and 2. Protection diodes are not required when using TRI-FET amplifiers such as the AD542 or AD544.

BASIC OPERATION

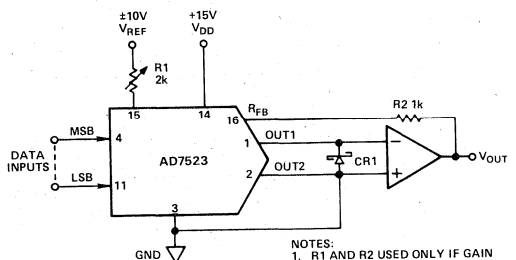


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$-V_{REF}\left(\frac{255}{256}\right)$
10000001		$-V_{REF}\left(\frac{129}{256}\right)$
10000000		$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111		$-V_{REF}\left(\frac{127}{256}\right)$
00000001		$-V_{REF}\left(\frac{1}{256}\right)$
00000000		$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table 1. Unipolar Binary Code Table

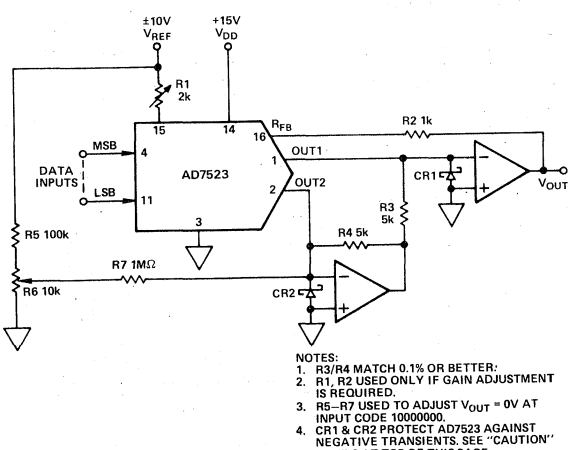


Figure 2. Bipolar (4-Quadrant) Operation

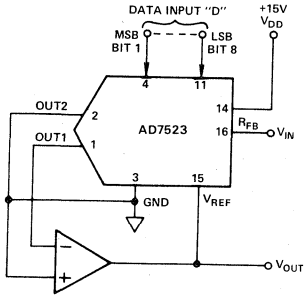
DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$-V_{REF}\left(\frac{127}{128}\right)$
10000001		$-V_{REF}\left(\frac{1}{128}\right)$
10000000		0
01111111		$+V_{REF}\left(\frac{1}{128}\right)$
00000001		$+V_{REF}\left(\frac{127}{128}\right)$
00000000		$+V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$$V_{OUT} = -\frac{V_{IN}}{D}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{1}{D} \quad \text{where: } A_V = \text{Voltage Gain}$$

and where:

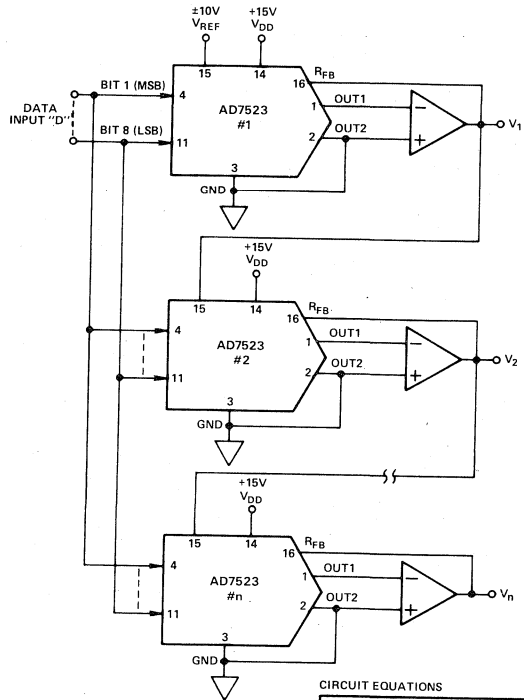
$$D = \frac{\text{BIT 1}}{2^1} + \frac{\text{BIT 2}}{2^2} + \frac{\text{BIT 8}}{2^8}$$

(BIT N = 1 or 0)

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)
D = 00000001, $A_V = -256$
D = 10000000, $A_V = -\frac{256}{128} = -2$
D = 11111111, $A_V = -\frac{256}{255}$

POWER GENERATION



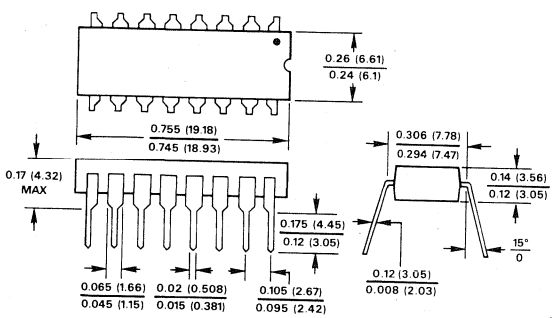
CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$
$V_2 = +(V_{REF})(D^2)$
$V_n = -(V_{REF})(D^n)$, n an odd integer
$V_n = +(V_{REF})(D^n)$, n an even integer

OUTLINE DIMENSIONS

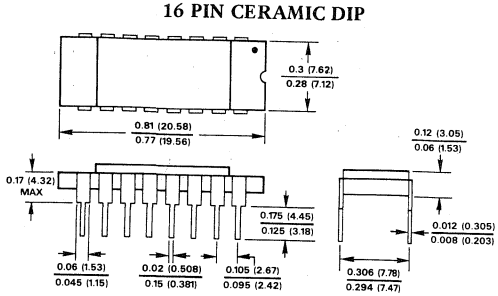
Dimensions shown in inches and (mm).

16 PIN PLASTIC DIP



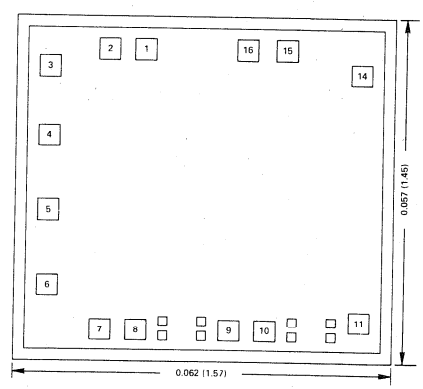
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. LEADS ARE SOLDER PLATED KOVAR OR ALLOY 42.

16 PIN CERAMIC DIP



1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. LEADS ARE GOLD PLATED (50mm) KOVAR OR ALLOY 42.

BONDING DIAGRAM



NOTES:
1. Pad numbers correspond to pin numbers shown on pin configuration.
2. Dimensions in inches (mm).
3. Pad 3, GND, should be bonded 1st.
4. Pads are 0.004" x 0.004" (0.102 x 0.102mm).

ANALOG DEVICES

CMOS 8-Bit Buffered Multiplying DAC

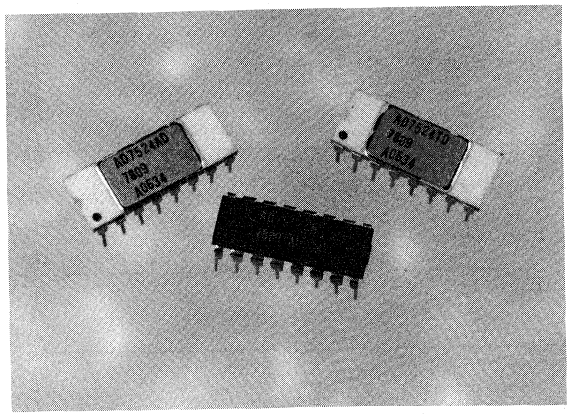
AD7524

FEATURES

- Low Cost
- On-Chip Bus Interface Logic
- Full Four-Quadrant Multiplication
- +5V to +15V Operation
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments



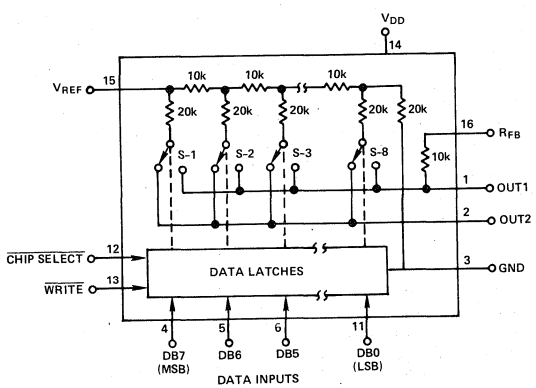
GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8 LSB with power dissipation of only 20 milliwatts.

Featuring operation from +5V to +15V, the AD7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

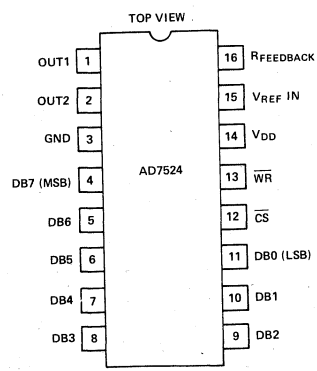
FUNCTIONAL DIAGRAM



ORDERING INFORMATION

	Temperature Range and Package		
Nonlinearity @ +15V	Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±1/2 LSB	AD7524JN	AD7524AD	AD7524SD
±1/4 LSB	AD7524KN	AD7524BD	AD7524TQ
±1/8 LSB	AD7524LN	AD7524CD	AD7524UD

PIN CONFIGURATION



SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

PARAMETER	LIMIT, T_A = +25°C[1] V_{DD} = +5V	LIMIT, T_A = +25°C[1] V_{DD} = +15V	LIMIT, T_A = OPERATING RANGE V_{DD} = +5V	LIMIT, T_A = OPERATING RANGE V_{DD} = +15V	UNITS	TEST CONDITION
STATIC ACCURACY						
Resolution	8	8	8	8	Bits min	
Nonlinearity						
AD7524JN, AD, SD	±1/2	±1/2	±1/2	±1/2	LSB max	
AD7524KN, BD, TD	±1/2	±1/4	±1/2	±1/4	LSB max	
AD7524LN, CD, TD	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	guaranteed	guaranteed	guaranteed	guaranteed	—	
Gain Error[1]	±1.0	±0.5	±1.4	±0.6	% FSR max	Max gain change from T_A = 25°C to T_{min} or T_{max} is ±0.4% (V_{DD} = 5V) or ±0.1% (V_{DD} = +15V)
dc Supply Rejection, Gain[2]						
$\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% per % max	ΔV_{DD} = ±10%
Output Leakage Current						
I_{OUT1} (pin 1)	±50	±50	±400	±200	nA max	DB0 – DB7 = V_{IH}; $\overline{WR}$, $\overline{CS}$ = V_{IL}; V_{REF} = ±10V
I_{OUT2} (pin 2)	±50	±50	±400	±200	nA max	DB0 – DB7 = V_{IL}; $\overline{WR}$, $\overline{CS}$ = V_{IL}; V_{REF} = ±10V
DYNAMIC ACCURACY						
Output Current Settling Time (To 1/2 LSB)	150[3]	100[3]	200[2]	150[2]	ns max	OUT1 Load = 100Ω; $\overline{WR}$, $\overline{CS}$ = V_{IL} DB0 – DB7 = V_{IH} to V_{IL} or V_{IL} to V_{IH}
ac Feedthrough Current[2]						
@ OUT1 (pin 1)	±1/2	±1/2	±1	±1	LSB max	V_{REF} = 100kHz, 20V p-p sinewave
@ OUT2 (pin 2)	±1/2	±1/2	±1	±1	LSB max	DB0 – DB7 = V_{IL}; $\overline{CS}$, $\overline{WR}$ = V_{IL}
REFERENCE INPUT						
R_{IN} (pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[2]						
C_{OUT1} (pin 1)	90	90	90	90	pF max	DB0 – DB7 = V_{IH}; $\overline{WR}$, $\overline{CS}$ = V_{IL}
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB0 – DB7 = V_{IL}; $\overline{WR}$, $\overline{CS}$ = V_{IL}
C_{OUT2} (pin 2)	90	90	90	90	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement						
V_{IH}	+3.5	+14.5	+4.0	+14.5	V min	
Input LOW Voltage Requirement						
V_{IL}	+0.8	+0.5	+0.8	+0.5	V max	
Input Current (per input)						
I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[2] (per input)						
C_{IN}	20	20	20	20	pF max	
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time						
t_{CS}[3]	280	180	310	210	ns min	
Chip Select to Write Hold Time						
t_{CH}[3]	60	50	80	70	ns min	
Write Pulse Width						
t_{WP}[3]	220	130	240	160	ns min	
Data Setup Time						
t_{DS}[3]	180	140	200	160	ns min	
Data Hold Time						
t_{DH}[3]	100	80	120	100	ns min	
POWER SUPPLY						
I_{DD}	500	500	500	500	μA	All Digital Inputs = V_{IL}
	500	500	500	500	μA	All Digital Inputs = V_{IH}

NOTES:
[1] Gain error is measured when using internal feedback resistor. Ideal Full Scale Range (FSR) = (V_{REF} – 1 LSB) as shown in Table I.
[2] Guaranteed, not tested.
[3] AC parameter, sample tested @ +25°C to assure conformance to specifications.
[4] DAC thin film resistor temperature coefficient is approximately -300ppm/°C
[5] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{IH}, V_{IL}, I_{IN} and I_{DD} at +25°C and +125°C (SD, TD, UD versions) or +25°C and +85°C (AD, BD, CD versions).
Specifications subject to change without notice.

CAUTION

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V⁻ during power-up or power-down sequencing. To prevent the AD7524 OUT1 or OUT2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figures 5 and 6. The protection diodes are not required if using TRI-FET amplifiers such as the AD542 or AD544.
4. Do not insert this device into powered sockets. Remove power before insertion or removal.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0.3V, +17V
V_{RFB} to GND. . . . . ±25V
Digital Input Voltage (to GND) . . . . . -0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2)(to GND) . . . . . -0.3V to V_{DD}
Power Dissipation (package)
Plastic (N. Suffix)
To +70°C. 670mW
Derates above +70°C by . . . . . .8.3mW/°C
Ceramic (D Suffix)
To +75°C. 450mW
Derates above +75°C by . . . . . .6mW/°C
Operating Temperature
Commerical (JN, KN, LN) Grades. . . . . 0 to +70°C
Industrial (AD, BD, CD) Grades . . . . . -25°C to +85°C
Military (SD, TD, UD) Grades . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

TERMINOLOGY

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's full scale operational amplifier output voltage to the reference voltage. "Zero" gain error (for an 8-bit DAC) is defined when V_{OUT} equals $-V_{REF}$ (255/256).

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage (at the amplifier output) of typically 0.2LSB.

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB_0-DB_7 data bus inputs. In this mode, the AD7524 acts like a non-latched input D/A converter.

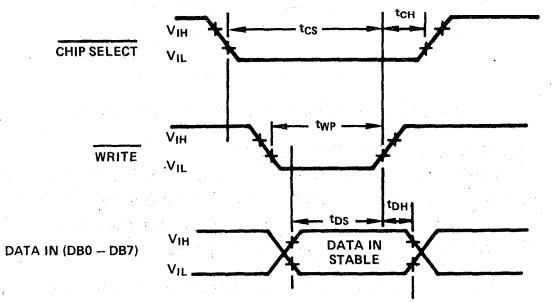
HOLD MODE

When either $\overline{CS}$ or $\overline{WR}$ are HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB_0-DB_7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the high state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when $\overline{WR}$ assumed HIGH state. L = LOW state H = HIGH state Y = Don't care state

WRITE CYCLE TIMING DIAGRAM



NOTE: IF $\overline{CS}$ AND $\overline{WR}$ ARE EXERCISED SIMULTANEOUSLY, THE t_{DH} SPECIFICATION (AS SHOWN IN SPECIFICATION TABLE), MUST BE INCREASED BY 60ns.

ANALOG CIRCUIT DESCRIPTION

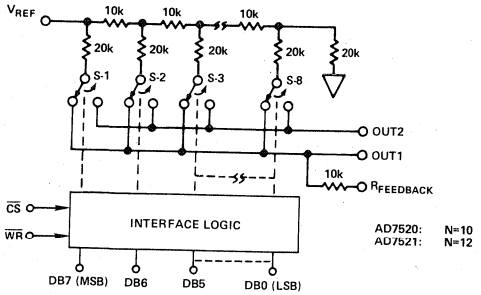
GENERAL CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

One of the current switches is shown in Figure 2. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20 ohms, switch 2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that

each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.



(Switches shown for Inputs "High")

Figure 1. AD7524 Functional Diagram

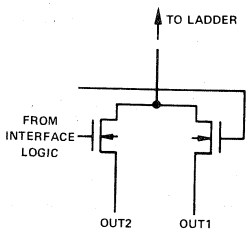


Figure 2. N-Channel Current Steering Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{256}$ current source represents a constant 1-bit current drain through the

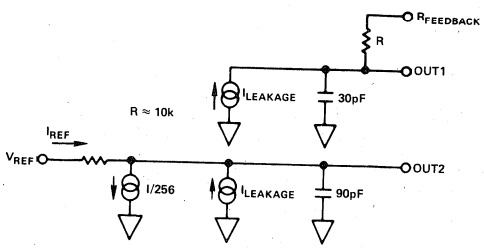


Figure 3. AD7524 DAC Equivalent Circuit – All Digital Inputs Low

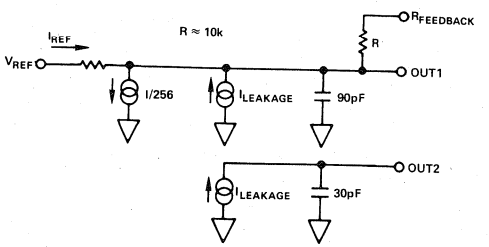


Figure 4. AD7524 DAC Equivalent Circuit – All Digital Inputs High

termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 90pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 90pF at that terminal.

APPLYING THE AD7524

ANALOG CIRCUIT CONNECTIONS

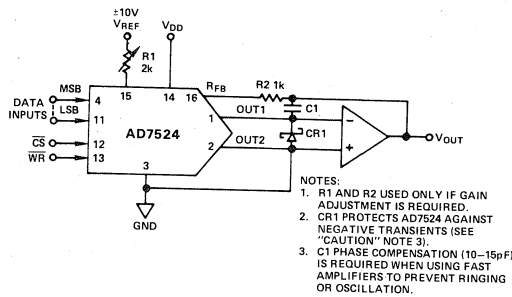


Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}\ (V_{REF})$

Table 1. Unipolar Binary Code Table

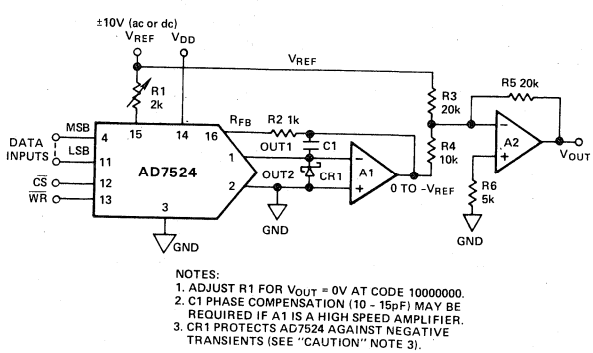


Figure 6. Bipolar (4-Quadrant) Operation

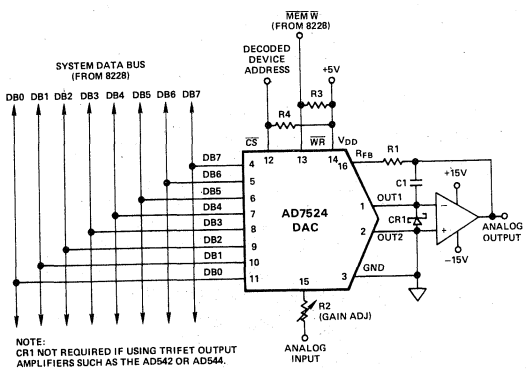
DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$+V_{REF}\left(\frac{127}{128}\right)$
10000001	$+V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{REF}\left(\frac{1}{128}\right)$
00000001	$-V_{REF}\left(\frac{127}{128}\right)$
00000000	$-V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS — MICROPROCESSOR INTERFACE

AD7524/8080A INTERFACE



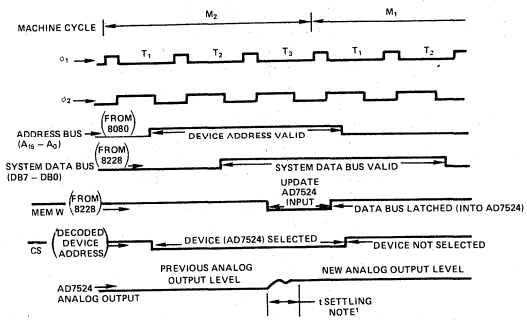
AD7524/8080A INTERFACE

The illustration above shows the AD7524 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080 CPU, 8224 clock generator and 8228 system controller/bus driver. The AD7524 $\overline{WR}$ input is connected to the 8228 $\overline{MEMW}$ output and the DB0 – DB7 inputs are connected to the 8228 system data bus outputs. The $\overline{CS}$ input is connected to the system address decoding logic. Note that pullup resistors R3 and R4 are required to ensure that the $\overline{CS}$ and $\overline{WR}$ input HIGH states reach 4.0V minimum.

System timing is shown. Data is loaded into the AD7524 when the $\overline{WR}$ and $\overline{CS}$ inputs are both LOW. The data is latched into the AD7524 when $\overline{WR}$ returns HIGH. AD7524 updating is accomplished by using any of the 8080A memory write instructions (such as MOV M, r).

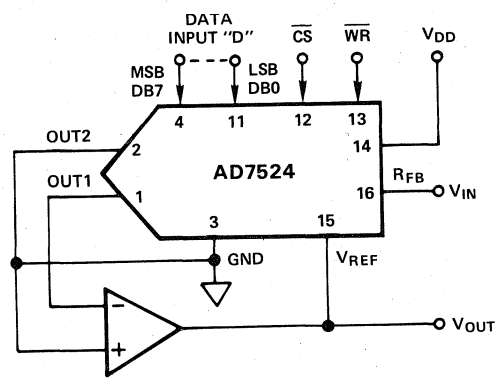
The AD7524 can also be addressed and loaded as an isolated Output Device by connecting the AD7524 $\overline{WR}$ input to the 8228 $\overline{I/O\ W}$ terminal (instead of $\overline{MEMW}$).

TIMING DIAGRAM



NOTE: 1SETTLING TIME IS DEPENDENT PRIMARILY UPON OUTPUT AMPLIFIER SLEWING AND SETTLING CHARACTERISTICS. WAVEFORM SHOWN IS NOT REPRESENTATIVE OF ANY SPECIFIC AMPLIFIER.

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$$V_{OUT} = \frac{-V_{IN}}{D}$$

$$A_V = \frac{-V_{OUT}}{V_{IN}} = -\frac{1}{D} \quad \text{WHERE: } A_V = \text{VOLTAGE GAIN}$$

and where:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$$

DB_N = 1 or 0

EXAMPLES

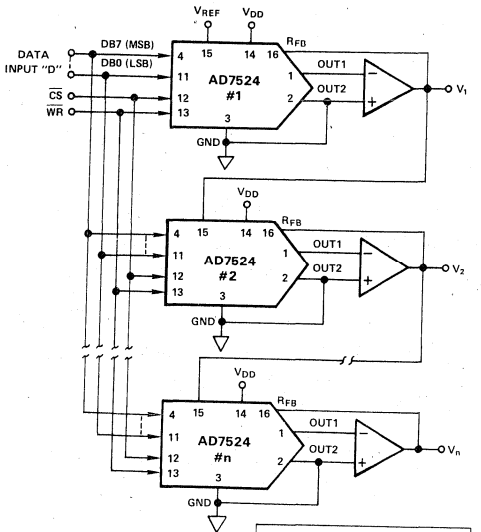
D = 00000000, $A_V = -A_{OL}$ (OP AMP)

D = 00000001, $A_V = -256$

D = 10000000, $A_V = -\frac{256}{128} = -2$

D = 11111111, $A_V = -\frac{256}{255}$

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$

$V_2 = +(V_{REF})(D^2)$

$V_n = -(V_{REF})(D^n)$, n an odd integer

$V_n = +(V_{REF})(D^n)$, n an even integer

WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \cdots \frac{DB0}{2^8}$$

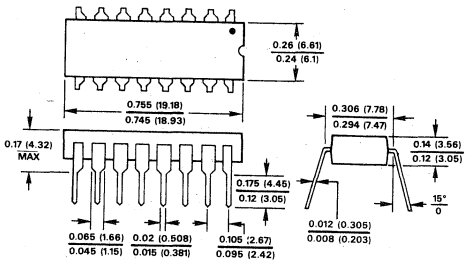
and

DB_n = 1 or 0

OUTLINE DIMENSIONS

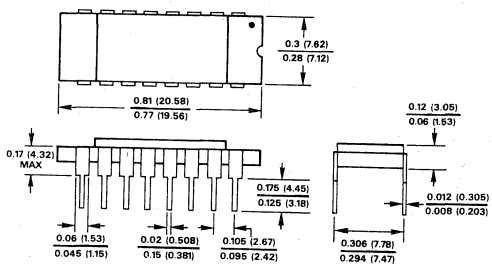
Dimensions shown in inches and (mm).

16 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

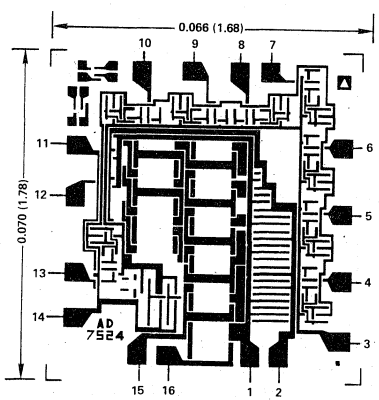
16 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

BONDING DIAGRAM

Dimensions shown in inches and (mm).



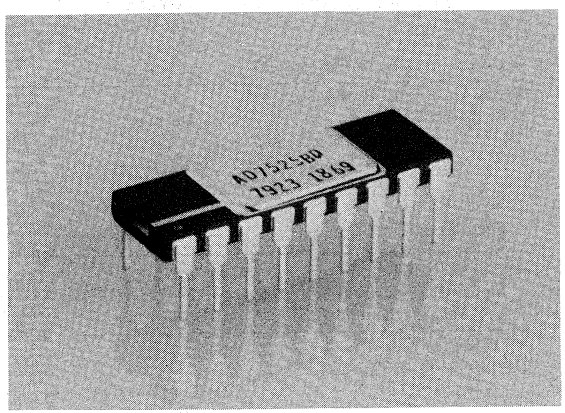
Notes:
1. Pad numbers correspond to pin numbers shown in pin configuration.
2. Pad 3 (GND) should be bonded first to minimize ESD hazards.
3. Pads are 0.004 in. x 0.004in. (0.102mm x 0.102mm).

3½ Digit BCD Monolithic CMOS Digitally Controlled Potentiometer

AD7525

FEATURES
Resolution: 3 1/2 Digit BCD (1999 Counts)
Nonlinearity: ±1/2LSB T_{min} to T_{max}
Gain Error: ±0.05% FS
Excellent Repeatability Accuracy
Low Power Dissipation

APPLICATIONS
Thumbwheel Switch Voltage Dividers
Digitally Controlled Gain Circuits
Digitally Controlled Attenuators
BCD Multiplying DACs
Low Power Converters



GENERAL DESCRIPTION
The AD7525 is a monolithic CMOS 3½ digit BCD digitally controlled potentiometer designed for precision incremental voltage-divider applications.

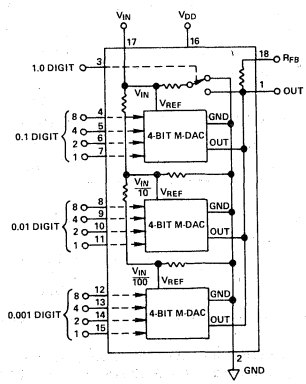
With the addition of an external op amp, the output can be digitally controlled from 0 to 1.999V_{IN} with resolution of 0.001V_{IN}.

AC or DC voltage up to ±10V can be applied to the input providing high application flexibility in fields such as audio gain control, etc.

Digital control, excellent repeatability and 0.2% accuracy make the AD7525 an ideal replacement for 10-turn potentiometers or thumbwheel switch voltage dividers using discrete resistor networks.

Packaged in an 18-pin DIP, the AD7525 uses an advanced CMOS fabrication process combined with wafer laser trimming.

FUNCTIONAL DIAGRAM

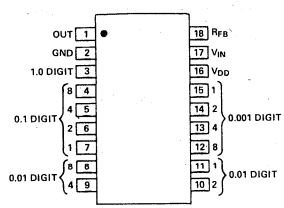


ORDERING INFORMATION

Package and Temperature	Nonlinearity ±1/2LSB	Nonlinearity ±1LSB
18 Pin Plastic 0 to +70°C	AD7525LN	AD7525KN
18 Pin Ceramic -25°C to +85°C	AD7525CD AD7525CD/883B[1]	AD7525BD AD7525BD/883B[1]
18 Pin Ceramic -55°C to +125°C	AD7525UD AD7525UD/883B[1]	AD7525TD AD7525TD/883B[1]

[1] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for class B device.

PIN CONFIGURATION



SPECIFICATIONS (V_{DD}=+15V; V_{PIN1} = 0V; V_{IN} = +10V unless otherwise stated)

PARAMETER	T_A = +25°C	T_A = Operating Temperature Range	CONDITION
ACCURACY			
Resolution[1]	1 part in 2000	1 part in 2000	
Nonlinearity[2, 3]			
AD7525KN, BD, TD	±1LSB max	±1LSB max	BCD 0.000 to 1.999
AD7525LN, CD, UD	±1/2LSB max	±1/2LSB max	BCD 0.000 to 1.999
Gain Error[3, 4]	±0.05% FS typ	–	BCD = 1.999
Gain TC	±25ppm/°C max	–	BCD = 1.999
Output Leakage Current (pin 1)	100nA max	400nA max	BCD = 0.0000
DYNAMIC PERFORMANCE			
Switching Time	1µs max[5]	1µs max[6]	V_{IN} = +5V, R_{OUT} (pin 1) = 100Ω, Digital Inputs = V_{IL} to V_{IH} or V_{IL}, V_{PIN1} measured from 10% to 90%
Feedthrough Error	±0.05%V_{IN} max[6]	±0.1%V_{IN} max[6]	V_{IN} = ±10V, 20kHz sinewave
ANALOG INPUT			
Input Resistance (pin 17)[7]	2kΩ min/10kΩ max	2kΩ min/10kΩ max	
V_{IN} Range (recommended)	±10V max	±10V max	
ANALOG OUTPUT			
Output Capacitance			
C_{OUT} (pin 1)	60pF max[6]	60pF max[6]	Digital Inputs = BCD 0000
	200pF max[6]	200pF max[6]	Digital Inputs = BCD 1999
R_{FB} Resistance (pin 18 to pin 1)[7]	8kΩ min/40kΩ max	8kΩ min/40kΩ max	
DIGITIAL INPUTS			
Input HIGH Voltage			
V_{IH}[3]	+14.5V min	+14.5V min	
Input LOW Voltage			
V_{IL}[3]	+0.5V max	+0.5V max	
Input Leakage Current	±1µA max	±10µA max	Digital Input = 0V or V_{DD}
Input Capacitance	5pF max[6]	5pF max[6]	
Input Coding	3½ Digit BCD (1999 Counts)	3½ Digit BCD (1999 Counts)	
POWER SUPPLY			
V_{DD} Range	+5V to +17V	+5V to +17V	Functional with Degraded Performance
V_{DD}	+15V ±5%	+15V ±5%	Rated Accuracy
I_{DD}[3]	500µA max	1mA max	Digital Inputs = V_{IL} or V_{IH}

NOTES:
[1] Commercial devices are sample tested over temperature.
[2] Monotonicity is guaranteed on the AD7525LN, CD and UD versions over T_{min} to T_{max}.
[3] Final electrical tests on 883B screen parts are: Gain Error, Nonlinearity, V_{IH}, V_{IL}, Digital Input Leakage Current and I_{DD} at +25°C and +125°C (TD/883B Version) or +25°C and +85°C (BD/883B Version).
[4] Gain Error is measured using the AD7525 internal feedback resistor. FS is "Full Scale" (BCD = 1.999).
[5] AC parameter, sample tested at +25°C to ensure conformance to specification.
[6] Guaranteed, not tested.
[7] Thin Film resistor temperature coefficient is approximately -300ppm/°C.
Specifications subject to change without notice.

CAUTION

1. ESD (electro-static discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
2. Do not apply voltages more negative than GND or more positive than V_{DD} to any pin except V_{IN} (pin 17) and R_{FB} (pin 18).
3. The inputs of some IC amplifiers (especially high speed types) present a low impedance to V− during power sequencing. To prevent the AD7525 OUT terminal (pin 1) from exceeding −300mV (which causes catastrophic substrate current), a Schottky diode, HSCH 1001 or equivalent, is recommended. While not required for most amplifier types, provision for the diode should be made during layout. The diode should be connected between OUT (pin 1) and GND (pin 2) as shown in Figure 4. Protection Schottkys not required when using TRI-FET output amplifiers such as the AD542 or AD544.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V_{DD} (to GND) . . . . . −0.3V, +17V
V_{IN} (to GND) . . . . . ±25V
R_{FB} (to GND) . . . . . ±25V
Digital Input Voltage (to GND) . . . . . −0.3V to V_{DD}
V_{PIN1} (to GND) . . . . . −0.3V to V_{DD}
Power Dissipation (Package)
  Plastic (Suffix N)
    To +70°C 670mW
    Derates above +70°C by . . . . . 8.3mW/°C
  Ceramic (Suffix D)
    To +75°C 450mW
    Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
  Commercial Plastic (KN, LN Versions) . . . . . 0 to +70°C
  Industrial Ceramic (BD, CD Versions) . . . . −25°C to +85°C
  Military Ceramic (TD, UD Versions) . . . . −55°C to +125°C

TERMINOLOGY

SWITCHING TIME: In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time, which is a function of the output amplifier used.

OUTPUT CAPACITANCE: Capacitance from OUT terminal (pin 1) to ground.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{IN} (pin 17) to OUT (pin 1) with all digital inputs LOW.

PRINCIPLES OF OPERATION

CIRCUIT DESCRIPTION

The AD7525, a 3½ digit BCD multiplying DAC, consists of a thin-film R/2R ladder, interquad voltage dividers and 13 N-channel MOS SPDT current steering switches. Most applications require the addition of only an external operational amplifier.

Referring to Figure 1, the "1.0 Digit" is a 1-bit multiplying DAC (composed of SW_1 and R_1) while the 0.1, 0.01, and 0.001 digits are 4-bit multiplying DAC's (DAC1, DAC2, and DAC3) connected by 10:1 dividers (composed of R_{IN2}, R_2, R_3 and R_{IN3}, R_4, R_5.

DAC1 is expanded to show the R/2R ladder and switch network. With input voltage V_{IN}, the currents in each shunt arm are (starting at the left) $V_{IN}/2R$, $V_{IN}/4R$, $V_{IN}/8R$ and $V_{IN}/16R$. A logic ONE applied to a digital input steers that shunt arm's current to OUT, while a logic ZERO steers the current to GND.

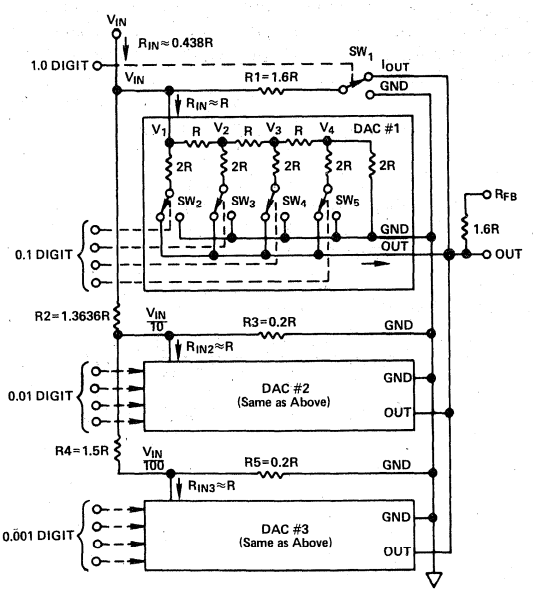


Figure 1. AD7525 Circuit Diagram

EQUIVALENT CIRCUIT

As shown in Figure 2, the AD7525 is a digitally controlled π-network attenuator with signal input "V_{IN}" (pin 17), signal output "OUT" (pin 1), signal common "GND" (pin 2) and digital control "BCD input" (pins 3–15).

With OUT (pin 1) terminated at op amp virtual ground and R_{FB} (pin 18) connected to the op amp output, the nominal transfer equation is:

$$V_{OUT} = -V_{IN}\ BCD$$
where $0.000 \leq BCD \leq 1.999$

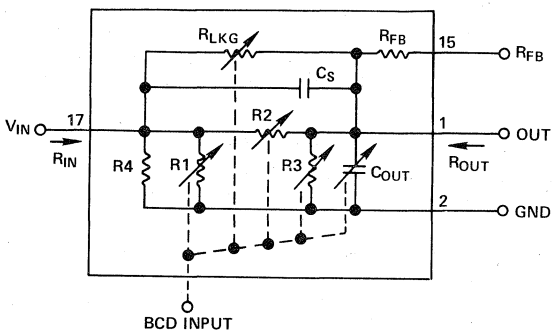


Figure 2. Functional Equivalent Circuit

OUTPUT AMPLIFIER CONSIDERATIONS

Amplifier Offset

The output resistance at OUT (pin 1) is code dependent, varying between ∞ to 0.35 R_{LDR}. For a fixed feedback resistor of value 1.6 R_{LDR} (Figure 3), the output error for a fixed amplifier offset (V_{OS}) is:

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{R_{OUT}}\right) V_{OS}$$

Case 1: ($R_{OUT} = \infty$)

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{\infty}\right) V_{OS}$$

$$V_{ERROR} = V_{OS}$$

Case 2: ($R_{OUT} = 0.35\ R_{LDR}$)

$$V_{ERROR} = \left(1 + \frac{1.6\ R_{LDR}}{0.35 R_{LDR}}\right) V_{OS}$$

$$V_{ERROR} = (1 + 4.6)V_{OS} = 5.6\ V_{OS}$$

Cases 1 and 2 show that amplifier offset in conjunction with a changing output resistance at OUT (pin 1) create nonlinearity error, in addition to a simple offset term.

It is therefore recommended that amplifier initial offset be adjusted to less than 100μV (as measured between the amplifier input terminals). The offset voltage over the temperature range of interest should not exceed 250μV. See application hint #2, below.

Do not include the usual bias current compensation resistor in the amplifier noninverting terminal. Instead, the amplifier should have a bias current which is low over the temperature range of interest. Bias current causes "output offset" of magnitude $(I_B)R_{FB}$.

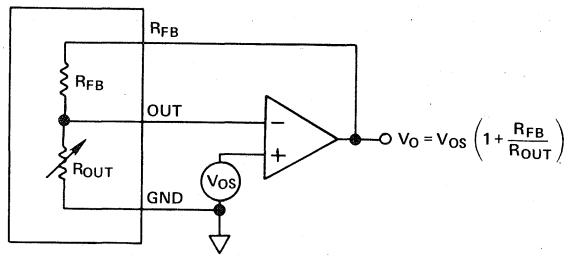


Figure 3. Noise Gain Equivalent Circuit

High Frequency Amplifiers

R_{FB} and C_{OUT} create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 5–20pF of feedback capacitance ensures stability.

APPLICATION HINTS

1. If an output voltage range of ±19.99 volts is required (i.e., AD7525 V_{IN} = ±10V, BCD = 1.999), a high voltage output amplifier with appropriate supply voltages must be used.
2. To maintain circuit linearity, the op amp offset voltage should not exceed 2% of the circuit resolution. (Resolution = $V_{IN} \div 1000$)
3. CMOS logic inputs exhibit an input impedance on the order of 100MΩ. Whereas an "open" TTL input can be assumed to be a logic HIGH, an open CMOS input gate can only be assumed to be a logic MAYBE. Unused CMOS inputs must always be tied to a known logic state. If single-pole single-throw thumbwheel switches are used to drive the digital inputs of the AD7525, external 10kΩ pull-down (pull-up if switch coding is complementary BCD) resistors must be used.

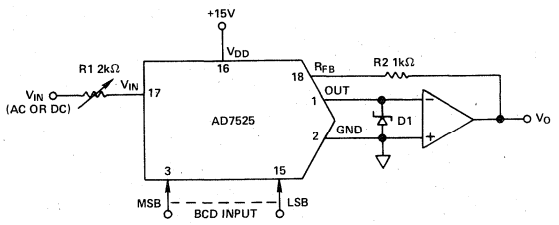


Figure 4. Digitally Controlled Attenuator Circuit

BCD INPUT					ANALOG OUTPUT	
	Digital Input			Equivalent Decimal Input	V_O/V_{IN}	V_O
1.0	0.1	0.01	0.001			
1	1001	1001	1001	1.999	-1.999	$-1.999V_{IN}$
1	0000	0000	0001	1.001	-1.001	$-1.001V_{IN}$
1	0000	0000	0000	1.000	-1.000	$-1.000V_{IN}$
0	1001	1001	1001	0.999	-0.999	$-0.999V_{IN}$
0	0101	0000	0000	0.500	-0.500	$-0.500V_{IN}$
0	0000	0000	0000	0.000	0	0

Note 1:
For proper BCD coding, the 0.1 digit, 0.01 digit or 0.001 digit must not exceed BCD "9" (1001).

Table 1. Analog Input/Output Relationship vs. Digital Input

CALIBRATION PROCEDURE

Offset Adjustment:

1. Apply BCD code 0.000 (0 0000 0000 0000) to the AD7525 digital inputs.
2. Connect a high resolution, high impedance voltmeter between pins 1 and 2 of the AD7525.
3. Adjust amplifier's trimpot for minimum reading on the voltmeter (<100μV).

Gain Adjustment:

1. Apply BCD code 1.000 (1 0000 0000 0000) to the AD7525 digital input.
2. Apply +10V to the V_{IN} input of Figure 1.
3. Connect the voltmeter between V_O (amplifier output) and pin 2 of the AD7525.
4. Adjust R_1 until $V_O = -10V$.

APPLICATION – THUMBWHEEL SWITCH ATTENUATOR

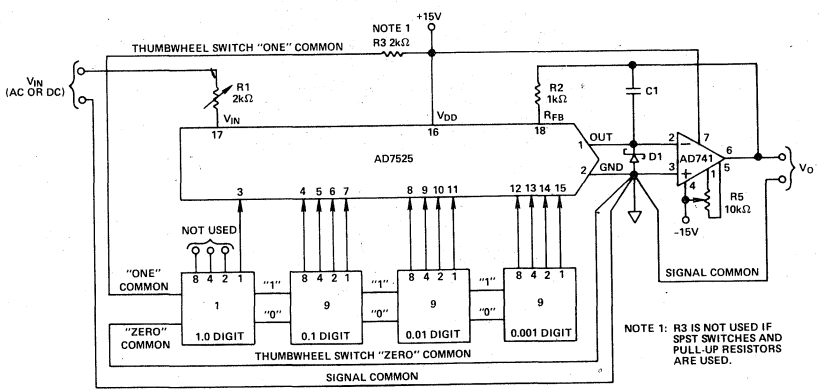


Figure 5. Thumbwheel Switch Attenuator

The circuit shown in Figure 5 is a precision voltage divider similar to 10-turn pots and thumbwheel switch incremental-voltage-divider assemblies. Advantages of the circuit are:

- ☐ Economy
- ☐ Low Output Impedance
- ☐ Resolution 0.1% V_{IN}
- ☐ Excellent Repeatability Accuracy
- ☐ Overrange Capability

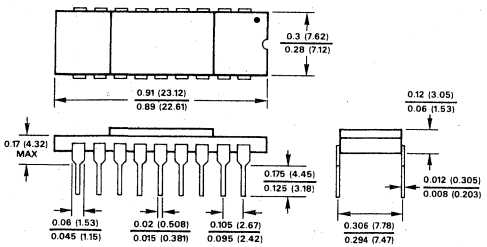
The BCD coded thumbwheel assembly applies BCD data to the AD7525 digital inputs. The switch assembly shown has single-pole-double-throw action, thus the BCD inputs are pulled either to +15V or GND (available from AMP, Harrisburg, PA; CHERRY, Waukegan, Illinois; or SAE, Santa Clara, California). Resistor R_3 limits current if make-before-break switches are used. SPST switch assemblies can be used; however, appropriate pull-up or pull-down resistors must be used on each digital input, depending upon whether the switch coding is BCD or complementary BCD. This ensures each digital input has appropriate V_{IH} or V_{IL} levels applied.

Resistors R_1 and R_2 provide gain adjustment capability. R_5 is used to adjust the amplifier offset voltage (as measured between the amplifier input terminals) to less than 100μV. Diode D_1 (HSCH 1001) provides AD7525 output protection (see Caution note 3).

MECHANICAL INFORMATION

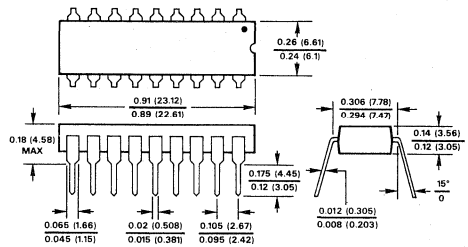
Dimensions shown in inches and (mm).

18 PIN CERAMIC DIP



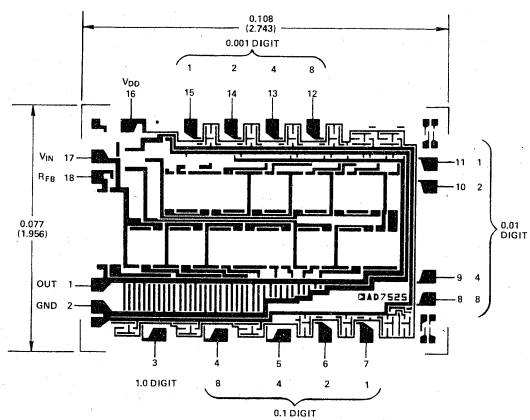
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD-PLATED (50 MICROINCHES MIN)
KOVAR OR ALLOY 42

18 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

BONDING DIAGRAM



NOTES:
1. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN IN PIN CONFIGURATION.
2. PAD 2 (GND) SHOULD BE BONDED FIRST TO MINIMIZE ESD HAZARDS.
3. PADS ARE 0.004in X 0.004in (0.102mm X 0.102mm).

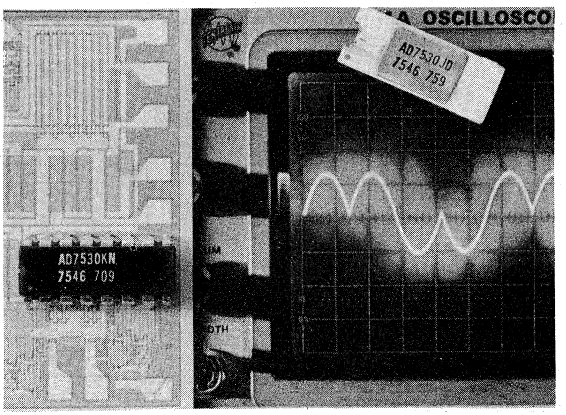
SEE ANALOG DEVICES CHIP CATALOG
FOR ADDITIONAL CHIP INFORMATION

CMOS 10- & 12-Bit Monolithic Multiplying D/A Converters

AD7530, AD7531

FEATURES
AD7530: 10-Bit Resolution
AD7531: 12-Bit Resolution
8-, 9- and 10-Bit Linearity
DTL/TTL/CMOS Compatible
Nonlinearity Tempco: 2ppm of FSR/°C
Low Power Dissipation: 20mW
Current Settling Time: 500ns
Feedthrough Error: 10mV p-p @ 50kHz
Low Cost

Note: AD7533 is recommended for new 10-bit designs. AD7541, AD7542 or AD7543 is recommended for new 12-bit designs.



GENERAL DESCRIPTION

The AD7530 (AD7531) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The device uses advanced CMOS and thin film technologies providing up to 10-bit accuracy with DTL/TTL/CMOS compatibility.

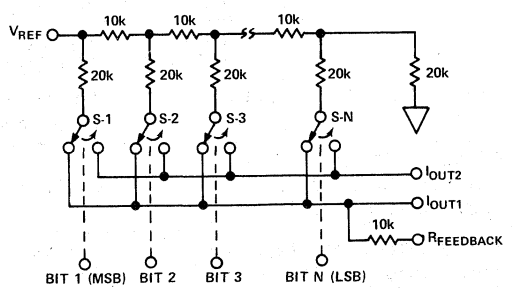
The AD7530 (AD7531) operates from a +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

ORDERING INFORMATION

Nonlinearity	Temperature Range	
	0 to +70°C	−25°C to +85°C
0.2% (8-Bit)	AD7530JN	AD7530JD
	AD7531JN	AD7531JD
0.1% (9-Bit)	AD7530KN	AD7530KD
	AD7531KN	AD7531KD
0.05% (10-Bit)	AD7530LN	AD7530LD
	AD7531LN	AD7531LD

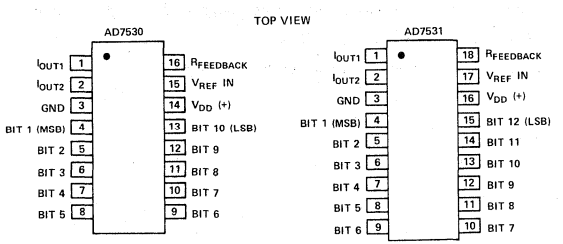
FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7530: N = 10
AD7531: N = 12
(Switches shown in "High" state)

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER		AD7530	AD7531	TEST CONDITIONS
DC ACCURACY (Note 1)				
Resolution		10 Bits	12 Bits	
Nonlinearity	AD7530J	0.2% of FSR max (8 Bit)	*	
	AD7530K	0.1% of FSR max (9 Bit)	*	
	AD7530L	0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco		2ppm of FSR/°C max	*	$-10V < V_{REF} < +10V$
Gain Error		0.3% of FSR typ	*	
Gain Error Tempco		10ppm of FSR/°C max	*	
Output Leakage Current (Either Output)		300nA max	*	Over specified temperature range.
Power Supply Rejection		50ppm of FSR/% typ	*	
AC ACCURACY				To 0.05%
Output Current Settling Time		500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error		10mV p-p max	*	V_{REF} = 20V p-p, 50kHz. All digital inputs low
REFERENCE INPUT		±10V	*	
Input Range		±1mA	*	
Input Resistance		10kΩ typ	*	
ANALOG OUTPUT				
Output Current Range (Both Outputs)		±1mA	*	
Output Capacitance	I_{OUT1}	120pF typ	*	All digital inputs high
	I_{OUT2}	37pF typ	*	
	I_{OUT1}	37pF typ	*	All digital input low
	I_{OUT2}	120pF typ	*	
Output Noise (Both Outputs)		Equivalent to 10kΩ Johnson noise typ	*	
DIGITAL INPUTS (Note 2)				
Low State Threshold		0.8V max	*	Over specified temperature range
High State Threshold		2.4V min	*	Over specified temperature range
Input Current (low to high state)		1μA typ	*	
Input Coding		Binary	*	See Tables 1 & 2
POWER REQUIREMENTS				
Power Supply Voltage Range		+5V to +15V	*	
I_{DD}		5nA typ	*	All digital inputs at GND
		2mA max	*	All digital inputs high or low
Total Dissipation		20mW typ	*	

NOTES:
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

*Same specifications as for AD7530.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to Gnd) . . . . . +17V
V_{REF} (to Gnd) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to Gnd
Voltage at Pin 1, Pin 2 . . . . . −100mV to V_{DD}
Power Dissipation (package)
up to +75°C 450mW
Operating Temperature
JN, KN, LN Versions . . . . . 0 to +75°C
JD, KD, LD Versions . . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 1 shows the circuit connections required for unipolar operation. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1. Protection Schottky shown is not required when using TRI-FET output amplifiers such as the AD542 or AD544.

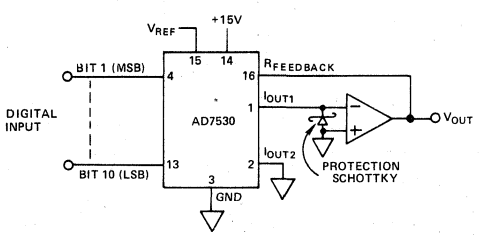


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table 1. Code Table — Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 2 illustrates the AD7530 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})\,(10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal. Protection Schottky is not required if using TRIFET output amplifiers such as the AD542 or AD544.

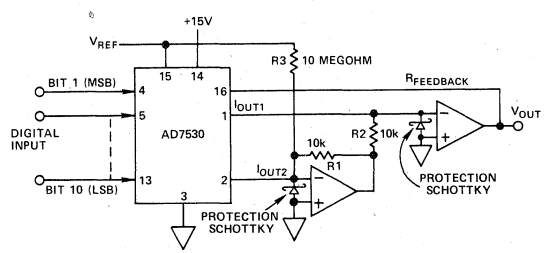


Figure 2. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table 2. Code Table — Bipolar (Offset Binary) Operation

TERMINOLOGY

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

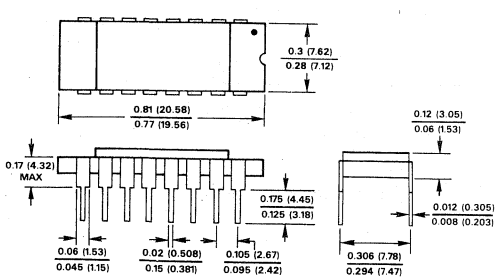
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

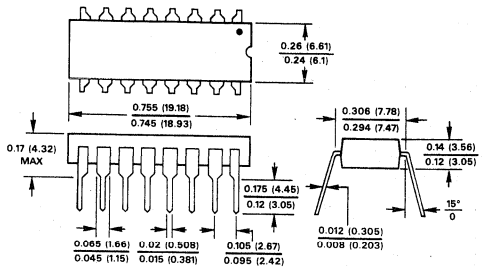
AD7530

16 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

16 PIN PLASTIC DIP



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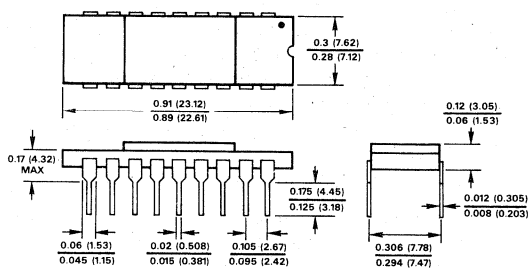
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

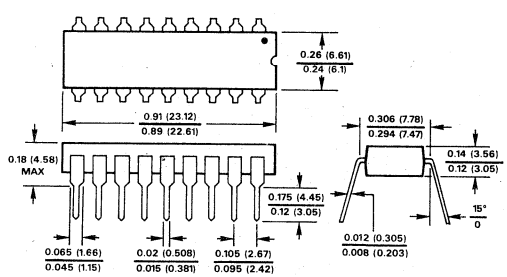
AD7531

18 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

18 PIN PLASTIC DIP

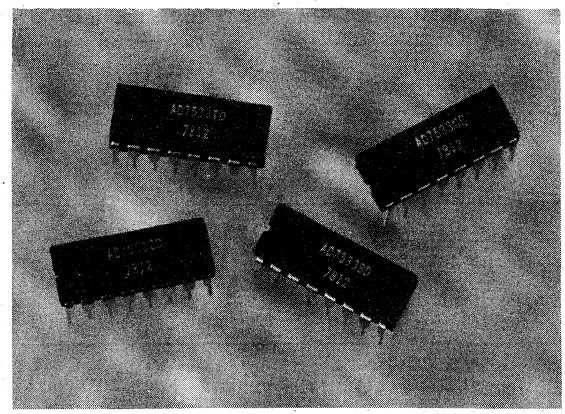


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

CMOS
Low Cost 10-Bit Multiplying DAC
AD7533

FEATURES
- Lowest Cost 10-Bit DAC
- Low Cost AD7520 Replacement
- Linearity: 1/2, 1 or 2LSB
- Low Power Dissipation
- Full Four-Quadrant Multiplying DAC
- CMOS/TTL Direct Interface
- Latch Free (Protection Schottky not Required)

APPLICATIONS
- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control



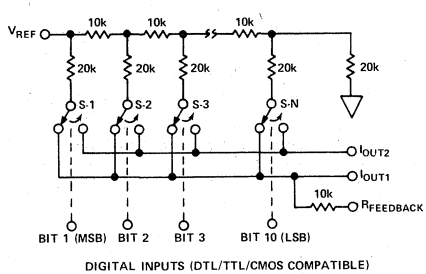
GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

FUNCTIONAL DIAGRAM



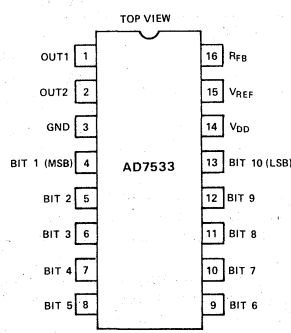
Logic: A switch is closed to $I_{OUT\ 1}$ for its digital input in a "HIGH" state.

ORDERING INFORMATION

Nonlinearity	Temperature Range and Package		
	Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Military (Ceramic) -55°C to +125°C
±0.2%	AD7533JN	AD7533AD AD7533AD/883B[1]	AD7533SD AD7533SD/883B[1]
±0.1%	AD7533KN	AD7533BD AD7533BD/883B[1]	AD7533TD AD7533TD/883B[1]
±0.05%	AD7533LN	AD7533CD AD7533CD/883B[1]	AD7533UD AD7533UD/883B[1]

[1] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for Class B device.

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range[1]	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Nonlinearity[2,3]			
AD7533JN, AD, SD	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD	±0.05% FSR max	±0.05% FSR max	
Gain Error[3,4,5]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[6]			
ΔGain/ΔV_{DD}	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2} (pin 2)	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[7]	800ns[6]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[6]	±0.1% FSR max[6]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sinewave.
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[8]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max[6]	100pF max[6]	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	35pF max[6]	35pF max[6]	
C_{OUT1} (pin 1)	35pF max[6]	35pF max[6]	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max[6]	100pF max[6]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}[3]	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}[3]	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}[3]	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	5pF max[6]	5pF max[6]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[6]	+5V to +16V	+5V to +16V	Functionality with degraded performance
I_{DD}[3]	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}
I_{DD}[3]	100μA max	150μA max	Digital Inputs = 0V or V_{DD}

NOTES:
[1] Plastic (JN, KN, LN versions): 0 to +70°C
Commercial Ceramic (AD, BD, CD versions): -25°C to +85°C
Military Ceramic (SD, TD, UD versions): -55°C to +125°C
[2] "FSR" is Full Scale Range.
[3] Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I_{DD} at +25°C and +125°C (SD, TD, UD versions) or +25°C and +85°C (AD, BD, CD versions).
[4] Full Scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$
[5] Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.
[6] Guaranteed, not tested.
[7] AC parameter, sample tested to ensure specification compliance.
[8] Absolute temperature coefficient is approximately -300ppm/°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0.3V, +17V
R_{FB} to GND . . . . . ±25V
V_{REF} to GND. . . . . ±25V
Digital Input Voltage Range . . . . . -0.3V to V_{DD}
Output Voltage (pin 1, pin 2) . . . . . -0.3V to V_{DD}
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C. 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C. 450mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial (JN, KN, LN versions) . . . . . 0 to +70°C
Industrial (AD, BD, CD versions) . . . . . -25°C to +85°C
Military (SD, TD, UD versions) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher the V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).

TERMINOLOGY

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

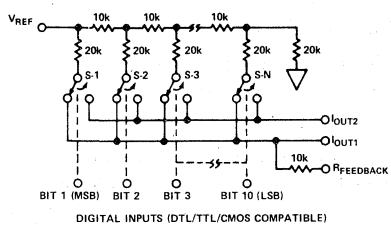


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20 ohms, switch 2 or 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

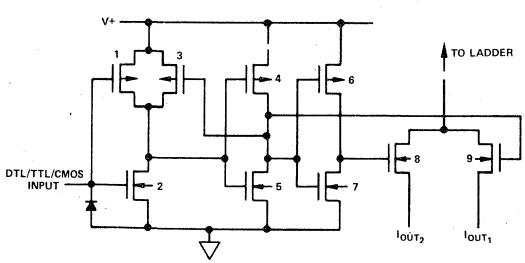


Figure 2. CMOS Switch

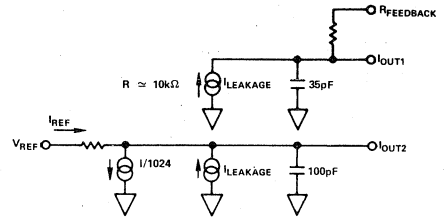


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 30pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

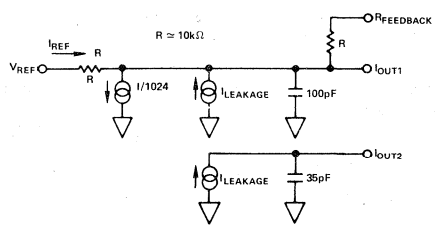
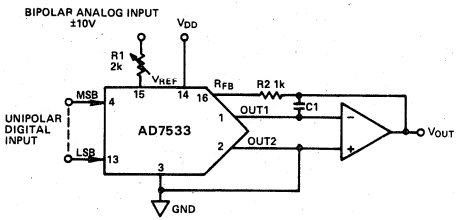


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

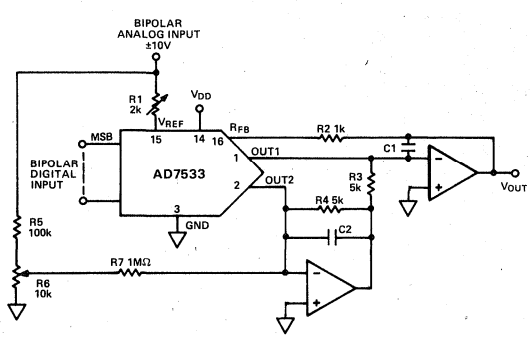
Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 1)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:
1. Nominal Full Scale for the circuit of Figure 5 is given by FS = $-V_{REF}\left(\frac{1023}{1024}\right)$
2. Nominal LSB magnitude for the circuit of Figure 5 is given by LSB = $V_{REF}\left(\frac{1}{1024}\right)$

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED
3. C1, C2 PHASE COMPENSATION (5 - 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

Figure 6. Bipolar Operation (4-Quadrant Multiplication)

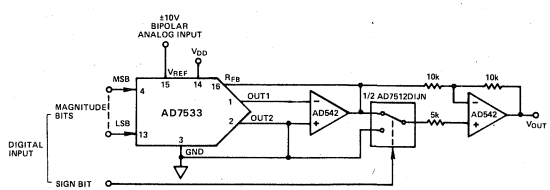
DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 2)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:
1. Nominal Full Scale Range for the circuit of Figure 6 is given by FSR = $V_{REF}\left(\frac{1023}{512}\right)$
2. Nominal LSB magnitude for the circuit of Figure 6 is given by LSB = $V_{REF}\left(\frac{1}{512}\right)$

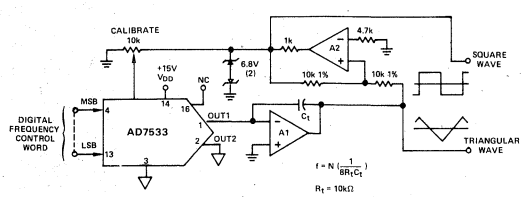
Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS

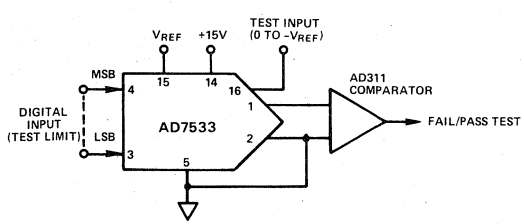
10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR

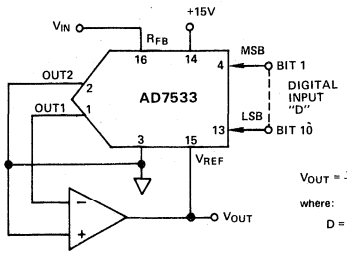


DIGITALLY PROGRAMMABLE LIMIT DETECTOR



APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



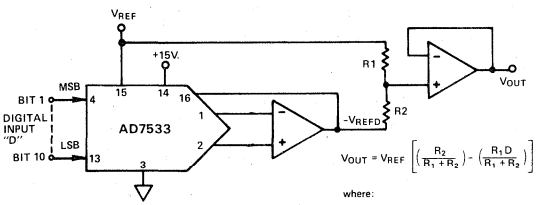
$$V_{OUT} = \frac{-V_{IN}}{D}$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$0 < D \leq \frac{1023}{1024}$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1+R_2}\right) - \left(\frac{R_1 D}{R_1+R_2}\right)\right]$$

where:

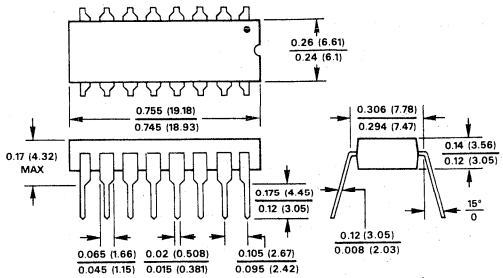
$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$\left(0 \leq D \leq \frac{1023}{1024}\right)$$

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

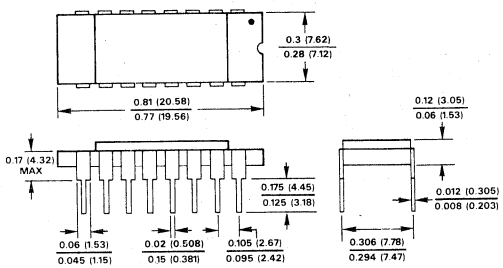
16 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

LEADS ARE SOLDER PLATED KOVAR

16 PIN CERAMIC DIP

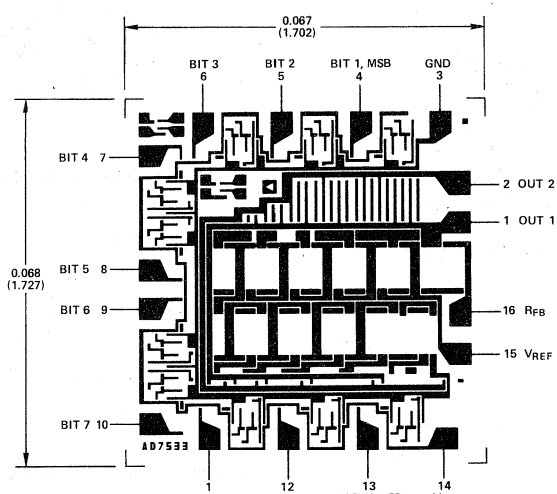


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

LEADS ARE GOLD-PLATED (50 MICROINCHES MIN.) KOVAR

BONDING DIAGRAM

Dimensions shown in inches and (mm).



NOTES:

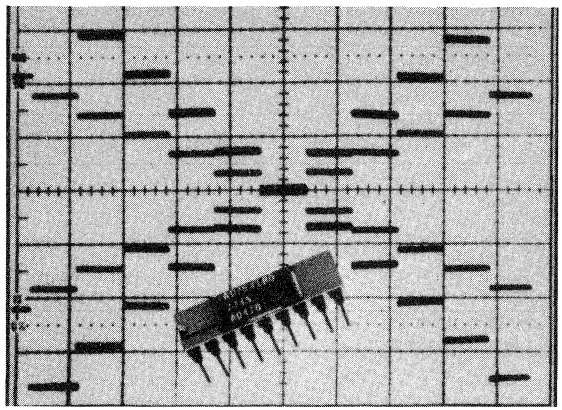
1. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN IN PIN CONFIGURATION ON PAGE 9-95.
2. PAD 3 (GND) SHOULD BE BONDED FIRST TO MINIMIZE ESD HAZARDS.
3. PADS ARE 0.004 X 0.004 (0.102 X 0.102).

CMOS 12-Bit Monolithic Multiplying DAC

AD7541

FEATURES
- Full Four Quadrant Multiplication
- 12-Bit Linearity (0.01%)
- Pretrimmed Gain
- TTL/CMOS Compatible
- Low Power Comsumption
- Low Feedthrough Error
- Low Cost

APPLICATIONS
- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratiometric A/D Conversion
- Function Generation



GENERAL DESCRIPTION

The Analog Devices AD7541 is a low cost, high performance 12-bit monolithic multiplying digital-to-analog converter fabricated using advanced double-layer-metal CMOS technology and packaged in a standard 18-pin DIP.

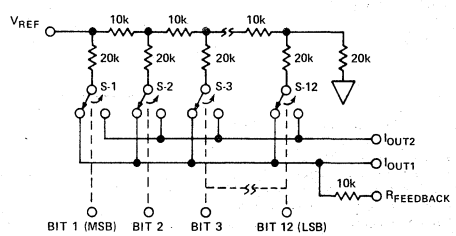
Pin compatible with the AD7521, this new device uses laser wafer trimming to provide full 12-bit linearity and excellent absolute accuracy.

The inherently low power dissipation, coupled with the current switching R-2R ladder, ensures that the performance is maintained over the full temperature range.

ORDERING INFORMATION

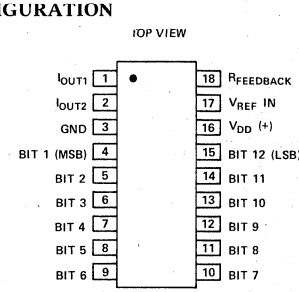
	Temperature Range and Package		
Nonlinearity	Plastic 0 to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
0.02%	AD7541JN	AD7541AD	AD7541SD
0.01%	AD7541KN	AD7541BD	AD7541TD

FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

PIN CONFIGURATION



MIL STD-883B PROCESSING

/883B versions are 100% screened to MIL STD 883, method 5004 para 3.1.1. through 3.1.12. for a class B device. Final electrical tests are: nonlinearity, gain error, output leakage current V_{INH}, V_{INL} input leakage current and I_{DD} at +25°C and +85°C (AD and BD versions) or +25°C and +125°C (SD and TD versions).

SPECIFICATIONS (V_{DD} = 15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = min-max	TEST CONDITION
STATIC ACCURACY			
Resolution	12 Bits min	12 Bits min	
Nonlinearity			V_{OUT1} =
AD7541JN, AD7541AD, AD7541SD[1]	±0.02% FSR[2] max	±0.02% FSR max	V_{OUT2} = 0V
AD7541KN, AD7541BD, AD7541TD[3]	±0.01% FSR max	±0.01% FSR max	
Gain Error[2,4,5]	±0.3% FSR max	±0.4% FSR max	Max full scale change from T_A = +25°C to T_{min} or T_{max} is ±0.1%.
Power Supply Rejection	±0.01% per % max	±0.02% per % max	V_{DD} = 14.5V – 15.5V
Output Leakage Current	±50nA max	±200nA max	V_{REF} = ±10V
DYNAMIC PERFORMANCE			
Output Current Settling Time[6]	1μs max	1μs max	To 0.01% of FSR
Feedthrough Error[6]	1mV p-p max	1mV p-p max	V_{REF} = 20V p-p @ 10kHz
REFERENCE INPUT			
Input Resistance	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max	
DIGITAL INPUTS			
V_{INH}	2.4V max	2.4V max	
V_{INL}	0.8V min	0.8V min	
Input Leakage Current	±1μA max	±1μA min	V_{IN} = 0 or 15V
Input Capacitance[6]	8pF max	8pF max	
Input Coding	Binary or Offset Binary (see Page 9-105)		
ANALOG OUTPUTS			
Output Capacitance[6]			
C_{OUT1}	200pF max	200pF max	Digital Inputs
C_{OUT2}	60pF max	60pF max	= V_{INH}
C_{OUT1}	60pF max	60pF max	Digital Inputs
C_{OUT2}	200pF max	200pF max	= V_{INL}
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Accuracy is not guaranteed over this range.
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES
[1] J, A and S versions are monotonic to 11 bits.
[2] FSR is Full Scale Range.
[3] K, B and T versions are monotonic to 12 bits.
[4] Using internal feedback resistor.
[5] Max gain change from +25°C to T_{min} or T_{max} is ±0.1% FSR max.
[6] Guaranteed by design, not subject to test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . –0.3V to V_{DD}
Power Dissipation (Package)
Up to +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C
Operating Temperature
JN, KN Versions . . . . . 0 to +70°C
AD, BD Versions. . . . . –25°C to +85°C
SD, TD Versions . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused inputs in conductive foam at all times.

SPECIFICATION DEFINITIONS

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

TYPICAL PERFORMANCE CHARACTERISTICS

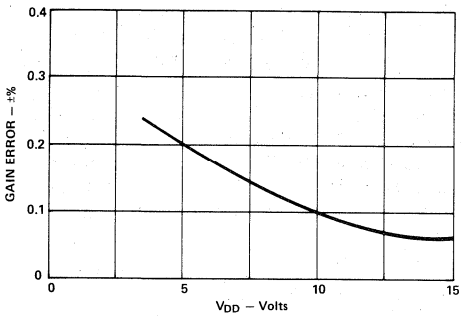


Figure 1. Gain Error vs. Supply Voltage

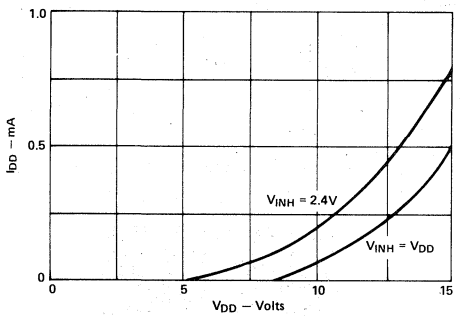


Figure 2. Supply Current vs. Supply Voltage

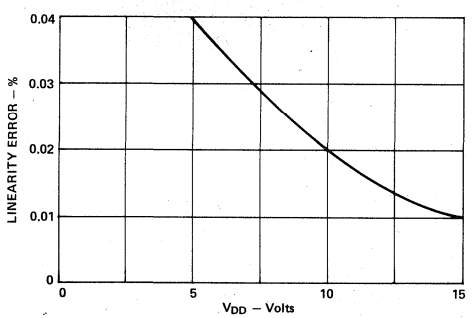


Figure 3. Linearity Error vs. Supply Voltage

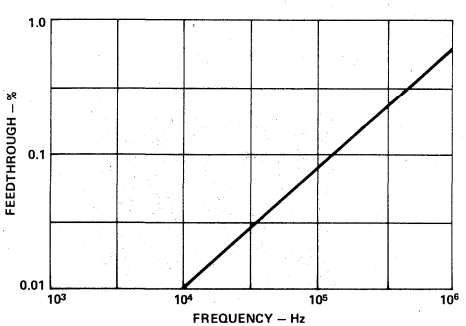


Figure 4. Feedthrough Error vs. Frequency

APPLICATION HINTS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and the output amplifiers non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifiers offset voltage and bias current is necessary.

The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent the absolute maximum rating for V_{OUT1} and V_{OUT2} being exceeded.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7541, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 5. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

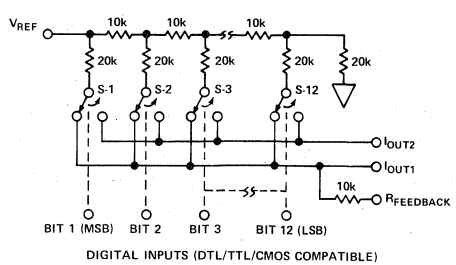


Figure 5. AD7541 Functional Diagram (Inputs "HIGH")

One of the CMOS current switches is shown in Figure 6. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 6 was designed for an "ON" resistance of 10 ohms, switch 2 of 20 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on,

thus maintaining a constant 5mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

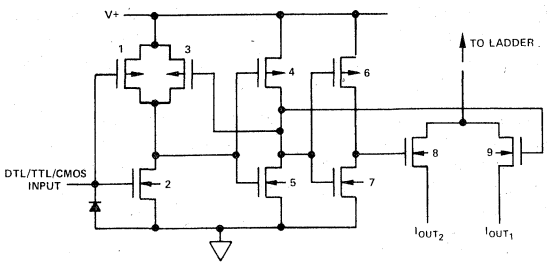


Figure 6. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 7 and 8. In Figure 7 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the 1/4096 current source represents a constant 1-bit current drain through the

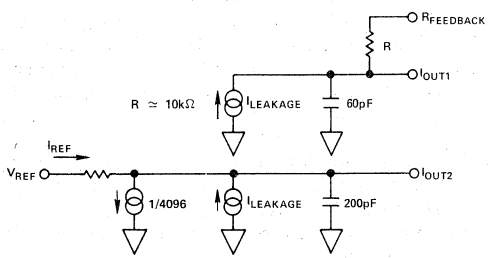


Figure 7. AD7541 Equivalent Circuit – All Digital Inputs Low

termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the I_{OUT2} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 8, is similar to Figure 7; however, the "ON" switches are now on terminal I_{OUT1}, hence the 200pF at that terminal.

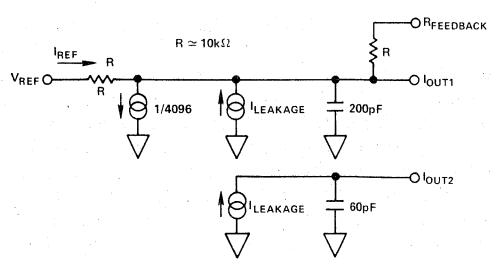


Figure 8. AD7541 Equivalent Circuit – All Digital Inputs High

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The preceding circuit analysis shows that the output capacitance is dependent upon the digital code, as is the output resistance. Looking back into I_{OUT1} the resistance seen is anything between 10kΩ ($R_{FEEDBACK}$ alone) and 5kΩ (R_{FB} in parallel with the 10kΩ network resistance).

This variation affects both static accuracy and dynamic performance. The effect on static accuracy is further considered on pages 9-105 and 9-106. The dynamic performance of the AD7541 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

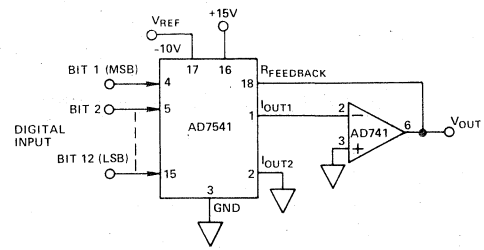


Figure 9. DAC Circuit Using AD741K

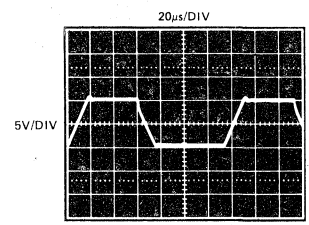


Figure 10. Output Waveform

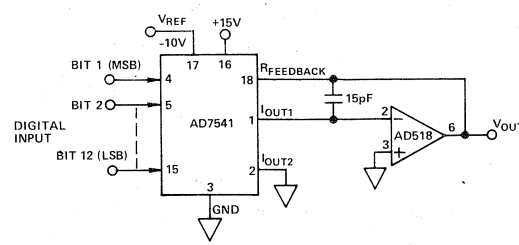


Figure 11. DAC Circuit Using AD518K

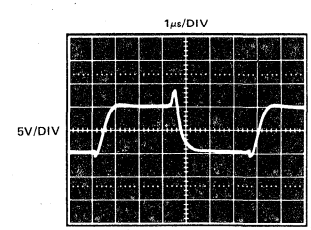


Figure 12. Output Waveform

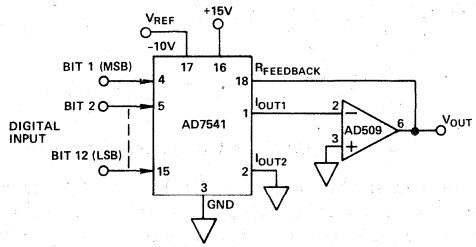


Figure 13. DAC Circuit Using AD509K

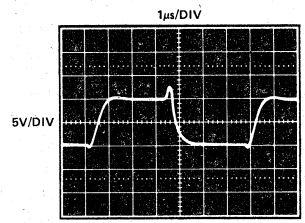


Figure 14. Output Waveform

The circuits and waveforms shown in Figures 9 to 14 are representative of the three principal types of output amplifiers. A general purpose low drift (AD741K), a high speed low cost (AD518), and a fast settling unit (AD509).

Points to remember when applying high speed amplifiers include:

1. Protection diodes as shown in Figures 15 and 16.
2. Phase compensation for the DAC's output capacitance.
3. Power supply decoupling and correct load earthing.

APPLICATIONS

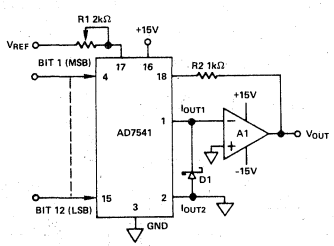


Figure 15. Unipolar Binary Operation

UNIPOLAR BINARY OPERATION

The connections required for unipolar digital binary operation are shown above. V_{REF} may be positive or negative so 2-quadrant multiplication may be performed. Schottky diode D1 (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers. The diodes are not required when using TRI-FET amplifiers such as the AD542 or AD544.

BIPOLAR (4-QUADRANT) BINARY OPERATION

The digital input is offset binary coded and multiplies V_{REF} according to Table 2. Resistors R1 and R2 should be equal within 0.1% at all temperatures, but need not track the resistors within the AD7541. D1 and D2 perform the same

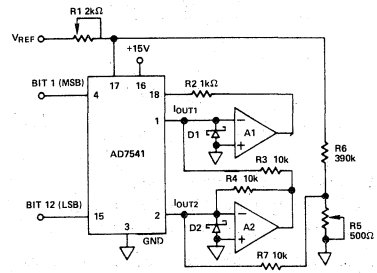


Figure 16. Bipolar (4-Quadrant) Binary Operation

function as in Figure 15. Network R5, R6, R7 sum 1/2LSB of current into I_{OUT2} to ensure correct coding at zero.

R1 can be adjusted to produce the outputs shown in Table 1. However, it is recommended that when the application permits it, R1 and R2 be committed. The maximum gain error in this condition is 0.3% of full scale. The offset voltage of amplifier A1 should be adjusted to less than 0.5mV over the temperature range.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99975 V_{REF}
100000000000	-0.50000 V_{REF}
011111111111	-0.49975 V_{REF}
000000000000	0

Table 1. Code Table for Circuit of Figure 15.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99951 V_{REF}
100000000001	-0.00049 V_{REF}
100000000000	0
010000000000	+0.50000 V_{REF}
000000000000	+1.00000 V_{REF}

Table 2. Code Table for Circuit of Figure 16.

Amplifiers A1 and A2 should be adjusted to an input offset of less than 0.1mV and should be better than 0.5mV over the temperature range. With V_{REF} set to approximately 10V, R5 should be adjusted so that with code 10000000000 V_{OUT} = 0V ±0.2mV. R1 should be adjusted so that with code 000000000000 $V_{OUT} = V_{REF}$.

As with the unipolar circuit R1 and R2 can be omitted, with a resulting maximum gain error of 0.3% of full scale. R5 may be replaced by a 100Ω fixed resistor. The maximum zero error if this is done is 0.015% of F.S.R.

OUTPUT AMPLIFIER CONSIDERATIONS

It has already been pointed out that the DAC output resistance varies with the digital code. The effect this has on static accuracy will now be considered.

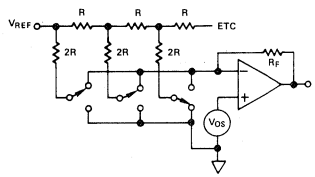


Figure 17.

$$\text{The error voltage} = V_{OS}\left(1 + \frac{R_F}{R_O}\right)$$

R_O is a function of the digital code.
$R_O \cong 10k\Omega$ for any more than 4-bits Logic 1.
$R_O \cong 30k\Omega$ for any single bit Logic 1.

The gain for offset, therefore, changes as follows:

$$\text{At code } 001111111111\ V_{ERROR1} = V_{OS}\left(1 + \frac{10k}{10k}\right) = 2\ V_{OS}$$

$$\text{At code } 010000000000\ V_{ERROR2} = V_{OS}\left(1 + \frac{10k}{30k}\right) = \frac{4}{3}\ V_{OS}$$

$$\text{The error difference is therefore } \frac{2}{3}\ V_{OS}$$

Since, for a 12-bit resolution DAC, one LSB has a weight (for V_{REF} = +10V) of 2.5mV, it is clearly important that V_{OS} be nulled, either using the amplifiers nulling facility or an external network.

It is important to realize that an offset can be caused by including the usual bias current compensation resistor in the amplifiers non-inverting input terminal. This should not be included. Instead the amplifier should have a bias current which is low over the temperature range of interest, and should certainly not exceed 75nA.

ANALOG/DIGITAL DIVISION

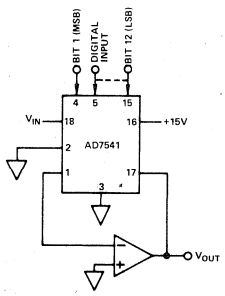


Figure 18. Analog/Digital Divider

With the AD7541 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 18, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero is not defined. With the LSB (Bit 12) ON, the gain is 4096. With all bits ON, the gain is 1 (±1LSB).

DIGITAL/SYNCHRO CONVERTER

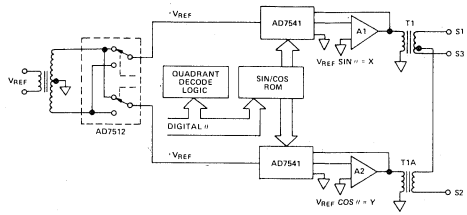


Figure 19. 14-Bit Digital to Synchro Converter

The low cost and high accuracy available from the AD7541, together with its bipolar multiplying capability is exploited fully in the circuit of Figure 19. V_{REF} is commonly 400Hz but by replacing the transformers with dc coupled circuits coordinate transformation may be performed.

The SIN/COS ROM is readily available at low cost and the AD7512 switch enables greater resolution to be obtained.

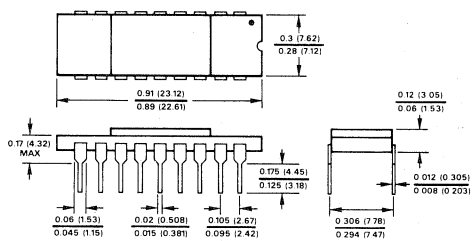
Resolver-to-synchro transformation is performed by the Scott connected pair T1 and T1A. The power available to the load connected to S1, S2 and S3 is determined by the amplifiers A1 and A2. A particular advantage of the circuit shown in Figure 19 is that it is invariant with respect to θ, and may be used to directly drive equipment such as CRT displays.

MECHANICAL INFORMATION

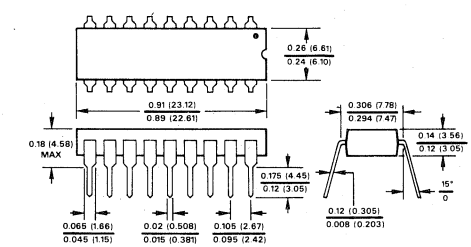
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

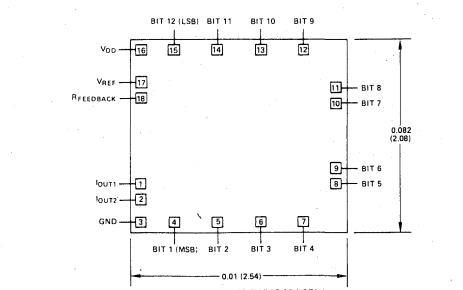
18 PIN CERAMIC DIP



18 PIN PLASTIC DIP



BONDING DIAGRAM



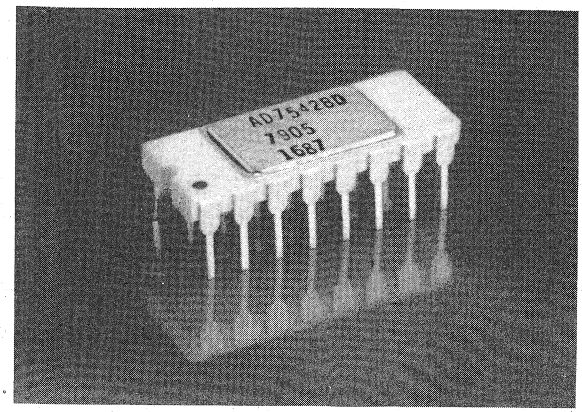
CMOS uP Compatible 12-Bit DAC

AD7542

PRELIMINARY TECHNICAL DATA

FEATURES

- Resolution: 12-Bits
- Nonlinearity: ±½LSB T_{min} to T_{max}
- Low Gain Drift: 2ppm/°C typ, 5ppm/°C max
- Microprocessor Compatible
- Full 4-Quadrant Multiplication
- Low Multiplying Feedthrough
- Low Power Dissipation: 40mW max
- Low Cost
- Small Size: 16 Pin DIP
- Latch Free (Protection Schottky Not Required)



GENERAL DESCRIPTION

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

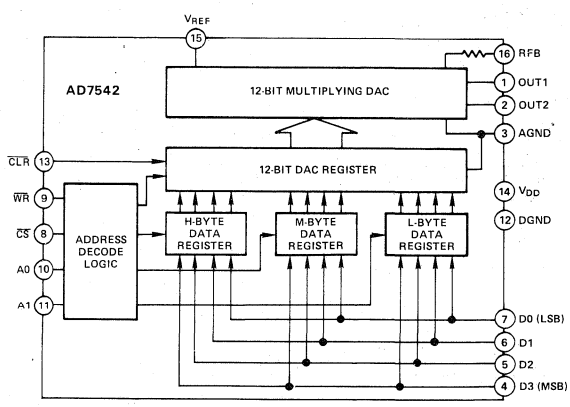
The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A Clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The AD7542 is manufactured using an advanced thin-film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16 pin DIP) and easy μP interface make the AD7542 ideal for many instrumentation and industrial control applications.

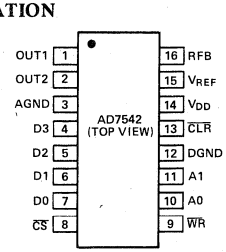
ORDERING INFORMATION

	Temperature Range and Package	
Nonlinearity	Plastic 0 to +70°C	Ceramic -25°C to +85°C
±1LSB	AD7542JN	AD7542AD
±1/2LSB	AD7542KN	AD7542BD

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

PARAMETER	Limit at T_A = +25°C	Limit at T_A = T_{min}, T_{max} [1]	UNITS	CONDITIONS/COMMENTS
ACCURACY				
Resolution	12	12	Bits	
Nonlinearity				
AD7542JN, AD	±1	±1	LSB max	
AD7542KN, BD	±1/2	±1/2	LSB max	
Differential Nonlinearity				
AD7542JN, AD	±2	±2	LSB max	AD7542JN and AD are monotonic to 11 bits over the full operating temperature range.
AD7542KN, BD	±1	±1	LSB max	AD7542KN and BD are guaranteed monotnoic over T_{min} to T_{max}
Gain Error (using internal RFB)	±0.3	±0.33	% FSR max[2]	DAC register loaded with 1111 1111 1111 Gain error is adjustable using the circuits of Figures 7 and 8.
Gain Change, +25°C to T_{min} or T_{max}		±0.03	% FSR max[2]	
dc Supply Rejection (Gain)				
$\Delta Gain/\Delta V_{DD}$	±0.005	±0.01	% per % max	V_{DD} = +4.5V to +5.0V
Output Leakage Current				
I_{OUT1} (pin 1)	±50	±200	nA max	DAC register loaded to 0000 0000 0000
I_{OUT2} (pin 2)	±50	±200	nA max	DAC register loaded to 1111 1111 1111
DYNAMIC PERFORMANCE				
Current Settling Time[3]	2.0	2.0	µs max	To 1/2LSB, OUT1 load = 100Ω, DAC output measured from falling edge of $\overline{WR}$
Multiplying Feedthrough Error[3]	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT				
Input Resistance (pin 15)	8/15/25	8/15/25	kΩ min/typ/max	
ANALOG OUTPUTS				
Output Capacitance				
C_{OUT1}[3]	75	75	pF max	DAC register loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	pF max	DAC register loaded to 0000 0000 0000
LOGIC INPUTS				
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	V max	
I_{IN}[5]	1	1	µA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 7 and 8). Data is loaded into data registers in 4-Bit bytes.			
SWITCHING CHARACTERISTICS[5]	(see Figure 2)			
t_{AWS1}	200	400	ns min	t_{AWS1}: Address valid-to-WRITE setup time (loading 4-Bit data registers)
t_{AWS2}	120	300	ns min	t_{AW2}: Address valid-to-WRITE setup time (loading 12-Bit DAC register)
t_{AWH}	50	65	ns min	t_{AWH}: Address-to-WRITE hold time
t_{CWS1}	180	350	ns min	t_{CWS1}: Chip select-to-WRITE setup time (loading 4-Bit data registers)
t_{CWS2}	60	150	ns min	t_{CWS2}: Chip select-to-WRITE setup time (loading 12-Bit DAC register)
t_{CWH}	50	100	ns min	t_{CWH}: Chip select-to-WRITE hold time
t_{WR}	120	220	ns min	t_{WR}: WRITE pulse width
t_{DS}	50	65	ns min	t_{DS}: Data setup time (loading 4-Bit data registers)
t_{DH}	50	65	ns min	t_{DH}: Data hold time (loading 4-Bit data registers)
t_{CLR}	200	300	ns min	t_{CLR}: Minimum CLEAR pulse width
POWER SUPPLY				
V_{DD} (Supply Voltage)	+5	+5	V	±5% for specified performance
I_{DD} (Supply Current)	8	8	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:
[1] Temperature Ranges as follows: AD7542JN, KN: 0 to +70°C
AD7542AD, BD: −25°C to +85°C
[2] FSR is Full Scale Range.
[3] Guaranteed but not tested.
[4] Logic inputs are MOS gates. Typical input current (+25°C) is iess than 1nA.
[5] Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to A_{GND} . . . . . 0V, +7V
V_{DD} to D_{GND} . . . . . 0V, +7V
A_{GND} to D_{GND} . . . . . V_{DD}
D_{GND} to A_{GND} . . . . . V_{DD}
Digital Input Voltage to D_{GND}
(pins 4 - 11, 13) . . . . . -0.3V, +15V
V_{PIN1}, V_{PIN2} to A_{GND} . . . . . -0.3V, +15V
V_{REF} to A_{GND} . . . . . ±25V
V_{RFB} to A_{GND} . . . . . ±25V
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial Plastic (JN, KN versions) . . . . . 0°C to +70°C
Industrial Ceramic (AD, BD versions) . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 secs.) . . . . . +300°C

TERMINOLOGY

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of –4095/4096. Gain error is adjustable using external trims as shown in Figures 7 and 8.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC register loaded to all 0's or at OUT2 with the DAC register loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0's.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

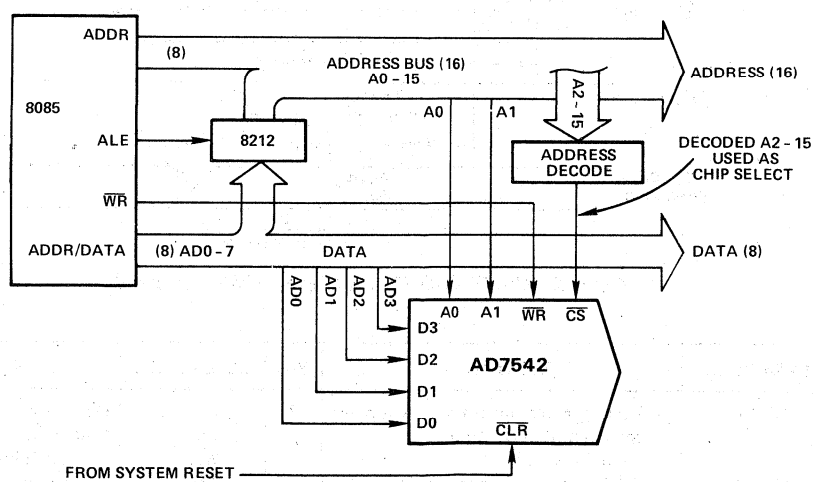


Figure 1. 8085/AD7542 Interface (Memory Mapped Output)

INTERFACE LOGIC

INTERFACE LOGIC INFORMATION

The AD7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown in Figure 1. CS is the decoded *device* address, and is derived by decoding the 14 higher order address bits. A_0 and A_1 is the AD7542 *operation* address, and is decoded internally in the AD7542 to point to the desired loading operation (i.e. load high byte, middle byte, low byte or DAC register). Table 1 shows the AD7542 truth table.

All data loading operations are identical to the write cycle of a RAM as shown in Figure 2.

Additionally, the CLR input allows the AD7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the AD7542 in a unipolar mode (Figure 7), a CLEAR causes the DAC output to assume 0V. In the bipolar mode (Figure 8), a CLEAR causes the DAC output to go to $-V_{REF}$.

In summary:

1. The AD7542 DAC register can be asynchronously cleared with the $\overline{CLR}$ input.
2. Each AD7542 requires 4 locations in memory.
3. Performing any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

AD7542 Control Inputs					AD7542 Operation	
A_1	A_0	$\overline{CS}$[6]	$\overline{WR}$[6]	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	1	1	No Operation Device Not Selected	
0	0	↓	0	1	Load LOW Byte[5] Data Register On Edges As Shown	Load Applicable Data Register With Data At $D_0 - D_3$
0	0	0	↓	1		
0	1	↓	0	1	Load MIDDLE Byte[5] Data Register On Edges As Shown	
0	1	0	↓	1		
1	0	↓	0	1	Load HIGH Byte[5] Data Register On Edges As Shown	
1	0	0	↓	1		
1	1	0	0	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers	
1	1	0	0	1		

NOTES:
[1] 1 indicates logic HIGH
[2] 0 indicates logic LOW
[3] X indicates don't care
[4] ↓ indicates LOW to HIGH transition
[5] MSB → XXXX XXXX XXXX ← LSB (high byte, middle byte, low byte)
[6] Although positive-going edge of either $\overline{CS}$ or $\overline{WR}$ will load Data Register, timing is optimized by using $\overline{WR}$ to latch data and using $\overline{CS}$ as a device enable.

Table 1. AD7542 Truth Table

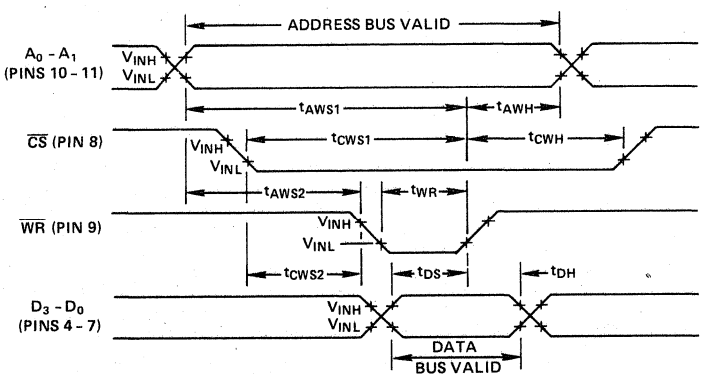


Figure 2. WRITE Cycle Timing Diagram (One 4-Bit Byte)

PIN	MNEMONIC	FUNCTION	PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground	7	D0	Data Input (LSB)
			8	$\overline{CS}$	Chip Select Input
			9	$\overline{WR}$	WRITE Input
2	OUT2	DAC current output bus. Normally terminated at ground	10	A0	Address Bus Input
			11	A1	Address Bus Input
3	AGND	Analog Ground	12	DGND	Digital Ground
4	D3	Data Input (MSB)	13	$\overline{CLR}$	Clear Input
5	D2	Data Input	14	V_{DD}	+5V Supply Input
6	D1	Data Input	15	V_{REF}	Reference Input
			16	R_{FB}	DAC Feedback Resistor

Table 2. Pin Function Descrption

GENERAL CIRCUIT INFORMATION

The AD7542, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 3. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the OUT_1 and OUT_2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

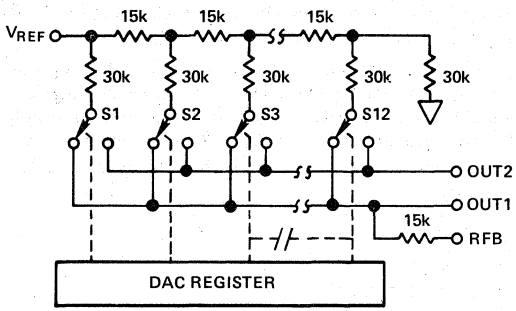


Figure 3. AD7542 Functional Diagram

One of the current switches is shown in Figure 4. The input resistance at V_{REF} (Figure 3) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

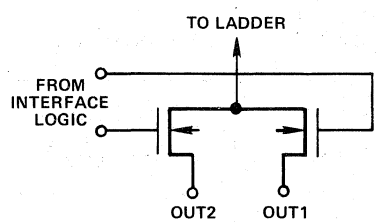


Figure 4. N-Channel Current Steering Switch

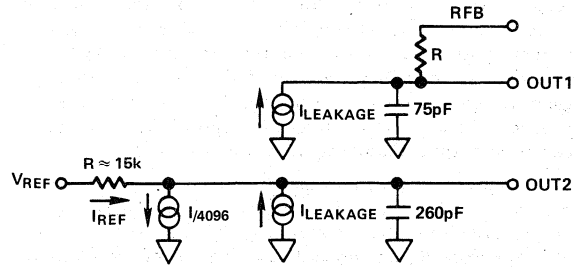


Figure 5. AD7542 DAC Equivalent Circuit All Digital Inputs LOW

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 5 and 6. In Figure 5 with all digital inputs LOW, the reference current is switched to OUT_2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT_2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT_1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 6, is similar to Figure 5; however, the "ON" switches are now on terminal OUT_1, hence the 260pF at that terminal.

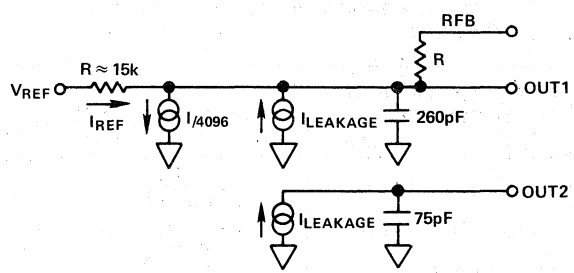


Figure 6. AD7542 DAC Equivalent Circuit All Digital Inputs HIGH

APPLYING THE AD7542

UNIPOLAR BINARY OPERATION (2 QUADRANT MULTIPLICATION)

Figure 7 shows the analog circuit connections required for unipolar binary (2 - quadrant multiplication) operation. The logic inputs are omitted for clarity. With a DC reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an AC reference voltage or current (again of + or – polarity) the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 3.

R_1 provides full scale trim capability [i.e. – load the DAC register to 1111 1111 1111, adjust R_1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R_1 and R_2 and trimming the reference voltage magnitude.

C_1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C_1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT_1).

Amplifier A_1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

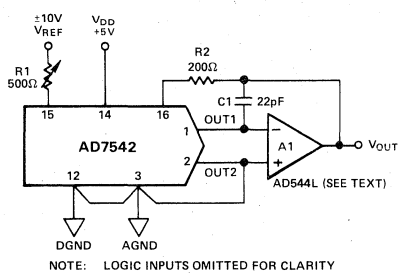


Figure 7. Unipolar Binary Operation (2-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 3. Unipolar Binary Code Table for Circuit of Figure 7

BIPOLAR OPERATION (4 QUADRANT MULTIPLICATION)

Figure 8 and Table 4 illustrate the circuitry and code relationship for bipolar operation. With a DC reference (positive or negative polarity) the circuit provides offset binary operation. With an AC reference, the eleven LSB's provide digitally controlled attenuation of the AC reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R_1 for $V_{OUT} = 0V$ (alternatively, one can omit R_1 and R_2 and adjust the ratio of R_3 to R_4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R_5.

As in unipolar operation, A_1 must be chosen for low V_{OS} and low I_B. R_3, R_4 and R_5 must be selected for matching and tracking. Mismatch of $2R_3$ to R_4 causes both offset and Full Scale error. Mismatch of R_5 to R_4 or $2R_3$ causes Full Scale error. C_1 phase compensation (10 to 25pF) may be required for stability.

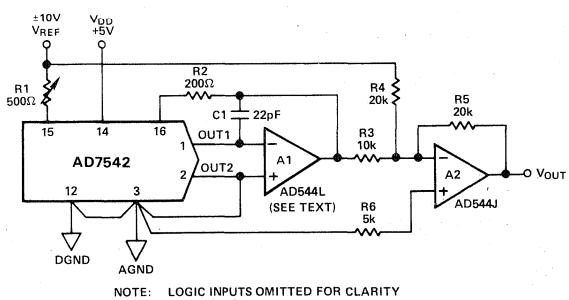


Figure 8. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 4. Bipolar Code Table for Offset Binary Circuit of Figure 8

APPLICATION HINTS

The AD7542 is a precision 12 - bit multiplying DAC designed for system interface. To ensure system performance consistent with AD7542 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7542 A_{GND} and D_{GND} cause loss of accuracy (DC voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at A_{GND} and D_{GND} are equal is to tie A_{GND} and D_{GND} together at the AD7542. In more complex systems where the A_{GND} - D_{GND} intertie is on the back - plane, it is recommended that diodes be connected back - to - back between the AD7542 A_{GND} and D_{GND} pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DAC's exhibit a code - dependent output resistance which in turn causes a code - dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output of magnitude $0.67V_{OS}$ (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}(2^{-n})$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

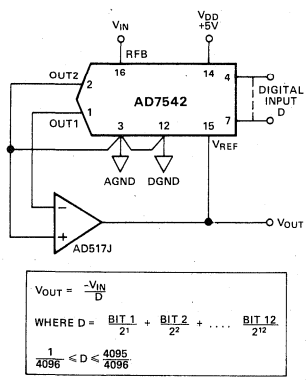


Figure 9. Divider (Digitally Controlled Gain)

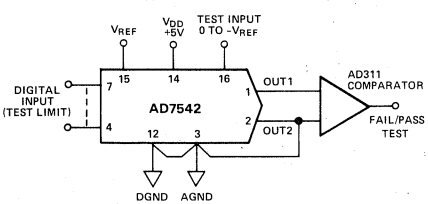


Figure 11. Digitally Programmable Limit Detector

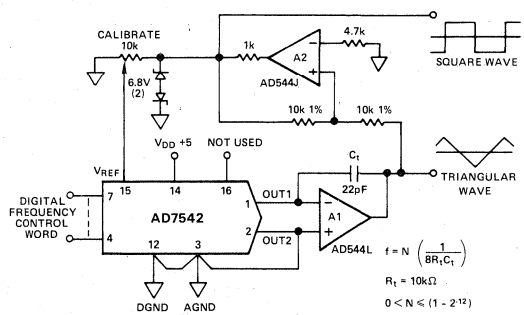


Figure 10. Programmable Function Generator

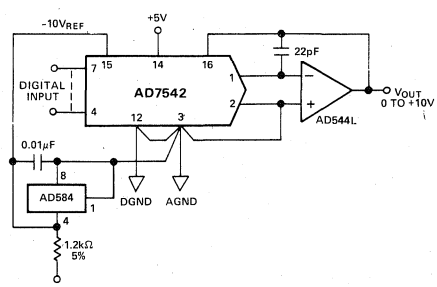


Figure 12. 0 to +10V Fixed Reference DAC

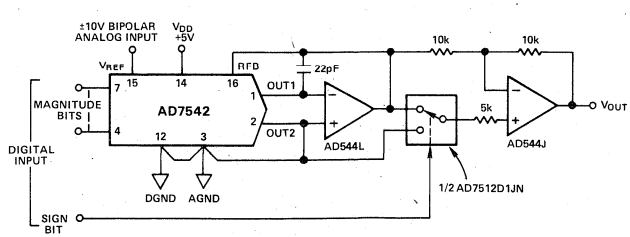


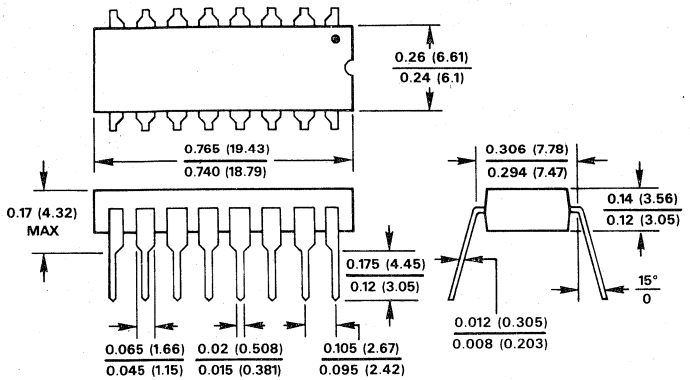
Figure 13. 12-Bit + Sign Multiplying DAC

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

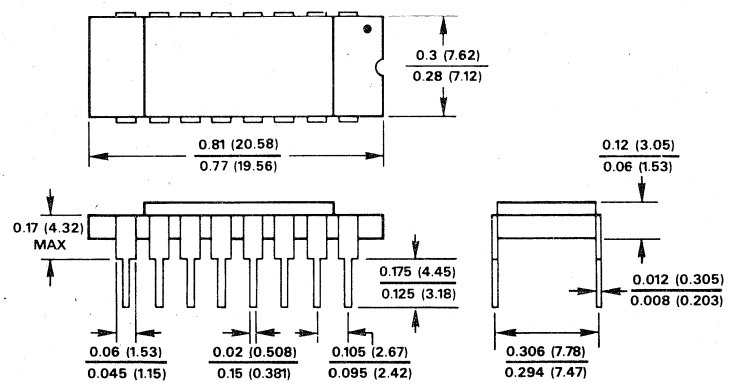
Dimensions shown in inches and (mm).

16 PIN PLASTIC DIP



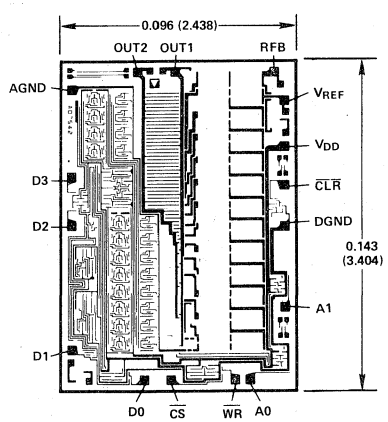
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

16 PIN CERAMIC DIP



1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. LEADS ARE GOLD PLATED (50 MICROINCHES MIN.) KOVAR OR ALLOY 42.

BONDING DIAGRAM



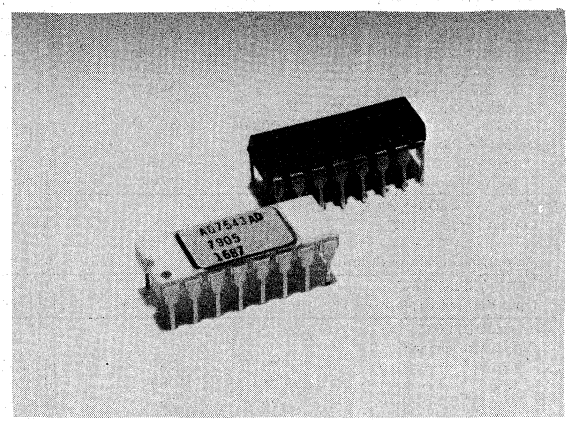
PADS ARE 0.004 X 0.004 INCHES (0.102 X 0.102mm) MIN.
TO MINIMIZE ESD HAZARD BOND DGND FIRST

ANALOG DEVICES

CMOS Serial Input 12-Bit DAC

AD7543

PRELIMINARY TECHNICAL DATA



FEATURES

- Resolution: 12 Bits
- Nonlinearity: ±1/2LSB T_{min} to T_{max}
- Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max
- Serial Load on Positive or Negative Strobe
- Asynchronous CLEAR Input for Initialization
- Full 4-Quadrant Multiplication
- Low Multiplying Feedthrough: 1LSB max @ 10kHz
- Requires no Schottky Diode Output Protection
- Low Power Dissipation: 40mW max
- +5V Supply
- Small Size: 16-Pin DIP
- Low Cost

GENERAL DESCRIPTION

The AD7543 is a precision 12-bit monolithic CMOS multiplying DAC designed for serial interface applications.

The DAC's logic circuitry consists of a 12-bit serial-in parallel-out shift register (Register A) and a 12-bit DAC input register (Register B). Serial data at the AD7543 SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input. Once Register A is full its contents are loaded into Register B under control of the LOAD inputs.

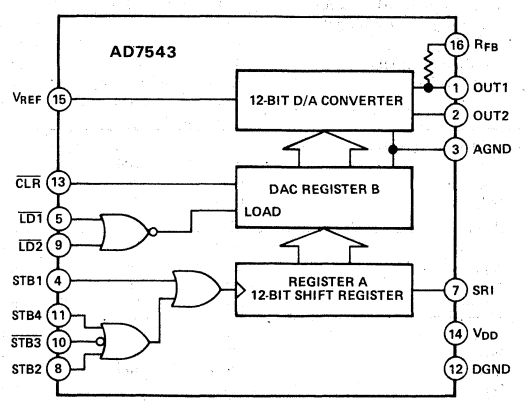
Initialization is simplified by the use of the CLR input which provides an asynchronous reset of Register B.

Packaged in a 16-pin DIP, the AD7543 features excellent gain T.C. (2ppm/°C typ; 5ppm/°C max), +5V operation and latch-free operation. (No protection Schottky diodes required.)

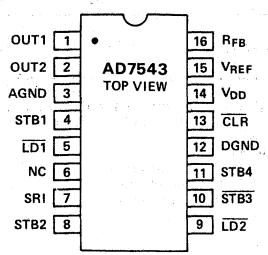
ORDERING INFORMATION

	Temperature Range and Package	
Nonlinearity	Plastic 0 to +70°C	Ceramic -25°C to +85°C
±1LSB	AD7543JN	AD7543AD
±1/2LSB	AD7543KN	AD7543BD

AD7543 FUNCTIONAL DIAGRAM



PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, unless otherwise noted)

PARAMETER	Limit at T_A = 25°C	Limit at T_A = T_{min}, T_{max} [1]	UNITS	CONDITIONS/COMMENTS
ACCURACY				
Resolution	12	12	Bits	
Nonlinearity				
AD7543JN, AD	±1	±1	LSB max	
AD7543KN, BD	±1/2	±1/2	LSB max	
Differential Nonlinearity				
AD7543JN, AD	±2	±2	LSB max	AD7543JN and AD are monotonic to 11 bits, T_{min} to T_{max}
AD7543KN, BD	±1	±1	LSB max	AD7543KN and BD are guaranteed 12-bit monotonic, T_{min} to T_{max}
Gain Error (using internal R_{FB})	±0.3	±0.35	% FSR max [2]	DAC register loaded with 1111 1111 1111
Gain Change from +25°C to T_{min} or T_{max}		±0.03	% FSR max	Gain error is adjustable using the circuits of Figures 6 and 7
dc Supply Rejection (Gain) $\Delta Gain/\Delta V_{DD}$	±0.005	±0.01	% per % max	V_{DD} = +4.5V to +5.5V
Output Leakage Current				
I_{OUT1} (pin 1)	±50	±200	nA max	Register B loaded to 0000 0000 0000
I_{OUT2} (pin 2)	±50	±200	nA max	Register B loaded to 1111 1111 1111
DYNAMIC PERFORMANCE				
Current Settling Time [3]	2.0	2.0	µs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{LD1}$ and $\overline{LD2}$, see Figure 5.
Multiplying Feedthrough Error [3]	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT				
Input Resistance (pin 15)	8/15/25	8/15/25	kΩ min/typ/max	Typical temperature coefficient is −150ppm/°C
ANALOG OUTPUTS				
Output Capacitance				
C_{OUT1} [3]	75	75	pF max	Register B loaded to 0000 0000 0000
C_{OUT1} [3]	260	260	pF max	Register B loaded to 1111 1111 1111
C_{OUT2} [3]	75	75	pF max	Register B loaded to 1111 1111 1111
C_{OUT2} [3]	260	260	pf max	Register B loaded to 0000 0000 0000
LOGIC INPUTS				
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	V max	
I_{IN} [4]	1	1	µA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance) [3]	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 6 and 7), serial load (MSB First)			
SWITCHING CHARACTERISTICS [5]				
t_{DS1}	50	100	ns min	(Serial Input to Strobe Setup Time) STB1 used as a strobe
t_{DS4}	0	0	ns min	(Serial Input to Strobe Setup Time) STB4 used as a strobe
t_{DS3}	0	0	ns min	(Serial Input to Strobe Setup Time) $\overline{STB3}$ used as a strobe
t_{DS2}	20	40	ns min	(Serial Input to Strobe Setup Time) STB2 used as a strobe
t_{DH1}	30	60	ns min	(Serial Input to Strobe Hold Time) STB1 used as a strobe
t_{DH4}	80	160	ns min	(Serial Input to Strobe Hold Time) STB4 used as a strobe
t_{DH3}	80	160	ns min	(Serial Input to Strobe Hold Time) $\overline{STB3}$ used as a strobe
t_{DH2}	60	120	ns min	(Serial Input to Strobe Hold Time) STB2 used as a strobe
t_{SR1}	80	160	ns min	SR1 data pulse width
t_{STB1}	80	160	ns min	STB1 pulse width
t_{STB4}	100	200	ns min	STB4 pulse width
t_{STB3}	100	200	ns min	$\overline{STB3}$ pulse width
t_{STB2}	80	160	ns min	STB2 pulse width
t_{LD1}, t_{LD2}	150	300	ns min	Load pulse width
t_{ASB}	0	0	ns min	Min time between strobing LSB into Register A and loading Register B
t_{CLR}	200	400	ns min	CLR pulse width
POWER SUPPLY				
V_{DD} (Supply Voltage)	+5	+5	V	
I_{DD} (Supply Current)	8	8	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:
[1] Temperature ranges as follows: AD7543JN, KN: 0 to +70°C
AD7543AD, BD: −25°C to +85°C
[2] FSR is Full Scale Range.
[3] Guaranteed but not tested.
[4] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
[5] Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to A_{GND} . . . . . 0V, +7V
V_{DD} to D_{GND} . . . . . 0V, +7V
A_{GND} to D_{GND} . . . . . V_{DD}
D_{GND} to A_{GND} . . . . . V_{DD}
Digital Input Voltage to D_{GND}
(pins 4 - 11, 13) . . . . . -0.3V, +15V
V_{PIN1}, V_{PIN2} to A_{GND} . . . . . -0.3V, +15V
V_{REF} to A_{GND} . . . . . ±25V
V_{RFB} to A_{GND} . . . . . ±25V
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial Plastic (JN, KN versions) . . . . . 0 to +70°C
Industrial Ceramic (AD, BD versions) . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 secs.) . . . . . +300°C

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7543 would exhibit a gain of -4095/4096. Gain error is adjustable using external trims as shown in Figures 6 and 7.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with Register B loaded to all 0's or at OUT 2 with Register B loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0's.

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at AGND
3	AGND	Analog Ground
4	STB1	Register A Strobe 1 input, see Table 2
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
6	N/C	No Connection
7	SRI	Serial Data Input to Register A
8	STB2	Register A Strobe 2 input, see Table 2
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
10	$\overline{STB3}$	Register A Strobe 3 input, see Table 2
11	STB4	Register A Strobe 4 input, see Table 2
12	DGND	Digital Ground
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference input. Can be positive or negative dc voltage or ac signal
16	R_{FB}	DAC Feedback Resistor

Table 1. Pin Function Description

GENERAL CIRCUIT INFORMATION

The AD7543, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

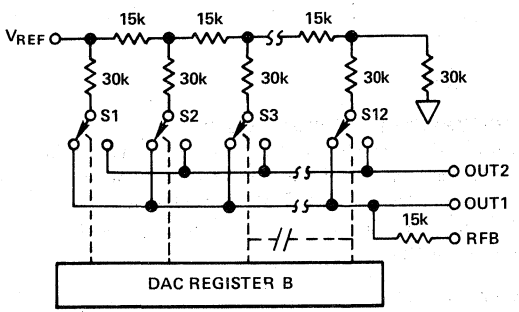


Figure 1. AD7543 Functional Diagram

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). The reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.

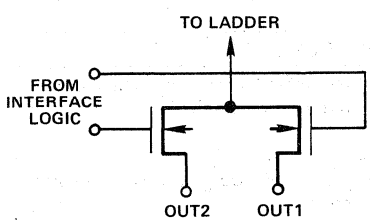


Figure 2. N-Channel Current Steering Switch

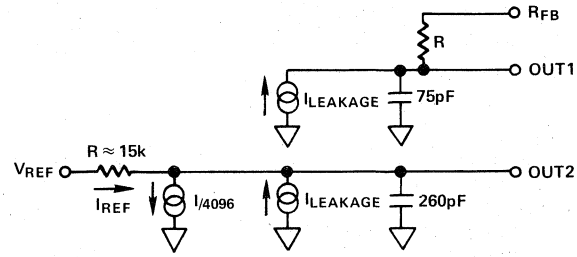


Figure 3. AD7543 DAC Equivalent Circuit All Digital Inputs LOW

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1 least significant bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 260pF at that terminal.

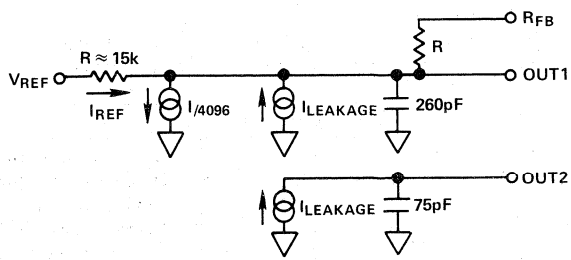


Figure 4. AD7543 DAC Equivalent Circuit All Digital Inputs HIGH

INTERFACE LOGIC INFORMATION

Shown in the AD7543 Functional Diagram Register A is a 12-bit shift register. Serial data appearing at pin SR1 is clocked into the shift register on the positive edge of STB1, STB2 or STB4 or on the negative edge of $\overline{STB3}$. Table 2 defines the various logic states required on the Register A control inputs, while Figure 5 illustrates the Register A loading sequence.

Once Register A is full, the data is transferred to Register B by bringing $\overline{LD1}$ and $\overline{LD2}$ momentarily LOW.

Register B can be asynchronously reset to 0000 0000 0000 by bringing $\overline{CLR}$ momentarily LOW. This allows the DAC output voltage to be set to a known condition, thus simplifying system initialization procedure. When operating the AD7543 in the unipolar circuit of Figure 6, a CLEAR causes the DAC output voltage to equal 0V. When using the bipolar circuit of Figure 7, a CLEAR causes the DAC output to equal V_{REF}.

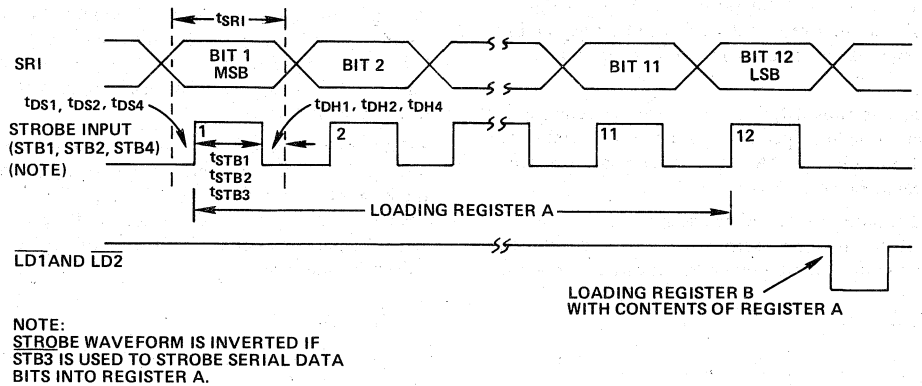


Figure 5. Timing Diagram

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↓	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	↓	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	↑	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
↓	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↓ is positive edge ↑ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table 2. AD7543 Truth Table

APPLYING THE AD7543

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current (again of + or – polarity) the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 3.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10pF to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

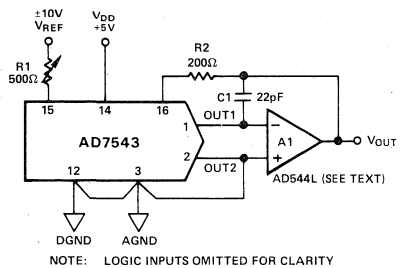


Figure 6. Unipolar Binary Operation (2-Quadrant Multiplication)

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table 4 illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 to 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

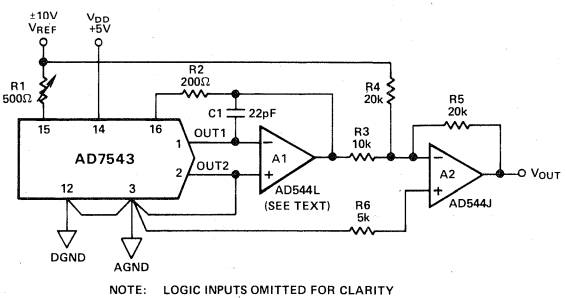


Figure 7. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 3. Unipolar Binary Code Table for Circuit of Figure 6

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 4. Bipolar Code Table for Offset Binary Circuit of Figure 7

APPLICATION HINTS

The AD7543 is a precision 12-bit multiplying DAC designed for serial interface. To ensure system performance consistent with AD7543 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7543 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7543. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7543 AGND and DGND pins to prevent possible device damage.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output of magnitude 0.67 V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}\ 2^{-n}$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7543 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

AD7543 INTERFACE TO MC6800

In this example, it is assumed that the 12-bit data is to be contained in two memory locations (0000 and 0001). The four most significant bits are assumed to occupy the lower half of memory location 0000. The eight least significant bits occupy memory location 0001. The data is presented bit by bit on the D7 line and strobed into the AD7543 by executing memory write instructions. In this case the strobe signal (STB1) is supplied by decoding address 2000, R/$\overline{W}$ and ϕ_2. A memory write instruction to a different address (4000) loads the data from Register A to the DAC register.

Figure 8 shows the interface circuitry and Table 5 gives a listing of the procedure.

LABEL	MNEMONIC	OPERAND	COMMENT
	LDA	B, 04	
	LDA	A, 0000	Load 4 Most Significant Bits
LOOP	ROL	A	Reposition the Data
	DEC	B	in A_{CC} A
	BNE	LOOP	
	LDA	B, 04	
	BSR	SHIFT	Output Data
	LDA	B, 08	
	LDA	A, 0001	Load 8 Least Significant Bits
	BSR	SHIFT	Output Data
	STA	A, 40000	Load DAC Register
	RTS		Return to Main Program
SHIFT	STA	A,2000	Strobe Data
	ROL	A	into AD7543
	DEC	B	
	BNE	SHIFT	
	RTS		

Table 5. Sample Routine for AD7543–MC6800 Interface

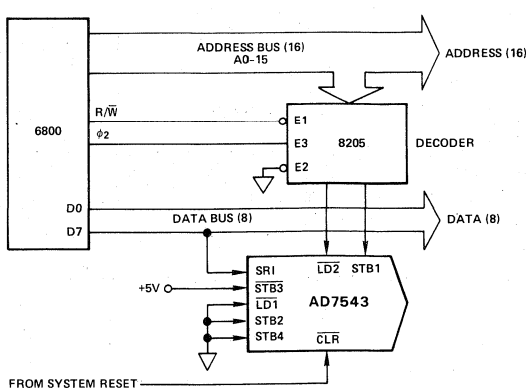


Figure 8. AD7543–MC6800 Interface

AD7543 INTERFACE TO MCS-85

Figure 9 shows the AD7543 interfaced to the 8085. This system makes use of the serial output facility (SOD) on the 8085.

The data is presented serially on the SOD line and strobed into the AD7543 by executing memory write instructions. In this example the strobe signal ($\overline{STB3}$) is supplied by decoding address 8000 and $\overline{WR}$. A memory write instruction to a different address (A000) loads the DAC Register with Register A data. Table 6 gives a listing of this procedure. Note, it is assumed that the required serial data is already present in right-justified format in Registers H and L when this procedure is implemented.

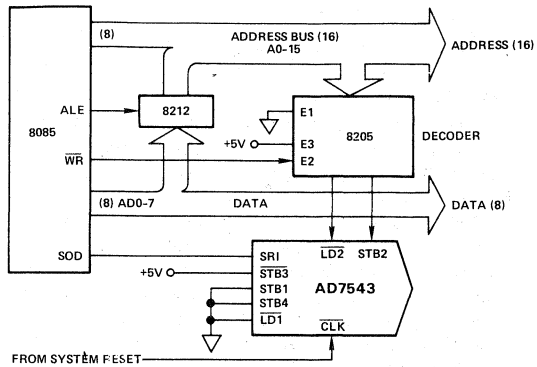


Figure 9. AD7543–8085 Interface

LABEL	MNEMONIC	OPERAND	COMMENT
	MVI	B, 05	Shift Data Up to
LOOP	CALL	SHIFT	Most Significant
	DCR	B	Segment of HL with
	JNJ	LOOP	MSB as Carry
	MVI	B, OC	
LUP	MVI	A, 80	SOD Enable in ACC
	RAR		Shift in MSB of H
	SIM		Set Interrupt Mask
	STA	8000	Strobe Data into AD7543
	CALL	SHIFT	Get Next Bit into Carry
	DCR	B	
	JNZ	LUP	Go Back if Not Finished
	STA	A000	Load DAC Register of AD7543
	RET		Return to Main Program
SHIFT	MOV	A, L	
	RAL		Shift H and L Left
	MOV	L, A	One Place and
	MOV	A, H	Leave Uppermost Bit
	RAL		of H in Carry
	MOV	H, A	
	RET		

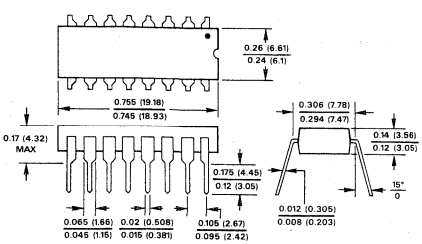
Table 6. Sample Routine for AD7543–8085 Interface

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

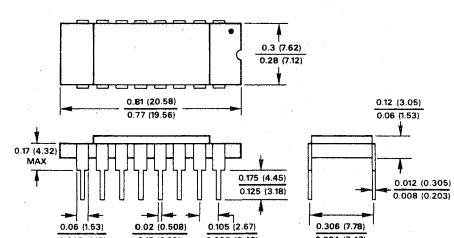
Dimensions shown in inches and (mm).

16 PIN PLASTIC DIP



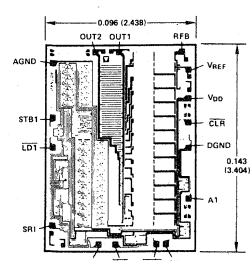
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

BONDING DIAGRAM



PADS ARE 0.004 × 0.004 INCHES (0.102 × 0.102mm) MIN.
TO MINIMIZE ESD HAZARD BOND DGND FIRST

ANALOG DEVICES

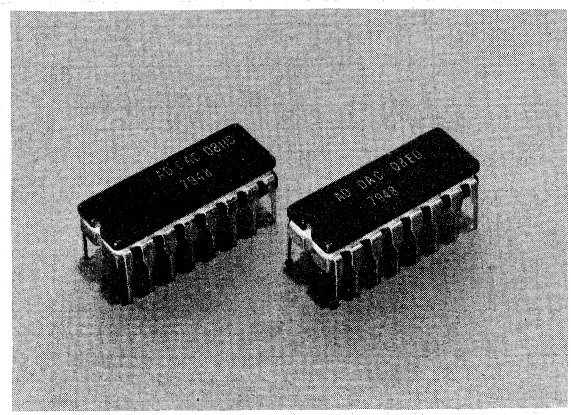
8-Bit Monolithic High Speed Multiplying D/A Converter

AD DAC-08

PRELIMINARY TECHNICAL DATA

FEATURES

- Exact Replacement for Industry Standard DAC-08
- Fast (85ns typical) Settling Time
- Linearity Error ±1/4LSB (±0.1%) Guaranteed Over Full Temperature Range
- Wide Output Voltage Compliance: -10V to +18V
- Single Chip Monolithic Construction
- 16-Pin Ceramic DIP Packaging
- Low Cost
- MIL-STD-883 Processing Available



PRODUCT DESCRIPTION

The AD DAC-08 is a low-cost, 8-bit monolithic multiplying digital-to-analog converter featuring typical settling times of 85ns. The chip contains 8 matched bipolar current steering switches, a precision resistor network, and high-speed control amplifier, thus integrating all important circuit functions on a single chip.

The AD DAC-08 provides matching of full-scale output current to the reference current within 1LSB. Analog Devices' precision linear processing makes this matching possible without the use of laser trimming. Diffused resistors are used rather than thin-film resistors in order to provide specified performance at low cost.

The AD DAC-08 is recommended for use in applications requiring 8-bit accuracy and fast settling times coupled with ease of use. The AD DAC-08 also provides an alternate source for designs already using the standard DAC-08.

The AD DAC-08 is available in 5 performance grades: the AD DAC-08A and AD DAC-08 are rated for the full -55°C to +125°C military temperature range; and the AD DAC-08H, E, and C grades are specified for the 0 to +70°C commercial temperature range. All models are guaranteed monotonic over their full temperature range, and all are packaged in a hermetically-sealed 16-pin ceramic dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD DAC-08 is a true second-source equivalent to the industry standard DAC-08.
2. The versatile current-in, current-out design, choice of fixed or variable reference, and CMOS or TTL compatible inputs offer the user greater flexibility in applying the device.
3. The fast settling time allows the AD DAC-08 to be used in applications such as CRT displays, waveform generators, and high-speed analog-to-digital converters.
4. The high impedance current output can drive a resistor directly, or be used with an external op amp to produce a low impedance output voltage.
5. The AD DAC-08 is available in chip form for use in hybrid microcircuits. Consult Analog Devices' chip catalog for available grades and application details.
6. The AD DAC-08 and AD DAC-08A are available fully screened to MIL-STD-883, Method 5004 Class B. A full list of tests appears on page 9-128.

SPECIFICATIONS

The AD DAC-08 and AD DAC-08A specifications apply for $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = -55°C$ to $+125°C$ unless otherwise noted.

MODEL / CHARACTERISTIC	SYMBOL	CONDITIONS	AD DAC-08 MIN	AD DAC-08 TYP	AD DAC-08 MAX	AD DAC-08A MIN	AD DAC-08A TYP	AD DAC-08A MAX	UNITS
RESOLUTION					8			8	Bits
MONOTONICITY		$T_A = -55°C$ to $+125°C$		GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = -55°C$ to $+125°C$			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	135		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60	ns
FULL SCALE TEMPCO	TC I_{FS}			±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$ typ	−10		+18	−10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, R_{15} = 5.000kΩ; $T_A = 25°C$	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	$(I_{FS4} - I_{FS2})$		±1.0	±8.0		±0.5	±4.0	μA
ZERO SCALE CURRENT	I_{ZS}			0.2	2.0		0.1	1.0	μA
OUTPUT CURRENT RANGE	I_{FSR}	V− = −5.0V	0	2.0	2.1	0	2.0	2.1	mA
		V− = −7.0 to −18V	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS									
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$							
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		−2.0	−10		−2.0	−10	μA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002	10	μA
LOGIC INPUT SWING	V_{IS}	V− = −15V	−10		+18	−10		+18	V
LOGIC THRESHOLD RANGE	V_{IHR}	$V_S = \pm 15V$	−10		+13.5	−10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	−1.0	−3.0	+0.1	−1.0	−3.0	μA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		mA/μs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		+0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V− = 4.5V to −18V		±0.002	±0.01		±0.002	±0.01	%/%
		$I_{REF} = 1.0mA$							
POWER SUPPLY CURRENT									
From $+V_S$	I+		0.4	2.3	3.8	0.4	2.3	3.8	mA
From $-V_S$	I−		−0.8	−6.4	−7.8	−0.8	−6.4	−7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48	mW
		+5V, −15V, $I_{REF} = 2.0mA$		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174	mW

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- AD DAC-08, DAC-08A. . . . . −55°C to +125°C
- AD DAC-08E, C, H . . . . . 0 to +70°C

Storage Temperature . . . . . −65°C to +150°C
- Power Dissipation 500mW
- Above 100°C Derate by . . . . . 10mW/°C

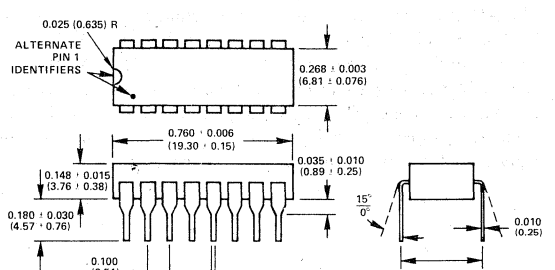
Lead Soldering Temperature . . . . . 300°C (60sec)
$-V_S$ Supply to $+V_S$ Supply 36V
Logic Inputs. . . . . $-V_S$ to ($-V_S$ +36V)
V_{LC} . . . . . $-V_S$ to $+V_S$
Reference Inputs (V_{14}, V_{15}). . . . . $-V_S$ to $+V_S$
Reference Input Differential
- Voltage (V_{14} to V_{15}). . . . . ±18V

Reference Input Current (I_{14}) 5.0mA

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN CERAMIC DUAL-IN-LINE

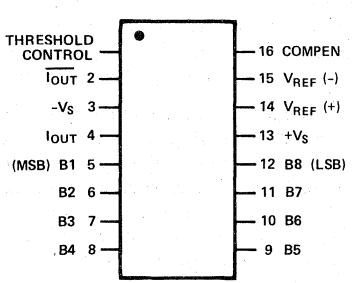


SPECIFICATIONS

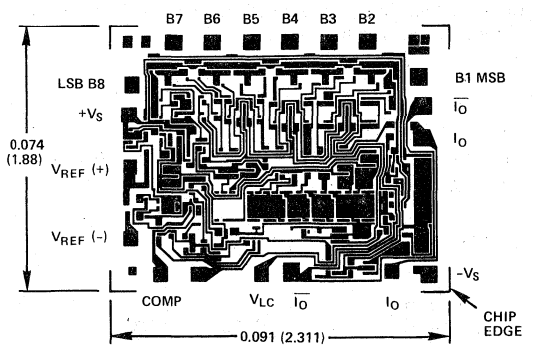
The AD DAC-08C, E, and H specifications apply for $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 0$ to $+70°C$ unless otherwise noted.

MODEL / CHARACTERISTIC	SYMBOL	CONDITIONS	AD DAC-08C MIN	AD DAC-08C TYP	AD DAC-08C MAX	AD DAC-08E MIN	AD DAC-08E TYP	AD DAC-08E MAX	AD DAC-08H MIN	AD DAC-08H TYP	AD DAC-08H MAX	UNITS
RESOLUTION					8			8			8	Bits
MONOTONICITY		$T_A = 0$ to $+70°C$		GUARANTEED			GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = 0$ to $+70°C$			±0.39			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	150		85	150		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60		35	60	ns
FULL SCALE TEMPCO	TC I_{FS}			±10	±80		±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$	−10		+18	−10		+18	−10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, $R_{15} = 5.000k\Omega$; $T_A = 25°C$	1.94	1.99	2.04	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	($I_{FS4} - I_{FS2}$)		±2.0	±16		±1.0	±8.0		±0.5	±4.0	μA
ZERO SCALE CURRENT	I_{ZS}			0.2	4.0		0.2	2.0		0.1	1.0	μA
OUTPUT CURRENT RANGE	I_{FSR}	V− = −5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V− = −7.0 to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS												
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		−2.0	−10		−2.0	−10		−2.0	−10	μA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002	10		0.002	10	μA
LOGIC INPUT SWING	V_{IS}	V− = −15V	−10		+18	−10		+18	−10		+18	V
LOGIC THRESHOLD RANGE	V_{IHL}	$V_S = \pm 15V$	−10		+13.5	−10		+13.5	−10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	−1.0	−3.0	+0.1	−1.0	−3.0	+0.1	−1.0	−3.0	μA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		+0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V− = −4.5V to −18V, $I_{REF} = 1.0mA$		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	%/%
POWER SUPPLY CURRENT	I+	From $+V_S$	0.4	2.3	3.8	0.4	2.3	3.8	0.4	2.3	3.8	mA
	I−	From $-V_S$	−0.8	−6.4	−7.8	−0.8	−6.4	−7.8	−0.8	−6.4	−7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48		33	48	mW
		+5V, −15V, $I_{REF} = 2.0mA$		108	136		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174		135	174	mW

Specifications subject to change without notice.



Pin Connections



THE AD DAC-08 IS ALSO AVAILABLE IN CHIP FORM. CONSULT ANALOG DEVICES' CHIP CATALOG FOR SPECIFICATIONS AND APPLICATIONS INFORMATION.

Chip Dimensions and Pad Layout. Dimensions shown in inches and (mm).

APPLYING THE AD DAC-08

Reference Connections

Figure 1 shows the block diagram of the AD DAC-08 circuit. A reference current (equal to the desired full-scale output current) is applied to pin 14. The reference amplifier adjusts the base voltage of the NPN current source transistors. The collector currents are binarily weighted, and their sum is equal to 255/256 times the reference current. The binary weighting is accomplished by the diffused resistor R-2R ladder network. The individual collector currents are steered into either the I_{OUT} or $\overline{I_{OUT}}$ lines by the current switches. These switches are driven by level shifters which can accept TTL or CMOS logic levels directly. The I_{OUT} and $\overline{I_{OUT}}$ lines can drive an op amp summing junction or can drive resistive loads directly due to the wide range of output compliance voltage.

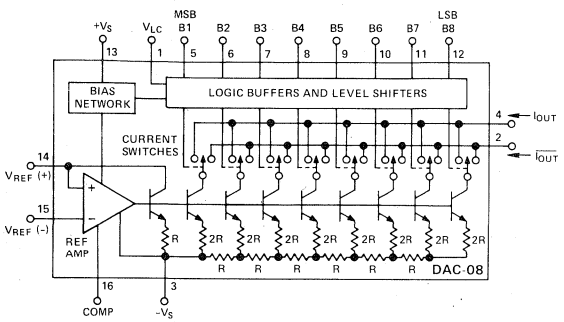


Figure 1. AD DAC-08 Block Diagram

Figure 2 illustrates the connections for positive and negative references. When a positive reference is used (Figure 2a), resistor R14 (equal to V_{REF} divided by the desired I_{FS}) establishes the reference current into pin 14. Reference amplifier bias current errors are minimized by connecting R15 (equal to R14) from pin 15 to ground. Adjustment of the output scale can be done by trimming R14, although in most applications the tight initial matching between reference current and output current will be adequate.

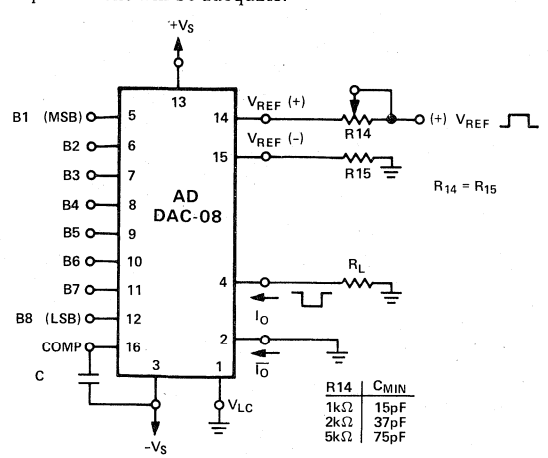


Figure 2a. Connections for Use with Positive Reference

Figure 2b shows the connections for a negative reference. Note that the reference current flows from ground into pin 14 through R14, which should be a low TC resistor as in the positive reference configuration. Resistor R15 serves the purpose

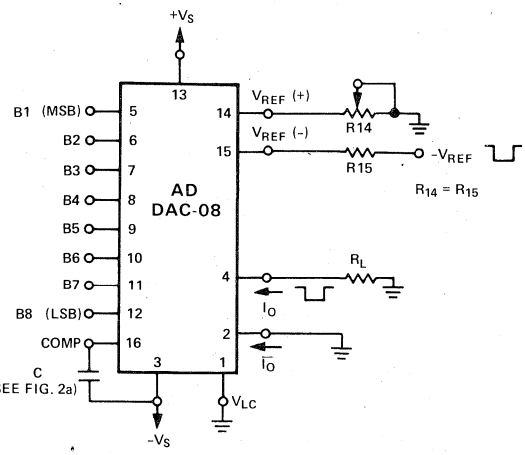


Figure 2b. Connections for Use with Negative Reference

of bias current cancellation only and need not be a precision resistor. Note that the input impedance for a negative reference is very high, while a positive reference sees an impedance equal to R14.

When a dc reference is used, a 0.01μF reference bypass capacitor is recommended. The reference should be a low-drift, well-regulated and filtered type, such as the AD581 10V reference IC. Other values of reference voltage may be used, provided that R14 is chosen for a reference current between 0.2mA and 4.0mA.

MULTIPLYING MODE PERFORMANCE

The AD DAC-08 can be used to perform two-quadrant digital-analog multiplication by applying an ac reference signal. When an ac reference is used, pin 15 must be offset to insure that pin 14 is always at a higher potential than pin 15.

The reference amplifier must be properly compensated in ac applications to insure stability. The value of the capacitor from pin 16 to $-V_S$ depends on the value of R14. Minimum values of compensation capacitor for R14 values of 1, 2 and 5kΩ are 15, 37 and 75pF respectively.

For fastest response to a pulsed reference, low values of R14 should be used, allowing smaller values of compensation capacitor. It is possible to lower the equivalent resistance at pin 14 by connecting a shunt resistor to ground. Figure 3 shows the performance with equivalent resistance of 200Ω and no compensation capacitor. Slew rate is approximately 15mA/μs under these conditions.

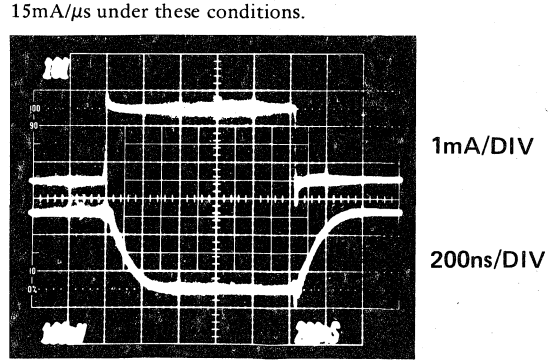


Figure 3. Fast Pulsed Reference Operation

The photographs on this page demonstrate the dynamic performance of the AD DAC-08. The AD DAC-08 is capable of extremely fast settling time, typically 85 nanoseconds for a full-scale step with I_{REF} = 2.0mA. As with any high speed circuitry, component layout must be optimized for minimum parasitic capacitances if full speed is to be realized.

Figure 4 below shows the output settling characteristic for a full-scale step. The vertical scale is 1LSB per division. Note that the zero-to-full scale settling time (Figure 4a) to within 1/2LSB is approximately 70 nanoseconds.

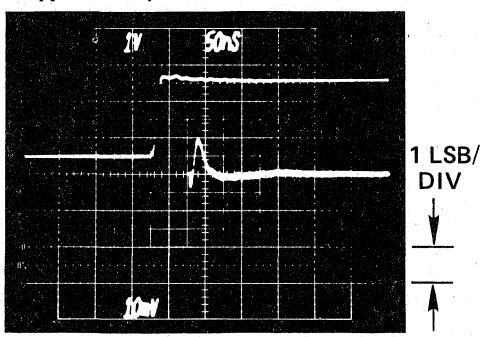


Figure 4a. Zero to Full-Scale Setting

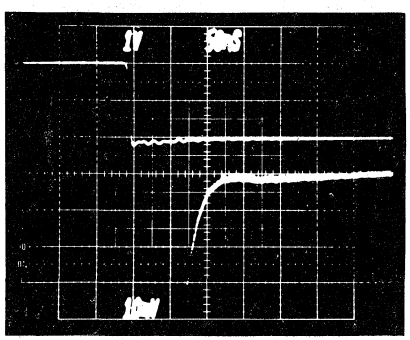


Figure 4b. Full-Scale to Zero Settling

Since the settling time of a DAC circuit includes propagation delay, slewing time, and final settling, switching time is best measured when only the LSB is switched. This minimizes the slewing time necessary. The LSB switching characteristic is shown in Figure 5.

SETTLING TIME MEASUREMENT

It should be noted that settling time measurement is not a simple matter. Since 1/2LSB of a 2.0mA full scale is only 4μA, a 1kΩ load resistance is needed to provide adequate drive for most oscilloscopes. However, any stray capacitance can cause the settling time of the fixture to be longer than the DAC settling time. For example, 15pF stray capacitance can cause a settling time to 1/2LSB of nearly 100 nanoseconds in the test fixture alone. The circuit of Figure 6 reduces the capacitance at the measurement node to less than 5pF, allowing more accurate determination of settling time.

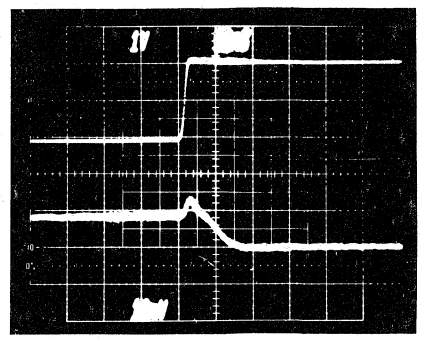


Figure 5. LSB Switching

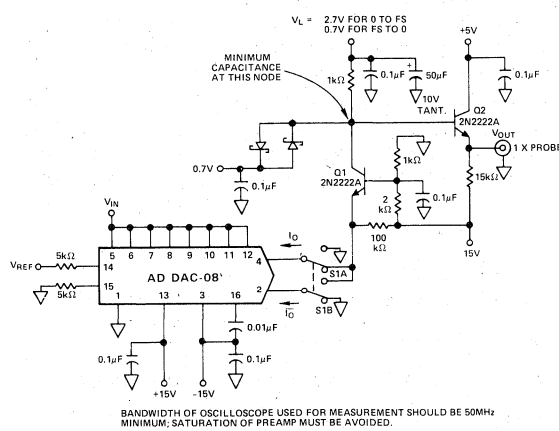


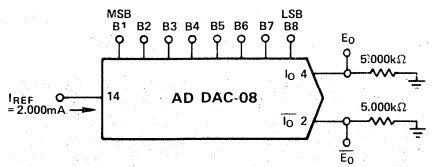
Figure 6. Settling Time Test Circuit

LOGIC INPUT CIRCUIT

The AD DAC-08 digital inputs will accommodate all popular logic families. The switching threshold is adjustable by applying a voltage to the logic threshold control pin (pin 1). The threshold is nominally 1.4 volts above V_{LC} at room temperature. For TTL/DTL interface, pin 1 is simply grounded. The logic inputs will tolerate wide voltage swings; for example, for $-V_S$ = −15V, the inputs may swing between −10V and +18V.

OUTPUT CONNECTIONS

The I_O and $\overline{I_O}$ outputs provide the user with several possible output configurations. Current is steered into the I_O terminal when a bit is at Logic "1", and into $\overline{I_O}$ when the bit is at Logic "0". Either output may be used, or both may be used simultaneously. If only one output is used, the unused output must still be connected to ground or some other point capable of sourcing I_{FS}.



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
FULL SCALE -LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
HALF SCALE + LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
HALF SCALE -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

Figure 7. High Impedance Voltage Output

The wide output compliance range permits the AD DAC-08 to drive a resistive load directly. For example, with I_{REF} = 2.0mA, and a 5kΩ resistor from pin 4 to ground, the voltage at pin 4 varies from 0V with all bits OFF to -9.960V with all bits ON. While this is the simplest current-to-voltage conversion, it presents a 5kΩ output impedance, which adversely affects settling time and requires buffering.

An operational amplifier configured as a current-to-voltage converter will lower the output impedance and provide a voltage inversion. An output range of zero to +9.960V is then produced with a 5kΩ feedback resistor as shown in Figure 8.

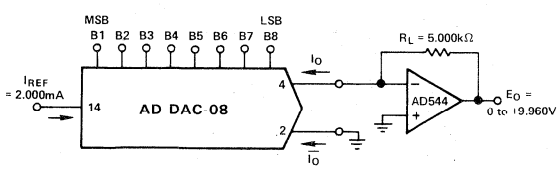
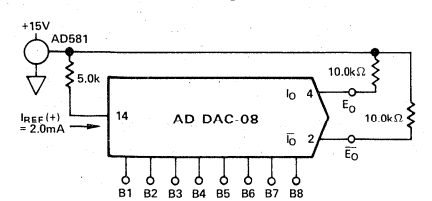


Figure 8. Low Impedance Voltage Output

Bipolar output voltage ranges are also possible. Figure 9 demonstrates the simplest scheme, providing a -9.92 to +10.00 volt scale in 80 millivolt steps. The voltage output has a high impedance as shown and should be buffered with an amplifier connected as a voltage follower.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	- 9.920	+10.000
POS FULL SCALE -LSB	1	1	1	1	1	1	1	0	- 9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	- 0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE -LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	- 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	- 9.920

Figure 9. Bipolar Voltage Output

MIL-STD-883

When designing systems for use in military/aerospace applications, components chosen must be available from several suppliers and have a proven record of reliability. The AD DAC-08, as a multiple-sourced product, represents Analog Devices' commitment to serve those customers involved in high-rel system design.

The AD DAC-08 is an ideal choice for operation in severe environments. Its monolithic construction and hermetically-sealed DIP package protect it from humidity and mechanical stress, while the guaranteed specifications over temperature assure proper system performance at the temperature extremes.

For the utmost reliability, the AD DAC-08 is available with screening to MIL-STD-883, Method 5004, Class B. Table I lists the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30,000G
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C.
7) Final Electrical Tests	Performed 100% to all min and max specifications on data pages.
8) External Visual	Method 2009

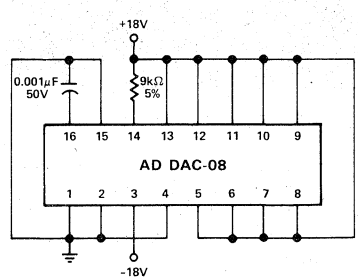


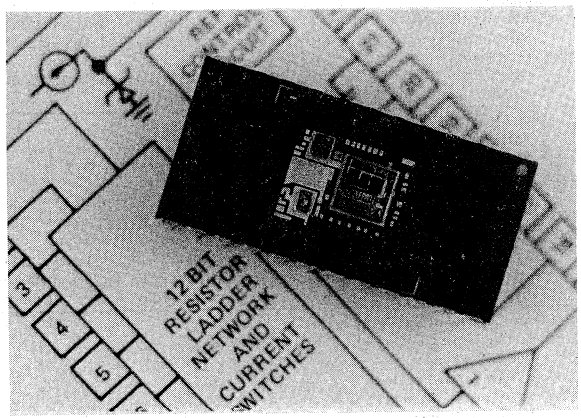
Figure 10. Burn-In Circuit

ANALOG DEVICES

Low Cost 12-Bit IC D/A Converter

AD DAC80

FEATURES
- Low Cost
- Improved Replacement for Standard DAC80
- 3 Chip, High Reliability Construction
- Low Power Dissipation
- Laser-Trimmed to High Accuracy:
  - ±½LSB Max Nonlinearity, 0 to +70°C
- Guaranteed Monotonicity, 0 to +70°C
- High Stability, High Current Output
  - Buried Zener Reference
- On-Board Output Amplifier (V Models)
- 24 Lead Side Brazed Ceramic DIP



PRODUCT DESCRIPTION

The AD DAC80 is a low cost 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and an optional output amplifier. Options include TTL compatible complementary 12-bit binary (CBI) or 3 digit BCD (CCD) input codes, as well as current or voltage output modes. The AD DAC80 offers output voltage ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either ±1mA or 0 to −2mA.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC80 devices. An innovative 3-chip construction improves reliability by a factor of two. The AD DAC80 incorporates a fully differential, non-saturating precision current switching cell structure[1] which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature cycle characteristics which challenge the best discrete zener references.

The AD DAC80 is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance. The AD DAC80 is also ideal for use in constructing A/D conversion systems and as a building block for higher resolution D/A systems.

[1] **COVERED BY PATENT NUMBERS: 3,978,473; Re 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.**

PRODUCT HIGHLIGHTS

1. The AD DAC80 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC80 the optimum choice for applications where low cost and high reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC80 offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and a total accuracy drift in the bipolar configuration of ±20ppm/°C maximum.
5. The low T.C. Binary ladder guarantees that all AD DAC80 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output modes are available in either of the BCD or binary input formats.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	DAC80-CBI	DAC80-CCD
DIGITAL INPUT		
Resolution	12 Bits max	3 Digits max
Logic Levels (TTL/Compatible)		
Logical "1" (at +1μA)	+2V dc min, +5.5V dc max	*
Logical "0" (at −100μA)	0V dc min, +0.8V dc max	*
ACCURACY		
Linearity Error 0 to +70°C	±1/4LSB typ, ±1/2LSB[1] max	±1/8LSB typ, ±1/4LSB max
Differential Linearity Error 0 to +70°C	±1/2LSB typ, ±3/4LSB max	±1/4LSB typ, ±1/2LSB max
Gain Error[2]	±0.1% typ, ±0.3% max	*
Offset Error[2]	±0.05% FSR typ, ±0.15% FSR[3] max	*
Monotonicity Temp. Range	0 to +70°C	*
DRIFT[4] (0 to +70°C)		
Total Bipolar Drift (Includes Gain, Offset, and Linearity Drifts)[5]	±20ppm FSR/°C max	*
Total Error Over 0 to +70°C[6]		
Unipolar	±0.08% FSR typ, ±0.15% FSR max	*
Bipolar	±0.06% FSR typ, ±0.10% FSR max	*
Gain	±15ppm/°C typ, ±30ppm/°C max	*
Exclusive of Internal Reference	±5ppm/°C typ, ±7ppm/°C max	*
Unipolar Offset	±1ppm FSR/°C typ, ±3ppm FSR/°C max	*
Bipolar Offset	±5ppm FSR/°C typ, ±10ppm FSR/°C max	*
CONVERSION SPEED/V Models		
Settling Time to ±0.01% of FSR For FSR Change		
with 10kΩ Feedback[7]	5μs typ	*
with 5kΩ Feedback	3μs typ	*
For 1LSB Change	1.5μs typ	*
Slew Rate	10V/μs min, 15V/μs typ	*
CONVERSION SPEED/I Models		
Settling Time to ±0.01% of FSR For FSR Change		
10 to 100Ω Load	300ns typ	*
1kΩ Load	1μs typ	*
ANALOG OUTPUT/V Models		
Ranges[7]	±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V	0 to +10V
Output Current	±5mA min	*
Output Impedance (dc)	0.05Ω typ	*
Short Circuit Duration	Indefinite to Common	*
ANALOG OUTPUT/I Models		
Ranges	±1mA, 0 to −2mA typ	0 to −2mA typ
Output Impedance - Bipolar	3.2kΩ typ	*
Output Impedance - Unipolar	6.6kΩ typ	*
Compliance	+10V, −1.5V	*
INTERNAL REFERENCE VOLTAGE	+6.3V ±2%max	*
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	*
External - Use Current[8]	+2.5mA max	*
Output Impedance	1.5Ω typ	*
POWER SUPPLY SENSITIVITY		
+15V Supply	±0.002% FSR/% V_S max	*
−15V and +5V Supplies	±0.002% FSR/% V_S max	*
POWER SUPPLY REQUIREMENTS		
DAC80	±14V dc, +4.75V dc min	*
	±15V dc, +5V dc typ	*
	±16V dc, +16V dc max	*
DAC80Z[7]	±11.4V dc, +4.75V dc min	*
	±12V dc, +5V dc typ	*
	±16V dc, +16V dc max	*
Supply Drain		
+15/+12V (Including 5mA Load)	10mA typ, 20mA max	*
−15/−12V (Including 5mA Load)	−20mA typ, −35mA max	*
+5V (Logic Supply)	8mA typ, 20mA max	
TEMPERATURE RANGE		
Specification	0 to +70°C max	*
Operating	−25°C to +85°C max	*
Storage	−55°C to +100°C	*

NOTES
[1] Least Significant Bit (LSB).
[2] Adjustable to zero with external trim potentiometer.
[3] FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
[4] To maintain drift spec internal feedback resistors must be used for current output models.
[5] See discussion on page 9-133.
[6] With gain and offset errors adjusted to zero at +25°C. See discussion on page 9-133.
[7] DAC80Z supply range is ±12.0V min to ±16.0V max for ±5V and 0 to +5V outputs.
[8] Maximum with no degradation of specifications with constant load.
Specifications subject to change without notice.

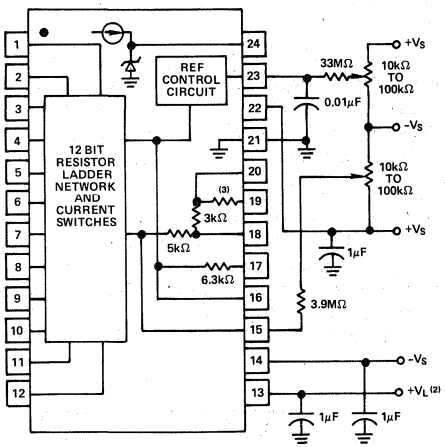


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

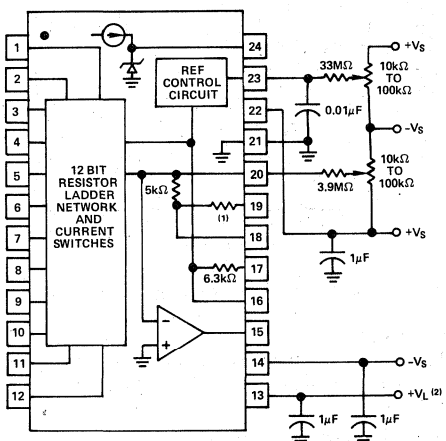


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

NOTES:
1. 3kΩ for CCD models. 5kΩ for CBI models.
2. If connected to $+V_S$ which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.

PIN CONFIGURATION

24 LEAD DUAL IN-LINE PACKAGE

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1(MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)

I Models	Pin #	V Models
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref Input	16	Ref Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
$6.3V_{REF}$ Out	24	$6.3V_{REF}$ Out

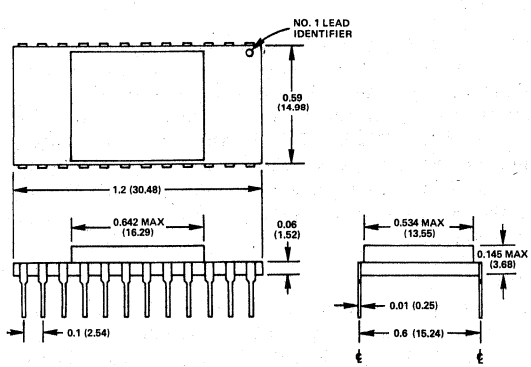


Figure 3. Outline Dimensions (Dimensions shown in inches and (mm))

AD DAC80 ORDERING GUIDE

MODEL	INPUT CODE	OUTPUT MODE	SUPPLY RANGE
AD DAC80-CBI-V	Binary	Voltage	Normal
AD DAC80-CBI-I	Binary	Current	Normal
AD DAC80-CCD-V	Binary Coded Decimal	Voltage	Normal
AD DAC80-CCD-I	Binary Coded Decimal	Current	Normal
AD DAC80Z-CBI-V	Binary	Voltage	Extended
AD DAC80Z-CBI-I	Binary	Current	Extended
AD DAC80Z-CCD-V	Binary Coded Decimal	Voltage	Extended
AD DAC80Z-CCD-I	Binary Coded Decimal	Current	Extended

DIGITAL INPUT CODES

The AD DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

	DIGITAL INPUT		ANALOG OUTPUT		
	MSB LSB		CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000		+Full Scale	+Full Scale	-LSB
	011111111111		+½ Full Scale	Zero	-Full Scale
	100000000000		Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111		Zero	-Full Scale	Zero
	MSB	LSB	CCD Complementary Coded Decimal - 3 Digits		
CCD Models	0110 0110 0110		+Full Scale		
	1111 1111 1111		Zero		

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table 1. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it can not be corrected for. The linearity error of the AD DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0 to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next. Monotonicity over the 0 to +70°C range is guaranteed in the AD DAC80 to ensure that the analog output will not decrease with increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC80 model at 0°C; +25°C and +70°C; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each AD DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 4).

Voltage Output Models. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 ... 1 1 to 1 0 0 0 ... 0 0), the point at which the worst case settling time occurs.

Current Output Models. Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistance of approximately 1000 to 1800 ohms for output voltage range of ±1V and 0 to -2V (see Table IV).

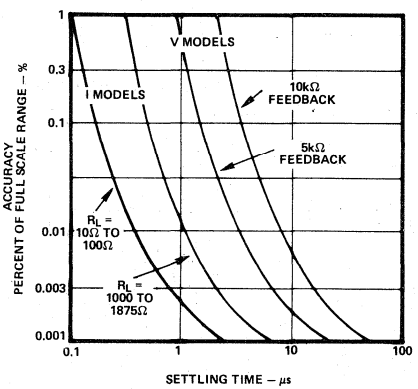


Figure 4. Full Scale Range Settling Time vs. Accuracy

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All AD DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven off of the reference will result in gain variations of the AD DAC80. All gain adjustments should be made under constant load conditions.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 5. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient, which is specified as ±20ppm/°C max. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried zener diode reference element results in superior wide temperature range performance. The full scale gain settling resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

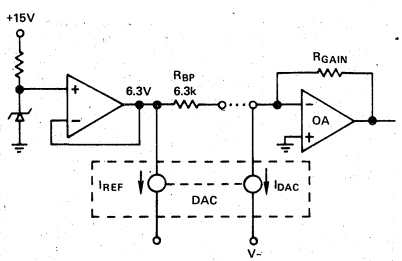


Figure 5. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ±1/2LSB max and the differential linearity error of ±3/4LSB max guarantee monotonic performance over the range of 0 to +70°C. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of 3ppm/°C max (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 6. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors for a total of 30ppm/°C max. Total absolute error due to all of these effects is guaranteed to be less than ±0.15% of full scale from 0 to +70°C.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see Figure 5) to generate a current which, exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 6. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD DAC80 this error is held to 10ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full scale drift, but again is held to 7ppm/°C max. The total of all these errors is held to ±0.1% of full scale from 0 to +70°C. Note that, in the bipolar ranges, full scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

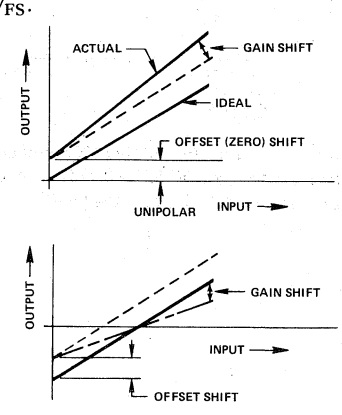


Figure 6. Unipolar and Bipolar Drifts

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V and 0V to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{SUPPLY}| - |V_{OUT}$ max $| < 2.0$V. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the AD DAC80Z and AD DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams (Figures 1 and 2). These capacitors (1μF electrolytic recommended) should be located close to the AD DAC80. Electrolytic capacapacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the AD DAC80 to prevent noise pick-up. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 7 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capacitor should be connected from this pin to common to prevent noise pick-up. Figures 8 and 9 show the relationship of the OFFSET and GAIN adjustments to the unipolar and bipolar D/A converters.

Offset Adjustment. For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COD, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes and the block diagrams for offset adjustment connections.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the block diagrams for gain adjustment connections.

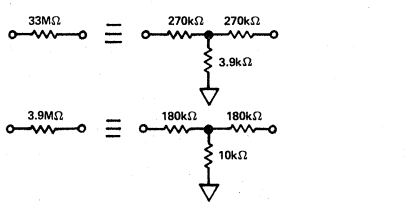


Figure 7. Equivalent Resistances

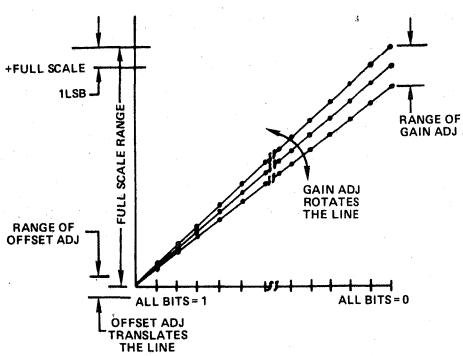


Figure 8. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter. (Input, Horizontal; Output, Vertical).

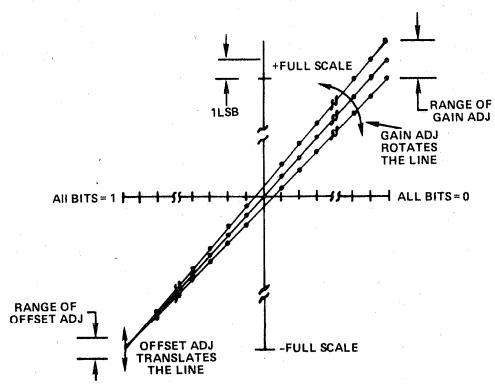


Figure 9. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A CONVERTER. (Input, Horizontal; Output, Vertical).

	DIGITAL INPUT	ANALOG OUTPUT			
	12 Bit Resolution	VOLTAGE*		CURRENT	
	MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	0.488μV
	1LSB	2.44mV	4.88mV	0.488mA	+1.000mA
	3 Digital Resolution				
	MSB LSB				
CCD Models	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	1LSB	10.00mV	N/A	1.25μA	N/A

*To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.
**Normal full scale range with correct codes; output can go higher if illegal codes are applied.

Table II. Digital Input/Analog Output

VOLTAGE OUPUT MODELS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 10).

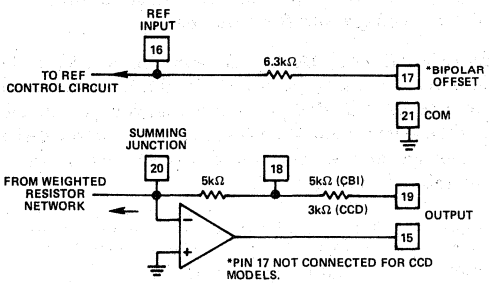


Figure 10. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections-Voltage Model AD DAC80

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 11 and 12. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

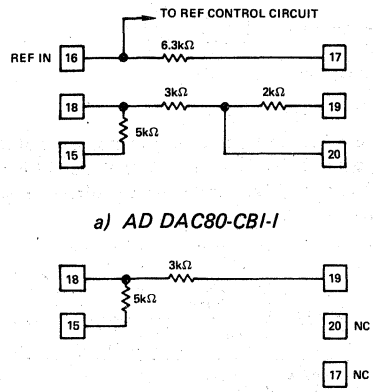


Figure 11. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the AD DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

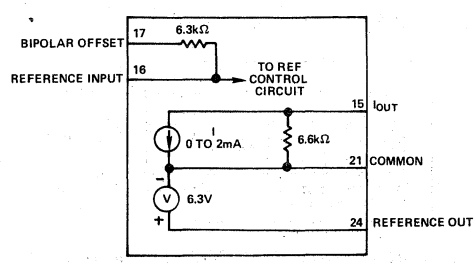


Figure 12. AD DAC80 Current Model Equivalent Output Circuit

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	1% Metal Film External Resistance R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset: R_{LS}	Bipolar Offset: R_{LP}
CSB	0 to -2V	0.968kΩ	210Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	3kΩ	N/A	3.57kΩ	N.C.	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	249Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

Table IV. Current Model/Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 13 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L} \right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = -2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With R_{LS} = 0, V_{OUT} = -1.69V.

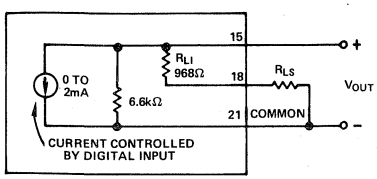


Figure 13. Equivalent Circuit AD DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 14 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}},$$

$$V_{OUT} = -1.25mA \left(\frac{6.9k \times R_L}{6.9k + R_L} \right)$$

If $R_{LP} = \infty$, V_{OUT} = -3.62V

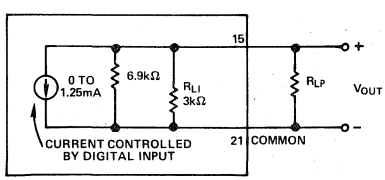


Figure 14. AD DAC80-CCD-I Connected for Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 15, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k} \right)$$

Where R_L max = 11.18kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 16.

$V_{OUT} = I_{OUT} \times R_F$

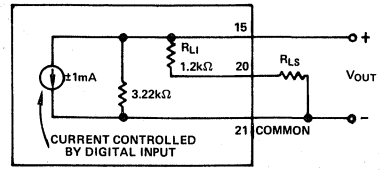


Figure 15. AD DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

where I_{OUT} is the AD DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC80 provides output voltage ranges the same as the voltage model AD DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 16.

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	A	24

Table V. Voltage Range of Current Output AD DAC80

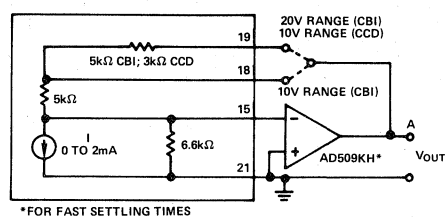


Figure 16. External Op Amp — Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges (see Figure 17). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

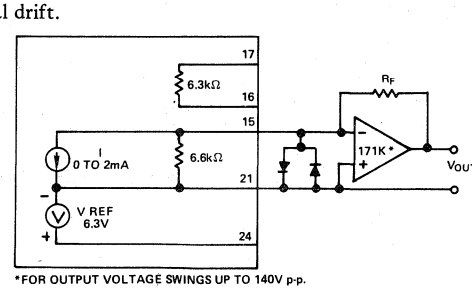


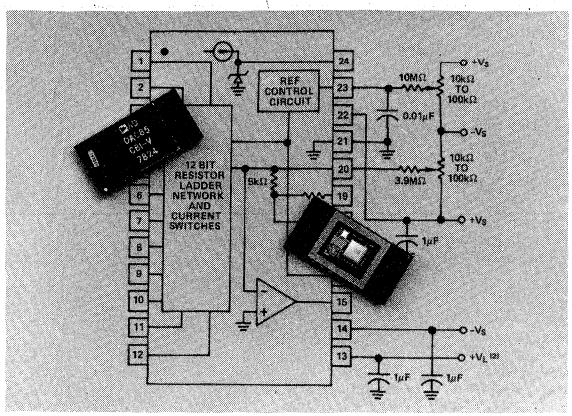
Figure 17. External Op Amp — Using External Feedback Resistors

High Performance 12-Bit IC D/A Converter

AD DAC85

FEATURES

- Improved Replacement for Standard DAC85
- 3 Chip, High Reliability Construction
- Low Power Dissipation
- Laser-Trimmed to High Accuracy:
  - ±3/4LSB Max Nonlinearity, -55°C to +125°C (AD DAC85 MIL)
- High Stability, High Current Output
  - Buried Zener Reference
- On-Board Output Amplifier (V Models)
- 24 Lead Side Brazed Ceramic DIP



PRODUCT DESCRIPTION

The AD DAC85 is a high performance 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and and an optional output amplifier. Options include TTL compatible complementary 12-bit binary (CBI) or 3 digit BCD (CCD) input codes, as well as current or voltage output modes. The AD DAC85 offers output voltage ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either ±1mA or 0 to -2mA.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC85 devices. An innovative 3-chip construction improves reliability by a factor of five.[1] The AD DAC85 incorporates a fully differential, non-saturating precision current switching cell structure* which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in low differential nonlinearity errors. A low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature cycle characteristics which challenge the best discrete zener references.

The AD DAC85 is recommended for all 12-bit D/A converter applications where reliability and performance over temperature are of paramount importance.

***COVERED BY PATENT NUMBERS: 3,978,473; RE 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.**

[1] For details of calculations see Application Note, "AD DAC85 Reliability Predictions".

PRODUCT HIGHLIGHTS

1. The AD DAC85 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC85 the optimum choice for applications where performance and reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC85 offers a maximum nonlinearity error of ±0.012%, ±20ppm/°C maximum gain drift, and a total accuracy drift in the bipolar configuration of ±10ppm/°C maximum.
5. The low T.C. Binary ladder guarantees that all AD DAC85 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output modes are available in either of the BCD or binary input formats.

SPECIFICATIONS (Typical @ +25°C unless otherwise specified)

MODEL	AD DAC85C CBI	AD DAC85C CCD	AD DAC85 CBI	AD DAC85 CCD	AD DAC85LD CBI	AD DAC85MIL CBI	UNITS
DIGITAL INPUT							
Resolution	12		12		12	12	Bits
		3		3			Digits
Logic Levels (TTL Compatible)							
Logic "1" (at +1μA)	+2V dc min, +5.5V dc max	*	*	*	*	*	V
Logic "0" (at −100μA)	0V dc min, +0.8V dc max	*	*	*	*	*	V
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ 25°C (max)	±1/2	±1/4	±1/2	±1/4	±1/2	±1/2	LSB
0 to +70°C (max)	±1/2	±1/2					LSB
−25°C to +85°C (max)			±1/2	±1/2	±1/2	±1/2	LSB
−55°C to +125°C (max)						±3/4	LSB
Differential Linearity Error	±1/2	*	*	*	*	*	LSB
Gain Error[1]	±0.1	*	*	*	*	*	%
Offset Error[1]	±0.05	*	*	*	*	*	% of FSR[2]
Minimum Temperature Range for Guaranteed Monotonicity	0 to +70	0 to +70	−25 to +85	−25 to +85	−25 to +85	−55 to +125	°C
DRIFT[3]							
Gain 0 to +70°C (max)	±20	±20	±20	±20	±10	±20	ppm/°C
−25°C to +85°C (max)	—	—	±20	±20	±10	±20	ppm/°C
−55°C to +125°C (max)	—	—	—	—	—	±20	ppm/°C
Offset							
Unipolar 0 to +70°C	+1	+1					ppm of FSR/°C
−25°C to +85°C			±1	±1	±1	±1	ppm of FSR/°C
−55°C to +125°C						±2	ppm of FSR/°C
Bipolar 0 to +70°C (max)	±10						ppm of FSR/°C
−25°C to +85°C (max)			±10		±5	±10	ppm of FSR/°C
−55°C to +125°C (max)						±10	ppm of FSR/°C
CONVERSION SPEED							
Voltage Models							
Settling Time to ±0.01% of FSR for FSR change							
with 10kΩ Feedback	5	*	*	*	*	*	μs
with 5kΩ Feedback	3	*	*	*	*	*	μs
for 1LSB change	1.5	*	*	*	*	*	μs
Slew Rate	20	*	*	*	*	*	V/μs
Current Models							
Settling Time to ±0.01% of FSR for FSR change 10 to 100Ω load	300	*	*	*	*	*	ns
1kΩ load	1	*	*	*	*	*	μs
ANALOG OUTPUT							
Voltage Models Ranges — CBI Units	±2.5, ±5, ±10, +5, +10	*	*	*	*	*	V
CCD Units	+10	*	*	*	*	*	V
Output Current (min)	±5	*	*	*	*	*	mA
Output Impedance (dc)	0.05	*	*	*	*	*	Ω
Current Models							
Ranges	±1, −2	*	*	*	*	*	mA
Output Impedance - Bipolar	3.2	*	*	*	*	*	kΩ
Unipolar	6.65	*	*	*	*	*	kΩ
Compliance	−2.5, +10.5	*	*	*	*	*	V
Internal Reference Voltage (V_r)	6.3	*	*	*	*	*	V
Output Impedance	1.5	*	*	*	*	*	Ω
Max. External Current[4]	2.5	*	*	*	*	*	mA
Max Reference Error	±2	*	*	*	*	*	%
Tempco of Drift	±10 typ, ±20 max	*	*	*	*	*	ppm of V_r/°C
POWER SUPPLY SENSITIVITY							
+15V Supply	±0.002	*	*	*	*	*	% of FSR/% V_S
−15 and +5V Supplies	±0.002	*	*	*	*	*	% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
Rated Voltage	±15 and +5	*	*	*	*	*	V
Range	±14.5 to ±15.5 and +4.50 to +15.5	*	*	*	*	*	V
Supply Drain							
+15V (including 5mA load)	15 typ, 20 max	*	*	*	*	*	mA
+5V	15 typ, 20 max	*	*	*	*	*	mA
−15V	25 typ, 30 max	*	*	*	*	*	mA
TEMPERATURE RANGE							
Specification	0 to +70	*	−25 to +85	−25 to +85	−25 to +85	−55 to +125	°C
Operating	−25 to +85	*	−55 to +125	−55 to +125	−55 to +125	−55 to +125	°C
Storage	−55 to +125	*	*	*	*	*	°C

NOTES

*Specifications same as AD DAC85C CBI.

[1] Adjustable to zero with external trim potentiometer.

[2] FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.

[3] To maintain drift spec internal feedback resistors must be used for current output models; the buried zener reference drift is a nonlinear function of temperature: all devices are tested to insure that actual drift at any temperature within the specified operating range is less than guaranteed maximum.

[4] With no degradation of specifications under constant load.

Specifications subject to change without notice.

MIL-STD-883B

The rigors of the military/aerospace environment (temperature extremes, humidity, mechanical stress, etc.), demand the utmost in electronic circuits. The AD DAC85 with the inherent reliability of integrated circuit construction, was designed with these applications in mind. To further insure reliability, the AD DAC85 is offered with 100% screening to MIL-STD-883B, method 5008.

Table I details the test procedures of MIL-STD-883B. All AD DAC85 models with an 883B suffix have been processed in accordance with these tests on a 100% basis: AD DAC85 MIL-CBI-V-883B is an example of 883B designation.

TEST	METHOD	PURPOSE
1) Internal Visual (Pre cap)	2017	Removes potentially defective parts with respect to bonding, metalization, etc.
2) Stabilization Bake	Method 1008, Test Condition C, 24 hours @ +150°C	Stabilizes circuit elements, thin film resistors.
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, −65°C to +150°C	Changes operating characteristics.
4) Constant Acceleration	Method 2001, Test Condition B, Y1 plane, 10kg	Removes potential failures due to weak wire or chip bonding; insures package integrity.
5) Seal, Fine and Gross	Method 1014, Test Condition A or B and C, 5 x 10^{-7} cc/sec	Verifies hermetic sealing.
6) Burn-in Test	Method 1015, Test Condition D, 168 hours @ +125°C	Removes potential electrical failures.
7) Final Electrical Tests	Performed at +25°C, maximum and minimum operating temperatures	Removes any failures from the above tests and verifies electrical specifications.
8) External Visual	Method 2009	Insures physical condition of package and branding.

AD DAC85 ORDERING GUIDE

MODEL	INPUT CODE	OUTPUT MODE	TEMPERATURE RANGE
AD DAC85C-CBI-V	Binary	Voltage	0°C to +70°C
AD DAC85C-CBI-I	Binary	Current	0°C to +70°C
AD DAC85-CBI-V	Binary	Voltage	−25°C to +85°C
AD DAC85-CBI-I	Binary	Current	−25°C to +85°C
AD DAC85LD-CBI-V	Binary	Voltage	−25°C to +85°C
AD DAC85LD-CBI-I	Binary	Current	−25°C to +85°C
AD DAC85MIL-CBI-V	Binary	Voltage	−55°C to +125°C
AD DAC85MIL-CBI-I	Binary	Current	−55°C to +125°C
AD DAC85C-CCD-V	Binary Coded Decimal	Voltage	0°C to +70°C
AD DAC85C-CCD-I	Binary Coded Decimal	Current	0°C to +70°C
AD DAC85-CCD-V	Binary Coded Decimal	Voltage	−25°C to +85°C
AD DAC85-CCD-I	Binary Coded Decimal	Current	−25°C to +85°C

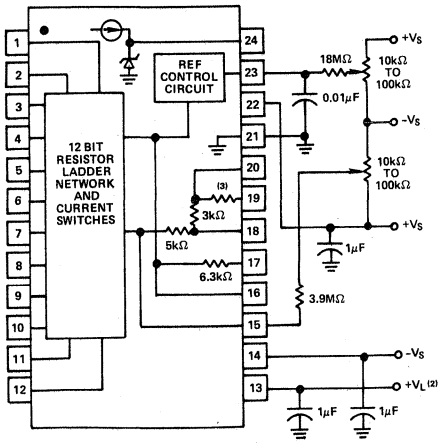


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

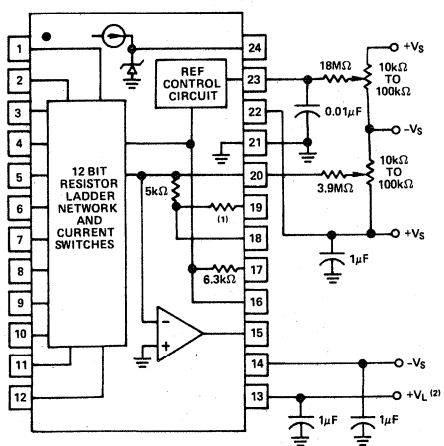


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

NOTES:

1. 3kΩ for CCD models. 5kΩ for CBI models.
2. If connected to $+V_S$ which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.

PIN CONFIGURATION

24 LEAD DUAL IN-LINE PACKAGE

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1(MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)

I Models	Pin #	V Models
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref Input	16	Ref Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
$6.3V_{REF}$ Out	24	$6.3V_{REF}$ Out

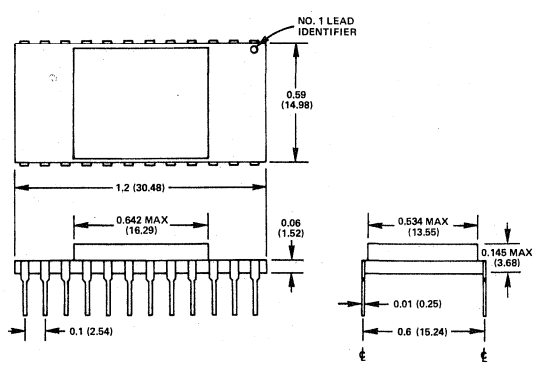


Figure 3. Outline Dimensions (Dimensions shown in inches and (mm))

DIGITAL INPUT CODES

The AD DAC85 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+½ Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
CCD Models	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table 1. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it can not be corrected for. The linearity error of the AD DAC85 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of -25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next. Monotonicity over the -25°C to +85°C range is guaranteed in the AD DAC85 to insure that the analog output will not decrease with increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC85 model at the lowest operating temperature, +25°C and the highest operating temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. For example, the offset for the "C" version is measured at 0°C, +25°C and +70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each AD DAC85 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 4).

Voltage Output Models. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 ... 1 1 to 1 0 0 0 ... 0 0), the point at which the worst case settling time occurs.

Current Output Models. Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage range of ±1V and 0 to -2V(see Table IV).

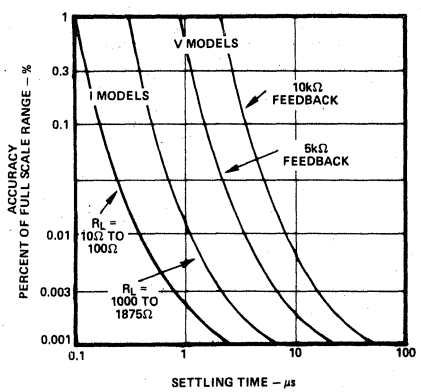


Figure 4. Full Scale Range Settling Time vs. Accuracy

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All AD DAC85 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven off of the reference will result in gain variations of the AD DAC85. All gain adjustments should be made under constant load conditions.

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams (Figures 1 and 2). These capacitors (1μF electrolytic recommended) should be located close to the AD DAC85. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 18MΩ resistors (20% carbon or better) should be located close to the AD DAC85 to prevent noise pick-up. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 7 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capcitor should be connected from this pin to common to prevent noise pick-up. Figures 8 and 9 show the relationship of the OFFSET and GAIN adjustments to the unipolar and bipolar D/A converter.

Offset Adjustment. For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COD, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes and the block diagrams for offset adjustment connections.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the block diagrams for gain adjustment connections.

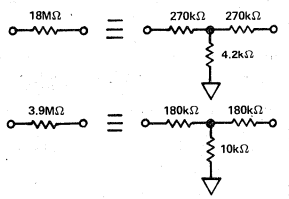


Figure 7. Equivalent Resistances

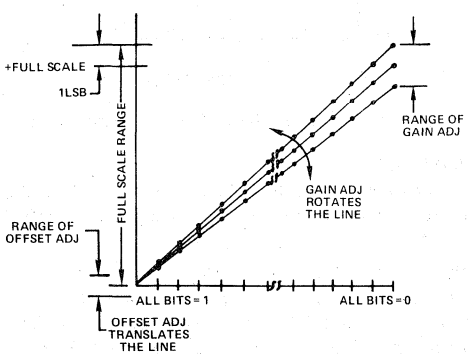


Figure 8. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter. (Input, Horizontal; Output, Vertical).

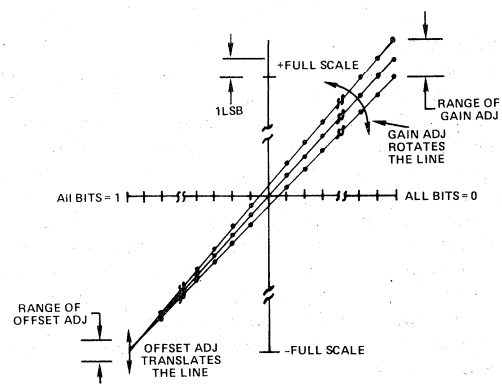


Figure 9. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A CONVERTER. (Input, Horizontal; Output, Vertical).

	DIGITAL INPUT	ANALOG OUTPUT			
	12 Bit Resolution	VOLTAGE*		CURRENT	
	MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	0.488μV
	1LSB	2.44mV	4.88mV	0.488mA	+1.000mA
	3 Digital Resolution				
	MSB LSB				
CCD Models	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	1LSB	10.00mV	N/A	1.25μA	N/A

*To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

**Normal full scale range with correct codes; output can go higher if illegal codes are applied.

Table II. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC85 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 10).

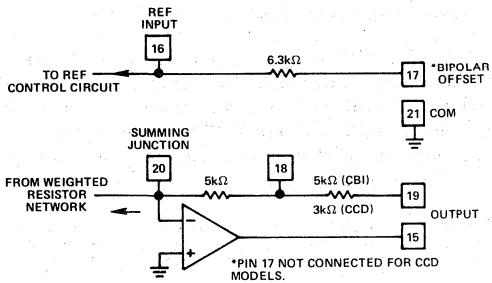


Figure 10. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC85 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections-Voltage Model AD DAC85

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 11 and 12. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC85 output specifications. If exact output ranges are not required, the external resistors are not needed.

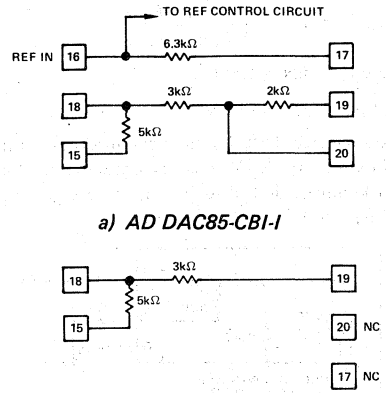


Figure 11. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the AD DAC85 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

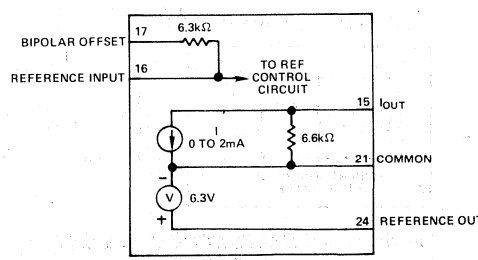


Figure 12. AD DAC85 Current Model Equivalent Output Circuit

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	1% Metal Film External Resistance R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset: R_{LS}	Bipolar Offset: R_{LP}
CSB	0 to -2V	0.968kΩ	210Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	3kΩ	N/A	3.57kΩ	N.C.	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	249Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

Table IV. Current Model/Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 13 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L} \right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = -2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With R_{LS} = 0, V_{OUT} = -1.69V.

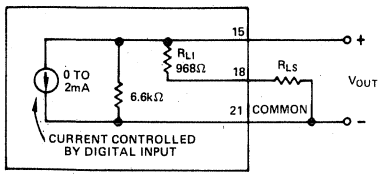


Figure 13. Equivalent Circuit AD DAC85-CBI-I Connected for Unipolar Voltage Output with Resistive Load

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 14 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}},$$

$$V_{OUT} = -1.25mA \left(\frac{6.9k \times R_L}{6.9k + R_L} \right)$$

If $R_{LP} = \infty$, V_{OUT} = -3.62V

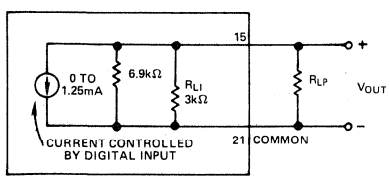


Figure 14. AD DAC85-CCD-I Connected for Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 15, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k} \right)$$

Where R_L max = 11.18kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC85 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 16,

$$V_{OUT} = I_{OUT} \times R_F$$

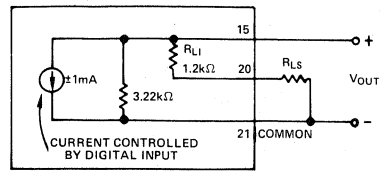


Figure 15. AD DAC85-CBI-I Connected for Bipolar Output Voltage with Resistive Load

where I_{OUT} is the AD DAC85 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC85 provides output voltage ranges the same as the voltage model AD DAC85. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 16.

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	A	24

Table V. Voltage Range of Current Output AD DAC85

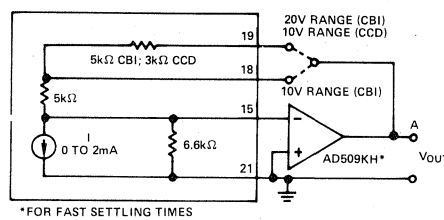


Figure 16. External Op Amp — Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges (see Figure 17). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

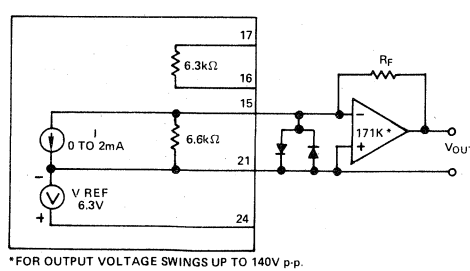


Figure 17. External Op Amp — Using External Feedback Resistors

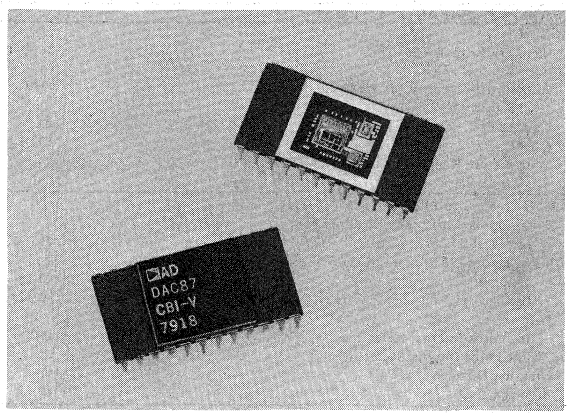
ANALOG DEVICES

Wide Temperature Range 12-Bit IC D/A Converter

AD DAC87

FEATURES

- Wide Temperature Range: -55°C to +125°C
- Pin-Compatible with AD DAC80 and AD DAC85
- 3 Chip, High Reliability Construction
- Low Power Dissipation
- Laser-Trimmed to High Accuracy:
  - ±3/4LSB Max Nonlinearity, -55°C to +125°C
- High Stability, High Current Output
  - Buried Zener Reference
- On-Board Output Amplifier (V Models)
- 24 Lead Side Brazed Hermetically-Sealed Ceramic DIP
- MIL-STD-883 Processing Available



PRODUCT DESCRIPTION

The AD DAC87 is a high performance 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and an optional output amplifier. The digital inputs are TTL compatible with complementary binary (CBI) input coding. The AD DAC87 offers output voltage ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either ±1mA or 0 to -2mA.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC87 devices. An innovative 3-chip construction improves reliability by a factor of five.[1] The AD DAC87 incorporates a fully differential, non-saturating precision current switching cell structure[2] which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability SiCr thin film resistors are trimmed with a fine resolution laser, resulting in low differential linearity errors. A low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete zener references.

The AD DAC87 is recommended for all 12-bit D/A converter applications where reliability and performance over temperature are of paramount importance.

PRODUCT HIGHLIGHTS

1. The AD DAC87 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC87 the optimum choice for applications where performance and reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC87 offers a maximum nonlinearity of ±0.012%, ±25ppm/°C maximum gain drift, and a total accuracy drift in the bipolar configuration of ±0.24% of FSR maximum over the -55°C to +125°C temperature range.
5. The low T.C. Binary ladder guarantees that all AD DAC87 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output models are available.
9. The solder-sealed ceramic package provides a reliable hermetic metal-to-metal seal.
10. All accuracy and drift parameters are 100% tested at -55°C and +125°C to insure high performance over the full temperature range.
11. Both voltage and current output models are available processed to the requirements of MIL-STD-883, method 5008, class B.

[1] For details of calculations see Application Note, "AD DAC87 Reliability Predictions".

[2] COVERED BY PATENT NUMBERS: 3,978,473; RE 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	AD DAC87-CBI			
	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (TTL Compatible)				
Logic "1" (at +1μA)	+2		+5.5	V
Logic "0" (at −100μA)	0		+0.8	V
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error @ +25°C		±1/4	±1/2	LSB
−55°C to +125°C			±3/4	LSB
Differential Linearity Error at +25°C		±1/2	±3/4	LSB
−55°C to +125°C			±1	LSB
Gain Error[1]		±0.1	±0.2	%
Offset Error[1]		±0.05	±0.1	%FSR[2]
Temperature Range for Guaranteed Monotonicity	−55		+125	°C
DRIFT[3] (−55°C to +125°C)				
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)		±15	±30	ppm of FSR/°C
Total Error (−55°C to +125°C)[4]				
Unipolar		±0.13	±0.3	% of FSR
Bipolar		±0.12	±0.24	% of FSR
Gain				
Including Internal Reference		±10	±25	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±5	±10	ppm of FSR/°C
CONVERSION SPEED				
Voltage Model (AD DAC87-CBI-V)				
Settling Time to ±0.01% of FSR for FSR change				
with 10kΩ Feedback		5		μs
with 5kΩ Feedback		3		μs
for 1LSB change		1.5		μs
Slew Rate	10	20		V/μs
Current Model (AD DAC87-CBI-V)				
Settling Time to ±0.01% of FSR				
for FSR Change 10 to 100Ω Load		300		ns
1kΩ Load		1		μs
ANALOG OUTPUT				
Voltage Models				
Ranges		±2.5, ±5, ±10, 0 to +5, 0 to +10		V
Output Current	±5			mA
Output Impedance (dc)		0.05		Ω
Short Circuit Duration		INDEFINITE TO COMMON		
Current Models				
Ranges		±1, 0 to −2		mA
Output Impedance − Bipolar	2.5	3.3	4.1	kΩ
− Unipolar	5.0	6.6	8.2	kΩ
Compliance	−1.5		+10.5	V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	V
Output Impedance		1.5		Ω
Max. External Current[5]			2.5	mA
Tempco of Drift		±5	±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY				
+15V Supply		±0.002	±0.003	% of FSR/%V_S
−15V and +5V Supplies		±0.002	±0.003	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS				
Rated Voltages		±15, +5		V
Range	±13.5, +4.5		±16.5, +16.5	V
Supply Drain				
+15V (Including 5mA Load)		10	20	mA
+5V		10	20	mA
−15V		20	30	mA
TEMPERATURE RANGE				
Specification	−55		+125	°C
Storage	−65		+150	°C

NOTES
[1] Adjustable to zero with external trim potentiometer.
[2] FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
[3] To maintain drift spec internal feedback resistors must be used for current output models; the buried zener reference drift is a nonlinear function of temperature: all devices are tested to insure that actual drift at any temperature within the specified operating range is less than guaranteed maximum.
[4] With gain and offset errors adjusted to zero at +25°C.
[5] With no degradation of specifications under constant load.

Specifications subject to change without notice.

MIL-STD-883

The rigors of the military/aerospace environment (temperature extremes, humidity, mechanical stress, etc.), demand the utmost in electronic circuits. The AD DAC87, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. To further insure reliability, the AD DAC87 is available with 100% screening to MIL-STD-883, method 5008. Consult factory for pricing.

TEST	METHOD	PURPOSE
1) Internal Visual (Pre cap)	2017	Removes potentially defective parts with respect to bonding, metalization, etc.
2) Stabilization Bake	Method 1008, Test Condition C, 24 hours @ +150°C	Stabilizes circuit elements, thin film resistors.
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C	Potential mechanical and electrical failures caused by thermal removes stresses.
4) Constant Acceleration	Method 2001, Test Condition B, Y1 plane, 10,000g	Removes potential failures due to weak wire or chip bonding; insures package integrity.
5) Seal, Fine and Gross	Method 1014, Test Condition A or B and C, 5 x 10^{-7} cc/sec	Verifies hermetic sealing.
6) Burn-in Test	Method 1015, Test Condition D, 168 hours @ +125°C	Removes potential electrical failures
7) Final Electrical Tests	Performed at +25°C, maximum and minimum operating temperatures	Removes any failures from the above tests and verifies electrical specifications.
8) External Visual	Method 2009	Insures physical condition of package and branding.

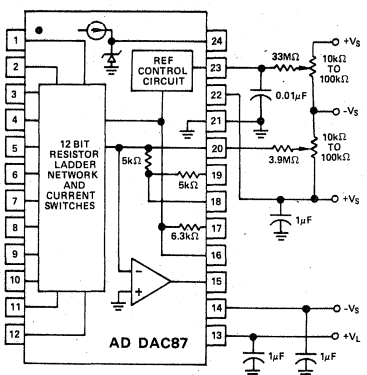


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

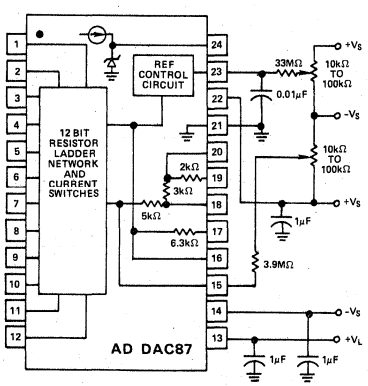


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

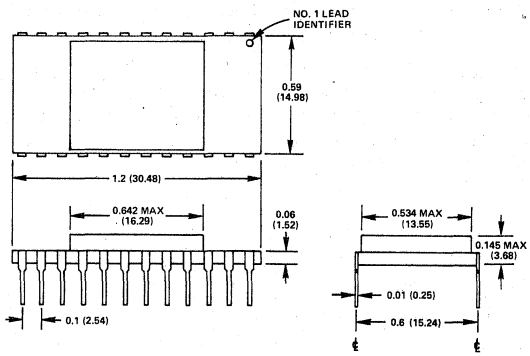


Figure 3. Outline Dimensions (Dimensions shown in inches and (mm))

PIN CONFIGURATION

24 LEAD DUAL IN-LINE PACKAGE

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1(MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref Input	16	Ref Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
$6.3V_{REF}$ Out	24	$6.3V_{REF}$ Out

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers, as shown in the block diagrams on the previous page. TCR of the potentiometers should be 100ppm/°C or less. If it is not convenient to use the 3.9MΩ and 33MΩ resistors shown, a functionally equivalent "T" network, as shown in Figure 4 may be substituted in each case.

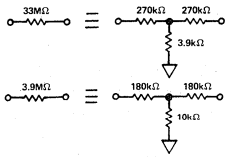


Figure 4. Equivalent Resistances

Offset Adjustment. For unipolar configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table I for corresponding codes and the block diagrams on the previous page for offset adjustment connections.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and the block diagrams for gain adjustment connections.

DIGITAL INPUT		ANALOG OUTPUT			
12 Bit Resolution		VOLTAGE		CURRENT	
MSB	LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000		+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111		+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000		+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111		0.0000V	-10.0000V	0.0000mA	+1.000mA
1LSB		2.44mV	4.88mV	0.488μA	0.488μA

Table I. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC87 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 5).

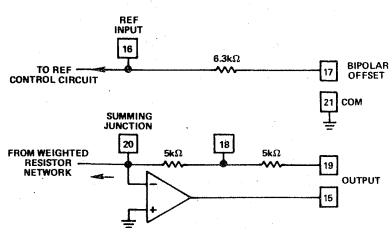


Figure 5. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC87 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table II.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24

Table II. Output Voltage Range Connections AD DAC87-CBI-V

CURRENT OUTPUT MODELS

The current output model of the AD DAC87 can be used to drive a resistive load directly to produce a voltage output. Recommended output ranges and pin connections are shown in Table III.

Digital Input Codes	Output Range	External Resistance R_{LS}	Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}
CSB	0 to -2V	210Ω	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)
COB or CTC	±1V	249Ω	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)

Table III. AD DAC87-CBI-I Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 6a will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L}\right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = -2.5V

To achieve specified drift connect the internal scaling resistor (R_{LI}) as shown in Table III to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, $V_{OUT} = -1.69V$.

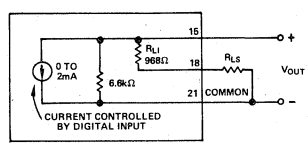


Figure 6a. Unipolar Voltage Output

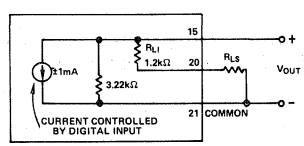


Figure 6b. Bipolar Voltage Output

Figure 6. AD DAC87-CBI-I Equivalent Circuit Driving Resistive Loads

DRIVING A RESISTIVE LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 6b, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k}\right)$$

Where R_L max = 11.18kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

ANALOG DEVICES

High Speed Digital to Analog Converters

DAC1106/DAC1108

FEATURES
High Speed
8 Bits in 25ns
10 Bits in 50ns
12 Bits in 60ns
Adjustment Free Operation
Gain TC: ±10ppm/°C
Linearity Error: ±½LSB max
Small Size: 2" x 2" x 0.4" Module

GENERAL DESCRIPTION

The DAC1108 is a high speed, current output digital-to-analog converter with 12-bit resolution and accuracy. The very fast settling times to 0.05% accuracy of 60ns and to 0.01% accuracy of 150ns make it ideal for use in high speed applications such as computer driven displays, automatic test equipment, and function generators. In addition to the ±½LSB maximum linearity error, the DAC1108 features temperature coefficients of 30ppm/°C for gain and 8ppm/°C for linearity.

The DAC1106 is also a high speed, current output digital-to-analog converter which is available in both 8- and 10-bit versions. The very fast settling times to ½LSB or 25ns (8-bit models) and 50ns (10-bit models). Accuracy specifications include ±½LSB linearity, 10ppm/°C temperature coefficient, and 0.002%/V power supply rejection.

Everything needed to perform high speed conversions is contained in the compact 2" x 2" x 0.4" package of the DAC1106/1108. Included are a precision temperature compensated reference source, high speed current switches and a carefully trimmed network of weighting resistors. Because of the inherent stability and careful factory adjustment of this device, no external zero or gain adjustment potentiometers are required.

The digital inputs of the DAC1106/1108 are fully DTL/TTL compatible. Binary code is used for unipolar operation and Offset Binary code is used for bipolar operation. The current output of this device can be applied directly to an external resistor to develop a voltage output or it can be applied to the input of a fast settling op amp if amplification or impedance transformation is desired.

INPUT CONSIDERATIONS

The binary weighted current sources which form the basis of the digital to analog conversion process are directly switched by their associated input bits. A change in the converter's current output will begin to occur approximately 10nsec after a new digital word is applied. Because of this extremely fast response, time skew in the digital input can result in momentary erroneous outputs or "glitches". Consider, for example, the case of a transition from 1000 . . . 0 to 0111 . . . 1, a step of only one LSB. If the MSB turns to a "0" before the rest of the bits have turned to "1"s, the input will momentarily be 0000 . . . 0 and the converter will start to respond accordingly as shown below in Figure 1.

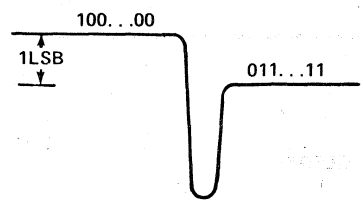


Figure 1. Switching Transient Caused by Time Skew

These switching transients will be minimized if the digital input data time skew is held to less than 5ns.

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODELS	DAC1106	DAC1108
RESOLUTION	8/10 Bits	12 Bits
DIGITAL INPUTS	TTL Compatible	*
0V ≤ Logic "0" ≤ 0.8V	@ -3.2mA (max)	*
+2V ≤ Logic "1" ≤ 15V	@ 80μA (max)	*
INPUT CODES		
Unipolar	Binary	*
Bipolar	Offset Binary	*
OUTPUT RANGES	0 to +5mA	*
	-2.5 to +2.5mA	*
OUTPUT IMPEDANCE	600Ω ±1% (Unipolar)	510Ω ±2%
OUTPUT VOLTAGE COMPLIANCE	±1.2V	*[1]
ABSOLUTE ACCURACY		
Full Scale	±0.1%	*
Offset	±2mA	*
SETTLING TIME		
To 0.2%	25ns (30 max)	
To 0.1%	40ns (50 max)	
To 0.05%	50ns (60 max)	60ns
To 0.01%		150ns
LINEARITY ERROR	±½LSB max	*
TEMPERATURE COEFFICIENT		
Gain	±10ppm/°C	±30ppm/°C
Zero	±75μV/°C	*
Linearity	±8ppm/°C	*
TEMPERATURE RANGE		
Operating	0 to +70°C	*
Storage	-55°C to +85°C	-55°C to +125°C
POWER REQUIREMENTS		
+15V ±5%	47mA max	42mA max
-15V ±5%	37mA max	10mA max
POWER SUPPLY SENSITIVITY		
Gain	0.002%/V	0.01%/%ΔV
OUTLINE DIMENSIONS	2" x 2" x 0.4"	*

[1] ±1V for rated dynamic performance.
*Specifications same as DAC1106.
Specifications subject to change without notice.

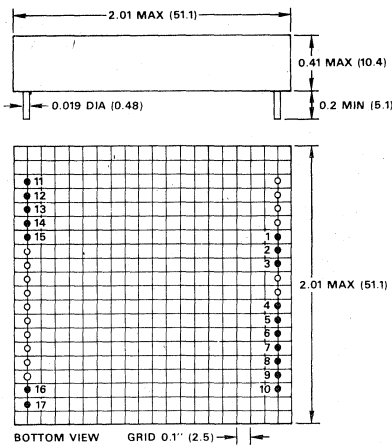
ORDERING GUIDE:

Model DAC1106/XXX

- 001 (EIGHT BIT)
- 002 (TEN BIT)

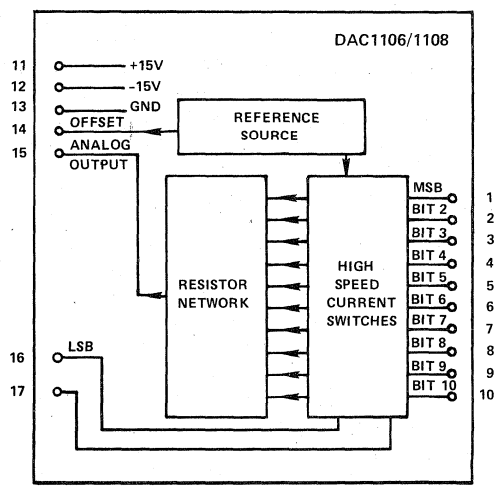
OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 2 ounces (57 grams).
Pins 9 and 10 included on 10-bit models only.
For plug-in mounting card order Board No. AC4102.

BLOCK DIAGRAM AND PIN DESIGNATIONS



NOTE:
DAC1106 PIN 16 - N.C.
PIN 17 DELETED

DIGITAL INPUTS

The DAC1106/1108 is fully TTL/DTL compatible with each input bit representing two standard TTL Loads. The logic levels of

$0V \leqslant$ Logic "0" $\leqslant 0.8V$
$+2V \leqslant$ Logic "1" $\leqslant 15V$ (Absolute Max)

are also compatible with CMOS logic systems. When using this device in a CMOS system, standard CMOS/TTL interface rules must be observed to insure that the driving gate is capable of sinking at least 3.2mA.

The simple addition of an external inverter ahead of the MSB input terminal, as shown below in Figure 2, allows the bipolar Two's Complement code to be used.

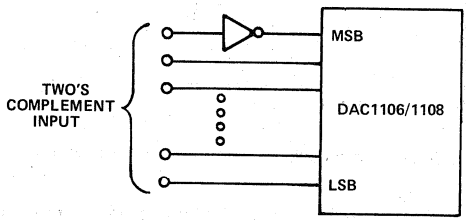


Figure 2. Two's Complement Input Connection

OUTPUT CHARACTERISTICS

The output of the DAC1106/1108 represents the sum of the currents produced by the individual binary-weighted current sources in response to the digital input word. This current varies from 0 to +5mA. In order to produce the half scale offset needed for bipolar outputs, a current of exactly -2.5mA must be added to the output. Such a current is generated internally and is available at pin 14. The analog outputs which are produced by various digital inputs are shown in the following tables.

UNIPOLAR

Digital Input	Analog Output		
	1106-001	1106-002	1108
111 111	+4.981mA	+4.995mA	+4.999mA
100 000	+2.500mA	*	*
000 001	+19.5μA	+4.88μA	+1.22μA
000 000	0mA	*	*

BIPOLAR

Digital Input	Analog Output		
	1106-001	1106-002	1108
111 111	+2.481mA	+2.495mA	+2.499mA
100 000	0mA	*	*
000 000	-2.500mA	*	*

Figures 3 and 4 illustrate the converter's output impedance characteristics for unipolar and bipolar operation.

*Specifications same as 1106-001.

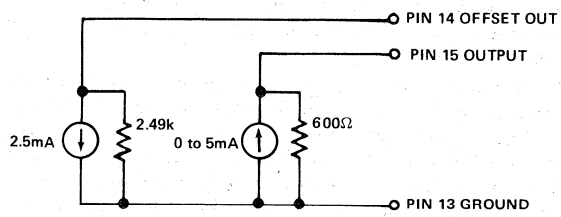


Figure 3. Equivalent Circuit DAC (Unipolar)

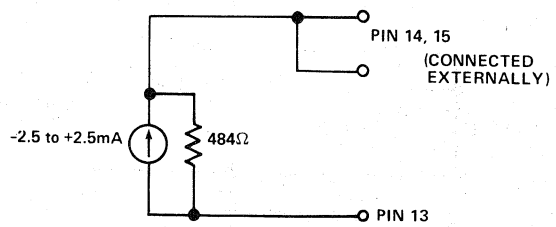


Figure 4. Equivalent Circuit DAC (Bipolar)

OUTPUT CONNECTIONS

The circuits used to develop an output voltage across a resistor are shown below in Figures 5 and 6 for unipolar and bipolar operation.

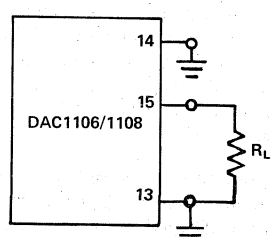


Figure 5. Voltage Output with Load Resistor (Unipolar)

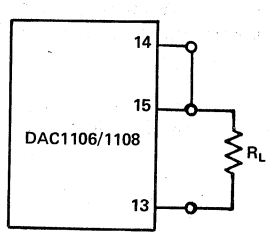


Figure 6. Voltage Output with Load Resistor (Bipolar)

In both cases, the output voltage is limited to ±1.2V max. By referring to Figures 3 and 4, the user can readily compute the value of R_L needed to produce the desired full scale voltage. For example, a 300Ω resistor will develop a 0 to +1V F.S. unipolar output and a 2.325kΩ resistor will develop a +1V F.S. bipolar output.

The DAC1106/1108 may be used in conjunction with a high speed external op amp when outputs greater than ±1.2V and 5mA are needed. Because current output converters such as the DAC1106/1108 are not ideal current sources, the op amp does not operate in a unity gain configuration. Figure 7 below shows, in simplified form, a unipolar DAC driving an op amp.

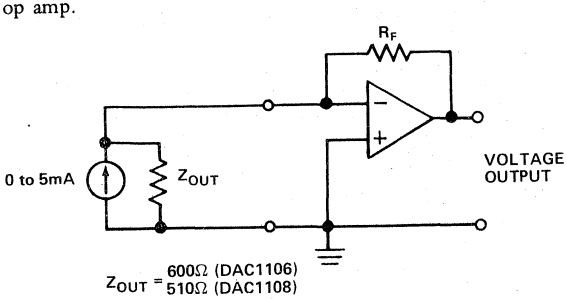


Figure 7. Voltage Output with an Op Amp Simplified Diagram

Because of the output impedance, the closed loop gain becomes $1 + R_F/Z_{OUT}$ instead of 1. For example with an R_F of 2kΩ the closed loop gain is 4.33 for DAC1106 and 4.92 for DAC1108.

This can complicate the job of selecting a suitable op amp since most manufacturers specify settling time at unity gain. One extremely fast op amp that performs well at gains of 2 to 6 is the Analog Devices' model 50 differential input, FET amplifier. The model 50 will settle to 10-bit accuracy (0.05%) in a maximum fo 200ns. The high current output of this device (100mA) also makes it ideal for use with the DAC1108 in CRT deflection applications.

Sometimes space or budgetary considerations dictate that an IC rather than a modular op amp be used. In these cases the AD509K fast settling IC op amp is recommended. The AD509K maintains its guaranteed maximum settling time specification (500ns to 0.1%) even at the closed loop gains encountered with the DAC1106/1108. Furthermore, when the closed loop gain is greater than 3, no external compensating components are required.

Figures 8 and 9 below show the proper means of connecting the converter to an op amp for unipolar and bipolar operation.

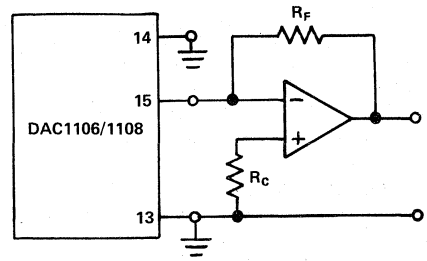


Figure 8. Connections to an External Op Amp (Unipolar)

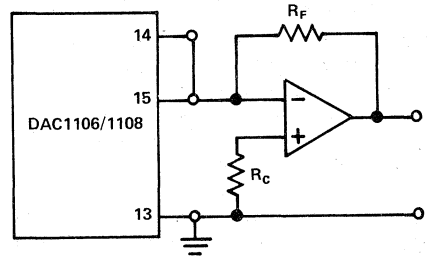


Figure 9. Connections to an External Op Amp (Bipolar)

The resistor R_C is used with the AD509K for bias current compensation. Because of the low bias currents inherent with the model 50, R_C is unnecessary and the noninverting input is connected directly to ground.

Great care must be taken in laying out the circuits of Figures 8 and 9 to assure true high speed performance. Several of the most important considerations are listed below:

1. Keep leads, especially those between the converter output and op amp summing junction, as short as possible to prevent the introduction of noise.
2. Orient components to minimize stray capacitance.
3. Carefully bypass power supplies to the op amp.
4. Select suitable components such as metal film resistors with their low capacitance and low stray inductance.
5. Design the signal and power supply ground circuits so as to prevent the introduction of extraneous voltages in ground signal path.
6. Use separate returns for analog and digital grounds. The DAC1106/1108 and op amp power supply returns go to analog ground; any logic circuits that precede the converter go to digital ground.

High Resolution 16- and 18-Bit Digital to Analog Converters

DAC1136/1137/1138

FEATURES

DAC1138
- 18-Bit Resolution and Accuracy (38μV, 1 Part in 262,144)
- Nonlinearity 1/2LSB Max
- Excellent Stability
- Settling to 1/2LSB (0.0002%) in 10μs
- Hermetically-Sealed Semiconductors

DAC1137
- 18-Bit Resolution, 16-Bit Accuracy
- Stable Linearity over Time & Temperature
- Settling to 1/2LSB (0.0002%) in 10μs

DAC1136
- 16-Bit Resolution and Accuracy
- Low Cost
- Nonlinearity 1/2LSB
- Settling to 1/2LSB (0.0008%) in 6μs

DEGLITCHER IV
- Eliminates DAC Glitches
- Available on DAC1136/1137/1138 Card-Mounted Assembly

GENERAL DESCRIPTION

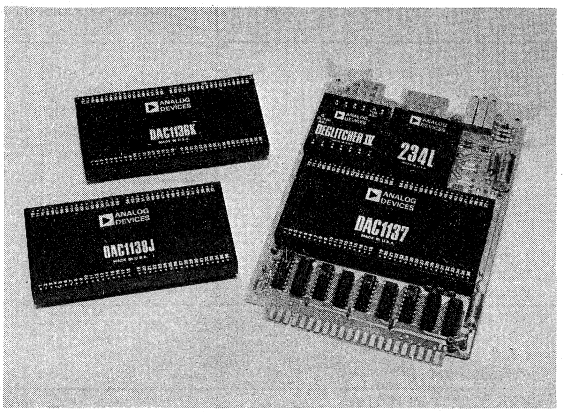
The DAC1136/1137/1138 are complete self-contained voltage or current output modular digital to analog converters with resolutions and accuracies of 16 and 18 bits.

The DAC1136/1137/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of 2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, or ±10V.

The DAC1136/1137/1138 are available as Card-Mounted Assemblies. In this configuration, selectable options include: input codes, output amplifiers, and a high speed transient-suppressing Deglitcher Module, Deglitcher IV.

WHERE TO USE HIGH RESOLUTION DAC'S

The DAC1136/1137/1138 deliver exceptional accuracy for a broad range of display, test, and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65536, and the DAC1137/1138 with a resolution of 18 bits or 1 part in 262,144, are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data distribution systems, high resolution CRT displays, automatic semiconductor testing, photo-typesetting, frequency synthesis and nuclear reactor control.



CERTIFICATE OF CALIBRATION

Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes 1000 hour stability data for the reference zener and linearity test data.

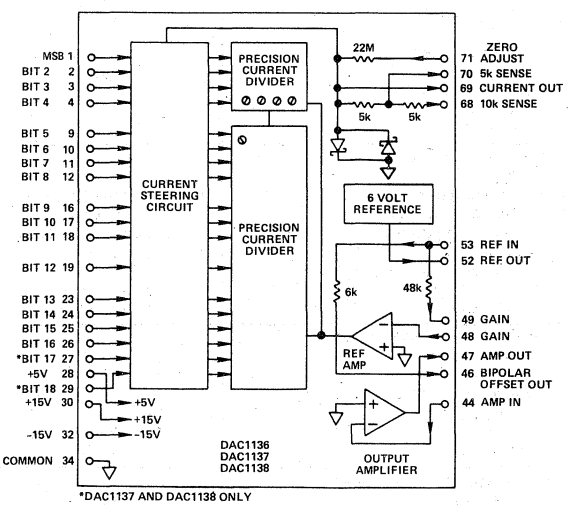


Figure 1. Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C, and rated supply voltage, unless otherwise noted)

Model	DAC1136 J	DAC1136 K	DAC1136 L	DAC1136 CARD-MOUNTED ASSY W/Internal Amp	DAC1136 CARD-MOUNTED ASSY W/44K	DAC1136 CARD-MOUNTED ASSY W/234L
RESOLUTION	16 Bits			Specifications are the same as module unless otherwise noted.		
Magnitude of 1LSB (10V range)	152μV					
DIGITAL INPUTS	TTL/See Figure 2					
Input Codes						
Unipolar	Complementary Binary			See Ordering Guide		
Bipolar	Complementary Offset Binary			See Ordering Guide		
Strobe	None			See Note 1		
ACCURACY						
Integral and Differential Nonlinearity (max)	±1LSB	±0.5LSB	±0.5LSB			
Zero Offset	Adjustable to Zero					
Gain	Adjustable to Full Scale					
Reference Voltage[2]	6.00V ± 0.4% max					
TEMPERATURE COEFFICIENTS (ppm/°C)[3]						
Integral Nonlinearity	±1	±1	±1.5 max			
Differential Nonlinearity	±1	±1	±1.5 max			
Offset						
Unipolar		±0.5		±2		±0.5
Bipolar		±5				
Gain[4]	±6	±6	±8 max			
Reference Voltage		±3				
STABILITY LONG TERM (ppm/10[4] hr)						
Offset		±6		±30		±6
Gain[4]		±5				
Reference Voltage		±7				
POWER SUPPLY REJECTION						
Voltage						
Offset[5]		75dB		80dB		100dB
Gain		80dB				
DYNAMIC CHARACTERISTICS						
Settling Time to ±1/2LSB						
Voltage						
Full Scale Step						
Unipolar		70μs		25μs		45μs
Bipolar		250μs		30μs		60μs
LSB Step		8μs		8μs		8μs
Current						
Full Scale Step		8μs		VOLTAGE OUTPUT ONLY		
LSB Step		6μs				
Noise (rms 10Hz – 100kHz)						
Voltage		30μV		35μV		40μV
Current		1nA		VOLTAGE OUTPUT ONLY		
ANALOG OUTPUTS						
Voltage						
Output Range	0 to +5V, 0 to +10V, ±5V, ±10V					
Rated Output Current	±4mA max			±20mA max		±5mA max
Output Impedance	See Characteristic Curves					
Current						
Output Range						
Unipolar	-2mA to 0mA					
Bipolar	-1mA to +1mA					
VOLTAGE COMPLIANCE						
Rated Accuracy		±2mV		±100μV(E_{OS}) (Factory Trimmed)		±20μV max E_{OS} (No Trim Required)
Clamp Limits[6]		±500mV				
Source Resistance						
Unipolar		>33kΩ				
Bipolar		>5kΩ				
Source Capacitance		150pF				
POWER SUPPLY REQUIREMENTS[7]						
+5V dc ±5%		9mA		95mA	95mA	95mA
±15V dc ±5%		30mA		30mA	40mA	37mA
TEMPERATURE RANGE						
Operating Temperature[8]		0 to +70°C				
Storage Temperature		-55°C to +85°C				

NOTES:
[1] Positive going transition (Logic "0" to Logic "1") will clock data into series 74LS, input, latching registers.
[2] The reference output is high impedance ($Z_{out} \approx 200\Omega$)
[3] Maximum temperature coefficients are guaranteed from 15°C to 35°C, typical from 0 to 70°C.
[4] Exclusive of reference.
[5] Unipolar and bipolar.
[6] Clamp limits are set by Schottky diodes.
[7] Recommended power supply: Analog Devices model 923.
[8] 5% to 95% relative humidity noncondensing.

Specifications subject to change without notice.

SPECIFICATIONS (typical @ +25°C, and rated supply voltage, unless otherwise noted)

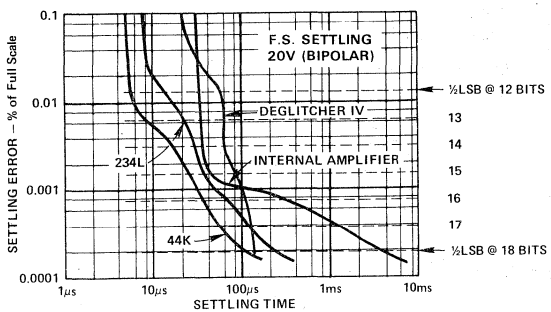
Model	DAC1137	DAC1138 J	DAC1138 K	DAC1137/1138 Card-Mounted Assy W/Internal Amp	DAC1137/1138 Card-Mounted Assy W/234L
RESOLUTION	18 Bits			Specifications are the same as	
Magnitude of 1LSB (10V range)	38μV			module unless otherwise noted	
DIGITAL INPUTS	TTL/See Figure 2				
Input Codes					
Unipolar	Complementary Binary			See Ordering Guide	
Bipolar	Complementary Offset Binary			See Ordering Guide	
Strobe	N.A.			See Note 1	
ACCURACY[2]					
Integral and Differential Nonlinearity (max)	±0.5LSB[3]	±1LSB	±0.5LSB		
Zero Offset Error	Adjustable to Zero				
Gain Error	Adjustable to Full Scale			Offset Pot Supplied on Card	
Reference Voltage[4] (max)	6.0V±0.25%	6.0V±0.13%	*	Gain Pot Supplied on Card	
TEMPERATURE COEFFICIENTS (ppm/°C)[5]					
Integral Nonlinearity	±0.5 max	±0.3	*		
Differential Nonlinearity	±0.5 max	±0.4	*		
Offset					
Unipolar	±0.5	±0.5	*		
Bipolar	±3	±1	*		
Gain[6]	±5 max	±0.8	*		
Reference Voltage	±3	±2	*		
STABILITY LONG TERM (ppm/10³ hr)					
Offset	±3	±2	*	±6	
Gain[6]	±5	±2	*		
Reference Voltage	±7	±10 max	*		
POWER SUPPLY REJECTION					
Voltage					
Offset[7]	75dB			100dB	
Gain	80dB				
DYNAMIC CHARACTERISTICS					
Settling Time to ±1/2LSB					
Voltage					
Full Scale Step					
Unipolar	70μs	250μs	*	130μs	
Bipolar	250μs	3ms	*	200μs	
LSB Step	6μs	18μs	*	20μs	
Current					
Full Scale Step	8μs	10μs	*	VOLTAGE OUTPUT ONLY	
LSB Step	6μs	8μs	*		
Noise (rms 10Hz - 100kHz)					
Voltage	30μV			40μV	
Current	1nA			VOLTAGE OUTPUT ONLY	
ANALOG OUTPUTS					
Voltage					
Output Range	0 to +5V, 0 to +10V, ±5V, ±10V			See Ordering Guide	
Rated Output Current	4mA max			±5mA	
Output Impedance	See Characteristic Curves				
Current					
Output Range					
Unipolar	-2mA to 0mA				
Bipolar	-1mA to +1mA				
VOLTAGE COMPLIANCE					
Rated Accuracy	±2mV max	±200μV max	*	±50μV max	±20μV max (E_{OS})
Clamp Limits[8]		±500mV			
Source Resistance					
Unipolar	>33kΩ				
Bipolar	>5kΩ				
Source Capacitance	150pF				
POWER SUPPLY REQUIREMENTS[9,10]					
+5V dc ±5%	9mA			95mA	95mA
±15V dc ±5%	30mA			30mA	37mA
TEMPERATURE RANGE					
Operating Temperature[11]	0 to +70°C				
Storage Temperature	-55°C to +85°C				

NOTES:
[1] Positive going transition (Logic "0" to Logic "1") will clock data into logic series 74LS network.
[2] Suggested calibration check: 6 months (DAC1137); 3 months (DAC1136, DAC1138).
[3] DAC1137 has 18-bit resolution and 16-bit accuracy, therefore LSB values are referred to 16 bits for the DAC1137.
[4] The reference output is high impedance, maximum load 1μA, $Z_{out} \approx 200\Omega$.
[5] Maximum temperature coefficients are guaranteed from 15°C to 35°C, typical from 0 to 70°C.
[6] Exclusive of reference.
[7] Unipolar and bipolar.
[8] Clamp limits are set by Schottky diodes.
[9] Recommended power supply: Analog Devices model 923.
[10] Change in differential linearity from factory setting due to power supply voltage variation from nominal is ≈ 3.5ppm/VΔV_S.
[11] 5% to 95% relative humidity noncondensing.

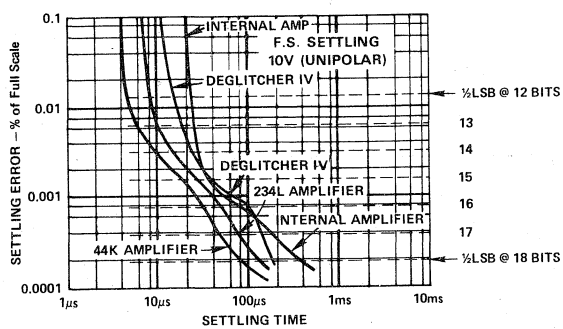
*Specifications same as DAC1138J.

Specifications subject to change without notice.

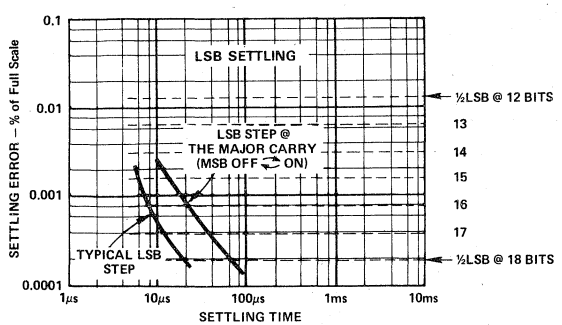
Characteristic Curves*



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 20V Output Step (+10V ⇄ -10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 10V Output Step (0V ⇄ +10V)

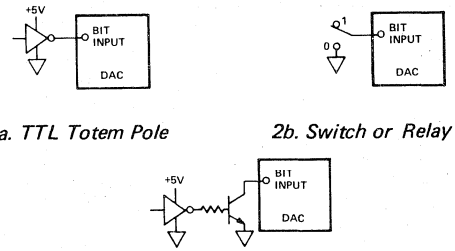


Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for LSB Steps (Essentially Independent of Amplifier Used). With Deglitcher IV, the LSB Step at the Major Carry Settles as Fast as the Typical LSB Step, Following the 11μs Hold Period.

*NOTE: All curves typical at rated supply voltage.
F.S. = Full Scale

INPUT CONSIDERATIONS

The DAC1136/1137/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.



2a. TTL Totem Pole *2b. Switch or Relay Input*[2]

2c. CMOS Input

1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULL-UP. THE CONVERTERS HAVE INTERNAL 10kΩ PULL-UP ON EACH INPUT TO 3.8V.
2. USE SPST SWITCH OR REPLAY TO GROUND. WHEN SWITCH IS OPEN, THE INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

Figure 2. Input Connections

OUTPUT CONNECTIONS AND GUARDING

The DAC1136/1137/1138 output connections for various voltage ranges are shown in Figure 3.

Since an LSB is only 38μV (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the current output of the converter from leakage current. Any connection made to the DAC's current output (pin 69) should be guarded. Suggested printed circuit board guarding is shown in Figure 3. The optional Card-Mounted Assemblies of the DAC1136/1137/1138 have been carefully designed for optimum guarding and performance.

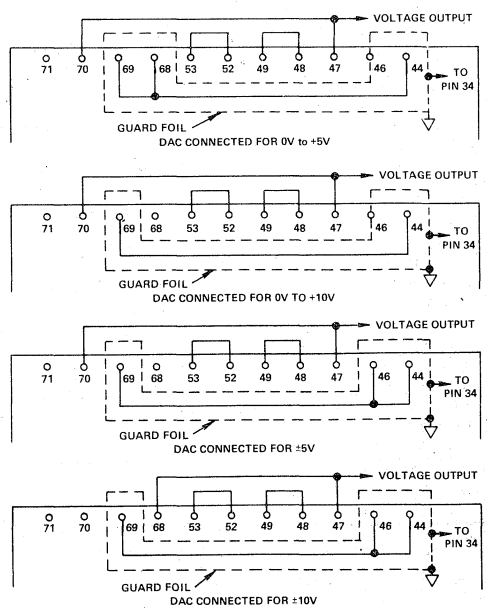
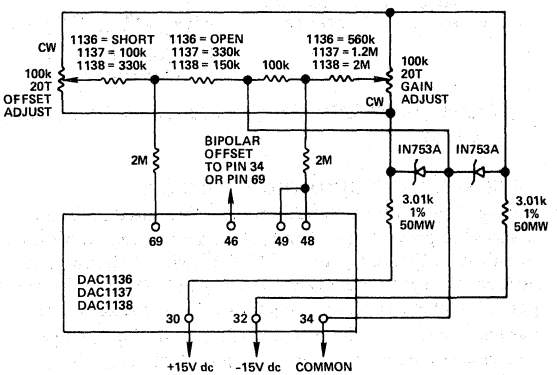


Figure 3. Output Voltage Connections and Suggested PCB Guarding (Unipolar and Bipolar)

GAIN AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with external potentiometers which the user supplies. With the appropriate digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The proper connections for offset and gain are shown in Figure 4. The voltmeter used to measure the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. Because of the interaction between offset and gain adjustments, the adjustment procedure described below should be carefully followed. Offset adjustment affects gain, but gain adjustment does not affect offset.



NOTES:
1. ALL FIXED RESISTORS ARE 5% CARBON COMP, UNLESS OTHERWISE NOTED.
2. ALL POTENTIOMETERS ARE 20-TURN INFINITE RESOLUTION TYPE.

Figure 4. Gain and Offset Adjustments

For unipolar mode, apply a digital input of all "1's" (complementary binary code for zero output) and adjust the offset potentiometer until a 0.00000V output is obtained (see Table 1). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output is obtained (see Table 1).

For bipolar mode, apply a digital input of all "1's" (complementary offset binary code for minus full scale) and adjust the offset potentiometer for the proper minus full scale output voltage (see Table 1). Once the appropriate minus full scale adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output shown below is obtained.

RANGE	IDEAL OUTPUT		
		DAC1137/ 1138	DAC1136
Unipolar:	All 11...1	All 00...0	
0V→+10V	0.00000V	+9.999962V	+9.999848V
0V→+5V	0.00000V	+4.999981V	+4.999924V
Bipolar:			
-10V→+10V	-10.00000V	+9.999934V	+9.999695V
-5V → +5V	-5.00000V	+4.999962V	+9.999848V
To adjust:	Adjust ZERO pot	Adjust GAIN pot	

Table 1. Full Scale Output

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1137/1138 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all previously described precautions have been taken to insure proper application at the 16- or 18-bit level. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting, if necessary, for a one LSB positive difference. The top 4 major carries, i.e., MSB minus the sum of bits 2-through-the-LSB, down through bit 4 minus the sum of bits 5-through-the-LSB, can be trimmed using the procedure outlined below. A differential voltmeter capable of 100μV Full Scale should be connected to V_{OUT} of the DAC. This will resolve an LSB which at 18 bits is 38μV (10V range). A Fluke 895A or equivalent is recommended.

1. Bit 4 Trim
   a. Set bit inputs to 11110 . . . . 0.
   b. Read the output voltage by nulling the voltmeter.
   c. Set bit inputs to 11101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required (see B4, Figure 7).

2. Bit 3 Trim
   a. Set bit inputs to 1110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set inputs to 1101 . . . . 1.
   d. Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required (see B3, Figure 7).

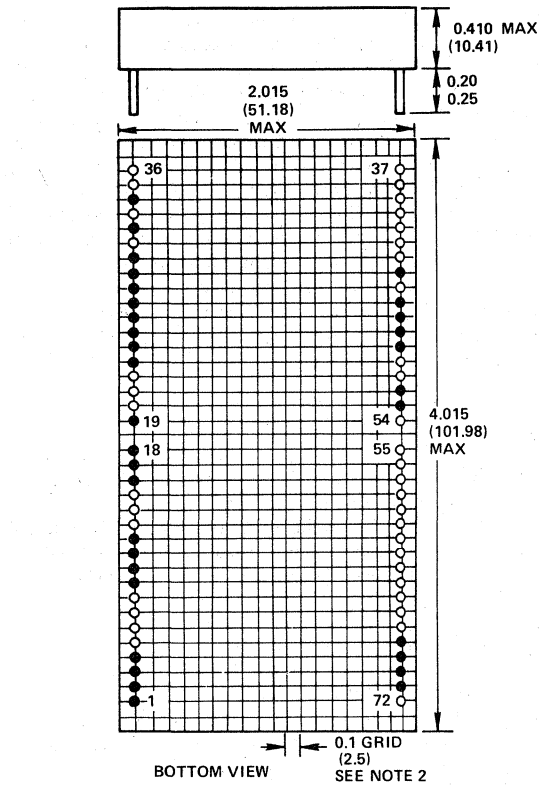
3. Bit 2 Trim
   a. Set bit inputs to 110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit inputs to 101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required (see B2, Figure 7).

4. Bit 1 (MSB) Trim
   a. Set bit switches to 100 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit switches to 011 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required (see MSB, Figure 7).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5-through-the-LSB (see Sum B5 → LSB, Figure 6) should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the sum of bits 5-through-the-LSB is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the DAC. The final step should be adjustment of gain (user supplied adjustment external to module, or pot at edge of mounting card).

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTES:
1. PINS: 0.019 ±0.001 DIA.
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
3. PINS 27 AND 29 ARE NOT PRESENT ON DAC1136.

USING AN EXTERNAL 6V REFERENCE

The DAC1136/1137/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be 1.125mA in bipolar mode or 0.125mA in unipolar mode (pin 46 should be left open and not grounded when using an external reference in the unipolar mode). When an external reference is used, pin 52, (the output of the internal reference) is left open.

Codi Semiconductor manufactures a reference module called Certavolt[1] with a 10 volt output accurate to 0.001%. This output is temperature compensated to within 1ppm/°C from +15°C to +55°C. The Certavolt requires a power supply of +28V dc @ 20mA. To convert the +10 volt output of the Certavolt to the +6 volt reguired by the DAC, the circuit shown in Figure 5 is recommended.

[1] Certavolt is a registered trade name by Codi Semiconductor.

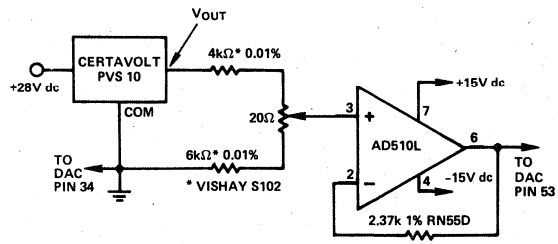


Figure 5. DAC1136/1137/1138 with External Precision Reference

OPTIONAL CARD-MOUNTED ASSEMBLY

Analog Devices offers an optional Card-Mounted Assembly designed to provide optimum performance at the 18-bit level. As shown in Figure 6, this 4 1/2″ X 6″ printed circuit card includes the appropriate DAC, GAIN and OFFSET adjustment potentiometers, and power supply bypass capacitors. The Card-Mounted Assembly can be ordered with input registers and code-setting logic, external output amplifiers, and a Deglitcher.

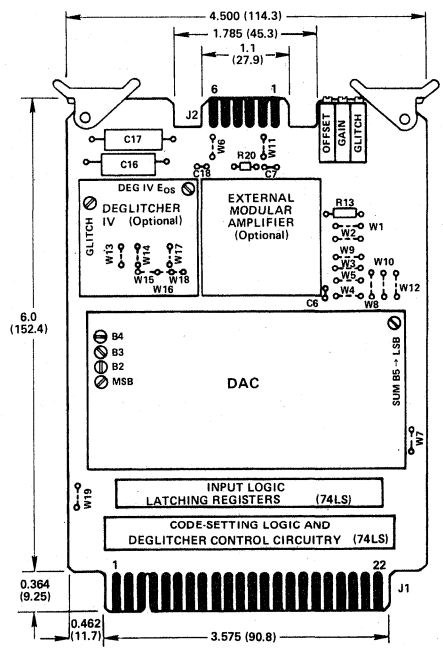


Figure 6. Card-Mounted Assembly

CARD-MOUNTED ASSEMBLY JUMPER DESIGNATIONS

The output voltage range, reference source, amplifier and deglitcher configurations are programmed at the factory by means of jumpers, resistors, and capacitors (see ordering guide for details). The mounting card can be programmed by the user, if necessary, as shown below.

Output Voltage Range	Install Jumpers
±10V	W10, W5
±5V	W12, W5
+10V	W12, W3

Reference	Install Jumpers
Internal	W2
External	W1

Amplifier	Install Jumpers
Internal	W4, W9
External[1]	W8, W13
Deglitcher IV[2]	W8, W15, W17, W18
Deg. IV with Ext Amp[3]	W8, W14, W16

NOTES:

[1] With a 234L amplifier install C7 (0.01μF, 10%, ceramic capacitor). With a 44K amplifier use a variable resistor (typ value ≈ 499Ω, 0.1W, 1%) to adjust the output voltage for a ±100μV reading as measured between pins 69 and 34 of the DAC (this step sets voltage compliance); install this value resistor (R13 position).

[2] With Deglitcher IV remove R20 (100Ω) and replace the resistor with a jumper.

[3] With Deglitcher IV and a 234L amplifier remove C6 (6.8pF Capacitor) and install: C7 (0.01μF, 10%, ceramic capacitor), C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (100Ω) with a jumper. With Deglitcher IV and a 44K amplifier perform the operation described in Note 1, remove C6 (6.8pF capacitor) and install: C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10% polystyrene capacitor) and replace R20 (100Ω) with a jumper.

CONNECTOR J1

PIN	FUNCTION	PIN	FUNCTION
A	BIT 1	U	STROBE
B	BIT 2	V	BIT 18[1]
C	BIT 3	W	+5V
D	BIT 4	X	+15V
E	BIT 5	Y	-15V
F	BIT 6	Z	DIGITAL GND
H	BIT 7	1-4	NC
J	BIT 8	5	INTERLOCK
K	BIT 9	6	INTERLOCK
L	BIT 10	7-16	NC
M	BIT 11	17	BIT 17[1]
N	BIT 12	18	
P	BIT 13	19	
R	BIT 14	20	
S	BIT 15	21	
T	BIT 16	22	

J1 MATES WITH CINCH P.N. 251-22-30-160 (SUPPLIED).

[1] DAC 1137/1138 ONLY

CONNECTOR J2

PIN	FUNCTION
1	ANALOG SENSE LOW
2	ANALOG SOURCE LOW
3	NC
4	ANALOG SOURCE HIGH
5	ANALOG SENSE HIGH
6	ANALOG REF. IN/OUT
A	ANALOG REF. IN/OUT
B	ANALOG SENSE HIGH
C	ANALOG SOURCE HIGH
D	NC
E	ANALOG SOURCE LOW
F	ANALOG SENSE LOW

J2 MATES WITH CINCH P.N. 251-06-30-160 (SUPPLIED).

Mounting Card Connector Designations

DEGLITCHER IV

The Deglitcher IV is a precision high-speed, high-isolation sample-and-hold circuit which eliminates the glitches that occur whenever a DAC is dithered through a major carry. Such momentary transients can be of concern in applications such as high-resolution CRT beam positioning, where glitch-free code transitions are often required for optimum display quality and legibility. Oscilloscope photographs in Figures 7a and 7b below show the output of a DAC1136 being dithered up and down through the major carry, between codes 1000000000000000 and 0111111111111111. In Figure 7b, the Deglitcher IV is turned on virtually elminating the glitches and allowing the 152μV LSB step to be clearly seen.

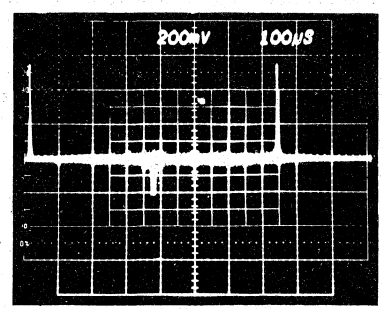


Figure 7a. DAC1136; Major-Carry Dither without Deglitcher IV (BW = 1MHz), Vertical Scale 0.2V/Division

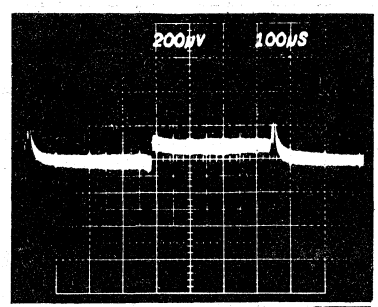


Figure 7b. Same Major-Carry Dither with Deglitcher IV (BW = 1MHz), Vertical Scale, 200μV/Division

The Deglitcher IV utilizes a proprietary sampling technique which isolates the output amplifier during the critical 10μs period immediately following a code change. The only discernible difference in DAC performance when used with Deglitcher IV is a delay of approximately 13μs after the strobe goes HI before the (deglitched) DAC output voltages starts slewing toward the new value.

GLITCH ADJUSTMENT

There are two "Glitch" adjustment potentiometers, accessible on the Card-Mounted Assembly. The adjustment on the card permits nulling of any Track-to-Hold offset, whereas the adjustment internal to the Deglitcher IV allows for precise nulling of the Hold-to-Track transient. Because of the near-infinite attenuation of the actual DAC current glitches, no current-glitch transient is visible on the output. For this reason, it is easiest to null the 2 Deglitcher adjustments while stroking the Card with a static digital input.

INPUT OPTIONS

The Card-Mounted Assembly contains input registers. The input code ordered by the user is set at the factory by means of various jumpers in the logic circuitry. See ordering guide for details.

Since the Card-Mounted Assembly contains input registers, the card requires a strobe pulse circuit. Strobe characteristics of input registers are:

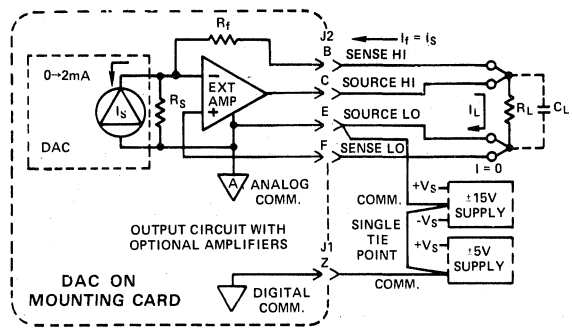
1. ⌐└ Strobe Pulse: One Std. series 74LS load, Leading-Edge-Triggered. Positive pulse should remain HI for > 100ns.
2. The digital input code can be changed at any time up to and including that instant when the strobe command goes HI.
3. The actual transfer of the input code to the DAC will occur ≈ 3μs after the strobe command; during this 3μs the digital input code to the card assembly should not be changed, in order to prevent the possible coupling of logic noise into the DAC output. At to +3μs, the deglitcher is automatically enabled for the following ≈ 8μs. Thus there will be a delay of ≈ 11μs before the deglitched output starts slewing to the new valve. Actual data transfer to the DAC automatically occurs at t_o +3.1μs.

OUTPUT OPTIONS

The Card-Mounted Assembly for the DAC1136/1137/1138 allows for several user-selectable output configurations:

1. Internal Output Amplifier inside the DAC Module.
2. Analog Devices model 234L; for low noise, low drift applications (2μV, ±0.1μV/°C).
3. Analog Devices model 44K; available only with DAC1136 or DAC1137; recommended only for high speed or high current applications.
4. Deglitcher IV with self-contained precision BI-FET output amplifier (AD542K).
5. Deglitcher IV with model 234L output amplifier.
6. Deglitcher IV with model 44K output amplifier. (Available with DAC1136 or DAC1137 only.)

When using an external amplifier, a four terminal output connection can be utilized on the Card-Mounted Assembly in order to allow for compensation of connector contact resistance.



NOTE:
1. VOLTAGE DROP BETWEEN SOURCE LO AND SENSE LO MUST OBSERVE CURRENT MODE COMPLIANCE LIMITS FOR RATED ACCURACY.
2. THIS CONNECTION SCHEME CANNOT BE USED WITH INTERNAL AMPLIFIER OF THE DAC OR WITH THE AMPLIFIER INTERNAL TO THE DEGLITCHER IV.

Figure 8. Four-Terminal Output Connections

ORDERING GUIDE

WHEN ORDERING THE DAC1136/1137/1138, ORDER EITHER:

DAC1136J	DAC1137	DAC1138J
DAC1136K		DAC1138K
DAC1136L		

When ordering the DAC1136/1137/1138 as a Card-Mounted Assembly, the part must be described with 6 suffixes as shown below.

DAC 113 ☐ ☐ ☐ ☐ ☐ ☐

CODE	CODE	DAC MODULE RESOLUTION	LINEARITY
6	J	16 BITS	15 BITS
6	K	16 BITS	16 BITS
6	L	16 BITS	16 BITS
7	–	18 BITS	16 BITS
8	J	18 BITS	17 BITS
8	K	18 BITS	18 BITS

CODE	OUTPUT AMPLIFIER
1	INTERNAL
2	44K[1]
3	234L
4	DEGLITCHER IV
5	DEGLITCHER IV[1] AND 44K
6	DEGLITCHER IV AND 234L

CODE	INPUT LOGIC CODE
1	BIN/OBIN
2	COMP BIN/COMP OBIN
3	2'S COMP
4	COMP 2'S COMP
5	SIGN PLUS MAG BIN
6	COMP SIGN MAG BIN

CODE	OUTPUT VOLTAGE RANGE
1	+10V
2	±5V
3	±10V

CODE	DAC VOLTAGE REFERENCE
1	INTERNAL
2	EXTERNAL

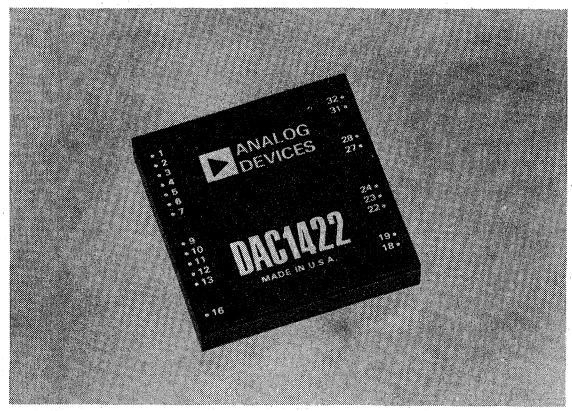
NOTE:
1. ORDER WITH DAC1136J & K ONLY.

4-20mA, 8- and 10-Bit Digital-to-Analog Converters

DAC1420, DAC1422

FEATURES
- ISA S50.1 Type 3 Class U Output
- Guaranteed Monotonic 0 to +70°C
- Totally Powered From Loop Supply
- Wide Supply Range +10V to +36V
- Self-Contained Data Latch
- Auxiliary Analog Input
- No Minimum Load Requirement

APPLICATIONS
- Direct Digital Controllers
- Computer Based Process Control Systems
- Digital Pressure Transducers



GENERAL DESCRIPTION
The DAC1420/1422 are low power 8- and 10-bit digital-to-analog converters with 4-20mA current outputs designed specifically for the process and industrial control industry. Each DAC1420/1422 comes complete with CMOS input latching register, CMOS digital-to-analog converter, a voltage-to-loop current converter, a reference and regulator circuit that enables single-supply operation. An additional voltage-to-loop current converter is included to provide transfer to an analog back-up mode in the event of computer power failure. The DAC1420/1422 operate on a single supply voltage in the range of +10V to +36V allowing the units to be entirely powered from the loop power supply or battery back-up, eliminating the need for bipolar or logic supplies.

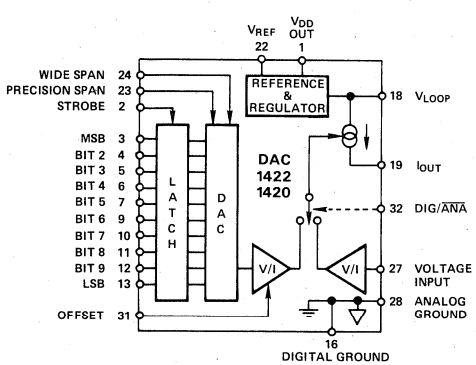


Figure 1. Block Diagram

DIGITAL INPUT	NOMINAL CURRENT OUTPUT
Binary Code	
1 1 1 1 1 1 1 1 1 1	+19.984mA
0 0 0 0 0 0 0 0 0 1	+ 4.016mA
0 0 0 0 0 0 0 0 0 0	+ 4.000mA

Table 1. Nominal Input-Output Relationships

FEATURES AND USER BENEFITS
The DAC1420/1422 incorporate several features to simplify their use in process control applications. Monotonicity is guaranteed from 0 to +70°C. The three terminal output structures conform to the Instrument Society of America Standard ISA-S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments". In addition to having all of their power supplied from the loop, the DAC1420/1422 provide +5V of V_{DD} output. Should computer power fail, the DACs can retain the last data word strobed into their latching registers. An additional safeguard has been provided that will allow the user to automatically switch-in a local analog voltage in the event of computer power failure. Since requirements for loop currents may vary, both offset and span are adjustable ±10%.

SPECIFICATIONS

(typical @ +25°C, V_{LOOP} = +24 volts unless otherwise specified)

MODEL	DAC1420	DAC1422
DIGITAL INPUTS		
Resolution	8 Bits	10 Bits
Levels		
(Except "$\overline{\text{ANA}}$/DIG")	CMOS V_{DD} =5V	*
	"1" = >3.3V @ 1μA	*
	"0" = <1.7V @ 1μA	*
$\overline{\text{ANA}}$/DIG Input		
Impedance	12kΩ	*
"1"	"1" = >2.4V @ 140μA	*
"0"	"0" = <0.7V @ 0μA	*
Latch Strobe	Rising Edge Sensitive	*
T_{DH} (Data Hold)	0ns (min)	*
T_{DS} (Data Set-Up)	50ns (min)	*
ANALOG OUTPUT		
Type	ISA S50.1 Type 3 Meets and Exceeds Class U	*
Nominal Range	4-20mA	*
Compliance	V_{LOOP} -6V	*
Output Impedance	>4MΩ @ dc	*
Minimum Load	0Ω	*
STABILITY AND ACCURACY		
Monotonicity (1)	Guaranteed, 0 to +70°C	*
Integral Nonlinearity	±1/2LSB	*
Differential Nonlinearity	±1/2LSB	*
Temperature Stability		
Offset	25ppm FSR/°C	*
Span	50ppm FSR/°C	*
Adjustability	±10% each, Offset and Span	*
Initial Error, Untrimmed[1]	±2LSB's each, Offset and Span	*
Power Supply Rejection	20ppm FSR/V	*
Noise, 10Hz to 100Hz[2]	4mV p-p	*
ANALOG BACKUP INPUT		
Range[3]	1 - 5V	*
Gain	4mA/Volt (1-5V produces 4-20mA)	*
Accuracy	±3%	*
Stability	±100ppm FSR/°C	*
Input Impedance	10^8 Ω	*
POWER		
Loop Supply, minimum	+10V	*
maximum	+36V	*
Supply Current	I_{OUT} +30mA	*
ENVIRONMENTAL		
Operating Temperature	0 to +70°C	*
Storage Temperature	-25°C to +85°C	*
SIZE	2" X 2" X 0.4"	*

NOTES

[1] Both offset and span error are adjustable to zero. See Figures 3 and 4 for details.

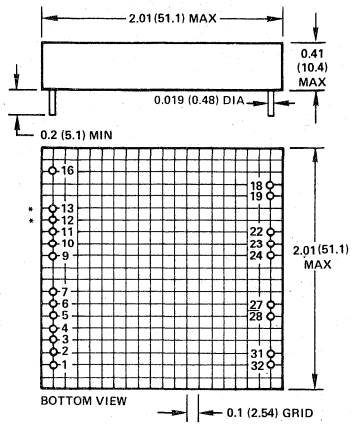
[2] Load = 750Ω|| 1,000pF

[3] This input should not exceed +5.5V and should be grounded if not used.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1577
(2 Required)

NOTE:
Module Weight: 1.6 ounces (45 g)

*Pins 12 & 13 appear on DAC1422 only.

POWER/OUTPUT CONNECTIONS (Figure 2)
The DAC1420/1422 outputs are current sources designed to drive a grounded load. The maximum value of R_L is dependent upon the loop supply and full scale output current according to the formula:

$$R_L\ (max) = \frac{V_{LOOP} - 6V}{I_{OUT}\ (FSR)}$$

For example, at 20mA, V_{LOOP} = 24 Volts, the maximum R_L is 900Ω. There is no minimum R_L required; the DAC1420/1422 maintain rated performance into a short circuit load.

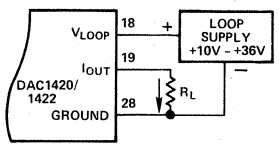


Figure 2. Output/Power Connections

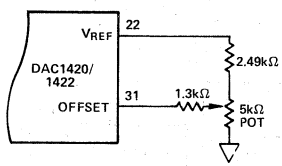


Figure 3. Offset Adjustment Circuit

OFFSET ADJUSTMENT (Figure 3)
The DAC1420/1422 are factory trimmed for offset to within ±0.2% FSR (2LSB's). For this performance, leave the offset pin (pin 31) unconnected. If potentiometer trimming is required, the circuit in Figure 3 will provide approximately ±10% offset adjustment. For greater adjustment resolution, increase the resistor in series with pin 31.

SPAN ADJUSTMENT (Figures 4a & 4b)
If no span adjustment is desired, connect pin 22 (V_{REF}) to pin 23 (Precision Span) for factory trimmed span accuracy of ±0.2% (2LSB's). If span adjust is required, the circuit in Figure 4b will allow ±10% minimum span adjustability. To increase the resolution of the adjustable span, use a resistor in series with the pot and reduce the value of the pot accordingly.

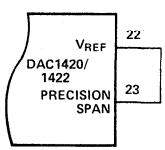


Figure 4a. Factory Trimmed

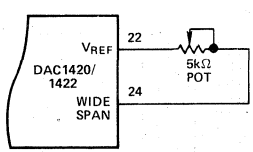


Figure 4b. Span Adjust

STROBE INPUT (Figure 5)
The input latches in the DAC1420/1422 are CMOS rising edge sensitive devices. The last loaded digital word remains latched during backup manual operation providing the strobe input does not change. The user is cautioned that the digital inputs remain active even when the control is switched to analog.

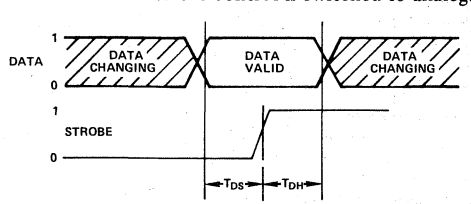


Figure 5. Input Timing

V_{DD} OUTPUT
The V_{DD} output may be utilized as a power supply for external CMOS circuitry such as tri state or buss transceivers, up to a limit of 1mA I_{DD}. If used in this fashion, it is recommended that the user add a 0.1μF bypass capacitor to ground from this pin to keep externally injected "glitches" from disturbing the internal circuitry of the DAC1420/1422.

ANALOG BACKUP INPUT (Figure 6)
An Analog Backup Input is provided for use in controlling the output in case the source of digital inputs fail. This is a high impedance voltage input scaled so that 1-5 volts input gives 4-20mA output and is unaffected by the offset and gain adjustments. To prevent induced errors, this input should not exceed +5.5 volts and should be grounded if not used. Switchover to the analog input is provided by pin 32, the Digital/$\overline{\text{Analog}}$ control input. When at Logic "1" the 4-20mA output is controlled by the digital input. When at Logic "0", the 4-20mA output is controlled by the analog input. Figure 6 shows one possible use of the analog input: to provide for potentiometer-variable control in the event of computer failure. The V_{DD} OUT (pin 1) is used as a 5 volt reference for the potentiometer. If this feature is not used, connect pin 32 to pin 1 and pin 27 to ground.

Figure 7 shows an alternative back-up mode using increment/decrement digital control.

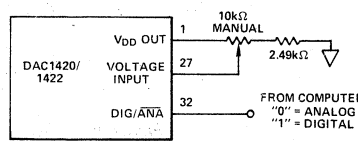


Figure 6. Potentiometer Backup Control

NOISE AND BANDWIDTH CHARACTERISTICS
The DAC1420/1422 are used in control systems of modest bandwidth and speed. The noise specification given in the Electrical Characteristics is the typical noise that would be seen under that condition of load and bandwidth. The noise seen at the output of the DAC depends upon the capacitive and resistive load and the bandwidth of the instrument doing the measurement. The majority of the output noise is generated at approximately 65kHz by an internal charge pump inverter which supplies power to the internal DAC. Since the noise fundamental is at a much higher frequency than the systems where the DAC1420/1422 are likely to be used, the output noise should be observed over a limited bandwidth. Therefore, Analog Devices recommends the use of an external capacitance typically in the range of 1000pF to 1μF. This capacitance includes the distributed capacitance of any cable connected to the output of the DACs as well as any value of discrete capacitance that may be used. The capacitive load also has an effect on the time constant of the DAC output. Capacitive load and load resistance form an RC time constant. For example, it takes approximately 7 time constants for the output to step from 4mA and be within 0.2% of full scale, 20mA.

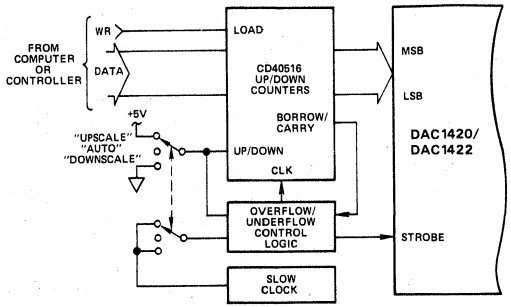


Figure 7. Block Diagram – Manual Incremental Control Scheme Using Up/Down Counters

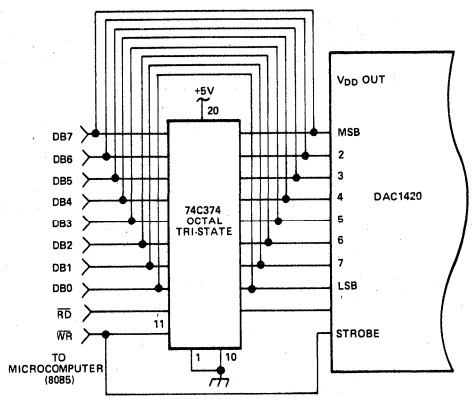


Figure 8. DAC1420 with μP Interface and Readback Capability

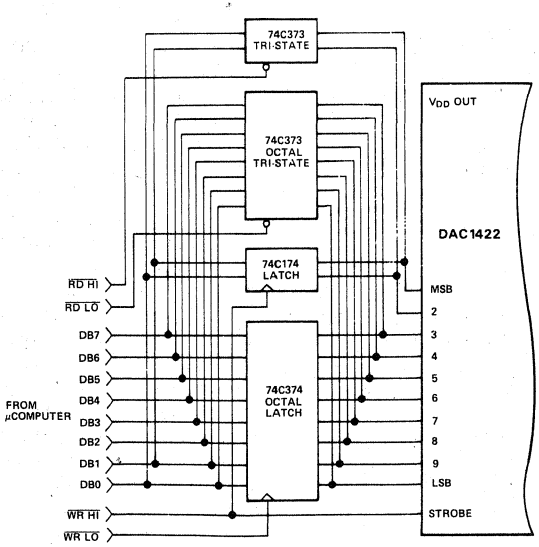


Figure 9. DAC1422 with μP Interface and Readback Capability

4-20mA, 10-Bit, Isolated Digital-to-Analog Converter

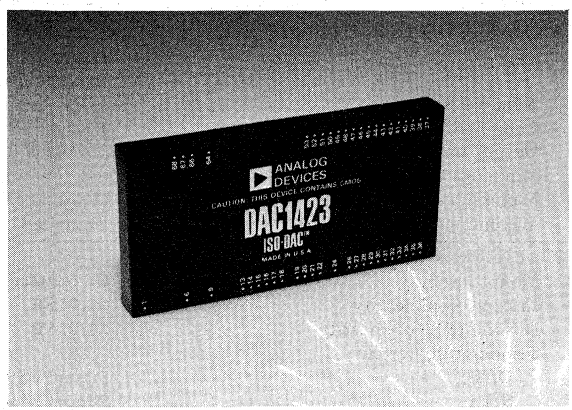
DAC1423

FEATURES

- 3-Port Galvanic Isolation
- Guaranteed Monotonic 0 to +70°C
- Microprocessor Compatible Interface
- Increment/Decrement Backup Control
- May be Powered from Loop Supply
- Low Power: 450mW typ
- Output Will Drive 0Ω Loads
- Bumpless Transfer, Auto to Manual

APPLICATIONS

- Direct Digital Controllers
- Ground Loop Elimination in Industrial and Process Control
- High Voltage Protected Data Acquisition Systems
- Digital Pressure Transducers
- Driving Analog Recorders



GENERAL DESCRIPTION

Analog Devices' ISO-DAC™ (ISOlated Digital-to-Analog Converter) model DAC1423 is a low power 10-bit DAC with 4-20mA current output, designed specifically for the process and industrial control industry. Its advanced features and excellent performance make for easy application within new and existing control systems. The DAC1423 contains a CMOS holding register, allowing direct interface with microprocessors, CMOS digital-to-analog converter, voltage-to-voltage isolator and a voltage-to-loop current converter. The small size and low profile (2" X 4" X 0.4") allows much greater functional density than previously available solutions.

DESIGN FEATURES AND USER BENEFITS

Microcomputer Interface: The parallel digital interface is a 5V CMOS design with independently controllable input latches and Tri-State* buffers, split into upper and lower sections (an 8-bit and a 2-bit byte) so that 8- or 16-bit bus compatibility may be achieved.

True 3-Port Isolation: The output connections and power connections are galvanically isolated, both from each other and from the digital section. Each will accommodate a wide range of power supply voltages and may be operated from the same supply, if desired.

Increment/Decrement: Increment/decrement control is achieved via the input latch/counter. An internal slow speed clock is supplied for this operation. Overflow/underflow lockout circuitry is used to prevent full scale "bumps" from occurring.

*Tri-State is a trademark of National Semiconductor Corporation.

Adjustable Offset and Span: The ISO-DAC has offset and span accuracies of ±2LSB's (±0.2% FSR) each. However, if the user desires adjustable offset and span, there are provisions for ±10% adjustment range for each.

High CMV Isolation: The isolation barriers will withstand 1.5kV dc continuously, or 1kV rms @ 60Hz for 60 seconds. The ISO-DAC is designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). Common Mode Rejection is excellent; typically, 103dB @ 60Hz for a 250Ω load.

Synchronized: The ISO-DAC may be synchronized to an external system clock, multiple DAC1423's may be on synchronized to one another. In the event of loss of external sync, the DAC1423 will "free run" on its own oscillator.

Isolated Power Out: An internally derived +5V supply is brought out so that the user may power a small amount of application circuitry from the DAC1423's power supply.

ISA-S50.1: The three terminal output structure conforms to the Instrument Society of America Standard ISA-S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments."

SPECIFICATIONS (typical @ +25°C, V_{LOOP} = +24 volts unless otherwise specified)

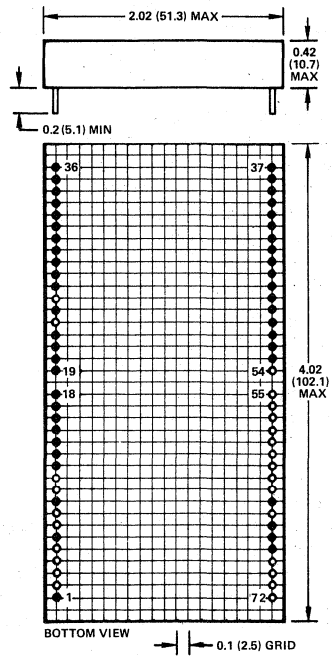
MODEL	DAC1423
DIGITAL INPUTS	
Resolution	10 Bits
Levels, CMOS V_{DD} = 5V	"1" = >3.3V @ 1μA "0" = <1.7V @ 1μA
Strobe	Level Sensitive (See Table 2)
ANALOG OUTPUTS	
Type	ISA S50.1 Type 3 Meets or Exceeds Class U
Nominal Range	4-20mA
Compliance	V_{LOOP} -6V
Output Impedance	>4MΩ @ dc
Minimum Load	0Ω
Maximum Load	(V_{LOOP} -6V/I_{OUT})
Maximum Capacitive Load	Unlimited
STABILITY AND ACCURACY	
Monotonicity	Guaranteed, 0 to +70°C
Integral Nonlinearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Temperature Stability	
Offset	50ppm FSR/°C
Span	50ppm FSR/°C
Adjustability	±10% each, Offset and Span
Initial Error, Untrimmed[1]	±2LSB's each, Offset and Span
Power Supply Rejection	20ppm FSR/V
Noise, 10Hz to 100Hz[2]	0.1LSB
Warm Up Time to Rated Accuracy	5 minutes
Warm Up Drift	0.5LSB
ISOLATION	
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 minute	1000V rms
dc, Continuous	1500V dc
CMR, Inputs to Outputs, 60Hz, R_L = 250Ω	103dB
POWER	
Loop Supply Range	12–36V dc
Loop Supply Current	I_{OUT} + 5mA
Power Supply Range[3]	14–36V dc
Power Supply Current[3]	20mA
ENVIRONMENTAL	
Operating Temperature	0 to +70°C
Storage Temperature	-25°C to +85°C

NOTES:
[1] Both offset and span error are adjustable to zero. See Figure 2 for details.
[2] Load = 750Ω|| 1,000pF and slow clock disabled.
[3] The DAC1423 can be entirely powered from the loop supply. See Figures 4 and 5 for details.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.
MODULE WEIGHT: 60.8G

MATING SOCKET
AC1582
(See Figure 13)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	I_{OUT}	72	NC
2	NC	71	NC
3	NC	70	NC
4	NC	69	NC
5	NC	68	SYNC IN
6	+V_{LOOP}	67	+V POWER
7	NC	66	SYNC OUT
8	NC	65	NC
9	COMMON	64	PWR COMMON
10	NC	63	NC
11	NC	62	NC
12	NC	61	NC
13	WIDE SPAN	60	NC
14	PRECISION SPAN	59	NC
15	+V_{REF}	58	NC
16	WIDE OFFSET	57	NC
17	PRECISION OFFSET	56	NC
18	SPAN COMMON	55	NC
19	DIGITAL COMMON[1]	54	NC
20	+5V_{OUT}	53	DIGITAL COMMON[1]
21	READ HIGH	52	CLOCK IN
22	READ LOW	51	LSB OUT
23	NC	50	BIT 9 OUT
24	LSB IN	49	BIT 8 OUT
25	NC	48	BIT 7 OUT
26	BIT 9 IN	47	BIT 6 OUT
27	BIT 8 IN	46	BIT 5 OUT
28	UP/$\overline{DN}$	45	READ HIGH
29	BIT 7 IN	44	READ LOW
30	BIT 6 IN	43	BIT 4 OUT
31	BIT 5 IN	42	BIT 3 OUT
32	BIT 4 IN	41	BIT 2 OUT
33	BIT 3 IN	40	MSB OUT
34	BIT 2 IN	39	CLOCK OUT
35	MSB IN	38	C_T
36	CLEAR	37	DIGITAL COMMON[1]

[1] PINS 19, 37 and 53 ARE INTERNALLY CONNECTED.

THEORY OF OPERATION

The ISO-DAC produces an isolated 4 to 20mA output current which is proportional to the input digital word. Each ISO-DAC contains a µcomputer compatible input section consisting of a 10-bit input latch, a 10-bit tri-state output and the associated control lines for read and write operations. A 10-bit CMOS digital-to-analog converter converts the digital word to a voltage that is modulated, carried across the isolation barrier, demodulated, and converted to a 4 to 20mA current output.

The remarkable performance of the ISO-DAC is derived from the carrier isolation technique which is used to transfer both signal and power between the input circuitry and the output stage. High CMV isolation, with excellent linearity, is achieved by the transformer coupling between the internal DAC, modulator section and the current output circuitry.

The power oscillator supplies isolated power to the front-end logic and internal DAC via Transformer T2 and also supplies excitation to the Mod and Demod circuits via Transformer T1. The internal reference and regulator circuit provides the necessary internal voltages to allow single power supply operation.

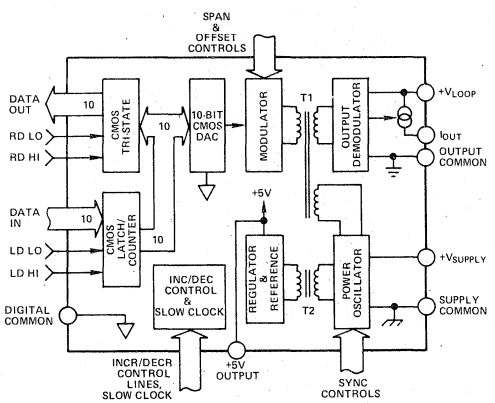


Figure 1. Block Diagram of DAC1423, Isolated 4-20mA DAC

OFFSET AND SPAN ADJUSTMENTS

The DAC1423's initial offset and span accuracies are typically ±2LSB's (±0.2% FSR) each. If offset and span adjustments are not necessary, use the connections shown in Figure 2a.

Both offset and span errors are adjustable to zero with two external potentiometers, as shown in Figure 2b. To adjust the offset, apply a digital input of 0000000000 and adjust the offset potentiometer until an output of 4mA is obtained. Once the appropriate offset adjustment has been made, apply a digital input of 1111111111 and adjust the span potentiometer until 19.984mA is obtained. The offset and span adjustments are slightly interactive.

The offset and span potentiometers can provide a wide adjustment range to satisfy the particular needs of the application.

DIGITAL INPUT	NOMINAL CURRENT OUTPUT
Binary Code	
1111111111	+19.984mA
0000000001	+ 4.016mA
0000000000	+ 4.000mA

Table 1. Nominal Input-Output Relationships

The adjustment range of the span control will be typically ±10% full scale range (±2mA), while that of the offset control will be ±10% of offset (±0.4mA). Owing to the impedances involved, it is suggested that the adjustment pots be located near their respective connections or be well-guarded in order to avoid noise pickup.

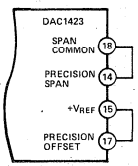


Figure 2a.

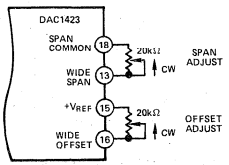


Figure 2b.

Figure 2. Precision and Adjustable Offset and Span

APPLICATION HINTS

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

ISOLATION CHARACTERISTICS

The DAC1423 employs a "three port" isolation architecture which allows for a great deal of flexibility in its application (see Figure 3). The power connections (pins 64, 66–68) are galvanically isolated from any other part of the module and may be subjected to the full common mode range with respect to either digital common or output common. Similarly, the output connections (pins 6, 8, 9) are isolated in the same manner from either power common or digital common.

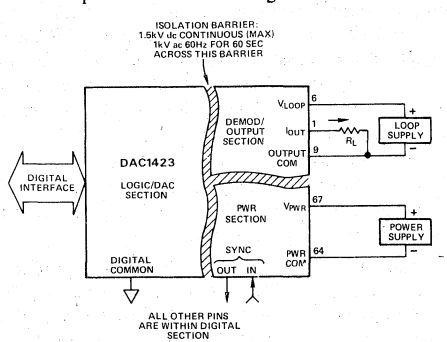


Figure 3. Illustration of Isolation Barrier Within the DAC1423

Figures 4 and 5 show two methods of utilizing the isolation characteristics of the DAC1423. In Figure 4, the DAC1423 is shown with separate loop supply and power supply. This configuration is useful when it is desirable to derive power for the module from the system without losing output isolation. This configuration is also useful when using external synchronization or multiple units, since the sync controls are referenced to power common. Figure 5 shows the use of a single supply for both power and loop current. This technique is useful when

the loop supply is the most secure power source, since the DAC1423 will remain operable even though the system has failed, as long as the loop supply continues to operate.

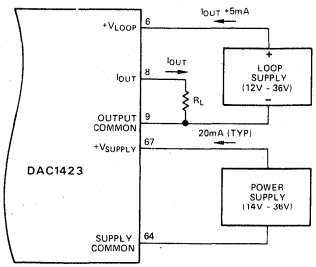


Figure 4. Operation with Isolated Loop and Power Supplies DAC1423

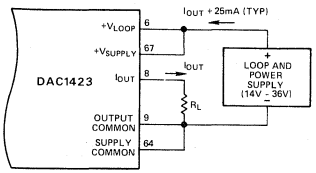


Figure 5. Operation with Common Supply DAC1423

SYNCHRONIZATION

The DAC1423 contains an internal oscillator which generates the carrier frequency for the modulation process. In most cases, there is no appreciable leakage from this oscillator, and it may be ignored by the user. However, when a DAC1423 is used in a system which contains a clock at or near this carrier frequency, or when several DAC1423's are used adjacent to one another, it is possible that a heterodyning phenomenon can occur which results in beat notes that may (or may not) fall within the system's passband. For this reason, the DAC1423 contains provisions for external or multiple synchronization. Pin 68 is the SYNC IN pin which can be driven from an external clock. The external clock should be within 15% of free running frequency of the DAC1423 (200kHz ±15%). It should be a 5V CMOS level (50% duty cycle) via a 2200pF capacitor in series with pin 68.

If external sync is not used, leave the SYNC IN pin unconnected; the DAC1423 will free run at approximately 200kHz. Note that the SYNC IN signal is referred to power common, not loop common or digital common.

When multiple DAC1423's are used, it is recommended that their sync provisions be "daisy chained" as shown in Figure 6. The SYNC OUT pin of one DAC1423 is used as the external sync drive for the next DAC1423. Note that the first DAC1423 in the chain may either "free run" or be synchronized from an external source.

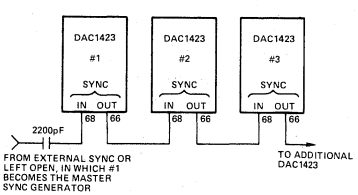


Figure 6. Synchronizing Multiple DAC1423's

The performance of the DAC1423 running in the sync mode is essentially no different from the free running mode, except that there may be slight offset and span shifts (≈1LSB) if the carrier frequency is pulled appreciably from its free running frequency. In no case should the carrier frequency be pulled more than ±15% from its nominal free running frequency.

DIGITAL INTERFACE (PARALLEL)

The parallel interface of the DAC1423 is a 5V CMOS design, arranged to offer a great deal of interfacing flexibility to a variety of user systems.

The interface consists of a 10-bit input latch, a 10-bit tri-state output, and the associated control lines for read and write operations. As shown in Figure 7, the 8 lower bits and 2 upper bits of both the latch and the tri-state are separately controlled, allowing interfaces to both 8-bit and 16-bit bus architectures. For 10-bit or greater bus operation, the LO and HIGH write lines may be connected together, as well as the LO and HIGH read lines.

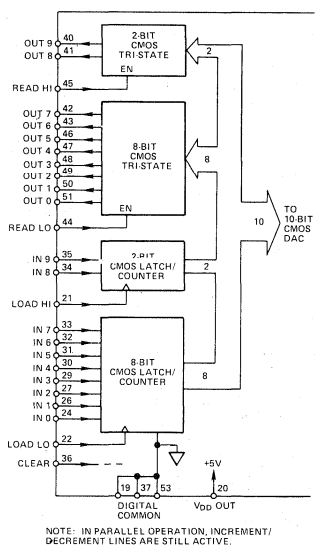


Figure 7. DAC1423 Digital Interface Architecture

An example of an 8-bit microprocessor interface is shown in Figure 8. In this case, the data is arranged as two bytes, right justified. The digital inputs to the DAC1423 are CMOS, therefore, rigid logic levels are required. In some cases, double buffering may be required for bus interface.

The output drive capability of the tri-states is 1 TTL load; in general, the DAC1423 may be used directly on most NMOS or CMOS microcomputer buses if the 3.3V minimum logic "1" level is observed. In some cases, pullups may be required.

In the event of computer failure, the bus inputs must go to either a high or a low state, but read, write and clear lines must go to a low state.

BUMPLESS TRANSFER

In process control applications, there will be times when the computer power fails and critical controls must be operated manually. To avoid causing a "bump" in the process, such as commanding a manually closed valve to fully open when switched to automatic control, it is essential that the computer knows the exact condition of the system when it resumes control. This is known as "bumpless transfer".

Bumpless transfer, when switching between automatic and manual control, is provided by the readback capability of the ISO-DAC's input tri-state logic. It constantly monitors the status of the input register; therefore, when switching from manual to automatic control, the computer can read the status of the ISO-DAC before resuming the algorithm.

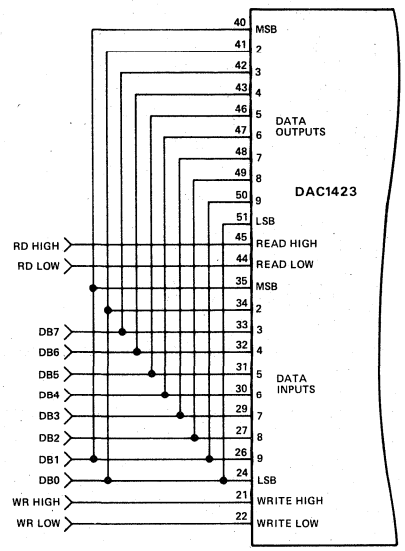


Figure 8. Typical Interface to 8-Bit µComputer

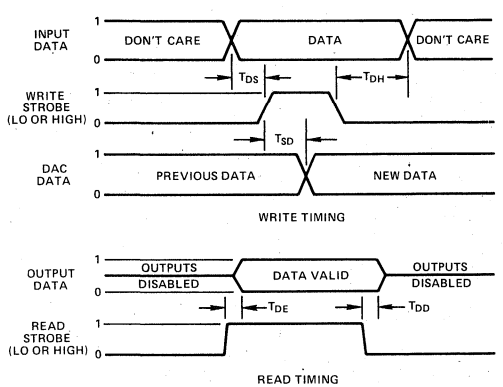
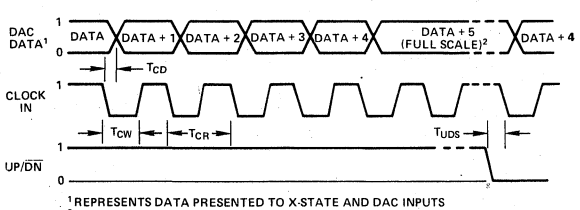


Figure 9. Read/Write Timing



[1]REPRESENTS DATA PRESENTED TO X-STATE AND DAC INPUTS
[2]SAME CHARACTERISTIC OCCURS WHEN DECREMENTED TO ZERO

Figure 10. Increment/Decrement Timing

SYMBOL	MEANING	MIN	TYP	MAX	UNITS
t_{SD}	Strobe to Data Time	–	315	–	ns
t_{DS}	Data Set-Up Time	0	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{WS}	Write Strobe Width	–	100	–	ns
t_{OE}	Output Enable Time	–	100	–	ns
t_{OD}	Output Disable Time	–	80	–	ns
t_{CD}	Clock to Data Time	–	315	–	ns
t_{CW}	Clock Width	–	200	–	ns
t_{UDS}	Up/Down Set-Up Time	–	250	–	ns
t_{CR}	Clock Repetition Period	–	–	330	ns

Table 2. Timing Requirements

INCREMENT/DECREMENT CONTROL

Increment/decrement operation under computer or manual control is possible with the input latch/counter in the DAC1423. The DAC1423 also contains overflow/underflow lockout circuitry, and a slow speed clock output is provided. The timing diagram shown in Figures 9 and 10 give guidelines for increment/decrement operation. Figure 11 shows the ISO-DAC in the manual back-up mode using increment/decrement control logic. In this circuit, part of Z_1 latches the direction line, UP/$\overline{DN}$. Z_2 and the remainder of Z_1 gate the clock "on"–after one RC time delay. The RC time delay is determined by R_T and C_T which the user supplies. The same circuit could be used for computer control by simply replacing the pushbutton switch with the proper logic.

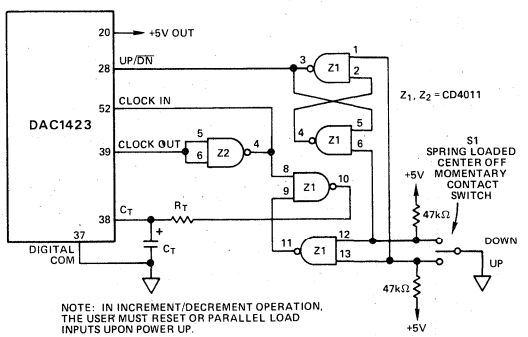


Figure 11. Increment/Decrement Control

SLOW CLOCK OPERATION

The DAC1423 provides a slow speed clock circuit for the user's convenience in operating the increment/decrement feature. This clock requires a resistor and capacitor to set its operating frequency, as shown in Figure 12. When the slow clock is not used, connect pin 38 to digital common (pin 37) and disable the slow clock to prevent any feedthrough of the clock signal to the output.

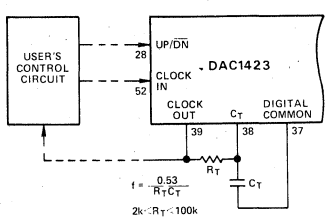


Figure 12. Using the Slow Clock

CLEAR

In many industrial controls, it is desirable to have the ISO-DAC go to a known state when the system is first powered up. The clear pin, pin 36, is provided for just such cases. Strobing the clear pin will reset the input latch/counter to all 0's. Tying pin 36 to the computer reset bus provides an asynchronous means to initiate the system to a known state.

+5V OUTPUT

A +5V output is provided for powering a small amount of user supplied circuitry. This output is referred to digital common and is, therefore, isolated both from the loop and from the power supply. The outboard devices may draw up to a maximum of 0.5mA from this pin (pin 20); however, it is suggested that the user by-pass this pin to digital common with a 0.1μF or greater capacitor in order to avoid externally injected glitches from disturbing the internal circuitry of the DAC1423.

AC1582 MOUNTING CARD

The AC1582 mounting card is available to assist in evaluating the DAC1423. As shown in Figure 13, the AC1582 is an edge connector card with pin receptacles for plugging in the DAC1423. This card includes offset and span adjustment potentiometers, power supply bypass capacitors and the logic needed for increment/decrement control. Increment/decrement control is enabled via connection to J2. In addition, the card allows for several user-selectable configurations:

1. 8- or 16-bit bus interface;
2. Single supply for both power and loop current. Supply delivered via P_1 or TB_1;
3. Separate loop supply and power supply;
4. Offset and Span—fixed or adjustable.

These configurations can be programmed by user-installed jumpers, as shown in the wiring chart of Table 3. Jumper locations are not shown in Figure 13, but are labeled on the mounting card.

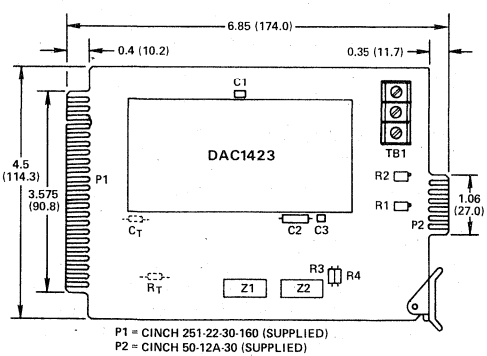


Figure 13. AC1582 Mounting Card. Dimensions shown in inches and (mm).

P1

PIN	FUNCTION	PIN	FUNCTION
1	MSB IN	A	MSB OUT
2	BIT 2 IN	B	BIT 2 OUT
3	BIT 3 IN	C	BIT 3 OUT
4	BIT 4 IN	D	BIT 4 OUT
5	BIT 5 IN	E	BIT 5 OUT
6	BIT 6 IN	F	BIT 6 OUT
7	BIT 7 IN	H	BIT 7 OUT
8	BIT 8 IN	J	BIT 8 OUT
9	BIT 9 IN	K	BIT 9 OUT
10	LSB	L	LSB OUT
11	WRITE HIGH	M	READ HIGH
12	WRITE LOW	N	READ LOW
13	CLEAR	P	DIGITAL COMMON
14	NC	R	+5V_{OUT}
15	NC	S	NC
16	NC	T	NC
17	+V POWER	U	PWR COMMON
18	SYNC IN	V	SYNC OUT
19	NC	W	NC
20	NC	X	NC
21	+V_{LOOP}	Y	LOOP COMMON
22	NC	Z	NC

P2

PIN	FUNCTION
A	DIG COM
B	DECREMENT
C	INCREMENT

TB1

PIN	FUNCTION
1	+V_{LOOP}
2	I_{OUT}
3	LOOP COMMON

Table 3. AC1582 Mounting Card Connector Designations

Options	User-Installed Jumpers[1]
8-Bit Bus Interface	J1, J2, J4, J5
16-Bit Bus Interface	J3, J6
Single Supply	J7, J8, J13, J14
Dual Supply (V_{LOOP} via P1)[2]	J13, J14
Offset and Span, Fixed	J10, J12
Offset and Span, Adjustable	J4, J11

Notes:
[1] Jumper locations are not shown in Figure 13, but are labeled on AC1582.
[2] Loop supply normally accessible via TB1.

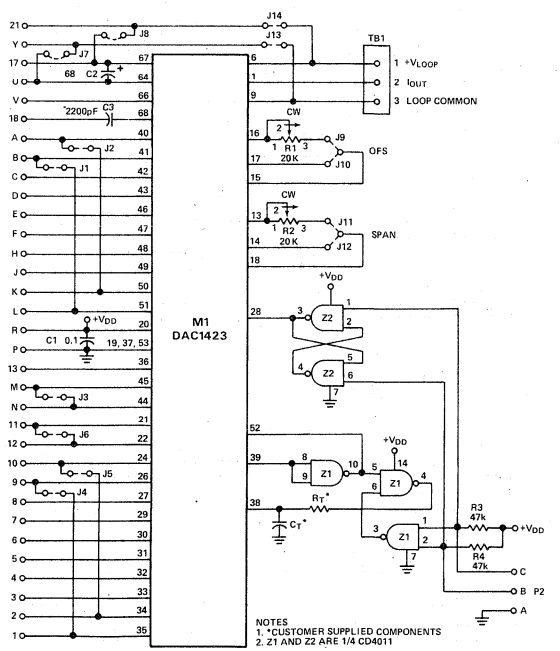


Figure 14. Schematic Diagram for AC1582 Mounting Card

8-, 10-, 12-Bit Video Speed Hybrid Current & Voltage Out D/A Converter

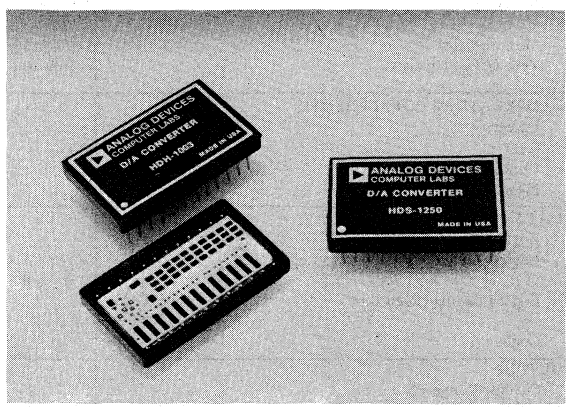
HDS-0820, -1025, -1250/HDH-0802, -1003, -1205

FEATURES

- **25ns Current Settling to 0.1% (HDS)**
- **200ns Voltage Settling to 0.1% (HDH)**
- **10mA Current Out (HDS)**
- **Guaranteed Monotonicity Over Temperature**
- **No External Parts Required**
- **Reliable Hybrid Construction**

APPLICATIONS

- **CRT Vector Displays**
- **TV Video Reconstruction**
- **Military Equipment (MIL-STD-883)**
- **Analytical and Medical Instruments**



GENERAL DESCRIPTION

The HDS/HDH series of digital to analog converters represent the fastest precision settling current and voltage DAC's available. Capable of processing to MIL-STD-883 and guaranteed monotonicity over their operating temperature range; their quiescent power is 1/2 that of competitive units. The current output models provide 10mA full scale allowing direct drive of capacitive loads and transmission lines. All versions have a precision reference and are active laser trimmed to specified accuracy, thus no external adjustment pots or other components are required.

With 6 available units engineering trade-offs can be made between resolution, speed, current or voltage output, and of course price. To facilitate this comparison major specifications are summarized in Table 1.

Model	Resolution	Full Scale Step Settling Time
Current Output		10mA Step
HDS-0820	8 Bits	20ns to 0.4%
HDS-1025	10 Bits	25ns to 0.1%
HDS-1250	12 Bits	35ns to 0.025%
Voltage Output		10V Step
HDH-0802	8 Bits	200ns to 0.4%
HDH-1003	10 Bits	300ns to 0.1%
HDH-1205	12 Bits	500ns to 0.125%

Table 1.

Other general specifications that apply to all devices include TTL logic; glass or hermetic metal package; unipolar or bipolar operation with internal offsetting reference.

The HDH voltage output devices provide access to the op amp summing point so that reduced full scale output voltage swing can be provided. Such operation with an external resistor shunting the internal 1k resistor will reduce the already low op amp offset drift.

SPECIFICATIONS (typical @ +25°C with nominal power supply voltages unless otherwise noted)

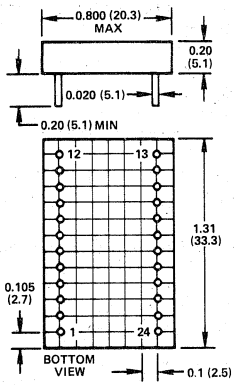
		CURRENT OUT			VOLTAGE OUT		
MODEL	UNITS	HDS-0820	HDS-1025	HDS-1250	HDH-0802	HDH-1003	HDH-1205
RESOLUTION FS = Full Scale	Bits	8	10	12	8	10	12
LSB WEIGHT		40μA	10μA	2.5μA	40mV	10mV	2.5mV
ACCURACY (Relative to FS Including Linearity)	±% FS	0.1	0.05	0.0125	0.1	0.05	0.0125
Linearity		±10μA	±5μA	±1.25μA	±10mV	±5mV	±1.25mV
	LSB	±1/4	±1/2	±1/2	±1/4	±1/2	±1/2
Monotonicity		Guaranteed Over Operating Temperature Range					
Zero Offset (Initial)		15nA max	*	*	10mV typ 50mV max	*	*
TEMPERATURE COEFFICIENTS							
Linearity	ppm/°C	3	*	*	*	*	*
Gain	ppm/°C	30	*	*	*	*	*
Unipolar Offset	ppm/°C	3	*	*	*	*	*
Bipolar Offset	ppm/°C	15	*	*	*	*	*
DATA INPUTS							
Logic Compatibility		TTL and 5V CMOS					
Logic Voltage Levels Positive Logic "1" =	V	+2 to +7	*	*	*	*	*
"0" =	V	0 to +0.8	*	*	*	*	*
Logic Loading (Each Bit) "1" =	μA	40	*	*	*	*	*
"0" =	mA	-2.6	*	*	*	*	*
Codes		BIN, OBN			BIN,OBN		
OUTPUT							
Current Range FS							
Unipolar	mA	+10.24	*	+10.24 ±0.05%	±25 max	**	**
Bipolar	mA	±5.12	*	±5.12 ±0.025%	±25 max	**	**
Voltage Out FS[1,2]							
Unipolar HDS with 200Ω Internal Connected R_L	V	+1.024	*	+1.024 ±0.05%	-10.24 ±0.1%	**	**
Bipolar	V	±0.512	*	±0.512 ±0.025%	∓5.12 ±0.05%	**	**
Compliance	V	+1.5, -2	*	*	N/A	**	**
Impedance, Internal (See Figure 1)	Ω	200	*	*	0.1 max	**	**
SETTLING TIME							
Current	ns to % FS	20 to 0.4	25 to 0.1	35 to 0.025	N/A	N/A	N/A
Voltage[2]							
Unipolar or Bipolar Out, 75Ω Load, 0.56V p-p	ns to % FS	30 to 0.4	35 to 0.1	50 to 0.025	N/A	N/A	N/A
Unipolar or Bipolar Out, Internal 200Ω Load, 1.024V p-p	ns to % FS	45 to 0.4	50 to 0.1	60 to 0.025	N/A	N/A	N/A
10V Output Step	ns to % FS	N/A	N/A	N/A	200 to 0.4	300 to 0.1	500 to 0.025
5V Output Step	ns to % FS	N/A	N/A	N/A	150 to 0.4	200 to 0.1	350 to 0.025
POWER REQUIREMENTS							
+14.5V to +15.5V	mA max	42	*	50	70	**	**
-12V to -16V	mA max	14	*	15	40	**	**
Power Supply Rejection Ratio	%/V	0.2	*	*	*	*	*
TEMPERATURE RANGE							
Operating – Glass Package	°C	0 to +70	*	*	*	*	*
Operating – "M" Metal Case[3]	°C	-55 to +125	*	*	*	*	*
Storage	°C	-55 to +125	*	*	*	*	*

NOTES:
[1] Other voltages may be obtained with external resistor.
[2] For HDS series, $V_{OUT} = I_{OUT} \times R_{equivalent}$ which is the value of the 200Ω internal impedance in parallel with the external load resistance. Thus, by correct selection of external R1 V_{OUT} can be any magnitude up to the + or – compliance voltage. See Figures 1 and 2.
[3] Contact factory or local Analog Devices sales office for "M" Metal Case device specifications and prices.

*Specifications same as HDS-0820.
**Specifications same as HDH-0802.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

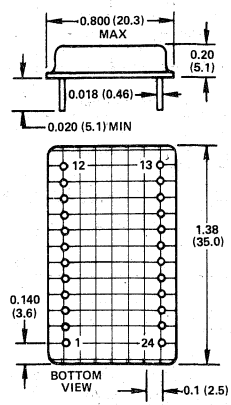
Dimensions shown in inches and (mm).



DOT ON TOP INDICATES POSITION OF PIN 1
PINS ARE GOLD PLATED.
GLASS PACKAGE

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



DOT ON TOP INDICATES POSITION OF PIN 1
METAL PACKAGE - M VERSION

PIN DESIGNATIONS HDS-0820, HDS-1025

PIN	FUNCTION
1	+15V
2, 3	BIT 1 (MSB)
4	BIT 2
5	BIT 3
6	BIT 4
7	BIT 5
8	BIT 6
9	BIT 7
10	BIT 8
11	BIT 9 (HDS-1025)
12	BIT 10
13-20	GND
21	OUTPUT
22	R_L 200Ω
23	BIPOLAR OFFSET
24	-15V

PIN DESIGNATIONS HDS-1250

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13-19	GND
20	OUTPUT
21	R_L 200Ω
22	BIPOLAR OFFSET
23	-15V
24	+15V

PIN DESIGNATIONS HDH SERIES

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13-19	GROUND
20	SUM NODE
21	OUTPUT
22	BIPOLAR OFFSET
23	-15V
24	+15V

ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12.
ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

Analog Output, ±5.12mA	Offset Binary
+5.11mA (1LSB)	111.....1
+2.56mA	110.....0
0mA	100.....0
-2.56mA	010.....0
-5.12mA	000.....0
Analog Output, 0 to +10.24mA	**Straight Binary**
+10.23mA	111.....1
+7.68mA	110.....0
+5.12mA	100.....0
+2.56mA	010.....0
0mA	000.....0

Table 2. Coding HDS Series

Analog Output, ±5.12V	Complement Offset Binary
-5.1175V	111.....1
-2.56V	110.....0
0V	100.....0
+2.56V	010.....0
+5.12V	000.....0
Analog Output, 0 to +10.24V	**Complement Binary**
-10.2375V	111.....1
-7.68V	110.....0
-5.12V	100.....0
-2.56V	010.....0
0V	000.....0

Table 3. Coding HDH Series

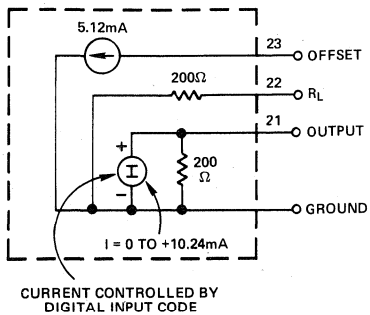


Figure 1. HDS Current Equivalent Circuit

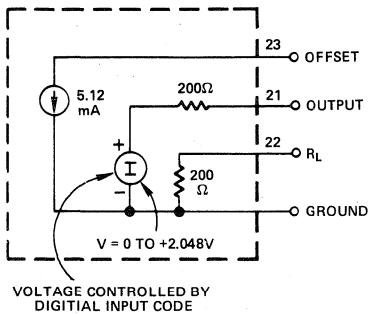


Figure 2. HDS Voltage Equivalent Circuit

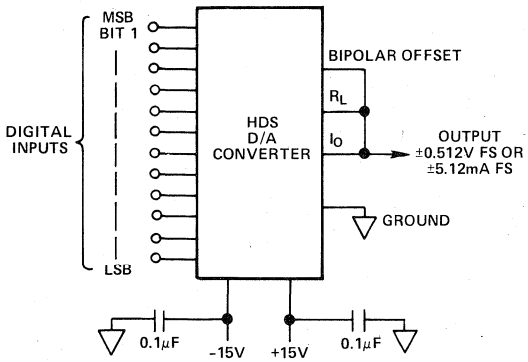


Figure 3. Bipolar Current Output

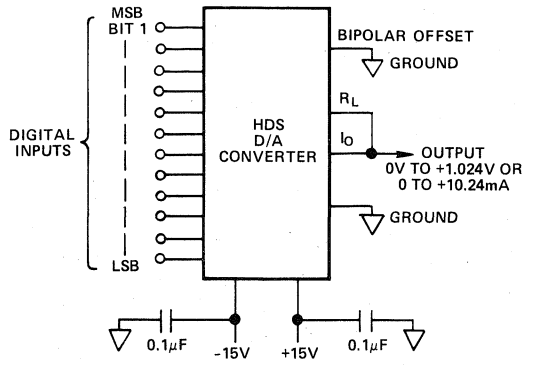


Figure 4. Unipolar Current Output

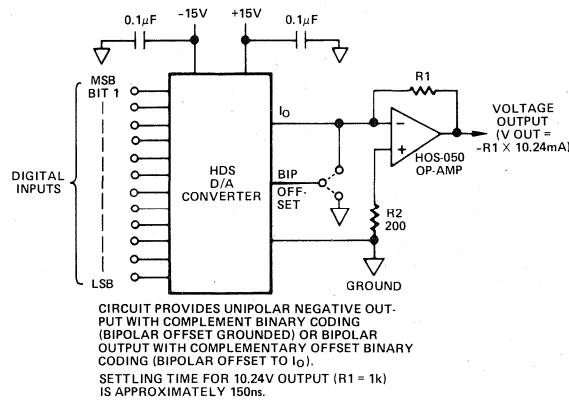
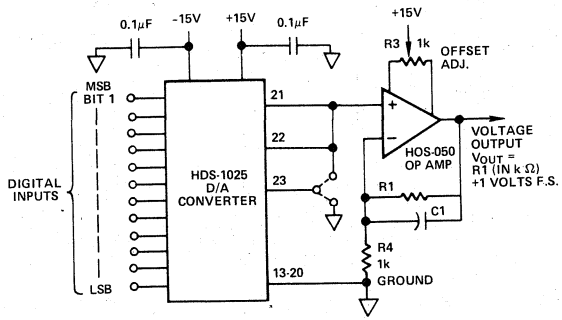


Figure 5. Inverting Unipolar or Bipolar Voltage Output

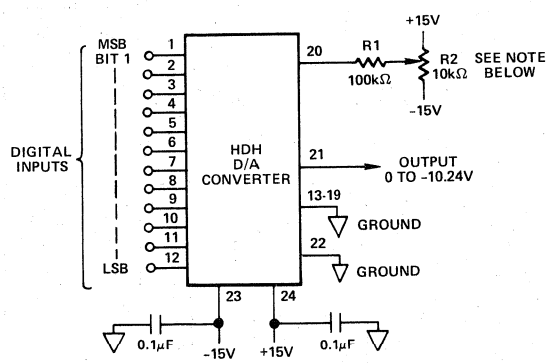
ORDERING INFORMATION

Order model number HDS-0820, HDS-1025, HDS-1250, HDH-0802, HDH-1003, HDH-1205. Models with extended operating temperature range, hermetically-sealed metal-case construction (M versions) and MIL-STD-883 processing are also available. Consult factory or local Analog Devices sales office for further information.



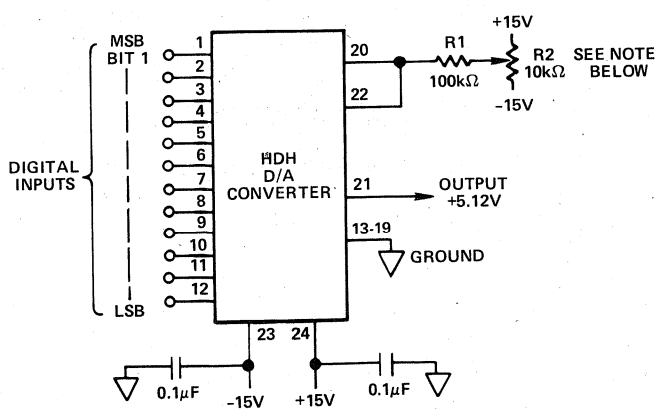
NOTES:
1. CIRCUIT SHOWN FOR UNIPOLAR POSITIVE OUTPUT. OUTPUT SETTING TIME IS APPROXIMATELY 150ns.
2. FOR 0 to +10V OUTPUT, R1 = 9kΩ.
3. R3 IS ADJUSTED TO COMPENSATE OP-AMP OFFSET.
4. FOR UNIPOLAR OUTPUT, GROUND PIN 23. FOR BIPOLAR OUTPUT, SHORT PIN 23 TO PIN 21 AND UNGROUND PIN 23.
5. C1 IS APPROXIMATELY 10pF AND MAY BE ADJUSTED FOR BEST TRANSIENT RESPONSE.

Figure 6. Noninverting Unipolar or Bipolar Voltage Output — HDS-1025



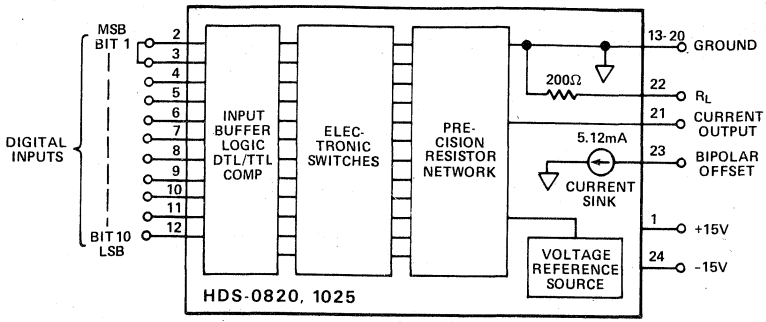
NOTE: R1 and R2 ARE OPTIONAL AND USED ONLY WHEN PRECISE ZEROING OF THE OUTPUT (<10mV) IS REQUIRED.

Figure 7. Unipolar Negative Output



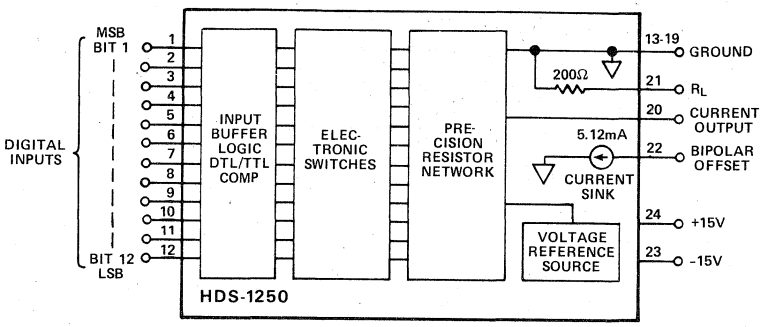
NOTE: R1 AND R2 ARE OPTIONAL AND USED ONLY WHEN PRECISE ZEROING OF THE OUTPUT (<10mV) IS REQUIRED.

Figure 8. Bipolar Output

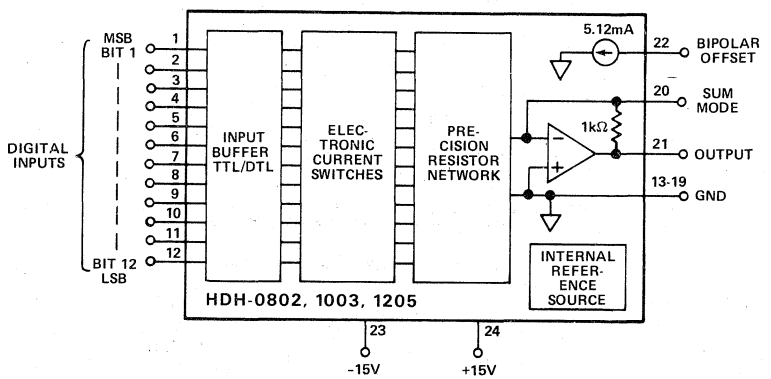


NOTE: ON 8-BIT VERSIONS, PINS 11 AND 12 ARE NOT CONNECTED INTERNALLY, AND PIN 10 IS LSB.

Block Diagram – HDS-0820 and HDS-1025



Block Diagram – HDS-1250



NOTE: ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12.
ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

Block Diagram – HDH-0802, HDH-1003 and HDH-1205

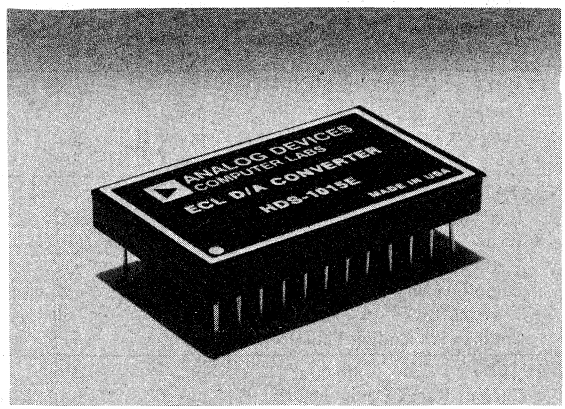
ANALOG DEVICES

Ultra High-Speed ECL Hybrid D/A Converter

HDS-0810E - HDS-1015E

FEATURES
- Settling Times to 10ns
- Low Glitch Energy – 200pV-sec.
- 100MHz Update Rates
- 8- & 10-Bit Versions Available
- Low Power < 1 Watt
- Available Screened to MIL-STD-883

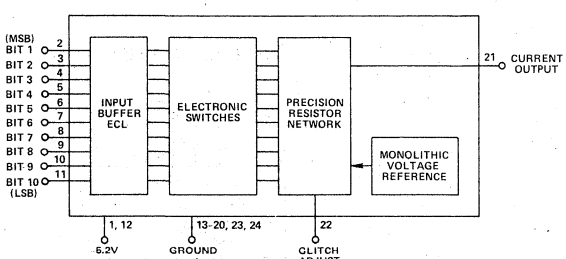
APPLICATIONS
- Raster Scan & Vector Graphic Displays
- TV Video Reconstruction
- Digital VCO's
- High-Frequency Waveform Generators
- Analytical & Medical Instrumentation



PRODUCT DESCRIPTION

The HDS-0810E and HDS-1015E represent the latest state-of-the-art in ultra-high-speed hybrid D/A converters. They are designed to be input compatible with standard ECL logic families, and feature internal high-precision monolithic voltage reference, active laser-trimmed resistor network, and 75Ω output impedance – allowing them to be used to drive 75Ω cable directly without external driver amplifiers. This feature assures that a full 1 volt is available at the load, since the D/A output is a full 27mA. In addition, these D/A's are monotonic over the full operating temperature range and require only one power supply (-5.2V) for operation.

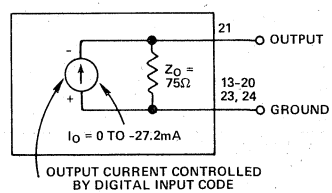
Packaged in an industry standard size 24-pin double width dual in-line case, the HDS-E Series D/A's are available in either ceramic/glass cases (commercial) or hermetically sealed metal cases (military). They are also available screened to MIL-STD-883.



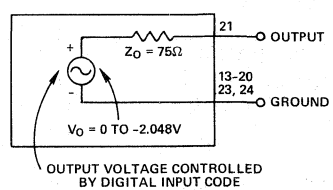
ON THE HDS-0810E, PINS 10 AND 11 ARE NOT CONNECTED INTERNALLY

Block Diagram

The HDS-E D/A's are ideally suited for use in a wide variety of applications, including graphic CRT displays, since they feature very low glitch energy and extremely fast settling time.



Current Equivalent Circuit



Voltage Equivalent Circuit

SPECIFICATIONS (typical @25°C with nominal power supplies and with 75Ω output load unless otherwise noted)

MODEL	UNITS	HDS-0810E	HDS-1015E
RESOLUTION FS = Full Scale	Bits	8	10
LSB WEIGHT (Current)	μA	106	27
LSB WEIGHT (Voltage)	mV	4	1
ACCURACY[1]	±% FS	0.1	0.05
Linearity	±μA	26.5	13
Monotonicity		Guaranteed	*
Zero Offset (Initial)	μA	5	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C	5	*
Zero Offset	ppm/°C	1	*
Gain	ppm/°C	80	*
DATA INPUTS			
Logic Compatibility		ECL	*
Logic Voltage Levels "1" =	V	-0.9	*
(Positive Logic) "0" =	V	-1.7	*
Logic Loading "1" =	mA	+13.6	*
(Each Bit) "0" =	μA	-50	*
Coding (See Coding Table)		BIN	*
OUTPUT			
Current Range (Unipolar) FS	mA	0 to -27.2	0 to -27.3
Voltage with 75Ω Ext. Load	V (±1%)	0 to -1.020	0 to -1.023
Compliance	V	-1.1 to +1.1	*
Impedance, Internal	Ω (±5%)	75	*
SPEED PERFORMANCE			
Settling Time (Voltage)[2]	ns (to % FS)	10 (0.2)	15 (0.1)
Slew Rate	V/μs	200	*
Update Rate[3]	MHz	100	67
Rise Time	ns	4	4
Glitch Energy[4]	pV-sec	200	*
POWER REQUIREMENTS			
-5.2V ±0.25V	mA	155	180
Power Supply Rejection Ratio	%/%	0.04	*
Reference		Monolithic, Internal	*
TEMPERATURE RANGE			
Operating; Glass Case	°C	0 to +70	*
Operating; "M" Metal Case	°C	-55 to +125	*
Storage	°C	-55 to +125	*

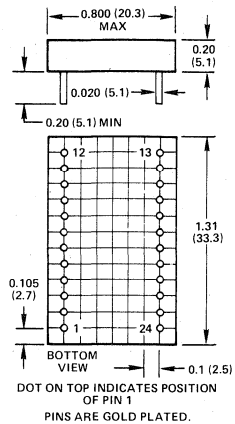
NOTES:
[1] Relative to FS, including linearity.
[2] Worst case settling time. Includes FS and MSB transitions. See Figure 1.
[3] Limited only by D/A settling time.
[4] Reducible to less than 100pV-sec with appropriate deskewing of digital inputs. See Figure 2.

*Specifications same as HDS-0810E.

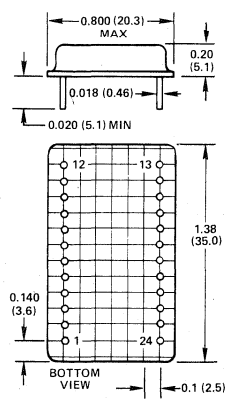
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



DOT ON TOP INDICATES POSITION OF PIN 1
PINS ARE GOLD PLATED.
GLASS PACKAGE

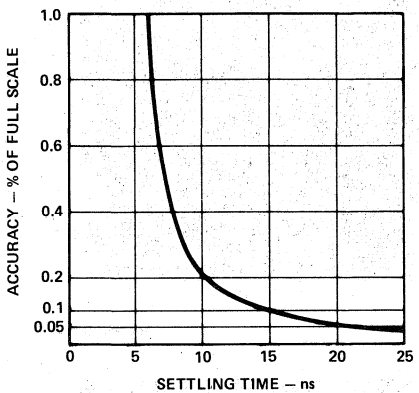


DOT ON TOP INDICATES POSITION OF PIN 1
METAL PACKAGE - M VERSION

PIN DESIGNATIONS

PIN	FUNCTION
1, 12	-5.2V
2	BIT 1 (MSB)
3	BIT 2
4	BIT 3
5	BIT 4
6	BIT 5
7	BIT 6
8	BIT 7
9	BIT 8
10	BIT 9
11	BIT 10 (LSB)
13-20	GROUND
21	OUTPUT
22	GLITCH ADJUST
23, 24	GROUND

ON THE HDS-0810E, PINS 10 AND 11 ARE NOT CONNECTED INTERNALLY, AND PIN 9 IS THE LSB. ALL GROUND PINS ARE CONNECTED TOGETHER INTERNALLY.



TIME IS MEASURED FROM 50% TRANSITION POINT OF MSB. WITH INPUT DATA LINES DESKEWED AND 75Ω LOAD. VOLTAGE OUTPUT.

Figure 1. HDS-0810E & HDS-1015E – Accuracy vs. Settling Time

Binary Input Code	Analog Output with 75Ω Load HDS-0810E	HDS-1015E
111...111	0	0
111...110	-4mV	-1mV
110...000	-252mV	-255mV
101...111	-256mV	-256mV
100...000	-508mV	-511mV
011...111	-512mV	-512mV
010...000	-764mV	-767mV
001...111	-768mV	-768mV
000...001	-1016mV	-1022mV
000...000	-1020mV	-1023mV

Table 1. Coding Table

APPLICATIONS INFORMATION

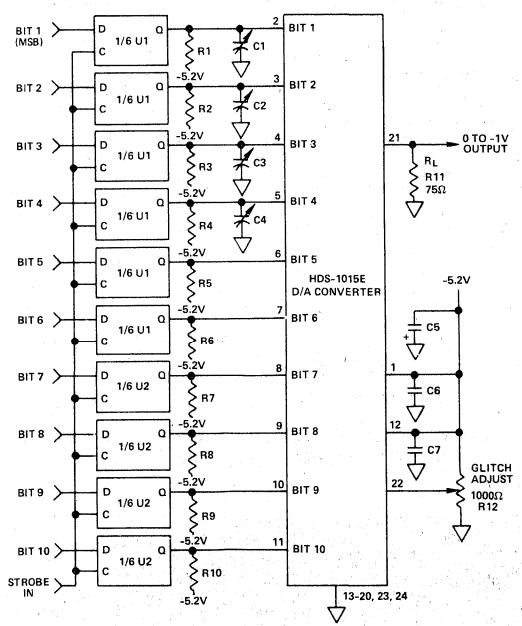
High-Speed Low-Glitch Operation Suggestions

The HDS-E Series D/A's offer the highest available speed. However, with this speed performance, certain precautions and operating conditions should be considered. You are now in the RF world.

1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with a 1μF (or larger) tantalum capacitor mounted between the -5.2V supply line and ground near the D/A.
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 1 and 12 to ground (see Figure 2).
4. The D/A converter should be driven with an ECL register as physically close to the D/A as possible. The 10176 HEX "D" Master-slave flip-flop is recommended. The six most significant bits should come from the same package as shown in Figure 2. The two or four least significant bits should come from a second package.
5. Each digital input should be terminated with a 510Ω resistor connected between the input and -5.2V (see Figure 2).
6. The threshold of the internal current switches can be optimized for low glitch energy by the addition of an external potentiometer connected to Pin 22 of the D/A (shown as R12 in Figure 2). This potentiometer is adjusted for minimum glitch energy as shown in Photo 3.

   If required, variable capacitors can be added to "deskew" the most significant bits for lowest glitch—although this is not usually required in many applications. These capacitors are added as shown in Figure 2 (C1-4). They are adjusted in conjunction with R12 for minimum glitch energy as shown in Photo 3.

   In composite television applications, C1-4 are adjusted for best differential phase performance, and R12 is adjusted for best differential gain performance. These may tend to interact, so going back and forth between adjustments may be required.
7. Standard 24-pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/A's should be soldered directly into the printed circuit board without sockets.



NOTES:
1. R1-10 = 510Ω, 1/4 W, 5%; R11 = OUTPUT LOAD; R12 = 1000Ω POTENTIOMETER, ADI P/N 79PR1K; C1 - ERIE 538-002F, 15-60pF, OR EQUIVALENT; C2, 3, 4 = ERIE 538-002D, 9-35pF, OR EQUIVALENT; C5 = 100μF TANTALUM; C6, 7 = 0.1μF CERAMIC; U1, 2 – 10176, 10K ECL TYPE "D" F.F.
2. IF THE HDS-0810E IS SUBSTITUTED, PINS 10 AND 11 AS WELL AS THE PARTS ASSOCIATED WITH BITS 9 AND 10 ARE UNUSED.
3. THE FIRST SIX MOST SIGNIFICANT BITS (BITS 1-6) SHOULD ALWAYS BE ROUTED THROUGH ONE 10176 FOR CONSISTENCY IN TIMING AND REDUCED DATA SKEW.

Figure 2. HDS-1015E – Typical Hook-Up and Test Circuit

GAIN ADJUSTMENT

The HDS-E Series D/A's are actively laser-trimmed to provide a voltage into exactly 75Ω which is an even binary multiple; i.e., the HDS-0810E has an LSB of 4mV and the HDS-1015E has an LSB of 1mV. This makes the full-scale output slightly greater than one volt. If an output of exactly one volt is required—such as for TV reconstruction—a 2k potentiometer may be placed across the output of the D/A for gain adjustment. For a one volt output, the adjusted value of this pot will be about 1500Ω.

ULTRA-LOW GLITCH OPERATION

For extremely low glitch requirements (<50 - 100pV-s), an HTS-0025 Track-and-Hold is recommended as a deglitcher (see Figure 2). The duration of the HDS Series D/A glitch is approximately 10ns. The hold time of the HTS-0025 should be at least 15ns to "mask out" the glitch. The minimum acquisition time of the HTS-0025 for 0.1% accuracy is 30ns. This implies that the circuit of Figure 2 can be operated up to 22MHz and still maintain 10-bit accuracy. For 0.2% accuracy, the acquisition time for the T&H can be reduced to 25ns, allowing the circuit to operate to 25MHz. This discussion assumes that the D/A will be required to slew full scale (one volt) between adjacent samples. In practice, the sample-to-sample variation is less than full scale depending on the amount of oversampling. In a practical situation, therefore, 10-bit accuracy should be achievable at 25MHz update rates.

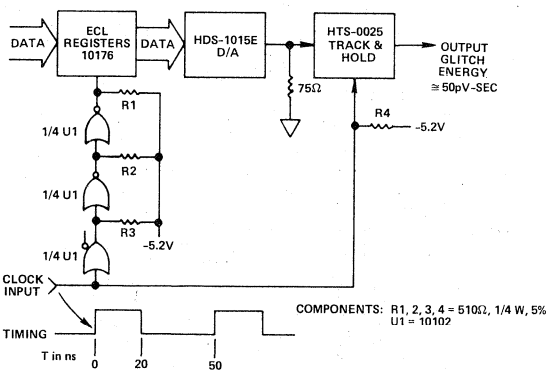


Figure 3. HTS-0025 Track & Hold Used with HDS-1015E D/A as Deglitcher @ 20MHz Update Rate

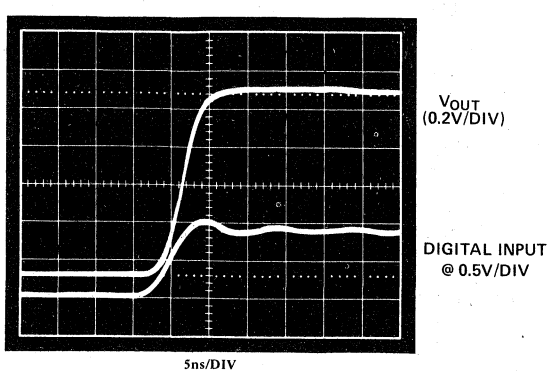


Photo 1. Voltage Output — Positive Going

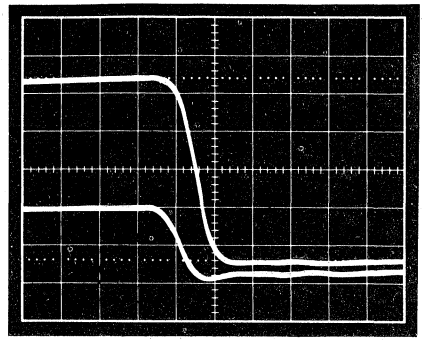
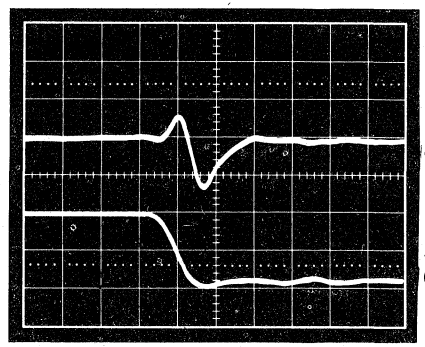


Photo 2. Voltage Output — Negative Going



GLITCH ENERGY = 100pV-SEC; FROM TEST CIRCUIT OF FIGURE 1.

Photo 3. Voltage Output — Glitch Characteristic

ORDERING INFORMATION

For commercial environment applications (0 to +70°C), order models HDS-0810E or HDS-1015E for 8- or 10-bit operation, respectively.

For extreme environment applications (-55°C to +125°C), order metal cased models HDS-0810EM or HDS-1015EM for 8- or 10-bit operation, respectively.

These devices are also available screened to MIL-STD-883. Consult the factory.

ANALOG DEVICES

Ultra High Speed Deglitched D/A Converter

MDD SERIES

FEATURES

- Ultra-High Speed: 20MHz Word Rate
- 8- and 10-Bit Versions Available
- TTL Compatible
- Smallest Size Available: 3″ X 4″ X 0.5″
- Completely Self-Contained with Input Register, D/A, Deglitcher, Timing, Internal References, and Output Buffering

APPLICATIONS

- Color-Television Video Reconstruction, Time-Base Correction and Frame Synchronization
- Graphic Displays
- Deflection Systems
- Character Generators
- High Speed D/A Systems

GENERAL DESCRIPTION

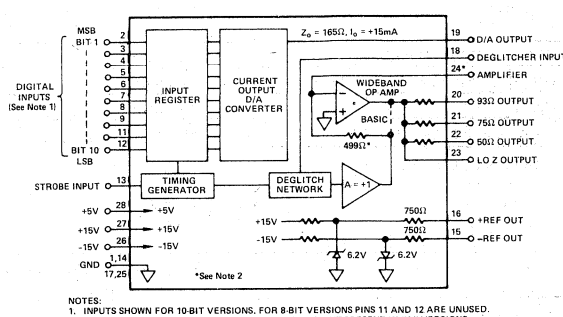
The MDD Series is a subsystem module which contains an input digital register, ultra-high speed current output D/A converter, deglitcher, output buffer amplifier, precision references, and timing circuitry within a 3″X4″X0.5″ case. The output of the device is an ultra-linear analog representation of the digital input. Requiring only external gain and offset potentiometers for final calibration, the MDD D/A solves the glitch problem associated with high-speed D/A converters. The incorporation of an internal register virtually eliminates the need for input bit time deskewing. While not totally eliminating the glitch per se, the remnant glitch is very small, and more importantly, constant (and therefore filterable) over the output range.

The MDD Series is available with 8- or 10-bit resolution and in two versions. The basic versions contain a unity gain output buffer and can deliver 2V p-p open circuit (or 1V p-p into a load) when the MDD output is both source and load terminated. The "A" versions contain a very high speed output gain amplifier to allow the MDD to deliver 4V p-p open circuit (or 2V p-p into a load) when the device is source and load terminated. Higher output voltages may be obtained—up to ±10V by external feedback resistor selection. However, settling time degradation must be expected.

TV APPLICATION

The "A" version of the MDD Series deglitched D/A is ideally suited for color television video reconstruction. Its output can directly drive the low impedances normally associated with video baseband transmission. Since the output impedance of the internal operational amplifier is less than 1Ω, the transmission-line match obtained with the internal source terminating resistor is almost perfect. Other applications include waveform generation, automatic test equipment, and fast process control systems.

Designed primarily for PC board mounting, these D/A's may also be plugged into pin sockets. The pins are 0.04″ diameter, gold plated, and are on 0.2″ centers. For increased reliability, each module is burned-in for 96 hours at +25°C before final test and shipment.



NOTES:
1. INPUTS SHOWN FOR 10-BIT VERSIONS. FOR 8-BIT VERSIONS PINS 11 AND 12 ARE UNUSED.
2. THESE PARTS (*) ARE OMITTED IN BASIC VERSIONS, BUT PRESENT IN "A" VERSIONS.

MDD Series Block Diagram

SPECIFICATIONS (typical at +25°C and nominal supply voltages unless otherwise noted)

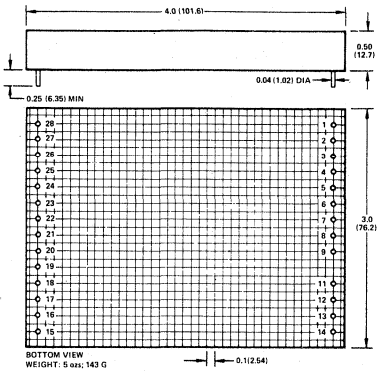
MODEL	MDD-0820 MDD-0820A	MDD-1020 MDD-1020A
RESOLUTION	8 Bits	10 Bits
Accuracy (including linearity) at Maximum Word Rate of 20MHz	±0.2%	±0.05%
Monotonicity	Guaranteed 0 to +70°C	
DIGITAL DATA BIT INPUTS		
Logic Level/Load	1 Standard "S" TTL Load.	
Positive Logic—Binary (BIN)	"1" = +2.4V to +5V "0" = 0V to +0.4V	
DIGITAL STROBE INPUT		
Logic Level/Load	2 Standard "S" TTL Loads	
Positive Logic	"1" = +2.4V to +5V "0" = 0V to +0.4V	
Risetime and Falltime	10ns max	
Width	15ns min	
Timing	Negative-Going Trailing Edge to Occur a Minimum of 20ns After Last Data Bit Change	
Frequency	20MHz max	
OUTPUT	**MDD-0820 MDD-1020**	**MDD-0820A MDD-1020A**
Voltage, No Load, Unipolar	0 to +2V	Externally Programmable with Gain and Offset Resistors to ±10V max
Bipolar	+1V to -1V	
Impedance		
Pin 23, Low Z	10Ω max	1Ω max
Pin 22, 50Ω	50Ω ±5%	50Ω ±1%
Pin 21, 75Ω	75Ω ±5%	75Ω ±1%
Pin 20, 93Ω	93Ω ±5%	93Ω ±1%
Amplifier Current	±50mA for dc load = 100Ω min, dc load = Z_{OUT} + R_{LOAD}	
DAC Current	+15mA	+15mA
SETTLING TIME		
DAC Current Output (to 0.1%)	15ns	15ns
Voltage Output	50ns to 0.1% 2V p-p	120ns to 0.1% 4V p-p
RESIDUAL GLITCH[1]	30mV for 2V p-p F.S. Output or 1.5% of F.S.	
PEDESTAL	10mV for 2V p-p F.S. Output or 0.5% of F.S.	
OUTPUT ZERO OFFSET	Adjustable to Zero	
OUTPUT ZERO OFFSET vs. TEMP	100ppm/°C	
GAIN	Adjustable	
REFERENCES AVAILABLE	±6.2V	
POWER REQUIREMENTS		
+15V ±3%	120mA	
-15V ±3%	150mA	
+5V ±5%	250mA	
Power Supply Rejection Ratio	0.1%/V	
CASE	Diallyl Phthalate (per MIL-M-14 type SDG-F)	
TEMPERATURE RANGE		
Operating	0 to +70°C	
Storage	-55°C to +85°C	

[1] Occurs at the update rate.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND*	15	-REF OUT
2	BIT 1 INPUT (MSB)	16	+REF OUT
3	BIT 2 INPUT	17	GROUND*
4	BIT 3 INPUT	18	DEGLITCHER INPUT
5	BIT 4 INPUT	19	D/A OUTPUT
6	BIT 5 INPUT	20	93Ω OUTPUT
7	BIT 6 INPUT	21	75Ω OUTPUT
8	BIT 7 INPUT	22	50Ω OUTPUT
9	BIT 8 INPUT	23	LO Z OUTPUT
10	NC	24	AMP FEEDBACK
11	BIT 9 INPUT	25	GROUND*
12	BIT 10 INPUT (LSB)	26	-15V POWER INPUT
13	STROBE INPUT	27	+15V POWER INPUT
14	GROUND*	28	+5V POWER INPUT

*ALL GROUNDS INTERNALLY CORRECTED

NOTES ON "DEGLITCHING"

An MDD Series D/A converter operating with a full-scale p-p analog output of 1V will typically have a glitch, or transient, in its output which is 15mV in amplitude and is 25ns wide, at the 50% points. These typical values are independent of whether the D/A converter is an 8-bit unit or a 10-bit unit.

This glitch remains constant, regardless of the transition points. In other words, it is the same for the transition from 0000000001 to 1000000000 as it is for the transition from 1000000000 to 1000000001 or any other two input words.

A constant glitch is the purpose of the deglitcher circuits. They are intended to hold the area under the curve at a constant value; they are not intended to get rid of all glitches per se.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line; i.e., a single-line spectrum at the sample rate frequency, and harmonics of the sample frequency.

If the glitch is a function of signal dynamics, as it is in the case of a D/A converter output which is not deglitched, a multitude of intermodulation products are formed. Some of these IM products appear in the video pass-band as spurious signals and increased noise level. The deglitcher circuits effectively eliminate these products. When they do, the S/N ratio approaches that of an ideally-quantized signal, where the rms noise is $Q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

In summary then:

- The residual glitch for an MDD Series D/A converter is typically 15mV for a full-scale 1V p-p output; this is 1.5% of F.S.
- The glitch width is typically 25ns at the 50% points.
- The amplitude and width of the glitch are constant, and independent of:
  - —the magnitude of change in successive transitions
  - —number of bits of digital output
  - —input (update) data rates

D/A converters without deglitching circuits (such as the Analog Devices' MDS/MDP D/A units) have smaller, shorter glitches, on the average; but this type of converter has larger glitches at the major crossings, especially at the mid-scale transition.

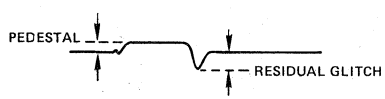


Figure 1. Pedestal/Glitch Relationship

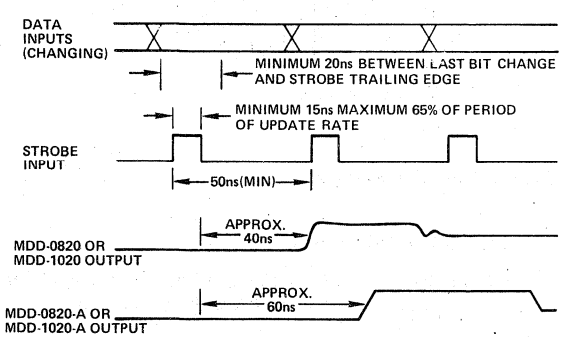


Figure 2. MDD Series Timing Diagram

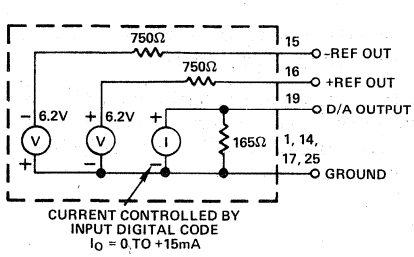


Figure 3. D/A Current Equivalent Circuit

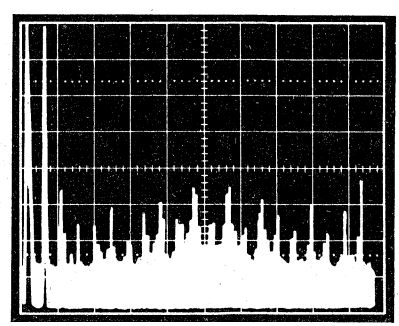


Figure 4. Spectrum of 10-bit D/A Operating at 11MHz Update Rate Without Deglitching — Unfiltered

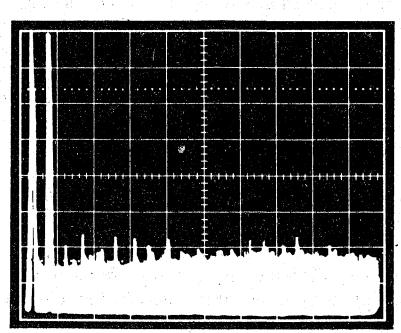


Figure 5. Spectrum of 10-bit D/A Operating at 11MHz Update Rate With Deglitching — Unfiltered

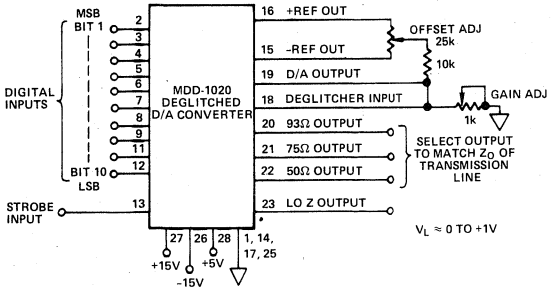


Figure 6. Unipolar Output Configuration Basic Versions

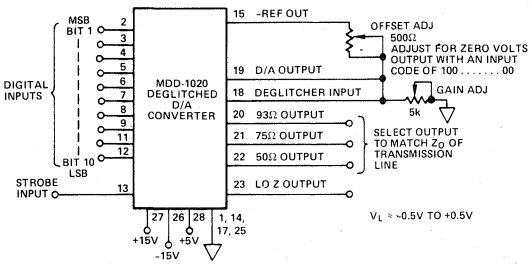
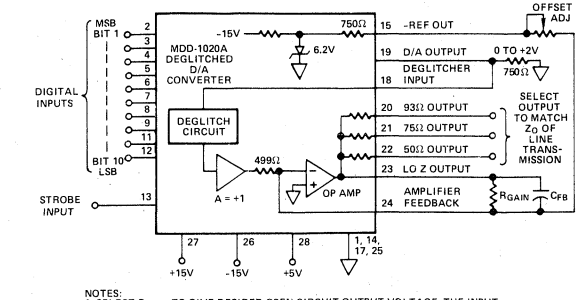


Figure 7. Bipolar Output Configuration Basic Versions



NOTES:
1. SELECT R_{GAIN} TO GIVE DESIRED OPEN CIRCUIT OUTPUT VOLTAGE. THE INPUT VOLTAGE TO THE OP AMP IS APPROXIMATELY 0 TO +2V. THE OUTPUT OF THE OP AMP IS THEREFORE ((2 × R_{GAIN})/500Ω) VOLTS p-p.
2. THE LOGIC IS INVERTED INTERNALLY FOR THE "A" VERSIONS SUCH THAT ALL "1'S" AT THE DIGITAL INPUTS YIELDS A FULL-SCALE POSITIVE VOLTAGE AT THE OP AMP OUTPUT.
3. FOR POSITIVE UNIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 800Ω, MAKING A 2000Ω POTENTIOMETER IDEAL.
4. FOR BIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 2300Ω, MAKING A 5000Ω POTENTIOMETER IDEAL. THE OUTPUT VOLTAGE SHOULD BE ADJUSTED FOR ZERO WITH AN INPUT CODE OF 10 . . . . . 00.
5. MAKE C_{FB} NOMINALLY 10pF. SELECT FOR OPTIMUM SETTLING TIME IF DESIRED.
6. IF ADJUSTABLE GAIN IS DESIRED, ADD A LOW-VALUE, LOW-INDUCTANCE CERMET TRIMMING POTENTIOMETER IN SERIES WITH R_{GAIN}. BY PUTTING THE GAIN ADJUSTMENT HERE, THE GAIN AND OFFSET ADJUSTMENTS ARE INDEPENDENT OF EACH OTHER.

Figure 8. Output Configuration — "A" Versions

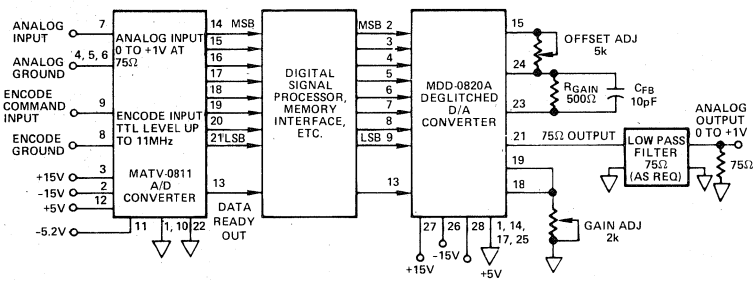


Figure 9. Typical A/D-D/A Back-to-Back Connections for Video Applications or Testing

The typical video differential phase and gain errors (disregarding quantization effects) for the configuration shown are 3° and 3%, respectively, using an encode command frequency of three times the NTSC color subcarrier (10.74MHz). For applications requiring digitization at frequencies of four times NTSC (14.32MHz) or three times PAL (13.29MHz) the MATV-0816 A/D Converter should be substituted. For applications requiring digitization at four times PAL (17.74MHz), the MATV-0820 A/D Converter should be substituted. Results are applicable for either NTSC or PAL test signals using the 20 IRE modulated ramp.

Due to the inherently stable characteristics of the output operational amplifier, the "A" versions are recommended for driving properly terminated video terminated lines.

ORDERING INFORMATION

For 8-Bit Models, Order:	MDD-0820	without output amplifier
	MDD-0820A	with output amplifier
For 10-Bit Models, Order:	MDD-1020	without output amplifier
	MDD-1020A	with output amplifier

Mating pin socket connectors for the MDD Series is model MSB-2. Prototyping socket is MSD-1.

The MDD Series D/A's are normally burned-in at +25°C for a minimum of 96 hours. For extended burn-in, consult the factory. All of Analog Devices' data acquisition products are covered by a one-year warranty.

ANALOG DEVICES

Ultra High Speed Multiplying D/A Converter

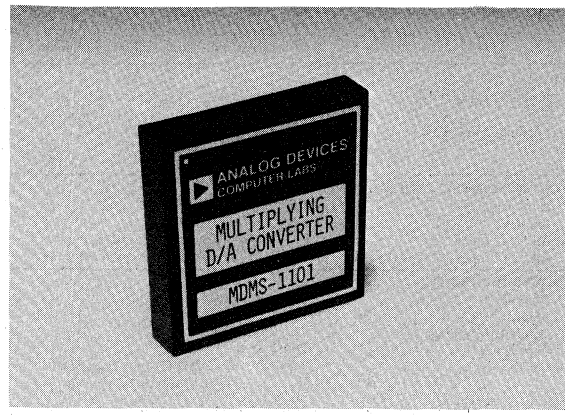
MDMS SERIES

FEATURES

- **Small Size: 2″ X 2″ X 0.4″**
- **Highest Speed Available**
- **High Multiplying Accuracy: Maintains Monotonicity and Linearity for any Analog Input within the Specified Range**
- **High Current Output: 10mA Full Scale**
- **High Reliability, Hybrid Microcircuit Construction**
- **Guaranteed Operation: -30°C to +85°C**

APPLICATIONS

- **CRT Displays**
- **Waveform Generation**
- **Vector Generation**
- **Fast Digital Attenuator**



GENERAL DESCRIPTION

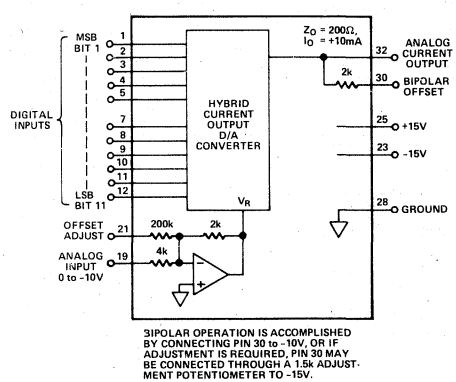
The MDMS series is an ultra-high speed, one or two-quadrant, multiplying D/A converter capable of 10MHz operation and 11-bit precision. The settling time for both analog and digital inputs is 100ns, and the large signal bandwidth of the analog input is in excess of 10MHz. The module is designed for the needs of the graphic display field and other applications requiring high-accuracy, high-speed multiplying operation.

The current output of the MDMS series D/A is precisely proportional to the analog input signal multiplied by the digital input code. The analog input signal may be any voltage between 0V and -10V, and can be a sine wave, triangle wave, sawtooth, or other waveform. The D/A output is an accurate scaled version of the input waveform, the scale factor being the digital input code. Alternatively, the analog input voltage may be used to scale a digitally generated signal. Various offsetting provisions are made so that the analog signal, digital signal, and output may be made bipolar or unipolar in order to accommodate various uses requiring one or two-quadrant operation.

The output impedance of the D/A is 200 ohms so that a two-volt output swing is possible with no load. Loading the output with 200 ohms results in a 1 volt p-p output. If an external operational amplifier such as the Analog Devices' HOS-050 Op Amp is connected to the output of the D/A, output voltages up to 20V p-p are obtainable at a small sacrifice in speed.

ORDERING INFORMATION

Order Model Number MDMS-0801, MDMS-1001, or MDMS-1101. Ruggedized versions with extended burn-in are also available. Consult the factory.



MDMS Series - Block Diagram

SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

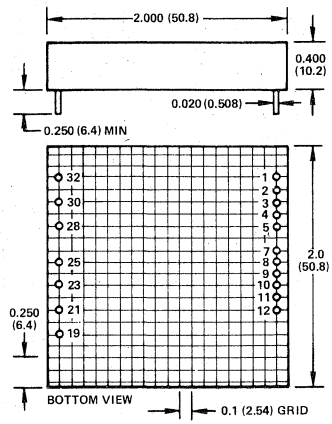
MODEL	MDMS-0801	MDMS-1001	MDMS-1101
RESOLUTION	8 Bits	10 Bits	11 Bits
LSB Weight	40μA	10μA	5μA
ACCURACY (ADJUSTABLE TO)	±0.2%	±0.05%	±0.025%
Monotonicity	Guaranteed	*	*
Linearity	20μA, ±1/2LSB	5μA, ±1/2LSB	2.5μA, ±1/2LSB
ANALOG INPUT			
Voltage Range	0 to -10V	*	*
Impedance	4kΩ ±2%	*	*
Transfer Function (inverting)	0V input scales D/A output to minimum output; -10V input scales D/A output to maximum output.		
DIGITAL INPUT (TTL)			
Positive Logic, "1" =	+2.4V to +5.0V	*	*
"0" =	0V to 0.4V	*	*
Loading, 2 Std. TTL Loads			
"0" =	-5mA	*	*
"1" =	50μA	*	*
CODING (PARALLEL INPUT DATA)			
Unipolar	BIN	*	*
Bipolar	OBN	*	*
All "1's" Input	Maximum Positive Output		
All "0's" Input	Maximum Negative Output		
OUTPUT (CURRENT)			
Unipolar	0 to +10mA	*	*
Bipolar	±5mA	*	*
Compliance Voltage	+1.5V, -2V	*	*
Impedance	200Ω, ±1%	*	*
Loading	200Ω for 0 to 1V p-p Out 0Ω for 0 to 2V p-p Out		
Zero Offset (max)	50nA	*	*
DYNAMIC CHARACTERISTICS			
Settling Time (digital & analog)	90ns to 0.2% F.S.	100ns to 0.1% F.S.	130ns to 0.05% F.S.
Bandwidth (analog in)	10MHz	*	*
TEMPERATURE COEFFICIENTS			
Linearity	2ppm/°C	*	*
Monotonicity	Guaranteed -30°C to +85°C		
POWER REQUIREMENTS			
+15V ±10%	60mA	*	*
-15V ±10%	20mA	*	*
Power Supply Rejection Ratio	0.005%/V	*	*
TEMPERATURE RANGE			
Operating	-30°C to +85°C		
Storage	-55°C to +125°C		
PHYSICAL CHARACTERISTICS			
Case	Diallyl Phthalate per MIL-M-14 Type SDG-F		

*Specifications same as MDMS-0801

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE: DOT ON TOP INDICATES POSITION OF PIN 1

WEIGHT: 1.6 OZ, 45.3 G

PINS ARE GOLD PLATED PER MIL-G-5204 TYPE II

MATING SOCKET MSA-1

PIN DESIGNATIONS

PIN	FUNCTION
1	BIT 1 INPUT (MSB)
2	BIT 2 INPUT
3	BIT 3 INPUT
4	BIT 4 INPUT
5	BIT 5 INPUT
7	BIT 6 INPUT
8	BIT 7 INPUT
9	BIT 8 INPUT
10	BIT 9 INPUT
11	BIT 10 INPUT
12	BIT 11 INPUT LSB
19	ANALOG INPUT
21	OFFSET ADJ
23	-15V POWER INPUT
25	+15V POWER INPUT
28	GROUND
30	BIPOLAR OFFSET
32	ANALOG OUTPUT

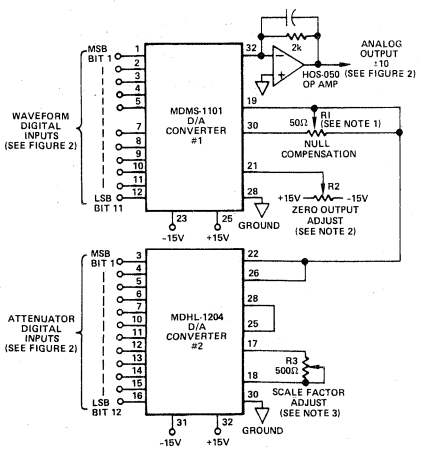
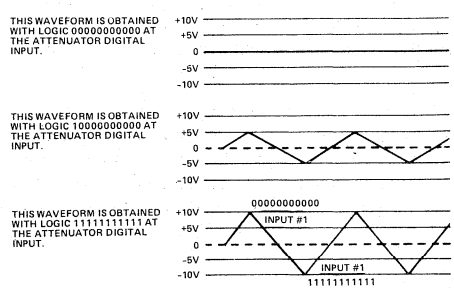


Figure 1. The MDMS-1101 Multiplying D/A Used as a Digital Waveform Generator with Digital Attenuator Control



NOTES
1. R1 MAY BE OMITTED IF 0.5% DC SHIFT IS PERMISSIBLE BETWEEN MINIMUM & MAXIMUM ATTENUATION.
2. ADJUST R2 FOR 0V OUTPUT WITH ATTENUATOR INPUT SET FOR 00000000000 AND WAVEFORM INPUT ACTIVE.
3. ADJUST R3 TO OBTAIN ±10V OUTPUT WITH ATTENUATOR INPUT SET FOR 11111111111 AND WAVEFORM INPUT ACTIVE.

THE ABOVE WAVEFORMS DEPICT THE ANALOG OUTPUT FOR VARIOUS VALUES OF ATTENUATOR DIGITAL INPUTS TO D/A #2 WITH A DIGITAL TRIANGLE BEING APPLIED TO THE WAVEFORM DIGITAL INPUT OF D/A #1.

PEAK POSITIVE LEVEL = 00000000000 DIGITAL INPUT
PEAK NEGATIVE LEVEL = 11111111111 DIGITAL INPUT

(THE OUTPUT OP AMP INVERTS THE SENSE OF THE INPUT BITS)

Figure 2. Operation of Multiplying D/A Circuit

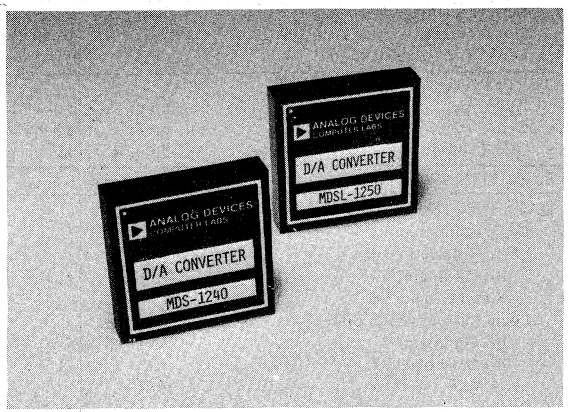
ANALOG DEVICES

8-, 10-, 12-Bit Video Speed Current and Voltage Out, D/A Converters

MDS/MDSE/MDSL/MDH SERIES

FEATURES
- Current Settling Times to 15ns
- ±1.5V Compliance
- Voltage Settling Times to 100ns (MDH)
- Monotonicity Guaranteed Over Temperature
- High Output Currents — 15mA
- -30°C to +85°C Operating Range
- Industry Standard Pin Outs
- 20V, p-p Out (MDH)
- TTL or ECL Logic

APPLICATIONS
- CRT Vector Displays
- Digitial Waveform Generation
- Automatic Test Equipment
- TV Picture Reconstruction



GENERAL DESCRIPTION

This broad family of digital-to-analog converters represents the "state of the art" in modular, high speed, voltage and current output devices. The family consists of a total of 11 devices in 4 series (MDS, MDSE, MDSL and MDH) that allow the user to make engineering trade-offs between resolution, speed, output and logic type. The first 3 are high compliance current output units which make possible linear output swings greater than ±1.5V. The voltage output MDH series contain a fast settling hybrid operational amplifier which provides ±10V output at ±50mA. To simplify selection these major specifications are summarized in Table 1.

MODEL	BITS	FULL SCALE OUTPUT	FULL SCALE SETTLING TIME	INPUT LOGIC
		(Fastest Settling High Current Out)		
MDS-0815	8	15mA	15ns to 0.4% FS	TTL
MDS-1020	10	15mA	20ns to 0.1% FS	TTL
MDS-1240	12	15mA	40ns to 0.025% FS	TTL
		(MDS with ECL Logic)		
MDS-0815E	8	15mA	15ns to 0.4% FS	ECL
MDS-1020E	10	15mA	20ns to 0.1% FS	ECL
		(Low Current MDS)		
MDSL-0825	8	5mA	25ns to 0.1%	TTL
MDSL-1035	10	5mA	25ns to 0.1%	TTL
MDSL-1250	12	5mA	50ns to 0.025%	TTL
		(Voltage Out MDSL)		
MDH-0870	8	10V/50mA	150ns to 0.4%	TTL
MDH-1001	10	10V/50mA	200ns to 0.1%	TTL
MDH-1202	12	10V/50mA	500ns to 0.025%	TTL

Table 1.

SPEED WITH PRECISION

Analog Devices' model MDS-1240 is the first D/A converter available with highly reliable, internal hybrid construction to achieve ultra-high speed operation. In fact, it is the fastest 12-bit D/A available, settling to 0.025% in 40ns. Hybrid construction eliminates the thermal lag problem inherent in 12-bit D/A's constructed with discrete components. This in turn means that the accuracy is maintained over the total frequency range of operation, yielding superior results for frequency domain applications.

The MDS-1240 is particularly well suited for CRT display applications because of its unsurpassed speed and drive capabilities. The high output current (15mA) allows the use of low impedance loads so that settling times remain short — even with higher output voltage levels. The ability to drive load capacitance is at least 3 times that of other 12-bit D/A's thus providing capability to drive a terminated transmission line directly. The MDS-815 and MDS-1020 provide similar performance at 8 and 10 bits, while the MDS-E units provide it with ECL logic. MDSL-0825, MDSL-1035 and MDSL-1250 also utilize this reliable hybrid construction. The use of laser trimmed resistor networks within the D/A's not only eliminates thermal time lag errors but provide the linearity tempco of 2ppm/°C; guaranteeing monotonic operation over the extended temperature range of -30°C to +85°C. The power dissipation of the MDSL series is one-half that of competitive D/A's, but a full 5mA output current is maintained. This allows driving transmission lines or other low impedance loads directly.

SPECIFICATIONS (typical @ +25°C unless otherwise specified)

MODEL	UNITS	CURRENT OUTPUT MDS 0815	MDS 1020	MDS 1240	CURRENT OUTPUT MDS-E (ECL) 0815	MDS-E (ECL) 1020
RESOLUTION	Bits	8	10	12	8	10
LSB (Weight)	μA	58.6	14.6	3.66	58.6	14.6
ACCURACY						
Initial (Adjust to 0)	±%FS	0.2	0.05	0.012	0.2	0.05
Linearity (Integral)	LSB max	±1/2	*	*	*	*
Monotonicity		Guaranteed Over Operating Temp Range			*	*
Zero Offset (Adjust to 0)		15nA max	*	*	*	*
TEMPERATURE COEFFICIENTS						
Linearity	ppm/°C	5	*	2	*	2
Gain	ppm/°C	30	*	20	*	*
Offset (Bipolar)	ppm/°C	15	*	*	*	*
STABILITY WITH TIME	±%/yr max	0.5	*	*	*	*
DATA INPUTS						
Logic Compatability		TTL	*	*	ECL	ECL
Logic Voltage Levels						
Bit On Logic "1"	V	+2 to +5.0	*	*	-0.9	-0.9
Bit Off Logic "0"	V	0 to +0.4	*	*	-1.7	-1.7
Logic Current (Each Bit)						
Bit On Logic "1"	μA	⩽50	*	*	*	*
Bit Off Logic "0"	mA	-8	*	-5 max	*	*
MSB	mA	N/A	*	-10 max	*	*
Coding		All Units Binary (BIN) for Unipolar,			*	*
		Offset Binary (OBN) for Bipolar			*	*
OUTPUT						
Current Range						
Unipolar	mA	0 to +15	*	*	0 to -15	0 to -15
Bipolar	mA	±7.5	*	*	*	*
Impedance (See Figure 3)	Ω	165	*	200 ±1%	*	*
Compliance (MDH V_{OUT})	V	+1.5, -2	*	*	-1.5, +2	-1.5, +2
Load Resistance for V_{OUT} (See Figure 5)						
0 to +1V	Ω	112	*	100	*	*
±1V	Ω	4.32k	*	750	*	*
INTERNAL REFERENCE VOLTAGE OUT	V	N/A	*	-6.2 ±5%	*	*
SETTLING TIME[2]						
Current	ns to %	15 to 0.4[3]	20 to 0.1[3]	20 to 0.1[3] 40 to 0.025	*	20 to 0.1[3]
Unipolar Voltage (R_L = 300Ω ‖ 10pF)	ns to %					
Bipolar Voltage (R_L = 2325Ω ‖ 10pF)	ns to %					
POWER REQUIREMENTS						
Range	V	±11 to ±16	*	±14.5 to ±16.5	*	*
Current at Nominal +V	mA max	105	120	55	*	120
Current at Nominal -V	mA max	15	*	20	*	*
POWER SUPPLY REJECTION RATIO	%/V	0.04	*		*	*
+15V	%/V			-0.0001		
-15V (Bipolar)	%/V			-0.002		
-15V (Unipolar)	%/V			-0.2		
TEMPERATURE RANGE						
Operating	°C	-20 to +75	*	-30 to +85	*	*
Storage	°C	-55 to +85	*	-55 to +125	*	*
CASE		Diallyl Phthalate per MIL-M-14 Type SDG-F			*	*

*Specifications same as MDS-0815.

NOTES:

[1] 1ppm/°C for current output. Op amp is 50μV/°C. (See tables in Figures 15, 16 and 17, for overall TC in various configurations.)

[2] For Full Scale Step, worst case.

[3] For the MDS and MDS-E series, the voltage and current output settling times are the same if the DAC's are operated with a load to give 1V p-p output.

[4] 0 to +5V Out
[5] 0 to +10V Out
[6] ±5V Out

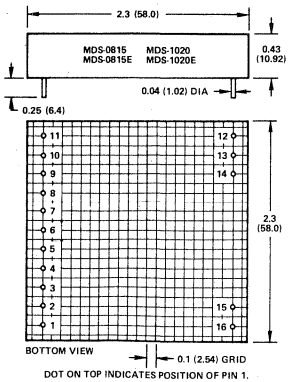
} See Figures 15 and 16 for test circuits.

Specifications subject to change without notice.

CURRENT OUTPUT MDSL			VOLTAGE OUT MDH		
0825	1035	1250	0870	1001	1202
8	10	12	8	10	12
19.6	4.88	1.22	Depends on V_{OUT}		
0.2	0.05	0.012	0.2	0.05	0.012
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	10mV	10mV	10mV
2	2	2	2	2	2
20	20	20	20	20	20
*	*	*	See Note 1		
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
-1.6	-1.6	-1.6	-1.6	-1.6	-1.6
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
0 to +5	0 to +5	0 to +5	±50 max	±50 max	±50 max
±2.5	±2.5	±2.5	±50 max	±50 max	±50 max
600 ±1%	600 ±1%	600 ±1%	0.1 max	0.1 max	0.1 max
*	*	*	±10	±10	±10
300	300	300	N/A	N/A	N/A
2.325k	2.325k	2.325k	N/A	N/A	N/A
-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%
25 to 0.1	25 to 0.1	50 to 0.025	15 to 0.2	25 to 0.10	50 to 0.025
45 to 0.4	70 to 0.1	70 to 0.1	70 to 0.4[4]	100 to 0.1[4]	200 to 0.025[4]
70 to 0.1	80 to 0.05	90 to 0.025	150 to 0.4[5]	200 to 0.1[5]	400 to 0.025[5]
75 to 0.4	100 to 0.1	100 to 0.1	100 to 0.4[6]	130 to 0.1[6]	250 to 0.025[6]
100 to 0.1	110 to 0.05	125 to 0.025			
±12 to ±15	±12 to ±15	±12 to ±15	±14.5 to ±16.5	±14.5 to ±16.5	±14.5 to ±16.5
26	26	26	50	50	50
16	16	16	35	35	35
0.0001	0.0001	0.0001	0.003	0.003	0.003
0.001	0.001	0.001	0.01	0.01	0.01
0.2	0.15	0.15	0.15	0.15	0.15
-30 to +85	-30 to +85	-30 to +85	-30 to +85	-30 to +85	-30 to +85
-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125
*	*	*	*	*	*

MDS-0815, 0815E, 1020, 1020E OUTLINE DIMENSIONS

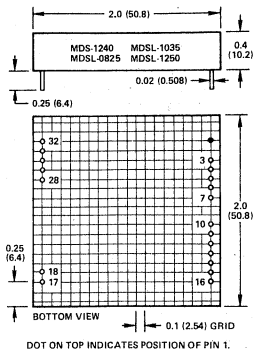
Dimensions shown in inches and (mm).



MATING SOCKET MSB-1

MDS-1240, MDSL-0825, 1035, 1250 OUTLINE DIMENSIONS

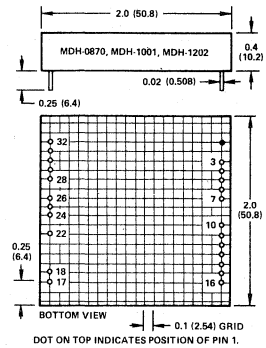
Dimensions shown in inches and (mm).



MATING SOCKET MSA-1

MDH-0870, 1001, 1202 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET MSA-1

PIN DESIGNATIONS MDS-0815E, 1020E

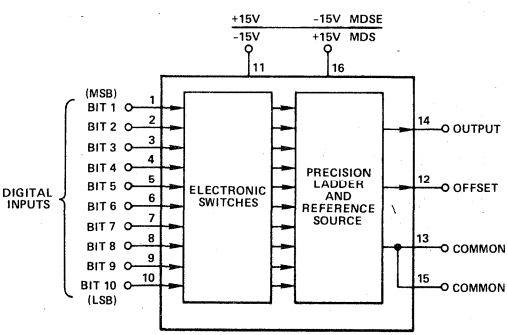
PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	9	BIT 9
2	BIT 2	10	BIT 10
3	BIT 3	11	+15V
4	BIT 4	12	OFFSET
5	BIT 5	13	COMMON
6	BIT 6	14	OUTPUT
7	BIT 7	15	COMMON
8	BIT 8	16	-15V

PIN DESIGNATIONS MDS-0815, MDS-1020

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	9	BIT 9
2	BIT 2	10	BIT 10
3	BIT 3	11	-15V
4	BIT 4	12	OFFSET
5	BIT 5	13	COMMON
6	BIT 6	14	OUTPUT
7	BIT 7	15	COMMON
8	BIT 8	16	+15V

PIN DESIGNATIONS MDS-1240, MDSL-0825, 1035, 1250

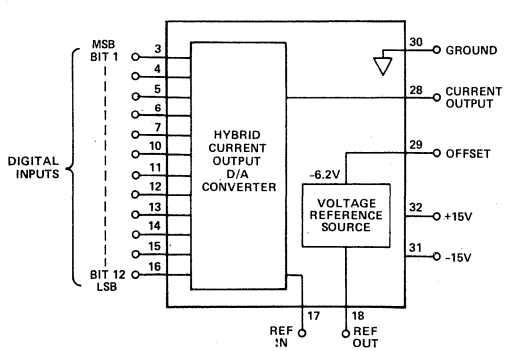
PIN	FUNCTION	PIN	FUNCTION
3	BIT 1 INPUT (MSB)	15	BIT 11 INPUT
4	BIT 2 INPUT	16	BIT 12 INPUT
5	BIT 3 INPUT	17	REFERENCE INPUT
6	BIT 4 INPUT	18	REFERENCE OUTPUT
7	BIT 5 INPUT	28	ANALOG OUTPUT
10	BIT 6 INPUT	29	OFFSET
11	BIT 7 INPUT	30	GROUND
12	BIT 8 INPUT	31	-15V POWER INPUT
13	BIT 9 INPUT	32	+15V POWER INPUT
14	BIT 10 INPUT		



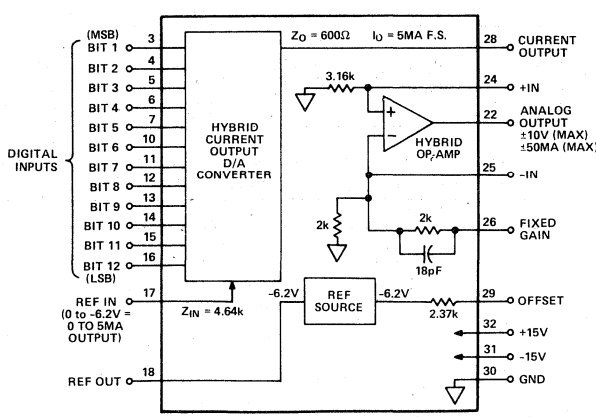
MDS and MDSE Block Diagram

PIN DESIGNATIONS MDH-0870, 1001, 1202

PIN	FUNCTION	PIN	FUNCTION
3	BIT 1 INPUT (MSB)	17	REFERENCE INPUT
4	BIT 2 INPUT	18	REFERENCE OUTPUT
5	BIT 3 INPUT	22	ANALOG OUTPUT
6	BIT 4 INPUT	24	+INPUT
7	BIT 5 INPUT	25	-INPUT
10	BIT 6 INPUT	26	FIXED GAIN
11	BIT 7 INPUT	28	CURRENT OUTPUT
12	BIT 8 INPUT	29	OFFSET
13	BIT 9 INPUT	30	GROUND
14	BIT 10 INPUT	31	-15V POWER INPUT
15	BIT 11 INPUT	32	+15V POWER INPUT
16	BIT 12 INPUT		



MDS-1240 and MDSL Series Block Diagram



MDH Series Block Diagram

Each D/A is housed in industry standard size cases, and each has an internal precision reference. Bipolar operation is achieved by external pin interconnection. In normal circumstances, no external components are required for operation into low impedance loads. Designed primarily for PCB mounting, these D/A's may also be plugged into standard DIL sockets mounted on 1.8″ centers (MDS series 2″ centers).

For ultra-high reliability, this D/A series is optionally available with burn-in extended beyond the Analog Devices standard of 96 hours at +25°C.

NOTES ON FAST-SETTLING D/A CONVERTERS

Invariably, fast-settling D/A converters use current rather than voltage switching.

There are inherent advantages to current-switching converters, since it eliminates an output amplifier. If there is no output amplifier, there is no slew rate limitation which slows settling. The absence of an output amplifier also means there are no overshoot and ringing problems often associated with feedback amplifiers.

The settling time of a current-switching D/A converter, then, is based on:

1. The RC time constant of the converter output.
2. The settling time of the output current change.

If the settling time of the D/A converter under consideration is determined by the RC time constant, the output capacitance and output impedance become very important.

As a typical example in the Analog Devices' D/A converters, output capacitance is 5pF, and nominal output impedance is 165Ω.

For test purposes, the output of these D/A converters are loaded with approximately 150Ω. (There is no "trick" or "gimmick" in loading the output of the converter; it is done to provide an output voltage of approximately 1.0V to 1.2V.) This loading means $RC = 80 \times 5 \times 10^{-12} = 0.4$ns. Since settling time is approximately 7 RC, the overall settling time, if determined by the RC time constant, would be 2.8ns.

Based on this, it becomes obvious the RC time constant of such converters outputs is not the limiting factor in establishing settling time. Instead, the settling time of the converters is based primarily on the settling time of the overall (output) current change, since the effect of the RC time constant is "swamped." Expressed in another way, this means settling time for the MDS series converters is relatively independent of load resistance, unless substantial load capacitance is present. The settling time of the output current, in turn, is based on:

1. The settling time of each switch within the converter.
2. The time skew among the digital inputs which cause the switching action.

Some manufacturers of fast-settling D/A converters spec settling time under the conditions of all digital inputs changing from "0" to "1", or vice versa. At first glance, it would appear this is the "worst case" condition for measuring settling time, since maximum current is being switched.

Unfortunately, this method of specifying neglects an important characteristic of saturated logic... the propagation delay for negative-going inputs is different from the delay for positive-going inputs on all forms of saturated logic. The TTL or DTL driving logic, and the D/A input circuits for current-switching D/A's are subject to this same characteristic.

Thus, the time skew of the individual current switches within the converter is worse when one or more input bits are out of phase with the others. This is true even for ideal inputs in which the digital inputs arrive simultaneously; if there is time skew among the bit inputs, of course, the problem becomes more pronounced.

Note, settling times even better than those specified for the MDS series become possible if digital input bit arrivals are deskewed.

These differences among the switches cause a discontinuity or "glitch" in the output. The true "worst case" glitch always occurs at the switching point of the Most Significant Bit or the center point of the output range, because nearly equal and opposite currents are being switched within the converter.

In addition, all "0" to all "1" switching overlooks the practical aspects involved. There are relatively few times when all of the input bits will be changing from one state to the other on successive input changes; however, the MSB will switch out of phase with all other bits each time the analog output of the converter crosses the midpoint.

In considering the choice of a "fast-settling" D/A converter, then, the user should look for the following points in the data sheet:

1. If the settling time spec has all bits changing state identically, it neglects the phenomenon associated with saturated logic discussed earlier.
2. Is the settling time specified with an impractically-low-impedance load?

If the RC time constant of the converter output is the major factor in establishing settling time (because of high output capacitance and/or resistance), a low impedance load helps make settling time look better.

A low impedance load means the voltage being developed at the output is oftentimes too small to be useful.

A higher-impedance load which can develop a useable output of 1.0V or more sometimes negates the fast settling time of the spec sheet.

A test setup for this worst-case measurement is shown in Figure 1. Two pulse generators are used to generate the required out-of-phase pulses, and the delays are adjusted for minimum skew. Figure 2 is an unretouched photo of the oscilloscope trace of an MDS-815 under test.

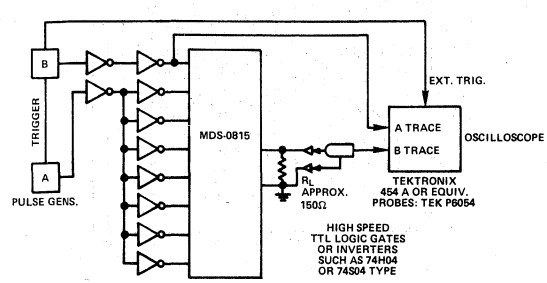


Figure 1.

ANALOG OUTPUT BIPOLAR, NONINVERTING	OFFSET BINARY	ANALOG OUTPUT UNIPOLAR, NONINVERTING	STRAIGHT BINARY
+FS, -1LSB	111.....1	+FS, -1LSB	111.....1
+1/2 FS	110.....0	+3/4 FS	110.....0
0	100.....0	+1/2 FS	100.....0
-1/2 FS	010.....0	+1/4 FS	010.....0
-FS	000.....0	0	000.....0

Table 2. Input Coding

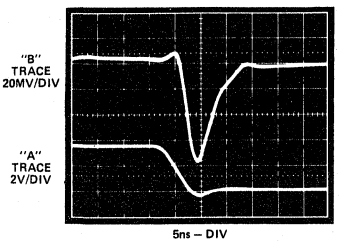


Figure 2.

INTERNAL CURRENT DAC CHARACTERISTICS

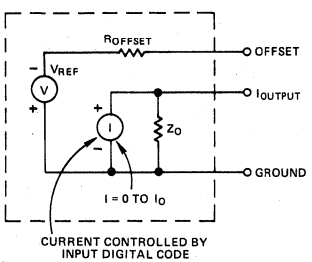


Figure 3. Current Equivalent Circuit

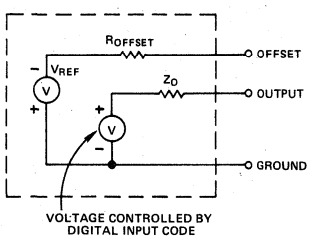


Figure 4. Voltage Equivalent Circuit

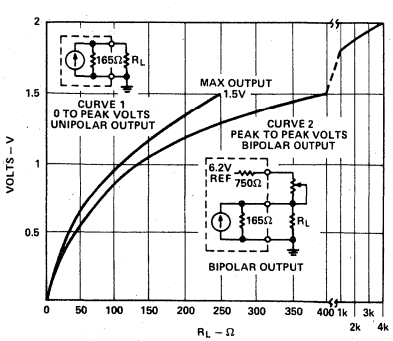


Figure 5. V_{OUT} vs. Load Resistance MDS-0815, -1020

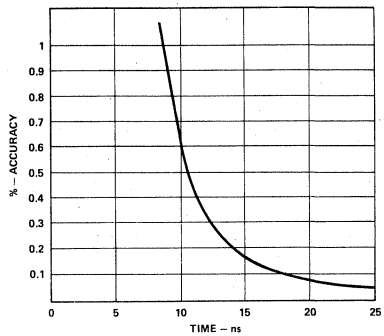


Figure 6. Accuracy vs. Time – MDS and MDSE

BASIC CONNECTIONS AND CALIBRATIONS

MDS/MDSE-0815, 1020

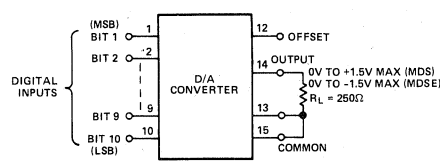


Figure 7. Unipolar Output Current

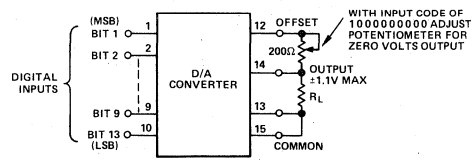
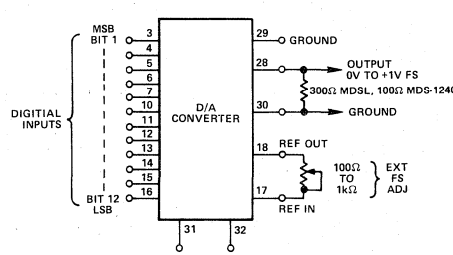


Figure 8. Bipolar Output Current

MDS-1240, MDSL-0825, 1035, 1250



The 100Ω POTENTIOMETER MAY BE OMITTED IF ABSOLUTE ACCURACY OF FULL SCALE IS NOT REQUIRED. IN THIS CASE PINS 17 AND 18 SHOULD BE SHORTED AND THE FULL SCALE CURRENT WILL BE 5.1mA ±5%. (MDS-1240, 10.2mA ±5%)

Figure 9. Unipolar Current Output

(MDS-1240, MDSL-0825, 1035, 1250 continued)

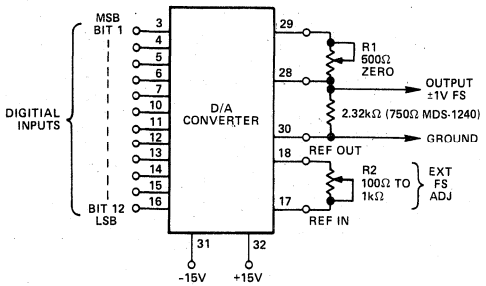


Figure 10. Bipolar Current Output

VOLTAGE OUTPUT
MDS/MDSE-815, 1040

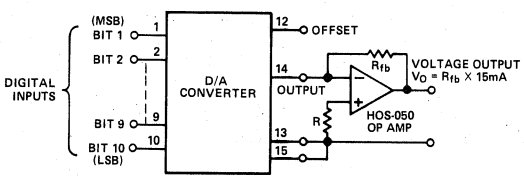


Figure 11. Voltage Output

MDS-1240, MDSL (all)

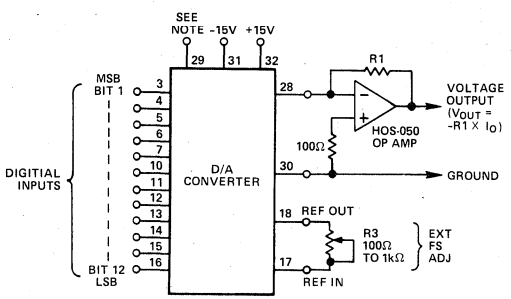


Figure 12. Inverting Unipolar or Bipolar Voltage Output

MDSL

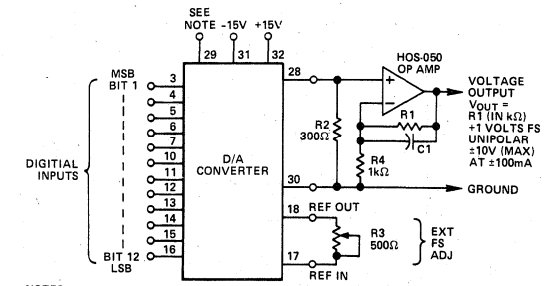


Figure 13. Noninverting Unipolar or Bipolar Voltage Output

APPLICATIONS

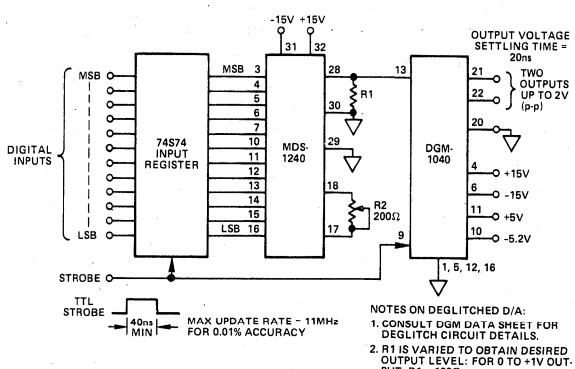
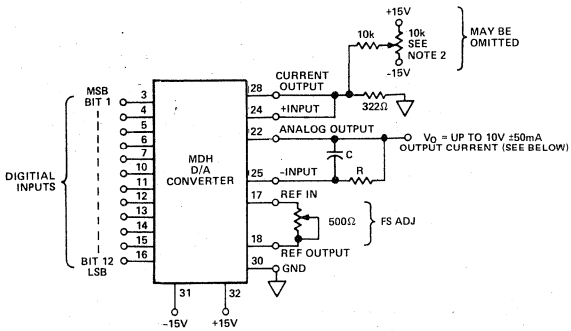


Figure 14. Ultra High-Speed Deglitched D/A

MDH SERIES APPLICATIONS

By using external feedback resistor and capacitor as shown in Figures 15 and 16, other full scale output ranges from 2V to 10V may be obtained.

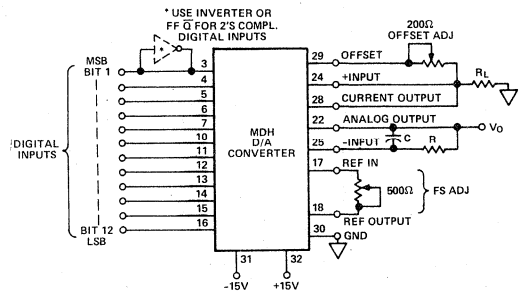


NOTES:

1. VALUE OF C IS APPROXIMATE. A FIXED CAPACITOR WITH TOLERANCE OF ±1pF MAY BE USED IF 50% DEGRADATION OF SETTLING TIME IS PERMITTED. IF SETTLING TIME IS TO BE OPTIMIZED, AN ADJUSTABLE CAPACITOR SHOULD BE USED FOR C AND ADJUSTED FOR MINIMUM SETTLING TIME.
2. OFFSET NULLING MAY BE ACCOMPLISHED BY CONNECTING A 10k POTENTIOMETER BETWEEN +15V AND -15V, AND CONNECTING ITS ADJUSTABLE TAP TO A 10k RESISTOR. THE OTHER END OF THE RESISTOR IS CONNECTED TO PIN 28. TYPICAL UNCOMPENSATED OFFSET IS 1% OF FULL SCALE.

VOLTAGE OUTPUT	SETTLING TIME	OFFSET TEMPCO	R	C
0 to +2V	70ns	100μV/°C	2k	10pF
0 to +5V	100ns	250μV/°C	8k	2pF
0 to +10V	200ns	500μV/°C	18k	0.5pF

Figure 15. Binary Coding Unipolar Output Configuration



NOTES:

1. The 200Ω POTENTIOMETER IS ADJUSTED FOR AN CUTPUT OF -FS WITH ALL ZEROES IN THE DIGITAL INPUT.
2. THE 500Ω POTENTIOMETER IS ADJUSTED FOR AN OUTPUT OF +FS-1LSB WITH ALL ONE'S IN THE DIGITAL INPUT.
3. FOR TWO'S COMPLEMENT (2SC) OPERATION, AN EXTERNAL INVERTER MUST BE USED TO COMPLEMENT BIT 1 (MSB).
4. AN ADJUSTABLE CAPACITOR MAY BE USED FOR C AND ADJUSTED TO OPTIMIZE SETTLING TIME.

VOLTAGE OUTPUT	SETTLING TIME	OFFSET TEMPCO	R_L	C	R
±1V	70ns	100μV/°C	383	10pF	2k
±2V	100ns	200μV/°C	383	2pF	6k
±5V	100ns	250μV/°C	9.1k	2pF	8k
±10V	200ns	500μV/°C	9.1k	0.5pF	18k

Figure 16. Offset Binary Coding or 2's Comp Coding Bipolar Output Configuration

Analog-to-Digital Converters

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AD572 Complete Hybrid IC 12-Bit Successive-Approximation ADCs	10–27
AD574 Complete IC 12-Bit A/D Converters with μP Interface	10–35
AD578● Fast Complete Hybrid IC 12-Bit ADCs	10–43
AD5200● Hybrid IC 12-Bit Successive-Approximation ADCs	10–45
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AD7555● CMOS IC 4 1/2-Digit 20,000-Count ADC Subsystem	10–57
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AD7574● CMOS Microprocessor-Compatible 8-Bit ADCs	10–81
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MOD-1205● 12-Bit 5MHz Video ADC with Built-In Track-Hold	10–137

●New product since the 1979 *Data Acquisition Products Catalog Supplement*.

Selection Guide
Analog-to-Digital Converters

The A/D converter families catalogued in this section are divided into seven overlapping categories:

1. General Purpose, Low Cost
2. High Performance (Speed and Accuracy)
3. High Speed
4. High Resolution
5. Low Power
6. Bus Compatible (3-State Outputs)
7. Multichannel

The specifications and features are key for each device. Complete and detailed descriptions, specifications, and application information can be found in the data sheets. General information and definitions of important specifications can be found in the pages that follow.

In general, the devices catalogued here by generic type number are available in various performance and temperature grades, and packages, as specified on the data sheets. All specifications are typical at rated supply voltage and $T_A = +25^\circ C$, unless noted otherwise. Devices are listed generally in order of resolution.

1. GENERAL PURPOSE, LOW COST

Model	Resolution (Bits)	Features	Page
AD570#	8	Monolithic IC, complete with reference, 3-state output, 25μs	10-11
AD7574●	8	CMOS IC, Interfaces to μP like RAM, ROM, or slow memory; ratiometric, single supply, 15μs conversion time	10-81
AD7570#	10, 8	CMOS IC, no missing codes, ratiometric, μP-compatible	10-69
AD571#	10	Monolithic IC, complete, 3-state output, 25μs	10-19
AD574	12	IC, complete, μP interface, 25μs conversion time	10-35
AD ADC80	12, 10	Hybrid IC, complete, improved replacement for standard ADC80	10-97
AD5200●	12	Hybrid IC, complete, improved replacement for standard 5200 series	10-45

2. HIGH PERFORMANCE (SPEED AND ACCURACY)

Model	Resolution (Bits)	Features	Page
MOD-1205●	12	Complete PC-board unit, 5MHz word rate, includes track-hold with 25ps aperture uncertainty, SNR>66dB	10-137
HAS-1202	12	Hybrid, 2.8μs conversion time, no missing codes over temperature	10-109
AD578●	12	Hybrid IC, conversion time adjustable to 4μs min (K, S), internal reference, no missing codes over temperature	10-43
AD574	12	IC, complete, including reference, μP interface, 25μs conversion time	10-35
AD572	12	Hybrid IC, 25μs max conversion time, no missing codes over temperature	10-27
ADC1131	14	Module, 12μs max conversion time	10-105
ADC1130	14	Module, 25μs max conversion time	10-105

3. HIGH SPEED

Model	Resolution (Bits)	Features	Page
MATV	8	Module, up to 20MHz word rate, includes track-and-hold (30ps aperture time)	10-123
MOD-1005	10	Complete PC-board unit, 5MHz word rate, includes track-hold with 25ps aperture, 20MHz analog input bandwidth	10-129
MOD-1020●	10	Complete PC-board unit, 20MHz word rate, includes track-hold with 25ps aperture uncertainty, SNR>56dB	10-133
MAH●	10, 8	Module, max conversion time 1μs/750ns to 10/8 bits, parallel and serial outputs, pin and function compatible with 4130, 4131	10-113
MOD-1205●	12	Complete PC-board unit, 5MHz word rate, includes track-hold with 25ps aperture uncertainty, SNR>66dB	10-137
AD578●	12	Hybrid IC, conversion time adjustable to 4μs (K, S), internal reference, no missing codes over temperature	10-43
HAS	12, 10, 8	Hybrid, 2.8/1.7/1.5μs conversion time, no missing codes over temperature	10-109
MAS	12, 10, 8	Module, 2/1.5/1μs max conversion time, parallel and serial outputs	10-117
ADC1131	14	Module, 12μs max conversion time	10-105

4. HIGH RESOLUTION

Model	Resolution (Bits)	Features	Page
AD7555●	4 1/2BCD 20,000 counts	CMOS IC: analog switching and all digital functions for quad-slope conversion, data formats include multiplexed BCD and serial count	10-57
ADC1130/31	14	Module, 25/12μs conversion time	10-105
AD7550#	13	CMOS IC, quad slope, 1ppm/°C gain and offset tempco	10-49

5. LOW POWER, CMOS

Model	Resolution (Bits)	Features	Page
AD7555●	4 1/2BCD	CMOS IC, analog switching and all digital functions for quad-slope conversion, data formats include multiplexed BCD and serial count (to 20,000)	10-57
AD7550#	13	CMOS IC, quad slope, 1ppm/°C gain and offset tempco	10-49
AD7570#	10	CMOS IC, no missing codes, ratiometric, μP-compatible	10-69
AD7574●	8	CMOS IC, 15μs conversion time, interfaces to μP like RAM, ROM, or slow memory; single-supply, ratiometric	10-81
AD7583●	8	CMOS IC, 9-channel (expandable), single supply, analog multiplexing and all digital functions for quad slope conversion and digital control, interface via I/O port	10-89

6. BUS COMPATIBLE (3-STATE OUTPUTS)

Model	Resolution (Bits)	Features	Page
AD7555●	4 1/2BCD	CMOS IC, analog switching and all digital functions for quad-slope conversion, data formats include multiplexed BCD and serial count (to 20,000)	10-57
AD7550#	13	CMOS IC, quad slope, 1ppm/°C gain and offset tempco	10-49
AD574	12	IC, complete, 2-chip, microprocessor interface, 25μs conversion time	10-35
AD7570#	10	CMOS IC, no missing codes, ratiometric, μP-compatible	10-69
AD571#	10	Monolithic IC, complete, pretrimmed, 3-state output	10-19
AD7583●	8	CMOS IC, 9-channel (expandable), single supply, analog multiplexing and all digital functions for quad-slope conversion and digital control, interface via I/O port	10-89
AD7574●	8	CMOS IC, 15μs conversion time, interfaces to μP like RAM, ROM, or slow memory; single-supply, ratiometric	10-81
AD570#	8	Monolithic IC, complete with reference, pretrimmed, 3-state output	10-11

7. MULTICHANNEL

Model	Resolution (Bits)	Features	Page
AD7583●	8	CMOS IC, 9-channel (expandable), single supply, analog multiplexing and all digital functions for quad-slope conversion and digital control, interface via I/O port	10-89

#Monolithic chips available with guaranteed performance for precision hybrids; information available upon request. All can be found in the 1979 Chip Catalog, available upon request.
●New product since the 1979 *Data Acquisition Products Catalog Supplement*.

Orientation
Analog-to-Digital Converters

FACTORS IN CHOOSING AN A/D CONVERTER

In the current issue of this catalog, there are listed some 19 different families of analog-to-digital converters (ADCs). If one were to consider all the variations, there would be considerably more than 40 different types to choose among (excluding digital panel meters, which are catalogued elsewhere). The reason for so many different types is the number of degrees of freedom in selection—technological, functional, performance, and package. Complete information on converters may be found in the 246-page book, *Analog-Digital Conversion Notes*, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood, MA 02062.

TECHNOLOGICAL FACTORS

The technologies represented here include modules (cards and potted circuits) and integrated circuits—monolithic and hybrid. Modules generally can provide the extremes of performance as well as arbitrary levels of functional completeness. For example, the 12-bit 5MHz MOD-1205 is built on a card that includes a track-hold amplifier. ICs are small and high in performance-per-dollar. Though some IC devices require external components for operation, an increasing number are complete in the package (and even on the chip—for example, the AD571 10-bit ADC is a one-chip complete converter with its own reference).

The three most important IC technologies in current use at Analog Devices are hybrid, thin-film-on-CMOS, and thin-film-on-bipolar. *Hybrid* provides the most-complete high-performance devices; for example, the HAS series are completely self-contained 12-bit successive-approximations ADCs, with internal reference and conversion time to 2.8μs max for 12 bits. *CMOS* provides high-density logic, low dissipation, and good voltage switches, but relatively limited-performance linear circuitry. The AD7574 is a complete 8-bit ratiometric successive-approximation converter on a chip that is designed for direct interfacing to microprocessors as ROM, RAM or slow memory. Another example of *CMOS* is the 13-bit "quad-slope" AD7550, a ratiometric integrating type that utilizes a patented digital error-correction scheme to obtain 1ppm/°C performance, despite the use of on-chip CMOS for both comparator and integrating amplifier. Analog Devices monolithic bipolar technology is the key to the performance and versatility of the AD570, AD571 and AD574. They use Integrated Injection Logic (I^2L), with its high logic density, and high accuracy analog circuitry, including buried-Zener references and laser-wafer-trimmed thin-film resistors, all on single monolithic chips. The A/D converter in the low-cost AD2040 Digital Thermometer is another example of the application of I^2L to monolithic bipolar ICs.

FUNCTIONAL CHARACTERISTICS

Block diagrams illustrating the various conversion techniques appear on individual data sheets.

The moderate-speed converters described in this catalog (<1MHz) employ two fundamental techniques—*successive approximations*, for moderate-to-high resolution at moderate-to-high speed, and *integration*, for high resolution at modest speeds. The AD ADC80 and ADC1131 are examples of the former, the AD7550 and AD7583, the latter.

Like a chemist's balance with binary weights (1/2, 1/4, 1/8, etc.), the *successive-approximation* converter compares the unknown input with sums of accurately-known binary fractions of full scale, starting with the largest (2^{-1}), and rejecting any that change the comparator's state ("tip the scale"). At the end of conversion (EOC), the output of the converter is a digital word, representing the ratio of the input to full scale by a fractional-binary code.

Integrating types count pulses for a period proportional to the input. Most-frequently used are *dual slope* types, which count off the period required for the integral of the reference to become equal to the average value of the input (over a fixed period). Integrating types can be made insensitive to drift by storing errors during an error-correcting cycle and subtracting them during the input-measuring cycle. This correction can be performed in analog fashion, using capacitance for storage, or digitally—using the information stored in a counter for correction (AD7550).

The video converters described here (MATV, MOD-1205, etc.) employ two basic encoding techniques: simultaneous, or *flash* conversion, and serial-Gray-Code conversion. High resolution and high speed are obtained by *subranging*, i.e., by performing an n-bit conversion in two steps; Analog Devices has perfected a form of subranging, known as DSC—*digitally corrected subranging*—which permits accurate resolutions of 12 bits and more.*

In *flash* conversion, the analog signal is compared against $2^n - 1$ graded voltage levels, using as many comparators, and the comparator output logic levels are processed by a priority encoder, which converts the "thermometer" output to a binary (or Gray) code. Since the whole conversion occurs essentially simultaneously, it is the fastest means of conversion, but it requires many accurate comparators and large numbers of gates.

In *serial*-analog-parallel-digital conversion, there are a number of cascaded stages, each having a gain of +2 for signals less than one-half the reference, and a gain of −2 for signals between one-half the reference and full scale. At each stage, a decision is made as to whether the signal is larger (1) or smaller (0) than one-half the reference; the stage's analog output becomes the input to the next stage. The complete time for one conversion is determined by the propagation delay of the analog signal through all stages; however, since the decision of each stage can be latched as soon as the stage has settled (and a new conversion can, in principle, be started as soon as the first bit has been latched), the rate at which conversions come out of the pipeline is considerably faster than the time for one sample to go through the conversion process. Though fast, this process is difficult to implement accurately

*A considerable amount of useful information about the differences between video conversion and moderate-speed conversion can be found in the article, "Very High Speed Data Acquisition," by Ed Graves, in *Analog Dialogue* 13-2, available upon request.

for more than a few bits, because of the compounding of gain (hence errors).

A *subranging* converter digitizes to a group of more-significant bits, and stores them in a latch. A fast, very-high-accuracy D/A converter converts them to an analog signal, which is then subtracted from the input. The difference, or residue, is amplified and digitized, and (in DCS) the result is combined digitally in such a way as to correct for mid-scale conversion errors.

Whatever the technique, these A/D converters comprise several essential functions: an analog section, a digital data-generating section, data outputs, and digital controls.

Analog Section

This section requires a reference, one or more high-gain comparators, and either a D/A converter (successive approximations) or a controllable integrator. The reference may be internal or external, fixed or variable, and of a specified polarity/sense in relation to the analog input. In ratiometric conversion, the reference is usually external and variable. For conversion with the AD7570, the comparator is connected externally.

In successive-approximation converters, the comparator is generally used in the *current-summing* mode; that is, the current output of the DAC is summed with the current developed in the DAC's "feedback resistor" by the input voltage (of opposite polarity), and the balancing action of the converter tends to bring the summing junction towards a voltage null (much like that of an op amp) at the end of conversion. The typical DAC feedback options, when applied in an ADC, provide input-scaling choices. When the bipolar-offset connection is jumpered to the summing point, input signals of both polarities can be handled. The current-switching action of the DAC, at the typically fast clock-rates used in successive-approximation converters, can disturb the output of the analog signal source, especially if it is a slow high-precision op amp. In such cases, buffering may be necessary; many of the modules, *and the AD572 IC,* have on-board analog buffer-followers.

In integrating types, absolute-value and polarity-sensing circuitry may be required at the front end to handle both polarities of input. Outputs are usually sign-magnitude BCD. However, the AD7550, which uses an offset-reference scheme, requires none of the above; and it has a two's-complement binary output. The AD7583 and AD7555 provide the quad-slope control logic, counters, and analog switching, but require external integrators and comparators.

Digital Data-Generating Section

In successive-approximation types, this section consists of a discrete or integrated successive-approximations register (SAR), its controls, and inputs from the comparator and clock (which is on-board, but in many cases permits external clock pulses, frequency adjustment, and/or control). In integrating types, this section consists of the clock-pulse generator, the counter(s), the input from the comparator, and the associated controls. Often, provisions are made for the pulse-train to be jumpered to the counter externally, so that the pulse train can be operated on externally, or can transmit its train of pulses to a remote counter. In a few types there are no on-board counters or registers; the pulse train, magnitude, overrange, and control terminals are intended to communicate with external counters and registers.

Data Outputs

Factors to consider here include coding, resolution, overrange information, levels, format, validity, and timing. *Coding* is usually binary, including jumper-connected offset-binary and/or two's complement for bipolar input signals. For some types, BCD is available, with sign-magnitude for bipolar inputs. Output coding specs should always be checked for digital polarity (positive- or negative-true) of both magnitude and sign information. The *resolution* (number of output bits) must be sufficient for the application; in addition, the specifications must be checked to ascertain that not only will all 2^n (binary) output codes be present (no missing codes), but they must all be present at any temperature in the operating range and related to the input with sufficient accuracy. Integrating types generally have no problems with missing codes (except sometimes at zero, with sign-magnitude coding); nevertheless, nonlinear integration can cause the conversion relationship to become nonlinear. Successive-approximation types have no way of determining *overrange;* they simply fill up. However, counter types roll over and put out a carry flag to signal overrange.

The *data levels* available at the converter output must be checked (TTL, low-voltage CMOS, high-voltage CMOS, ECL), as must the load-driving capability and fanout, and the supply conditions under which appropriate output levels will be furnished. The available choice of output *formats* must also be as desired—parallel, serial, byte-serial, and/or pulse-train. If the converter is intended to communicate directly with an 8-bit data bus, the output should have three-state capability, and parallel outputs must be enabled in bytes of 8 or fewer lines (AD7570, AD7550). If the output is serial, it is usually NRZ (non-return-to-zero) and should be accompanied by a set of synchronized clock-pulses.

A *status* (or *busy* or *EOC*) output changes state to indicate when the data becomes *valid.* The exact nature of this transition should be specified—polarity, timing, levels, etc. For serial data, the exact relationship between the data and the synchronizing clock should be specified, to indicate when each bit becomes valid, and for how long. In general, the *timing* of the whole conversion process must be clearly understood, especially if high speeds are necessary, either for conversion, or for communication with a processor (or both). The timing diagrams on specification sheets are usually accompanied by adequate descriptions of the conversion process and specifications of the critical interface parameters.

Controls

The functions, action (levels or edges), polarity, and timing of all control inputs and outputs should be clearly understood, as well as their loading characteristics and dependence on the supply. In addition to the essential *start-conversion-command* input and a *status* output, various control commands may be available, such as *clock inhibit, high (low)-byte enable, status*

enable, and—for speeding up conversion at the cost of resolution in successive-approximation converters—*short-cycle.*

Power Supplies

Appropriate power supplies should be made available, considering the logic levels and analog input signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specifications should be provided. Any recommended external protection circuitry (e.g., Schottky diodes to ensure that V_{CC} is never more than 0.4V above V_{DD} in the AD7570) should be planned for. In many cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

Application Checklist

The designer will generally require specific information in the following categories, before proceeding to the selection process:

- Accurate description of input and output
  1. analog signal range and source or load impedance
  2. digital code needed — binary, offset binary, 2's complement, BCD, etc.
  3. logic level system, i.e., TTL/DTL compatible
- What is the needed data throughput rate?
- What are the control interface details?
- What does the system error budget allow for the converter?
- What are environmental conditions — temperature range, time, supply voltage — over which the converter should operate to the desired accuracy?

For A/D converters, the following considerations are typical.

- What is the analog input voltage range, and to what resolution must the signal be measured?
- What is the requirement for linearity error (or relative accuracy error)?
- To what extent must the various sources of error be minimized as environmental temperature changes?
- How much time can be allowed in the system for each complete conversion? What aperture uncertainty and acquisition time are needed for the sample-hold?
- How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- Can the system tolerate missed codes under any conditions?
- What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? Is aliasing a potential problem?

SPECIFICATIONS & TERMS

Definitions of performance specifications, and related information, are to be found on the following pages, in alphabetical order.*

Accuracy, Absolute

The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see Quantizing Uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts (±1.2mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997V to 4.999V will produce that code will have absolute error of 1/2(4.997 + 4.999) − 5 volts = −2mV.

Absolute error comprises gain error, zero error, and nonlinearity, together with noise, Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative

Relative accuracy error, expressed in %, ppm, or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Accuracy, Absolute).

Aperture Time

This is the interval between the application of the *hold* command to a sample/track-hold and the actual opening of the switch. The aperture time consists of a delay (which depends on the logic and the switching device—50ns for SHA1144) and an uncertainty (due to jitter—20ps max rms for HTS-0025). When a sample-hold is used in an application where timing is critical, the timing of the hold command can be advanced to compensate for the known component of aperture delay. The jitter, however, imposes the ultimate limitation on timing accuracy. When a sample-hold is used with an ADC, the timing

*For video converters, there are a number of additional application-oriented specifications pertaining to the device's use in a system (e.g., *noise power ratio*, *differential phase*, *differential gain*, *signal-to-noise ratio*). Some useful references for understanding such specifications can be found in the following publications, available from Analog Devices:

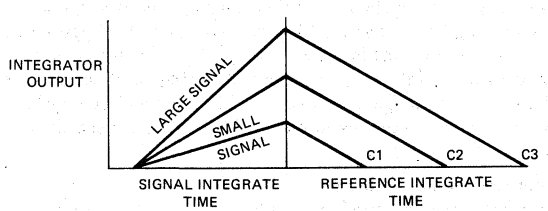
Kester, W.A., "PCM Signal Codecs for Video Applications", *SMPTE Journal*, Volume 88, November 1979, pp 770-778.
Pratt, W.J., "Test A/D Converters Digitally", *Electronic Design*, December 6, 1975
Smith, B.F. and Pratt, W.J., "Understanding High-Speed A/D Converter Specifications", Computer Labs, 1974

uncertainty of the conversion process is reduced by the ratio of aperture jitter to the conversion time, i.e., the maximum frequency which can be handled with less than 1LSB error due to timing is $2^{-n}/(\pi \tau_{au})$ instead of $2^{-n}/(\pi \tau_c)$, where τ_{au} is the aperture uncertainty and τ_c is the conversion time.

Common Mode Rejection (CMR)
The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as through it were a differential signal of one microvolt at the input.

Conversion Time and Conversion Rate
The time required for a complete measurement by an ADC is called *conversion time*. For most converters (assuming no significant additional systemic delays), this is identical to the inverse of *conversion rate*. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined; thus, for example, the MOD-1205 can provide 12-bit output data at a 5MHz word rate (200ns/conversion), even though the time for any one conversion, from start to finish, is two clock periods plus 275ns, or 675ns, at 5MHz.

Dual-Slope Converter
An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time-interval meter (i.e., counter) is generally used as the output indicator.



Feedthrough
Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplexer. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

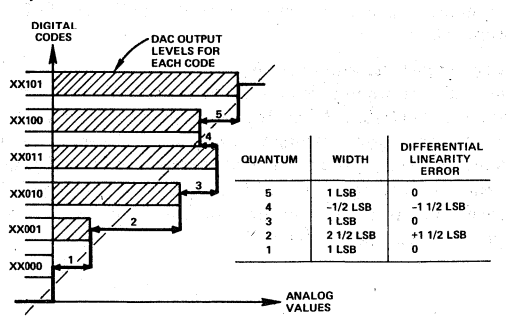
"Flash" Converter
A converter in which all the bit choices are made at the same time. It requires $2^n - 1$ voltage-divider taps and comparators, and a comparable amount of priority encoding logic. An extremely fast scheme, it requires large numbers of precision components. Flash converters are often used for partial conversions in *subranging converters*.

Gain Adjustment
The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g., 10V full scale, in a fixed-reference converter, or 100% of full-scale in a ratiometric converter. Gain- and zero-adjustment principles are discussed under *zero*.

Least Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest change that can be resolved by an n-bit converter.

Linearity Error
Linearity error of a converter, expressed in percent or parts-per-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative). Linearity has two components—*differential* and *integral* nonlinearity.

Linearity, Differential and Integral
A digital output code should correspond to a quantum of analog input values exactly 1 LSB in width (2^{-n} of full scale, for an n-bit converter). Any deviation of the measured "step" from the ideal width is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1 LSB can lead to nonmonotonic behavior of of a D/A converter, and missed codes in an A/D converter employing such a DAC. A flagrant example of differential nonlinearity is shown here.



QUANTUM	WIDTH	DIFFERENTIAL LINEARITY ERROR
5	1 LSB	0
4	-1/2 LSB	-1 1/2 LSB
3	1 LSB	0
2	2 1/2 LSB	+1 1/2 LSB
1	1 LSB	0

In the illustration, the horizontal bars represent the measured DAC output values corresponding to 6 adjacent digital codes. The DAC is nonlinear, in that the next-least-significant bit (XX010) is 1½ LSB too large. Thus, instead of the five quanta, or steps, being all equal (= 1 LSB), quantum 2 is 2½ LSB and quantum 4 is -½ LSB. The differential linearity error, the difference between the actual quantum width and the ideal 1 LSB, is +1½ LSB for quantum 2 and -1½ LSB for quantum 4.

When this DAC is used in successive-approximations conversion, it will lead to a missed code. Analog inputs slightly larger than the value of XX100 will be converted to XX100, and analog inputs slightly less than the value of XX100 will be converted to XX010. The code XX011 will not exist; it will be a *missed code.*

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missed codes", which implies a differential nonlinearity less than 1 LSB.

While differential nonlinearity deals with errors in step size, *integral nonlinearity* has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential linearity errors (e.g., integrating types) have integral linearity (sometimes just "linearity") errors.

Power-Supply Sensitivity
The sensitivity of a converter to dc changes in power-supply voltages is normally expressed in terms of percentage change in analog input value (or fractions of the analog equivalent of 1 LSB), corresponding to a given code, for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power-supply sensitivity may also be expressed in relation to a specified dc shift of the supply voltage. High-accuracy ADCs intended for battery operation require excellent rejection of large supply-variations.

Quad-Slope Converter
This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit single-chip AD7550 is a CMOS quad-slope A/D converter with typical tempcos (gain and zero temperature coefficients) of 1ppm/°C.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±½ LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as "±1 count."

Ratiometric Converter
The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation. Ratiometric conversion can also serve as a substitute for analog signal division (where the denominator changes but little during the conversion).

Stability
Stability of a converter, usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see "Temperature Coefficients").

Subranging Converters
In this type of converter, an extremely fast conversion produces the most-significant portion of the output word. This portion is converted back to analog with a fast high-accuracy D/A converter and subtracted from the input. The resulting residue is converted to digital at high speed and combined with the results of the earlier conversion to form the output word. In *digitally corrected subranging* (DCS), the two bytes are combined in a manner that corrects for the error of the LSB of the most-significant byte. For example, using 8-bit and 5-bit conversion, and this proprietary technique, a full-accuracy high-speed 12-bit converter can be built.

Successive Approximations
Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining on the scale will be within one LSB of the actual weight (±½ LSB, if the scale is properly biased – see *zero*).

Temperature Coefficients
In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero.* The last three are expressed in % or ppm of full-scale range per Celsius degree.

Gain Tempco: Two factors principally affect converter gain instability with temperature:

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is typically 5ppm/°C.
b) The ratiometric circuitry has a sensitivity to temperature.

Linearity Tempco: Sensitivity of linearity to temperature over the specified range. To avoid missed codes, it is sufficient that the differential nonlinearity error be less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a specified temperature range, and/or implied by a statement that there are no missed codes when operating within a specified temperature range.

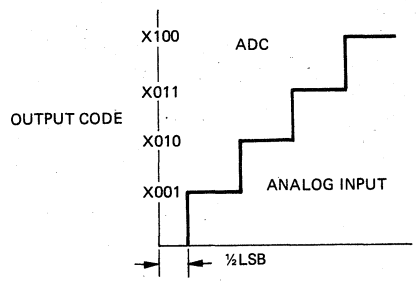
Offset Tempco The temperature coefficient of the all-DAC-switches-off (minus full-scale) point, of a bipolar successive-approximations converter, is dependent on three variables:

1) The tempco of the reference source
2) The voltage stability of the input buffer and the comparator
3) The tracking capability of the bipolar-offset resistors and the gain resistors.

Unipolar Zero The zero tempco of an ADC is dependent only on the zero stability of the integrator and/or the input buffer and the comparator. It may be expressed in $\mu V/^{\circ}C$, or in percent or ppm of full-scale per degree C.

Zero- and Gain-Adjustment Principles

The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $\frac{1}{2} \times 2^{-n}$ of nominal full-scale. The gain is set for the final transition



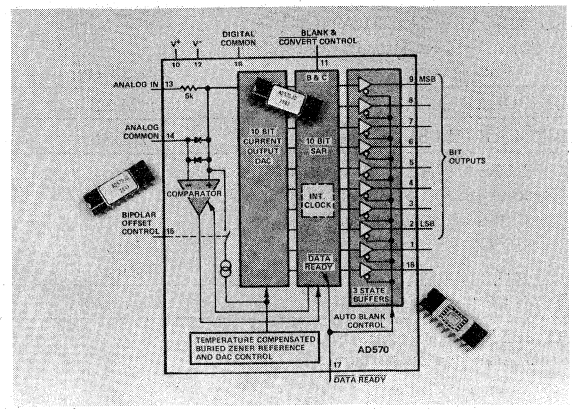
to all-bits-on to occur at F.S. $(1 - \frac{3}{2} \times 2^{-n})$. The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at -F.S. $(1 - 2^{-n})$ and the last transition at +F.S. $(1 - 3 \times 2^{-n})$. The data sheet instructions should be followed.

Low Cost, Complete IC 8-Bit A to D Converter

AD570*

FEATURES

- Complete A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion – 25μs
- No Missing Codes Over Temperature
  - 0 to +70°C – AD570J
  - -55°C to +125°C – AD570S
- Digital Multiplexing – 3 State Outputs
- 18-Pin Ceramic DIP
- Low Cost Monolithic Construction



PRODUCT DESCRIPTION

The AD570 is an 8-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 25μs.

The AD570 incorporates the most advanced integrated circuit design and processing technology available today. I^2L (integrated injection logic) processing in the fabrication of the SAR function along with laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) and a temperature compensated, subsurface Zener reference insures full 8-bit accuracy at low cost.

Operating on supplies of +5V and -15V, the AD570 will accept analog inputs of 0 to +10V unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD570 executes a true 8-bit conversion with no missing codes in approximately 25μs.

The AD570 is available in two versions; the AD570J is specified for the 0 to 70°C temperature range, the AD570S for -55°C to +125°C. Both guarantee full 8-bit accuracy and no missing codes over their respective temperature ranges and are packaged in 18-pin hermetically-sealed ceramic DIP's.

*Covered by Patent No. 3,940,760, other patents pending.

PRODUCT HIGHLIGHTS

1. The AD570 is a complete 8-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.8% (2LSB of 8 bits) is achieved without external trims.
2. The AD570 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD570 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V supplies. The device will also operate with a -12V supply.
6. The AD570S is also available with full processing to MIL-STD-883, Class B. The single chip construction and functional completeness make the AD570 especially attractive for high reliability applications.
7. Every AD570 is subjected to long-term stabilization bakes and given a powered burn-in at +125°C prior to final test to ensure reliability and long-term stability. In addition, all units are tested 100% at the extremes of their respective temperature ranges for all parameters to guarantee full performance.

SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD570JD	AD570SD/AD570SD-883B[1]
RESOLUTION[2]	8 Bits	*
RELATIVE ACCURACY @ 25°C[2,3,4]	±1/2LSB max	*
T_{min} to T_{max}	±1/2LSB max	*
FULL SCALE CALIBRATION[4,5] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	*
UNIPOLAR OFFSET (max)[4]	±1/2LSB	*
BIPOLAR OFFSET (max)[4]	±1/2LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)		
+25°C	8 Bits	*
T_{min} to T_{max}	8 Bits	*
TEMPERATURE RANGE	0 to +70°C	-55°C to +125°C
TEMPERATURE COEFFICIENTS[4]		
Guaranteed max Change		
T_{min} to T_{max}		
Unipolar Offset	±1LSB (88ppm/°C)	±1LSB (40ppm/°C)
Bipolar Offset	±1LSB (88ppm/°C)	±1LSB (40ppm/°C)
Full Scale Calibration[6] (With 15Ω Fixed Resistor or 200Ω Trimmer)	±2LSB (176ppm/°C)	±2LSB (80ppm/°C)
POWER SUPPLY REJECTION[4]		
Max Change In Full Scale Calibration		
TTL Positive Supply		
$+4.5V \leqslant V+ \leqslant +5.5V$	±2LSB max	*
Negative Supply		
$-16.0V \leqslant V- \leqslant -13.5V$	±2LSB max	*
ANALOG INPUT RESISTANCE	3kΩ min	*
	5kΩ typ	*
	7kΩ max	*
ANALOG INPUT RANGES (Analog Input to Analog Common)		
Unipolar	0 to +10V	*
Bipolar	-5V to +5V	*
OUTPUT CODING		
Unipolar	Positive True Binary	*
Bipolar	Positive True Offset Binary	*
LOGIC OUTPUT		
Bit Outputs and $\overline{\text{Data Ready}}$		
Output Sink Current	3.2mA min	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*
Output Source Current (Bit Outputs)[7]		
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*
Output Leakage When Blanked	±40μA max	*
LOGIC INPUT		
Blank and Convert Input		
$0 \leqslant V_{in} \leqslant V+$	±40μA max	*
Blank – Logic "1"	2.0V min	*
Convert – Logic "0"	0.8V max	*
CONVERSION TIME	15μs min	*
	25μs typ	*
	40μs max	*

MODEL	AD570JD	AD570SD/AD570SD-883B[1]
POWER SUPPLY		
Absolute Maximum		
V+	+7V	*
V-	-16.5V	*
Specified Operating – Rated Performance		
V+	+5V	*
V-	-15V	*
Operating Range		
V+	+4.5V to +5.5V	*
V-	-12.0V to -16.5V	*
Operating Current		
Blank Mode		
V+ = +5V	2mA typ (10mA max)	*
V- = -15V	9mA typ (15mA max)	*
Convert Mode		
V+ = +5V	5mA	*
V- = -15V	10mA	*

*Specifications same as AD570J

Specifications subject to change without notice.

NOTES:

[1] The AD570S is available fully processed and screened to the requirements of MIL-STD-883, Class B. A complete list of tests is given in Table I. When ordering, specify the AD570SD/883B.

[2] The AD570 is a selected version of the AD571 10-bit A to D converter. As such, some devices may exhibit 9 or 10 bits of relative accuracy or resolution, but that is neither tested nor guaranteed. Only TTL logic inputs should be connected to pins 1 and 18 (or no connection made) or damage may result.

[3] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[4] Specifications given in LSB's refer to the weight of a least significant bit at the 8-bit level, which is 0.39% of full-scale.

[5] Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1 LSB, or 9.961 volts.

[6] Full Scale Calibration Temperature Coefficient includes effects of unipolar offset drift as well as gain drift.

[7] The Data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . .0 to +7V
V- to Digital Common . . . . . .0 to -16.5V
Analog Common to Digital Common. . . . . .±1V
Analog Input to Analog Common. . . . . ±15V
Control Inputs . . . . . 0 to V+
Digital Outputs (Blank Mode). . . . . 0 to V+
Power Dissipation. 800mW

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

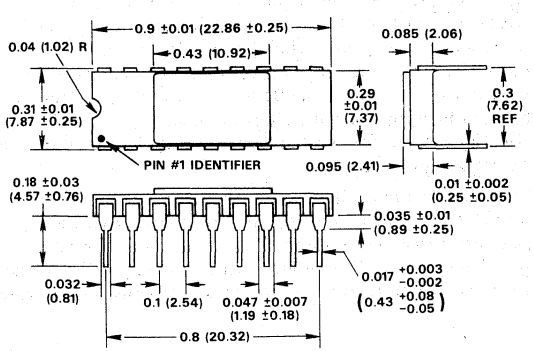


Figure 1. 18-Lead Ceramic Dual-In-Line Package

CIRCUIT DESCRIPTION

The AD570 is a complete 8-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD570 is shown in Figure 2. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 8-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 8-bit binary code which accurately represents the input signal to within ±1/2LSB (0.20%).

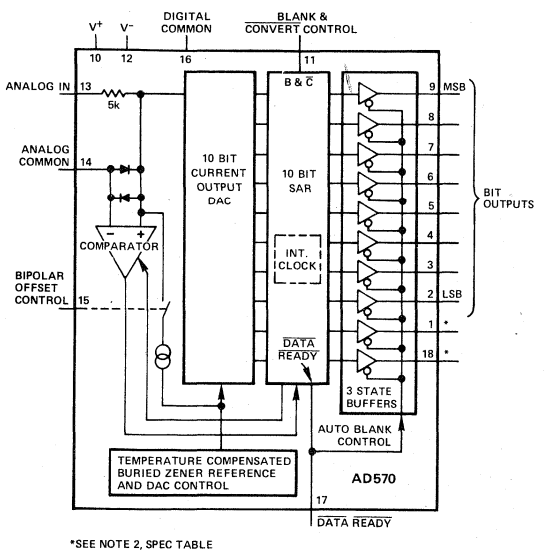


Figure 2. AD570 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

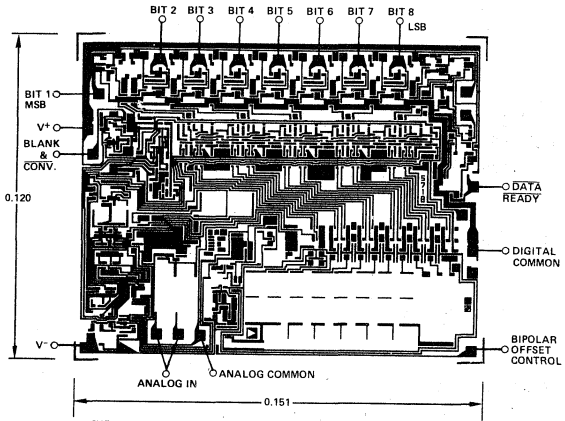


Figure 3. Chip Bonding Diagram

POWER SUPPLY SELECTION

The AD570 is designed and specified for optimum performance using a +5V and −15V supply. The supply current drawn by the device is a function of the operating mode (BLANK or CONVERT), as given on the specification page. The supply currents change only moderately over temperature as shown in Figure 4, and do not change significantly with changes in V^- from −10.8 volts to −16 volts.

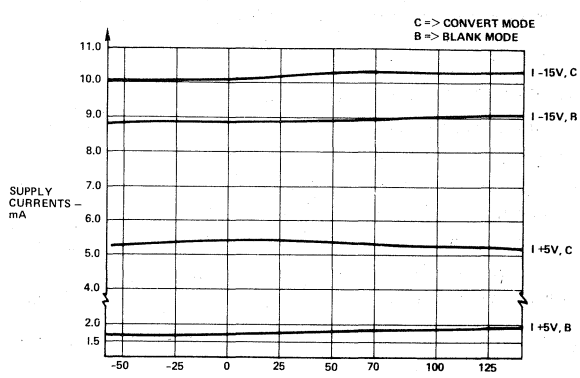


Figure 4. AD570 Power Supply Current vs. Temperature

CONNECTING THE AD570 FOR STANDARD OPERATION

The AD570 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 5.

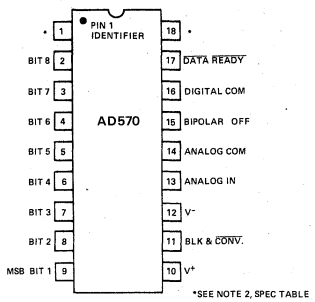


Figure 5. AD570 Pin Connections

FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.961 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.8%. If a more precise calibration is desired, a 200Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 11111110 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 40.00mV), a 50Ω resistor in series with a 200Ω trimmer (or a 500Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

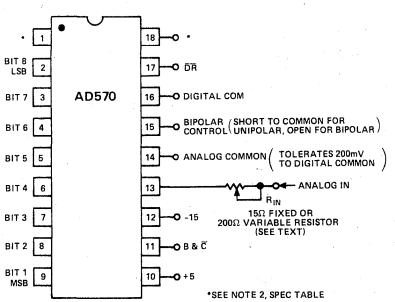


Figure 6. Standard AD570 Connections

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5V to +5V range with an offset binary output code. (-5.00 volts in will give a 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and 4.96 volts at the input yields the 11111111 code.) The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 7.

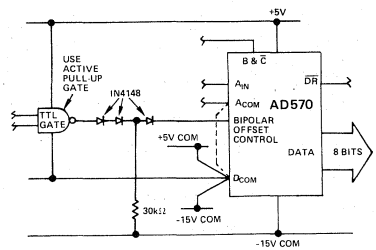


Figure 7. Bipolar Offset Controlled by Logic Gate

Gate Output = 1 Unipolar 0 - 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

COMMON MODE RANGE

The AD570 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum differential voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes as shown in Figure 8 between the commons if they are not connected locally.

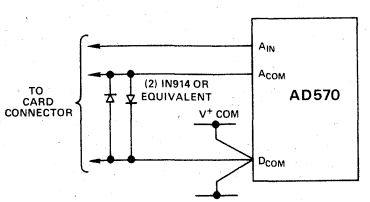


Figure 8. Differential Common Voltage Protection

ZERO OFFSET

The apparent zero point of the AD570 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 9 illustrates two methods of providing this offset. Figure 9A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

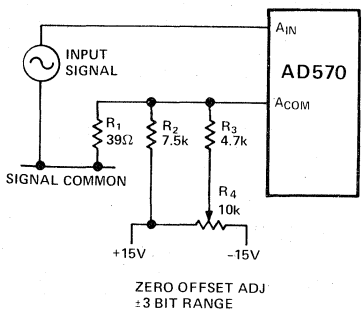


Figure 9. (A)

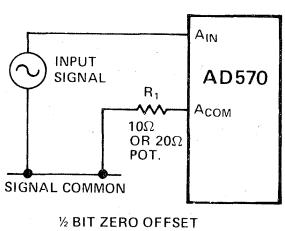


Figure 9. (B)

Figure 10 shows the nominal transfer curve near zero for an AD570 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 9B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 10Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 20Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.941 volts.

NOTE: During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common should go to the signal input side of the resistive offset network.

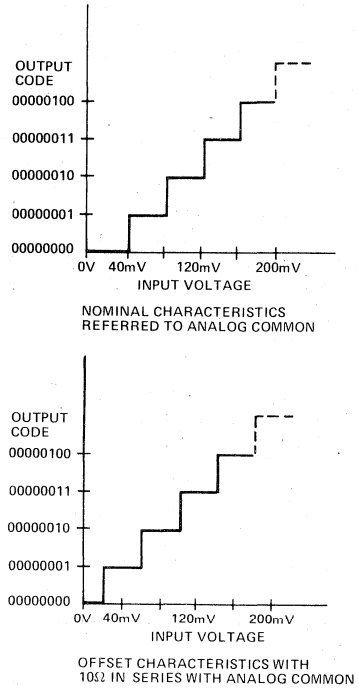


Figure 10. AD570 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 36.1mV)

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD570, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further ensure reliability, the AD570 is offered with 100% screening to MIL-STD-883, Class B, Method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition B and C
6) Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C min
7) Final Electrical Tests	Performed 100% to all min and max specifications on data pages.
8) External Visual	Method 2009

CONTROL AND TIMING OF THE AD570

There are several important timing and control features on the AD570 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 11.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

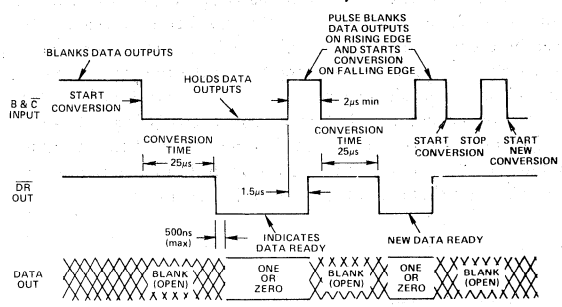


Figure 11. AD570 Timing and Control Sequence

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD570 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode – In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 12 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 15, in which μP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode – In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 13. A typical AD570 multiplexing application is shown in Figure 16.

This operating mode allows multiple AD570 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD570 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 8-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD570's are multiplexed in sequence, a new conversion may be started in one AD570 while data is being read from another. As long as the data is read and the first AD570 is cleared within 15μs after the start of conversion of the second AD570, no data overlap will occur.

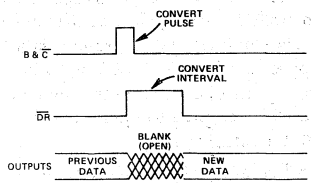


Figure 12. Convert Pulse Mode

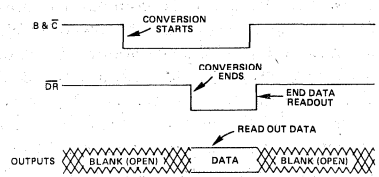


Figure 13. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD570

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD570, a SHA can also serve as a high input impedance buffer.

Figure 14 shows the AD570 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD570 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

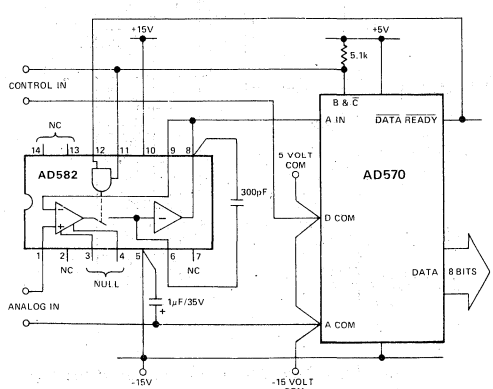


Figure 14. Sample-Hold Interface to the AD570

first comparator decision inside the AD570). The $\overline{\text{DATA READY}}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DATA READY}}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle to give the most accurate measurements.

INTERFACING THE AD570 TO A MICROPROCESSOR

The AD570 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12-or 16-bit) with a minimum of additional control components. The configuration shown in Figure 15 is designed to operate with an 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to ensure that the AD570 receives a sufficiently long B & $\overline{\text{C}}$ input pulse. When the converter is ready to start a new conversion, the B & $\overline{\text{C}}$ line is low, and $\overline{\text{DR}}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{\text{WR}}$. The B & $\overline{\text{C}}$ line will now go high, followed about 1.5μs later by $\overline{\text{DR}}$. This resets the external flip-flop and brings B & $\overline{\text{C}}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DR}}$ line goes low, the data outputs will become active with the new data and the control lines will return to the stand-by state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. An 8-bit data word is loaded onto the bus when its decoded address goes low and the $\overline{\text{RD}}$ line goes low. Polling the converter to determine if conversion is complete can be done by addressing the gate (shown dotted) which buffers the $\overline{\text{DR}}$ line, if desired. In this configuration, there is no need for additional buffer register storage. The data is stored indefinitely in the AD570, since the B & $\overline{\text{C}}$ line is continually held low.

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a μP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6821 Peripheral Interface Adapter (PIA). Shown in Figure 16 is a straightforward application of a PIA to multiplex up to 10 AD570 circuits. The AD570 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{\text{DATA READY}}$ output of the AD570 is an open collector with resistor pull-up, thus several $\overline{\text{DR}}$ lines can be wire-ORed to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is programmed as an 8-bit input port. The 8-bits of the second port are programmed as outputs, and along with the 2 control bits (which act as outputs), are used to control the 10 AD570's. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can then be read from port A. When the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ORed in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADC's are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{\text{DATA READY}}$ buffers. See the MC6821 data sheet for more application detail.

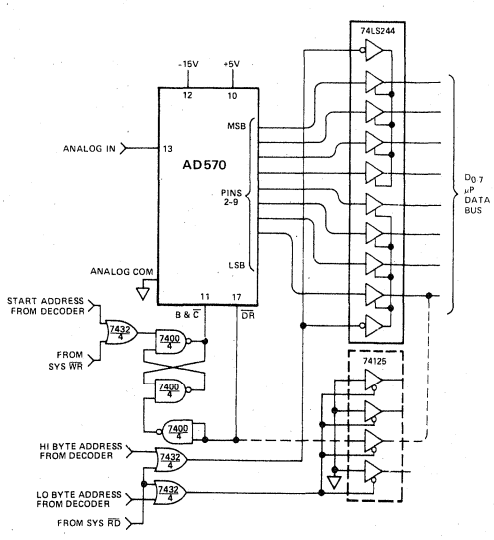


Figure 15. Interfacing AD570 to an 8-Bit Bus (8080 Control Structure)

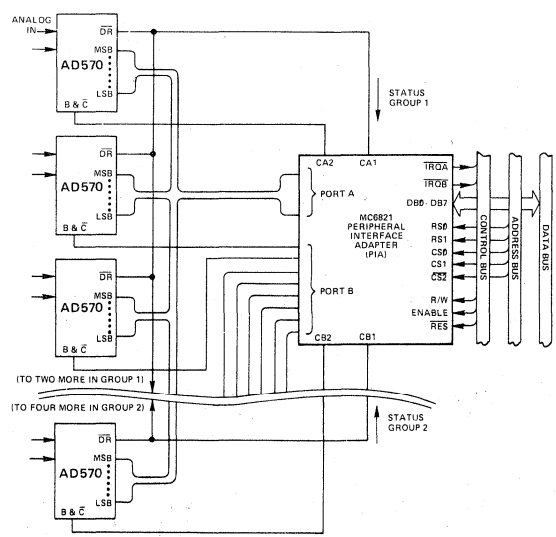


Figure 16. Multiplexing 10 AD570's Using Single PIA for µP Interface. No Other Logic Required (6800 Control Structure).

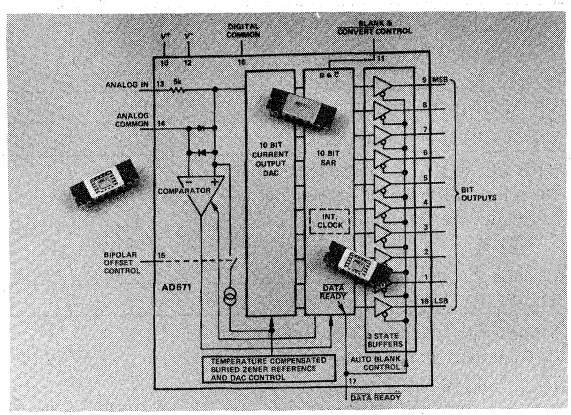
ANALOG DEVICES

Integrated Circuit 10-Bit Analog to Digital Converter

AD571*

FEATURES

Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
0 to +70°C – AD571K
-55°C to +125°C – AD571S
Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction



PRODUCT DESCRIPTION

The AD571 is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25μs.

The AD571 incorporates the most advanced integrated circuit design and processing technology available today. It is the first complete converter to employ I^2L (integrated injection logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and -15V, the AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD571 executes a true 10-bit conversion with no missing codes in approximately 25μs.

The AD571 is available in two versions for the 0 to +70°C temperature range, the AD571J and K. The AD571S guarantees 10-bit accuracy and no missing codes from -55°C to +125°C. All three grades are packaged in an 18-pin hermetically-sealed ceramic DIP.

*Covered by Patent No. 3,940,760, other patents pending.

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.3% is achieved without external trims.
2. The AD571 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD571 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V to +15V supplies. The device will also operate with a -12V supply.
6. The AD571S is also available with full processing to MIL-STD-883, Class B. The single chip construction and functional completeness make the AD571 especially attractive for high reliability applications.
7. Every AD571 is subjected to long-term stabilization bakes and given a powered burn-in at +125°C prior to final test to ensure reliability and long-term stability. In addition, all units are tested 100% at the extremes of their respective temperature ranges for all parameters to guarantee full performance.

SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD571JD	AD571KD	AD571SD/AD571SD-883[5]
RESOLUTION	10 Bits	*	*
RELATIVE ACCURACY @ 25°C[1]	±1LSB max	±1/2LSB max	±1LSB max
T_{min} to T_{max}	±1LSB max	±1/2LSB max	±1LSB max
FULL SCALE CALIBRATION[2]			
(With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	*	*
UNIPOLAR OFFSET (max)	±1LSB	±1/2LSB	*
BIPOLAR OFFSET (max)	±1LSB	±1/2LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	9 Bits	10 Bits	10 Bits
TEMPERATURE RANGE	0 to +70°C	*	-55°C to +125°C
TEMPERATURE COEFFICIENTS			
Guaranteed max Change			
T_{min} to T_{max}			
Unipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB (88ppm/°C)	±2LSB (44ppm/°C)	±5LSB (50ppm/°C)
POWER SUPPLY REJECTION			
Max Change In Full Scale Calibration			
CMOS Positive Supply (K only)			
+13.5≤V+≤+16.0V	N.A.	±1LSB max	N.A.
TTL Positive Supply			
+4.5V≤V+≤+5.5V	±2LSB max	±1LSB max	*
Negative Supply			
-16.0V≤V-≤-13.5V	±2LSB max	±1LSB max	*
ANALOG INPUT RESISTANCE	3kΩ min	*	*
	5kΩ typ	*	*
	7kΩ max	*	*
ANALOG INPUT RANGES			
(Analog Input to Analog Common)			
Unipolar	0 to +10V	*	*
Bipolar	-5V to +5V	*	*
OUTPUT CODING			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
LOGIC OUTPUT[3]			
Bit Outputs and $\overline{\text{Data Ready}}$			
Output Sink Current	3.2mA min	*	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*	*
Output Source Current (Bit Outputs)[4]			
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*	*
Output Leakage When Blanked	±40μA max	*	*
LOGIC INPUT			
Blank and Convert Input			
0≤V_{in}≤V+	±40μA max	*	*
Blank – Logic "1"	2.0V min	*	*
Convert – Logic "0"	0.8V max	*	*
CONVERSION TIME	15μs min	*	*
	25μs typ	*	*
	40μs max	*	*

MODEL	AD571JD	AD571KD	AD571SD/AD571SD-883[5]
POWER SUPPLY			
Absolute Maximum			
V+	+7V	+16.5V	*
V-	-16.5V	*	*
Specified Operating – Rated Performance			
V+	+5V	+5V to +15V	*
V-	-15V	*	*
Operating Range			
V+	+4.5V to +5.5V	+4.5V to +16.5V	*
V-	-12.0V to -16.5V	*	*
Operating Current			
Blank Mode			
V+ = +5V	2mA typ (10mA max)	*	*
V+ = +15V	5mA typ (10mA max)	*	*
V- = -15V	9mA typ (15mA max)	*	*
Convert Mode			
V+ = +5V	5mA	*	*
V+ = +15V	10mA	*	*
V- = -15V	10mA	*	*

*Specifications same as AD571J
**Specifications same as AD571K

Specifications subject to change without notice.

NOTES:

[1] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[3] Logic Input and Output Thresholds and Levels are a function of V+. They are guaranteed TTL compatible at V+ = +5V, CMOS compatible at V+ = 15V for the AD571K.

[4] The Data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[5] The AD571S is available fully processed and screened to the requirements of MIL-STD-883, Class B. A complete list of tests is given further. When ordering, specify the AD571SD/883B.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD571J, S . . . . . .0 to +7V
AD571K. . . . . 0 to +16.5V
V- to Digital Common . . . . . .0 to -16.5V
Analog Common to Digital Common. . . . . .±1V
Analog Input to Analog Common. . . . . ±15V
Control Inputs . . . . . 0 to V+
Digital Outputs (Blank Mode). . . . . .0 to V+
Power Dissipation. 800mW

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

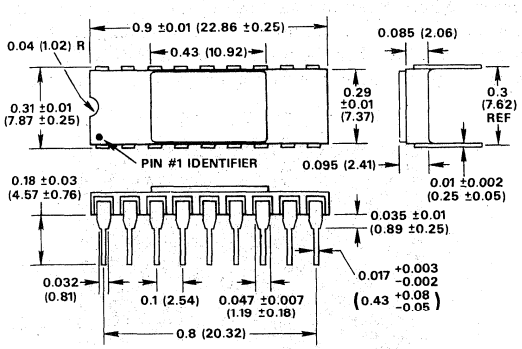


Figure 1. 18-Lead Ceramic Dual-In-Line Package

CIRCUIT DESCRIPTION

The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD571 is shown in Figure 2. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 10-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±½LSB (0.05%).

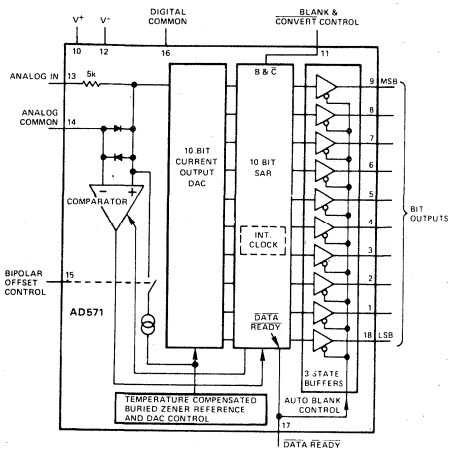


Figure 2. AD571 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further.

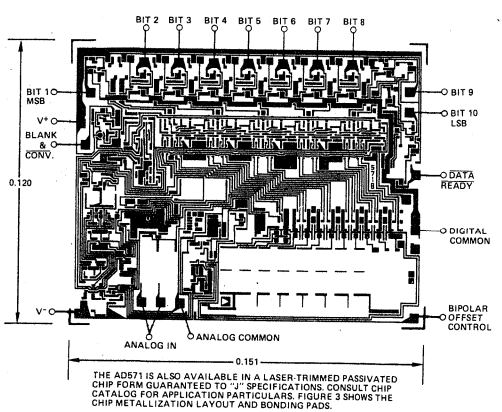


Figure 3. Chip Bonding Diagram

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

The AD571 is designed for optimum performance using a +5V and −15V supply, for which the AD571J and AD571S are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic. The input logic threshold is a function of V+ as shown in Figure 4. The supply current drawn by the device is a function of both V+ and the operating mode (BLANK or CONVERT). These supply current variations are shown in Figure 5. The supply currents change only moderately over temperature as shown in Figure 9.

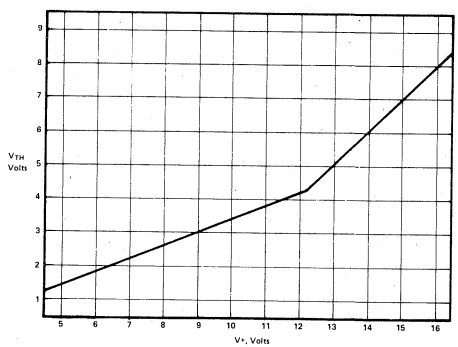


Figure 4. Logic Threshold (AD571K Only)

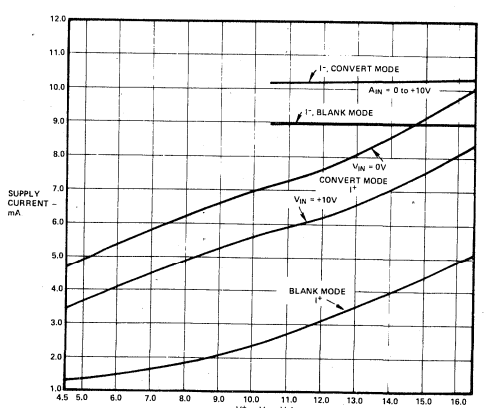


Figure 5. Supply Currents vs Supply Levels and Operating Modes

CONNECTING THE AD571 FOR STANDARD OPERATION

The AD571 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and −15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 6.

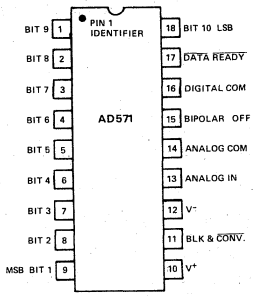


Figure 6. AD571 Pin Connections

FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.990 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.2%. If the more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 10.00mV), a 100Ω resistor in series with a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

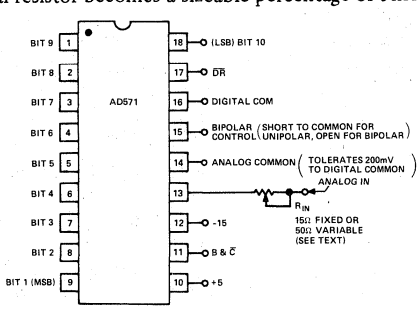


Figure 7. Standard AD571 Connections

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a −5V to +5V range with an offset binary output code. (−5.00 volts in will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000 and 4.99 volts at the input yeilds the 1111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 8.

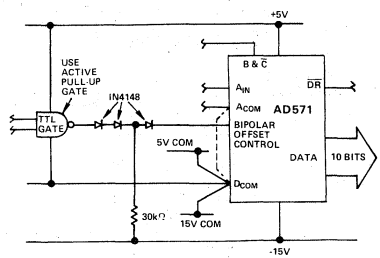


Figure 8. Bipolar Offset Controlled by Logic Gate

Gate Output = 1 Unipolar 0 - 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

COMMON MODE RANGE

The AD571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

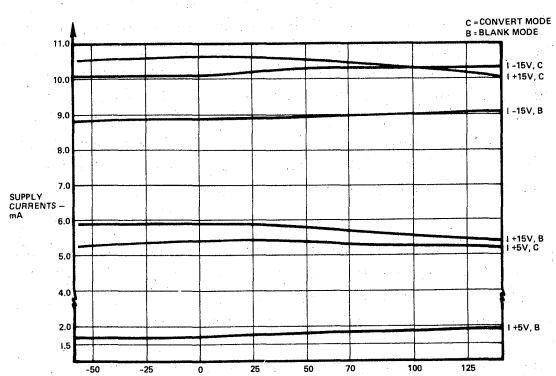


Figure 9. AD571 Power Supply Current vs Temperature

ZERO OFFSET

The apparent zero point of the AD571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 10 illustrates two methods of providing this offset. Figure 10A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

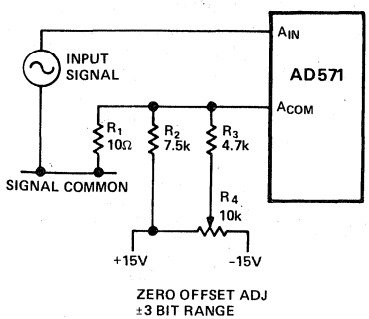


Figure 10.(A)

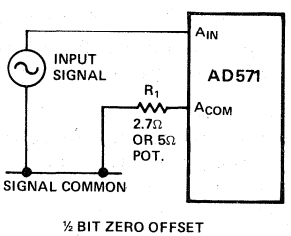


Figure 10.(B)

Figure 11 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 10B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common, should go to the signal input side of the resistive offset network.

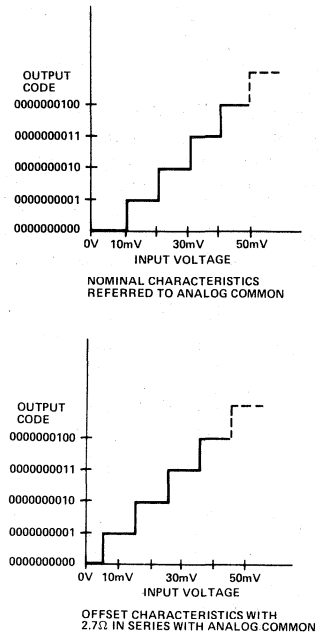


Figure 11. AD571 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766mV)

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD571, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further ensure reliability, the AD571 is offered with 100% screening to MIL-STD-883, Class B, Method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1015, Test Condition B, 168 hours @ +125°C
7) Final Electrical Tests	Performed 100% to all min and max specifications on data pages
8) External Visual	Method 2009

CONTROL AND TIMING OF THE AD571

There are several important timing and control features on the AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 12.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & C line during a conversion, the converter will clear and start a new conversion cycle.

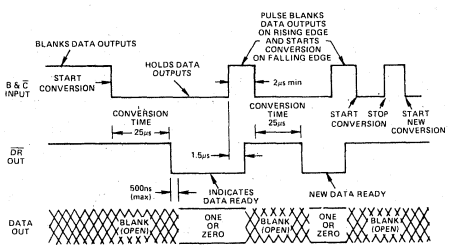


Figure 12. AD571 Timing and Control Sequence

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode — In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 13 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 16, in which μP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode — In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 14. A typical AD571 multiplexing application is shown in Figure 17.

This operating mode allows multiple AD571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD571's are multiplexed in sequence, a new conversion may be started in one AD571 while data is being read from another. As long as the data is read and the first AD571 is cleared within 15μs after the start of conversion of the second AD571, no data overlap will occur.

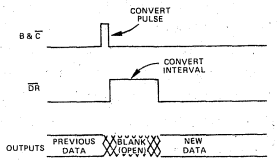


Figure 13. Convert Pulse Mode

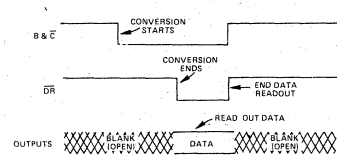


Figure 14. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD571

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD571, a SHA can also serve as a high input impedance buffer.

Figure 15 shows the AD571 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD571 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

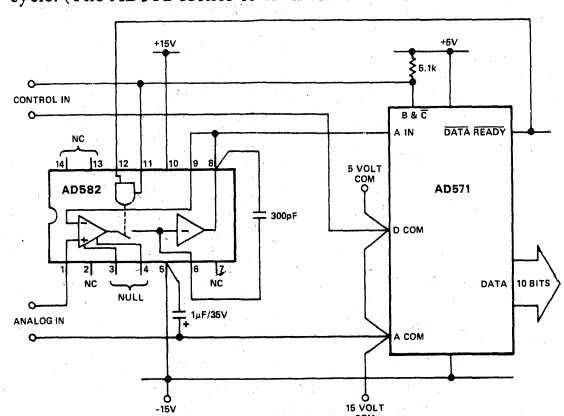


Figure 15. Sample-Hold Interface to the AD571

first comparator decision inside the AD571). The $\overline{\text{DATA READY}}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DATA READY}}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle to give the most accurate measurements.

INTERFACING THE AD571 TO A MICROPROCESSOR

The AD571 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12-or 16-bit) with a minimum of additional control components. The configuration shown in Figure 16 is designed to operate with an 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to insure that the AD571 receives a sufficiently long B & $\overline{\text{C}}$ input pulse. When the converter is ready to start a new conversion, the B & $\overline{\text{C}}$ line is low, and $\overline{\text{DR}}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{\text{WR}}$. The B & $\overline{\text{C}}$ line will now go high, followed about 1.5μs later by $\overline{\text{DR}}$. This resets the external flip-flop and brings B & $\overline{\text{C}}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DR}}$ line goes low, the data outputs will become active with the new data and the control lines will return to the stand-by state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. A data word (8-bit or 2-bit) is loaded onto the bus when its decoded address goes low and the $\overline{\text{RD}}$ line goes low. This arrangement presents data to the bus "left-justified," with highest bits in the 8-bit word; a "right-justified" data arrangement can be set up by a simple re-wiring. Polling the converter to determine if conversion is complete can be done by addressing the gate which buffers the $\overline{\text{DR}}$ line, as shown. In this configuration, there is no need for additional buffer register storage since the data can be held indefinitely in the AD571, since the B & $\overline{\text{C}}$ line is continually held low.

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a μP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6821 Peripheral Interface Adapter (PIA). Shown in Figure 17 is a straightforward application of a PIA to multiplex up to 8 AD571 circuits. The AD571 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{\text{DATA READY}}$ output of the AD571 is an open collector with resistor pull-up, thus several $\overline{\text{DR}}$ lines can be wire-ored to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is combined with 2-bits from the other port and programmed as a 10-bit input port. The remaining 6-bits of the second port are programmed as outputs and along with the 2 control bits (which act as outputs), are used to control the 8 AD571's. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can be read from the two peripheral ports; when the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ored in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADC's are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{\text{DATA READY}}$ buffers. See the MC6821 data sheet for more application detail.

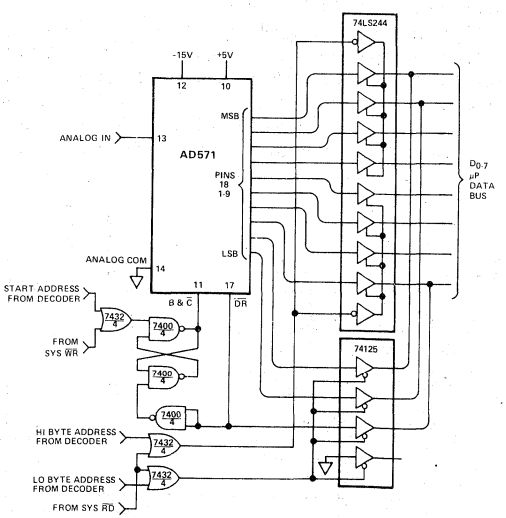


Figure 16. Interfacing AD571 to an 8-Bit Bus (8080 Control Structure)

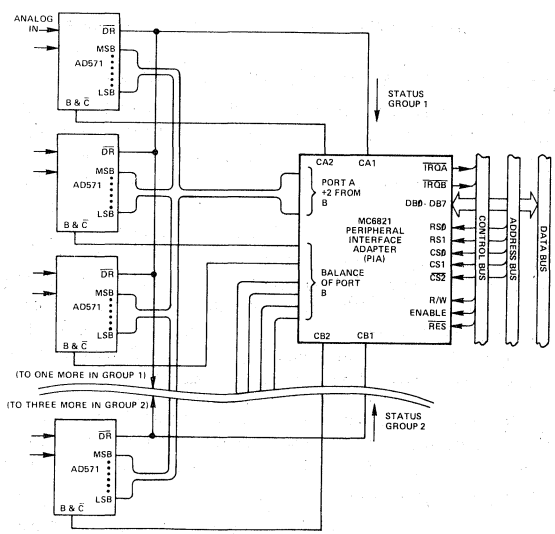


Figure 17. Multiplexing 8 AD571's Using Single PIA for μP Interface. No Other Logic Required (6800 Control Structure)

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572

FEATURES

Performance

- True 12-Bit Operation: Max Nonlinearity < ±0.012%
- Low Gain T.C.: < ±15ppm/°C (AD572B)
- Low Power: 900mW
- Fast Conversion Time: < 25μs
- Monotonic Feedback DAC Guarantees No Missing Codes
- Hermetically-Sealed, Electrostatically-Shielded DIP

Versatility

- Military/Aerospace Temperature Range: -55°C to +125°C (AD572S)
- MIL-STD-883 Processing Available
- Positive-True Serial or Parallel Logic Outputs
- Short-Cycle Capability

Value

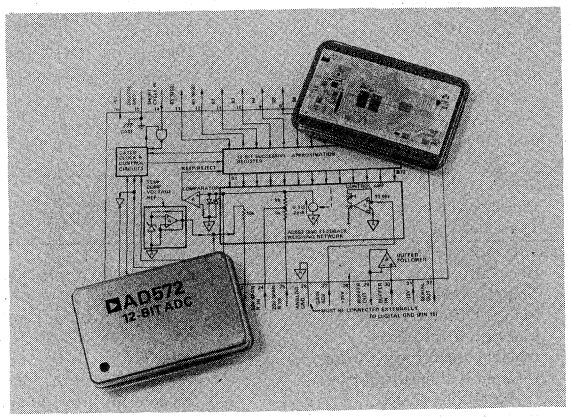
- Precision +10V Reference for External Application
- Internal Buffer Amplifier
- High Reliability Welded Metal Package
- Low Cost

GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide modular performance, flexibility, and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 900mW, and conversion time of less than 25μs. Of considerable significance in military and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD572S, and the availability of units processed to MIL-STD-883. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5.0, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.



The AD572 is packaged in a hermetically-sealed, all-metal DIP. Welding...rather than solder sealing...eliminates any possibility of contamination from flux and solder particles. The metal construction provides excellent shielding from random electrostatic and/or electromagnetic radiation which could cause incorrect output codes. To insure a level of reliability consistent with its performance, each AD572 receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, acceleration testing, fine and gross leak testing, and operating burn-in.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25°C to +85°C, and the "S" from -55°C to +125°C.

PRODUCT DESCRIPTION

The AD572 functional diagram and pin-out are shown in Figure 1. The device consists of the following monolithic bipolar transistor and thin-film resistor circuit elements:

1. 12-bit successive-approximation register
2. 12-bit feedback DAC weighing network
3. low-drift comparator
4. temperature-compensated precision +10V reference
5. high-impedance buffer follower
6. gated clock and digital control circuits

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	5.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time			
to 0.01% of FSR for 20V step	2μs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25°C to +85°C	Guaranteed: -55°C to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/%ΔV_S	*	*
±5V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)
Unipolar Offset	±3ppm FSR/°C	±3ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)	25μs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
$\overline{\text{Status}}$	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±5mV	*	*
Max External Current	±4mA	*	*
Voltage Temperature Coefficient (max)	±20ppm/°C	±10ppm/°C	**
POWER REQUIREMENTS			
Supply Voltages/Currents	+15V, ±5% @ +25mA	*	*
	-15V, ±5% @ -20mA	*	*
	+5V, ±5% @ +50mA	*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-55°C to +150°C	*	*

*Same specification as AD572AD

**Same specification as AD572BD

Specifications subject to change without notice.

Note 1 Positive pulse 200nsec wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.

Note 2 With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.

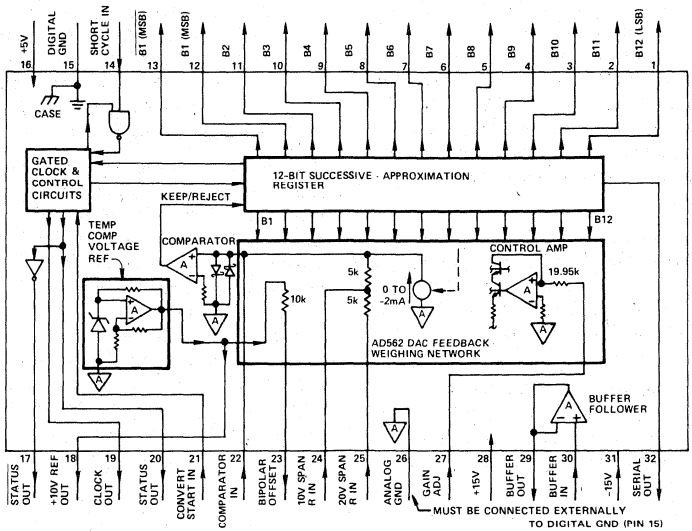


Figure 1. AD572 Functional Diagram & Pinout

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, ±1mV by active laser trimming of the thin-film resistors which determine the closed-loop gain of this op amp.

The DAC feedback weighing network is comprised of a proprietary 12-bit analog current switch chip and silicon-chromium thin-film ladder network (separately packaged as the AD562 12-bit D/A converter). This ladder network is active laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.0005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through

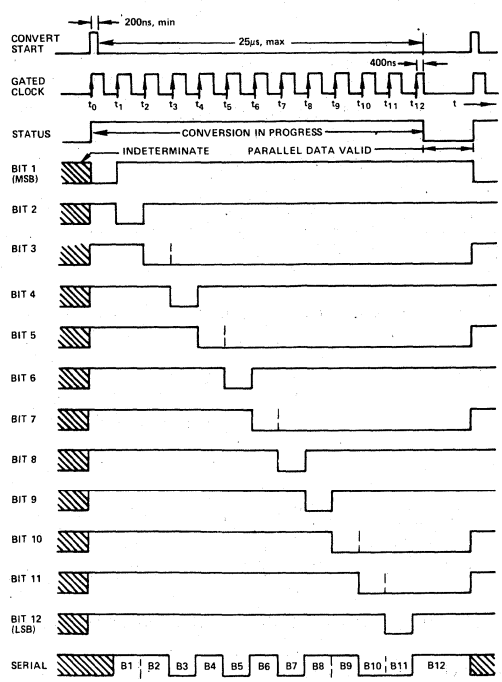


Figure 2. Timing Diagram (Binary Code 110101011001)

13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 400ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 8).

Incorporation of this 400ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

BINARY CODING

The AD572 binary output number $N_o = B_1\ B_2\ B_3 \ldots B_{12}$ is related to the analog input voltage E_{in} for all unipolar ranges by the expression:

$$\frac{B_1\,2^{11} + B_2\,2^{10} + B_3\,2^9 + \ldots + B_{12}\,2^0}{2^{12}} = \frac{E_{in}}{FSR} \qquad (1)$$

. . .where B_1 = MSB, B_{12} = LSB, and FSR = full-scale range. For all bipolar ranges a fixed bipolar offset equal to $\frac{+FSR}{2}$ is internally summed with E_{in} so that the sum of E_{in} plus this offset will be positive over the rated operating range. For bipolar ranges, expression (1) becomes:

$$\frac{B_1\,2^{11} + B_2\,2^{10} + B_3\,2^9 + \ldots + B_{12}\,2^0}{2^{12}} = \frac{E_{in} + \frac{FSR}{2}}{FSR} \qquad (2)$$

Expressions (1) and (2) can be put in an alternate form:

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR = E_{in} \qquad (3)$$

Unipolar (Binary Coding)

...and...

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR - \frac{FSR}{2} = E_{in} \qquad (4)$$

Bipolar (Offset Binary Coding)

Several examples will illustrate how this binary coding works.

0 TO +10V INPUT RANGE

Assume FSR = 10V and $B_1\ B_2\ B_3 \ldots B_{12}$ = 110001000001, then from (3), E_{in} = +5V +2.5V +0.1563V + 0.0024V = +7.6587V.

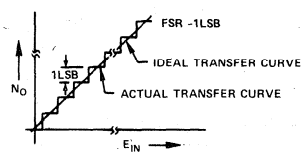
-5V TO +5V INPUT RANGE

Assume FSR = 10V as above, but that the bipolar offset is connected and $B_1\ B_2\ B_3 \ldots B_{12}$ = 0110000000001. Then from (4), E_{in} = (+2.5V + 1.25V + 0.0024V) - 5V = -1.2476V.

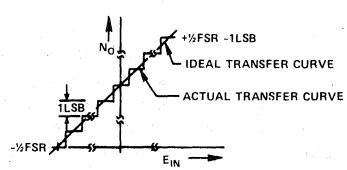
-10V TO +10V INPUT RANGE

Assume the bipolar offset is connected as above, but that the input span is now 20V. Assuming the same digital output code as in the -5V to +5V input range example, from (4), E_{in} = (+5V +2.5V +0.0049V) -10V = -2.4951V, or twice the value of the previous example (neglecting round-off errors).

The encoding process defined by the previous relations (1) and (2) or (3) and (4) determines that the analog input lies within one of the 2^{12} = 4096 quantization levels between 0 and FSR (or -FSR/2 and +FSR/2). Figures 3 (A) and 3 (B) show the actual device transfer curves for unipolar and bipolar ranges (offset binary coding). They also show the ideal straight-line transfer curves which pass through the center of each quantization level. As can be seen from these figures, the actual and ideal transfer curves differ by exactly ±½LSB at the end of each quantization interval, giving rise to the fundamental ±½LSB quantization error inherent in the digitizing process.



(A) Unipolar Range (Binary Coding)



(B) Bipolar Range (Offset Binary Coding)

Figure 3. Unipolar and Bipolar Range Transfer Curves

ANALOG INPUT AND POWER CONNECTIONS

Offset Adjust: Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 4 and 5, respectively. The Bipolar Offset pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator Input pin 22 for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9MΩ resistor to Comparator Input pin 22 for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of 8 x 244 x 10^{-6} x 1200ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

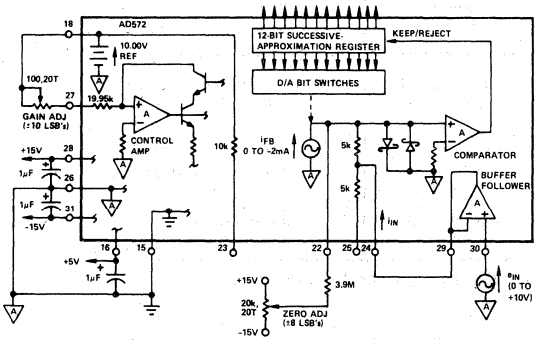


Figure 4. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

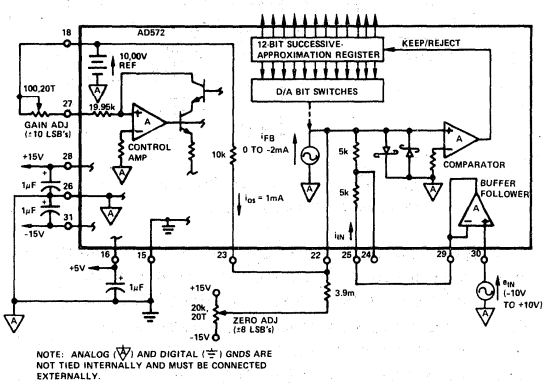


Figure 5. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 6.

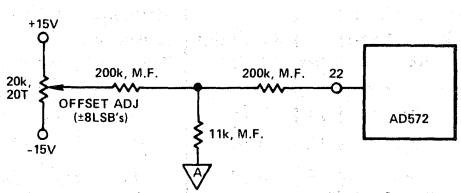


Figure 6. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin 22 connection runs short, since the Comparator Input pin 22 is quite sensitive to external noise pick-up.

Gain Adjust: The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input pin 27 for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco = 100ppm/°C max) types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to ±0.1% of FSR is guaranteed.

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground pin 26 and Digital Ground pin 15 are not connected internally; these two pins must be connected externally for the device to operate properly. Preferably, this connection is made at only one point, and as close to the device as possible. The case is connected internally to pin 15 to provide good electrostatic shielding.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed for optimum device performance. 1µF tantalum types are recommended; these capacitors should be located close to the device. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling (as is required with some competitive products), since each power lead is bypassed internally with a 0.039µF ceramic capacitor.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -½FSR for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table 1. Coding relationships and calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0	
:	:	:	:	:	:	
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0	
:	:	:	:	:	:	
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0	

Table 1. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

RANGE AND BUFFER FOLLOWER PIN CONNECTIONS

Analog pin connections for each of the ranges, with and without the buffer follower being used, are shown in Table 2.

Range	Buffer Follower	Connect Analog Input To Pin:	Connect Span Pin:	Connect Bipolar Pin 23 To:
0 to +5V	Used	30, and 29 to 24	25 to 22	—
	Not Used	24		
0 to +10V	Used	30, and 29 to 24	—	
	Not Used	24		
-2.5 to +2.5V	Used	30, and 29 to 24	25 to 22	22
	Not Used	24		
-5 to +5V	Used	30, and 29 to 24	—	
	Not Used	24		
-10 to +10V	Used	30, and 29 to 25	—	
	Not Used	25		

Table 2. Range and Buffer Follower Pin Connections

When the analog signal source has a low impedance (as would be the case if it were the output of the sample-hold amplifier of Figure 9), it can be connected to either of the direct input pins 24 or 25. The buffer follower is used in the application as shown in Figure 6, in which the analog input to the converter comes directly from the output of a FET analog multiplexer. The selected channel has a typical r_{on} = 200Ω which has a 3000ppm/°C tempco. If the multiplexer output were connected to the 0 to +10V direct input pin 24 (5kΩ input impedance, nominal), this r_{on} would introduce a 4% gain scale-factor loading error, which is well beyond the normal ±0.25% FSR external gain adjustment range, and a tempco of approximately 3000ppm/°C x 4% = 120ppm/°C. By connecting the buffer between the multiplexer output and direct input, these errors are eliminated. The buffer amplifier input bias current (50nA typical) must flow through the analog signal source, however. This limits the upper practical source impedance to several kilohms so that the offset voltage I_{BIAS} R_{SOURCE} can be kept negligible, even though the buffer amplifier dynamic input impedance ⩾ 100MΩ. The buffer amplifier has a 2μs settling time to 0.01% FSR for a 20V input step. This must be added to the conversion time when the input voltage can change significantly between successive conversions (as could be the case in the circuit of Figure 7).

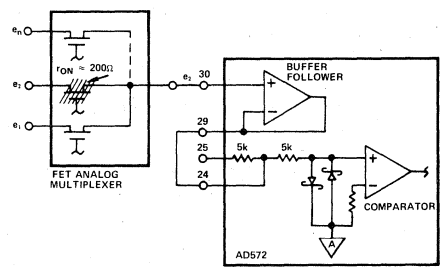


Figure 7. Using Buffer Follower With Multiplexed Analog Input

Short Cycle Input: A Short Cycle Input pin 14 permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +400ns in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12, 10, and 8-bit conversion times are summarized in Table 3.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at: (Figure 2)
16	12	0.024	25	t_{12} + 400ns
2	10	0.10	21	t_{10} + 400ns
4	8	0.39	17	t_8 + 400ns

Table 3. Short Cycle Connections

(One should note that the calibration voltages listed in Table 1 are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolutions.)

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary

or two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 8. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 2. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

APPLICATIONS

Sample-Hold Amplifier: A sample-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than ½LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 9. The $\overline{\text{STATUS}}$ output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the $\overline{\text{STATUS}}$ flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o\ S\text{-}H}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the $\overline{\text{STATUS}}$ flag returns to "1", restoring the SHA mode to SAMPLE, and $e_{o\ S\text{-}H}$ again tracks the analog signal voltage $e_{in\ S\text{-}H}$ (after the signal acquisition transient has subsided).

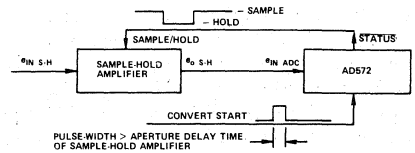


Figure 9. Sample-Hold Amplifier – AD572 Interconnections

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 9, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that $e_{o\ S\text{-}H}$ is in steady-state before conversion is initiated. This assures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 10.

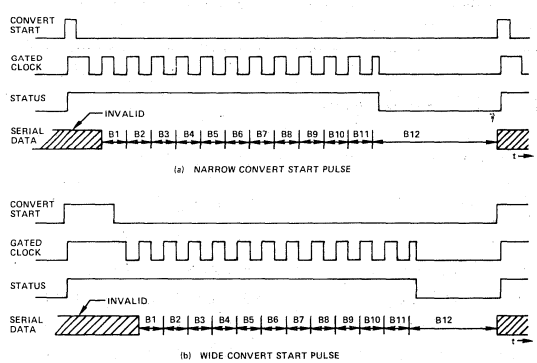


Figure 10. Effect of Convert Start Pulse-Width on Timing

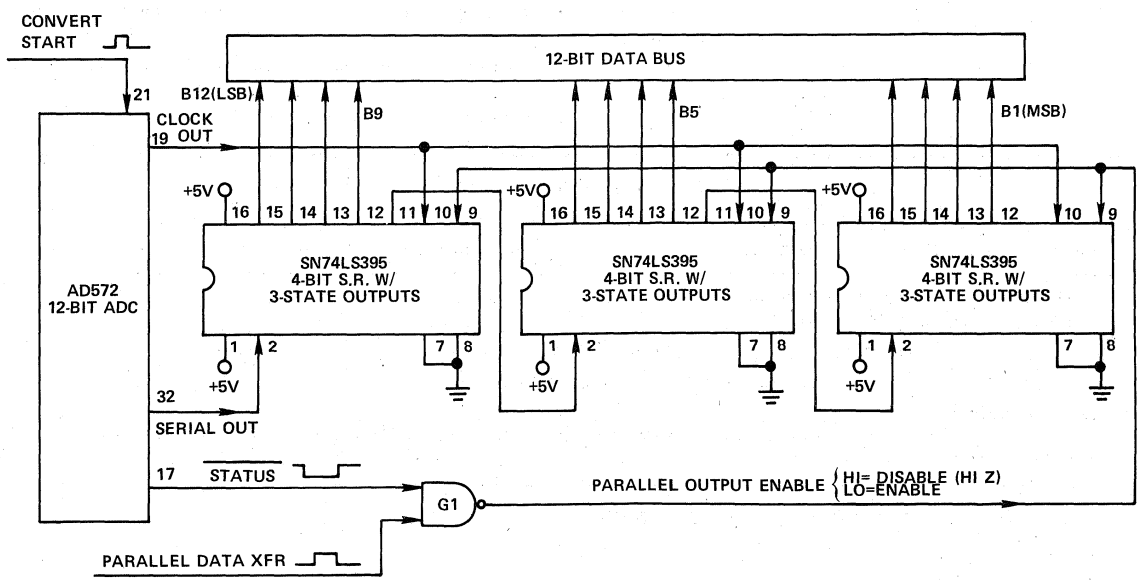


Figure 8. Serial Data Transfer Into Shift Register With Parallel Output to Data Bus

Digital Gain Control: Figure 11 shows a method of varying the AD572 gain digitally, using an 8-bit DAC. The 100Ω GAIN ADJ potentiometer is replaced by a 15Ω fixed resistor. This biases full-scale high by approximately 35Ω/20,000Ω = +0.18% of FSR. The AD559 has a large positive compliance voltage which permits its Current Output pin 4 to be connected directly to the AD572 Reference Input pin 27. The AD559 2.5mA output current is established by the AD580 +2.5V voltage reference connected through a 1kΩ resistor to Reference Current Input pin 14. The 2.5mA DAC full-scale output current removed from the AD572 pin 27 node changes the pin 27 input current -2.5mA x 15Ω/20kΩ = -1.88μA, or -1.88μA/500μA = -0.38% of FSR; this permits a digital gain adjustment range of approximately ±0.2% FSR from nominal.

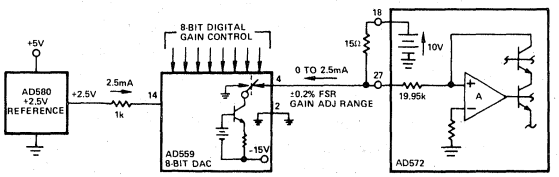
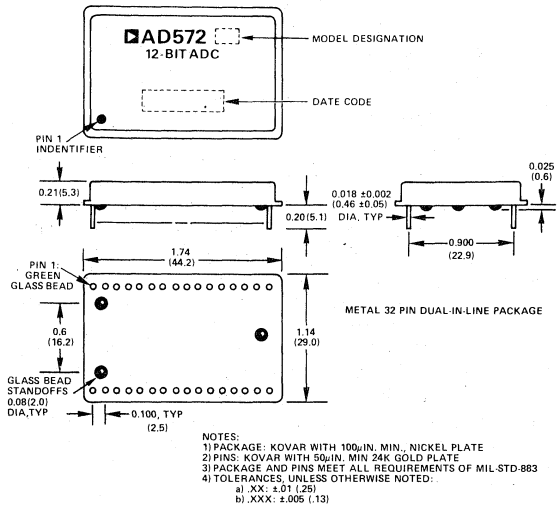


Figure 11. Digital Gain Control Using 8-Bit DAC

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all models of the AD572 receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Stabilization Bake	24 hours @ +150°C
3. Temperature Cycling	10 cycles, -65°C to +150°C
4. Constant Acceleration	5000G
5. Seal, Test, Fine and Gross	In-House Criteria
6. Operating Burn-In	24 hours @ +125°C

PROCESSING TO MIL-STD-883

All models ordered to the requirements of MIL-STD-883, Method 5004, Class B are identified with a /883 suffix, and receive the following processing.

1. Pre-Cap Visual Inspection	2010, Test Condition B
2. Stabilization Bake	1008, 24 hours @ +150°C
3. Temperature Cycling	1010, Test Condition C, 10 cycles, -65°C to +150°C
4. Constant Acceleration	2001, Y_1 plane, 5000G
5. Seal Test, Fine and Gross	1014, Test Condition A and C
6. Operating Burn-In	1015, Test Condition B, 160 hours @ +125°C
7. Final Electrical Testing	Performed at max and min operating temperatures
8. External Visual Inspection	2009

AD572 ORDERING GUIDE

Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes
AD572AD	-25°C to +85°C	±30ppm/°C	±20ppm/°C	0 to +70°C
AD572BD	-25°C to +85°C	±15ppm/°C	±10ppm/°C	-25°C to +85°C
AD572SD	-55°C to +125°C	+15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)	±10ppm/°C	-55°C to +125°C
AD572BD/883B AD572SD/883B	Meet all specifications after processing to the requirements of MIL-STD-883, Method 5004, Class B.			

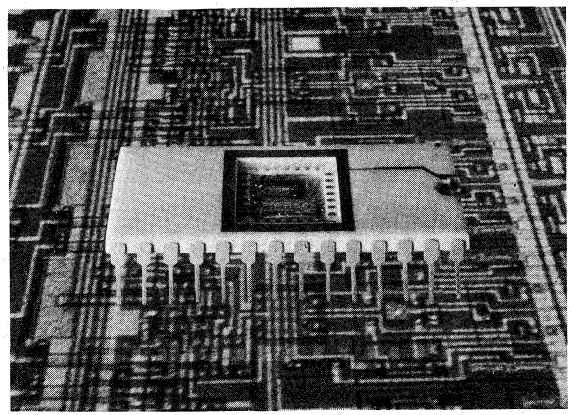
NOTE: D suffix = Dual-In-Line package designator.

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8- or 16-Bit Microprocessor Bus Interface
- Guaranteed Linearity Over Temperature
  - 0 to +70°C – AD574J, K, L
  - -55°C to +125°C – AD574S, T, U
- No Missing Codes Over Temperature
- Fast Successive Approximation Conversion - 25μs
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574L, 12.5ppm/°C max AD574U
- Low Profile 28-Pin Ceramic DIP
- Low Power: 450mW
- Low Cost



PRODUCT DESCRIPTION

The AD574 is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus. The AD574 design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

The second chip uses the newly-developed LCI (linear-compatible integrated injection logic) process to provide the low-power I^2L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

The AD574 is available in six different grades. The AD574J, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD574S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD574 interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The AD574 will also operate equally well in a self-cycling, stand alone mode and can perform conversions and latch data into an external latch at a 40kHz sample rate.
3. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges, 0 to +10 and 0 to +20 volts unipolar, or -5 to +5 and -10 to +10 volts bipolar. Typical bipolar offset and full scale calibration of ±0.1% can be trimmed to zero with one external component each.
4. The internal buried zener reference is trimmed to 10.00 volts with a 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.
5. The two-chip construction renders the AD574 inherently more reliable than hybrid multi-chip designs. All three military grades have guaranteed linearity error over the full -55°C to +125°C and are especially recommended for high performance needs in harsh environments. These units are available fully processed to MIL-STD-883B, Level B.

SPECIFICATIONS (typical @ +25°C with V_{CC} = +15, V_{LOGIC} = +5V, V_{DD} = -15V, unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	AD574J	AD574K	AD574L	UNITS
RESOLUTION (max)	12	12	12	Bits
NONLINEARITY ERROR				
25°C (max)	±1	±1/2	±1/2	LSB
T_{min} to T_{max} (max)	±1	±1/2	±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)	±2	±1	±1	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero) 25°C (max)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)	0.5	0.4	0.35	% of F.S.
(With Initial Adjustment)	0.22	0.12	0.05	% of F.S.
TEMPERATURE RANGE		0 to +70		°C
TEMPERATURE COEFFICIENTS (Using internal reference) Guaranteed max change T_{min} to T_{max}				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(50)	(27)	(10)	(ppm/°C)
POWER SUPPLY REJECTION Max change in Full Scale Calibration				
+13.5V ≤ V_{CC} ≤ +16.5V	±2	±1	±1	LSB
+4.5V ≤ V_{LOGIC} ≤ +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V≤V_{DD}≤-13.5V	±2	±1	±1	LSB
ANALOG INPUTS				
Input Ranges				
Bipolar		-5 to +5		Volts
		-10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5k (3k min, 7k max)		Ω
20 Volt Span		10k (6k min, 14k max)		Ω
POWER SUPPLIES				
Operating Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+13.5 to +16.5		Volts
V_{DD}		-13.5 to -16.5		Volts
Operating Current				
V_{LOGIC}		30 typ., 40 max		mA
V_{CC}		2 typ., 5 max		mA
V_{DD}		18 typ., 30 max		mA
POWER DISSIPATION		450 typ., 725 max		mW
INTERNAL REFERENCE VOLTAGE		10.00 ±0.1 (max)		Volts
Output Current (available for external loads) (External load should not change during conversion)		1.5 max		mA

Specifications subject to change without notice.

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	AD574S	AD574T	AD574U	UNITS
RESOLUTION (max)	12	12	12	Bits
NONLINEARITY ERROR				
25°C (max)	±1	±1/2	±1/2	LSB
-25°C to +85°C (max)	±1	±1/2	±1/2	LSB
-55°C to +125°C (max)	±1	±1	±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)	±2	±1	±1	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF IN to REF OUT) (Adjustable to zero) 25°C (max)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)	0.8	0.6	0.4	% of F.S.
(With Initial Adjustment)	0.5	0.25	0.12	% of F.S.
TEMPERATURE RANGE		-55 to +125		°C
TEMPERATURE COEFFICIENTS (using internal reference) Guaranteed max change T_{min} to T_{max}				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	±1	LSB
	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
POWER SUPPLY REJECTION Max change in Full Scale Calibration				
$+13.5V \leqslant V_{CC} \leqslant +16.5V$	±2	±1	±1	LSB
$+4.5V \leqslant V_{LOGIC} \leqslant +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V \leqslant V_{DD} \leqslant -13.5V$	±2	±1	±1	LSB
ANALOG INPUTS				
Input Ranges				
Bipolar		-5 to +5		Volts
		-10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5k (3k min, 7k max)		Ω
20 Volt Span		10k (6k min, 14k max)		Ω
POWER SUPPLIES				
Operating Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+13.5 to +16.5		Volts
V_{DD}		-13.5 to -16.5		Volts
Operating Current				
V_{LOGIC}		30 typ., 40 max		mA
V_{CC}		2 typ., 5 max		mA
V_{DD}		18 typ., 30 max		mA
POWER DISSIPATION		450 typ., 725 max		mW
INTERNAL REFERENCE VOLTAGE		10.00 ±0.1 (max)		Volts
Output Current (available for external loads) (External load should not change during conversion)		1.5 max		mA

Specifications subject to change without notice.

DIGITAL CHARACTERISTICS
ALL GRADES

(See Page 10-42 for Detailed Timing Specifications)

LOGIC INPUTS (Not including 12/$\overline{8}$, which must be hard-wired to V_{LOGIC} or DIGITAL COMMON)

$4.5V \leqslant V_{LOGIC} \leqslant 5.5V$

Input Threshhold	
T_{min} to T_{max}	
Logic "1"	2.0 Volts min
Logic "0"	0.8 Volts max
Input Current	
T_{min} to T_{max}	
Logic "1"	±50μA max
Logic "0"	±50μA max

LOGIC OUTPUTS

T_{min} to T_{max}	
Bit Outputs and STS	
Output Sink Current (V_{OUT} = 0.4V max)	1.6mA min (1 TTL Load)
Output Source Current (V_{OUT} = 2.4V min)	0.5mA min
Output Leakage when in High Impedance State	±40μA max

OUTPUT CODING

Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary

CONVERSION TIME	15μs min 25μs typ 35μs max

MINIMUM START PULSE WIDTH

AT CE (Pin 6) (Positive)	300ns
AT $\overline{CS}$ (Pin 3) (Negative)	500ns
AT R/$\overline{C}$ (Pin 5) (Negative)	400ns

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{DD} to Digital Common . . . . . .0 to −16.5V
V_{LOGIC} to Digital Common. . . . . .0 to +7V
Analog Common to Digital Common. . . . . .±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common . . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10 V_{IN}) to Analog Common . . . . . .±16.5V
20 V_{IN} to Analog Common . . . . . .±24V
REF OUT . . . . . Indefinite short to common Momentary short to V_{CC}
Chip Temperature (J, K, L grades) . . . . . 100°C
(S, T, U grades) . . . . . 150°C
Power Dissipation 1000mW
Lead Temperature, Soldering. . . . . .300°C, 10 sec.
Storage Temperature . . . . . .−65°C to +150°C
Thermal Resistance, θ_{JA}, ... 60°C/W

MIL-STD-883

The rigors of the military/aerospace environment temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD574, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD574 is offered with 100% screening to MIL-STD-883B, method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition B and C
6) Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C
7) Final Electrical Tests	Performed 100% to all min and max specifications on data pages
8) External Visual	Method 2009

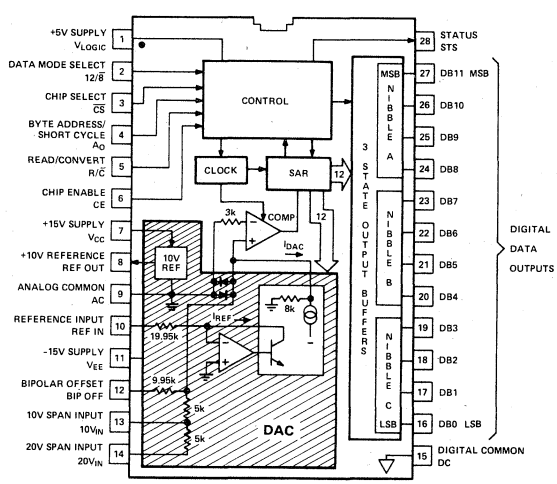


Figure 1. AD574 Block Diagram and Pin Configuration

THE AD574 OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

NONLINEARITY ERROR

Nonlinearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574K, L, T, and U grades are guaranteed for maximum nonlinearity error of ±1/2LSB over their respective temperature ranges. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574J and S grades are guaranteed to ±1LSB max error over their respective temperature ranges. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. (In actual practice, our test systems limit minimum code width to 1/4LSB.) For the AD574K, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574J and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figure 5. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

POWER SUPPLY REJECTION

The standard specifications for the AD574 assume use of +5.00 and ±15.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

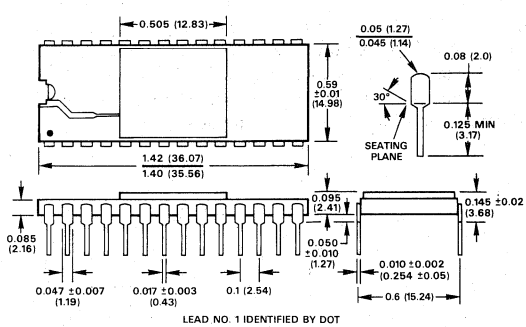


Figure 2. 28 Lead Dual-in-Line Package

AD574 ORDERING GUIDE

MODEL	TEMP RANGE	LINEARITY ERROR MAX (T_{min} to T_{max})	RESOLUTION NO MISSING CODES (T_{min} to T_{max})	MAX FULL SCALE T.C. (ppm/°C)
AD574JD	0 to +70°C	±1LSB	11 Bits	50.0
AD574KD	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574LD	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574SD	-55°C to +125°C	±1LSB	11 Bits	50.0
AD574TD	-25°C to +85°C	±1/2LSB		
	-55°C to +125°C	±1LSB	12 Bits	25.0
AD574UD	-25°C to +85°C	±1/2LSB		
	-55°C to +125°C	±1LSB	12 Bits	12.5

CIRCUIT OPERATION

The AD574 is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574 is shown in Figure 3. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. (Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers). The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it is buffered and can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation. (Details of full scale and offset trimming are given on the next page.)

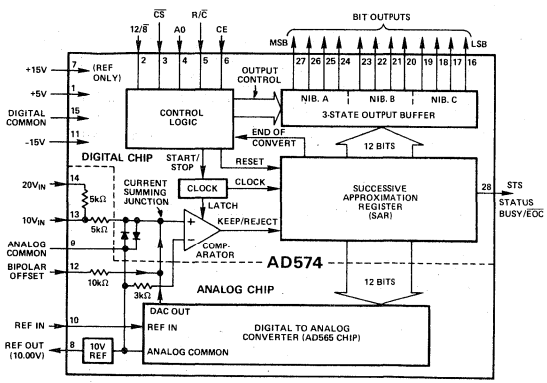


Figure 3. Block Diagram of AD574 12 bit A-to-D Converter

CONTROL FUNCTIONS

There are two sets of control pins on the AD574, the general control inputs (CE, $\overline{CS}$, and R/$\overline{C}$), and the internal register control inputs (12/$\overline{8}$ and A_0). The general control pins function similarly to those on most A/D converters, performing device timing, addressing, cycle initiation and read enable functions. The internal register control inputs, which are not found on most A/D converters, select output data format and conversion cycle length.

The two major control functions, convert start and read enable, are controlled by CE, $\overline{CS}$, R/$\overline{C}$. Although all three inputs must be in the correct state to perform the function (for convert start, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 0; for read enable, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 1), the sequence does not matter. For large systems, typically microprocessor controlled, standard operation for convert start would be to first set R/$\overline{C}$ = 0 (from R/$\overline{W}$ line); address the chip with $\overline{CS}$ = 0, then apply a positive start pulse to CE. A read would be done similarly but with R/$\overline{C}$ = 1.

For a much simpler stand-alone operation, CE can be wired high, $\overline{CS}$ wired low, and R/$\overline{C}$ toggled as needed to initiate conversion. In this mode, a 400ns negative pulse will initiate conversion, and the data will automatically appear at the end of conversion. Alternatively, the R/$\overline{C}$ input can be brought low to start conversion, then brought high at any time later (after completion of conversion) to enable the data output lines. Many combinations of the above can be implemented by proper manipulation of the three control lines. Exact timing of these functions is shown.

The A_0 (byte select) and 12/$\overline{8}$ (data format) inputs work together to control the output data and conversion cycle. In almost all situations 12/8 is hard-wired high or low, to V_{LOGIC} or Digital Common. If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface, 12/$\overline{8}$ will be wired low. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by A_0. For these applications, the 4LSB's (pins 16–19) should be hard-wired to the 4MSB's (pins 24–27). Thus, during a read, when A_0 is low the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled, the 4LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 and 23.

The A_0 input performs an additional function of controlling conversion length. If A_0 is held low prior to cycle initiation, a full 12-bit cycle in about 25μs will result; if A_0 is held high prior to cycle initiation a shortened 8-bit cycle in about 16μs will result. The A_0 line must be set prior to cycle initiation and held in the desired position at least until STS goes high. Thus, for microprocessor interface applications, the A_0 line must be properly controlled during both the convert start and read functions.

The STS or status line goes high at the initiation of the conversion cycle and will go low when the cycle is complete.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574

The AD574 contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +15, and −15 volts), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

All of the thin film application resistors of the AD574 are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574K guarantees ±1LSB max zero offset error and ±0.3% (12LSB) max full scale error. (Typical full scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574 easily accommodates an input signal beyond the +15V supply. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 (for a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14.) The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14.

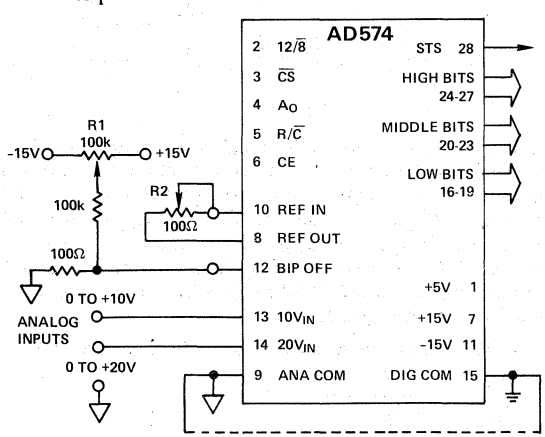


Figure 4. Unipolar Input Connections

UNIPOLAR CALIBRATION

The AD574 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 12 is connected to pin 9, the unit typically will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (−4.9988V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then, a signal is 1 1/2LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

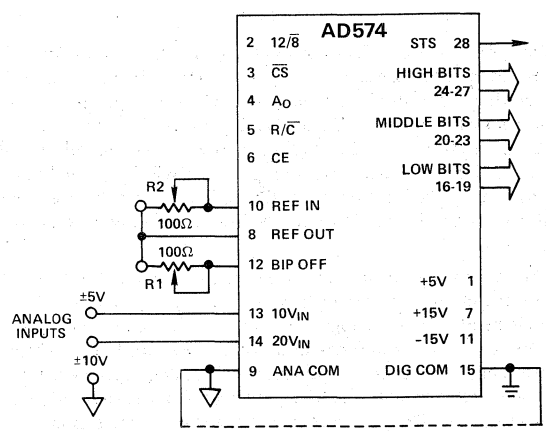


Figure 5. Bipolar Input Connections

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD574 in an environment of high digital noise content, it is recommended that the analog and digital commons be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required.

FULL CONTROL INTERFACE

The AD574 has a versatile set of control functions which will allow interface to a wide variety of microprocessor types as well as much simpler data acquisition systems, and even stand alone applications. It would be impossible to cover all of the potential AD574 control interface situations, but discussion of the two possible extreme situations and their timing will allow extension of the control concepts to most other applications.

STANDARD FULL CONTROL INTERFACE

The timing for the standard full control interface is shown in Figure 6. In this operating mode, $\overline{CS}$ is used as the address input which selects the particular device, R/$\overline{C}$ selects between the read data and start conversion functions, and CE is used to time the actual functions.

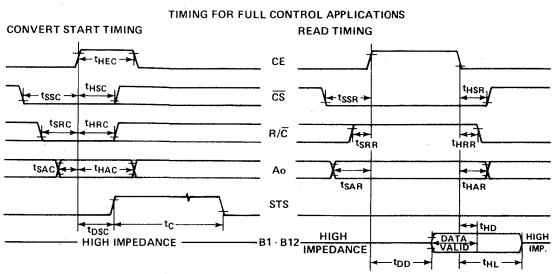


Figure 6.

The left side of the figure shows the conversion start control. $\overline{CS}$ and R/$\overline{C}$ are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and R/$\overline{C}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for $\overline{CS}$ and R/$\overline{C}$ after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The A_0 line determines the conversion cycle length, and must be selected prior to conversion initiation. If A_0 is low, a 12-bit cycle results; if A_0 is high, an 8-bit short cycle results. Minimum set-up and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal is allowed to vary until the STS goes high. It must then be held steady until STS again goes low at the end of conversion.

The data read function operates in a similar fashion except that R/$\overline{C}$ is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the A_0 line now functions as the byte select address, with set-up and hold times as shown. With A_0 low, pins 20 to 27 (DB4–11) come out of three-state and present data. With A_0 high, pins 16–19 (DB0–3) come out of three-state with data and pins 20–23 present active trailing zeros. In the 8-bit mode pins 16–19 will be hard-wired directly to pins 24–27 for direct two-byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low: t_{HD} is the delay until data is no longer valid; t_{HL} is the delay until the outputs are fully into the high impedance state.

TIMING SPECIFICATIONS – FULL CONTROL MODE

t_{DSC}	300ns max	t_{DD}	400ns max
t_{HEC}	300ns min	t_{HD}	100ns min
t_{SSC}	300ns min	t_{SSR}	350ns min
t_{HSC}	200ns min	t_{SRR}	0 min
t_{SRC}	200ns min	t_{SAR}	200ns min
t_{HRC}	200ns min	t_{HSR}	100ns min
t_{SAC}	0 min	t_{HRR}	0 min
t_{HAC}	300ns min	t_{HAR}	100ns min
t_C	15-35μs (12 bit)	t_{HL}	600ns max
	10-20μs (8-bit)		

STAND ALONE OPERATION

For simpler control functions, the AD574 can be controlled with just R/$\overline{C}$. In this case, CE is wired high, $\overline{CS}$ low, 12/$\overline{8}$ high, and A_0 low. There are two ways of cycling the device with this simple hook-up. If a negative pulse is used to initiate conversion as in Figure 7, the converter will automatically bring the 12 data lines out of three-state at the end of conversion. The data will remain valid on the output lines until another pulse is applied.

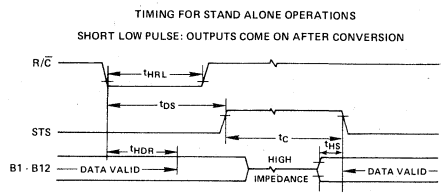


Figure 7.

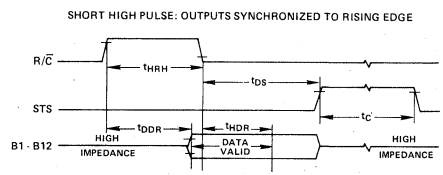


Figure 8.

If the conversion is initiated by a high pulse as shown in Figure 8, the data lines are held in three-state at the end of conversion until R/$\overline{C}$ is brought high. The next conversion cycle is initiated when R/$\overline{C}$ goes low, the data from the previous cycle will remain valid for the time t_{HDR}. An alternative to the above is to toggle R/$\overline{C}$ as needed to initiate a new cycle on read data. Data will appear when R/$\overline{C}$ is brought high, a new cycle is initiated when R/$\overline{C}$ goes low.

TIMING SPECIFICATIONS – STAND ALONE MODE

t_{HRL}	400ns min	
t_{DS}	500ns max	
t_{HDR}	300ns max	
t_{HS}	-100ns min	+200ns max
t_{HRH}	150ns min	
t_{DDR}	350ns max	

t_C (12 bit convert) 15-35μs
t_C (8 bit convert) 10-20μs

Very Fast, Complete 12-Bit A/D Converter

AD578

PRELIMINARY TECHNICAL DATA

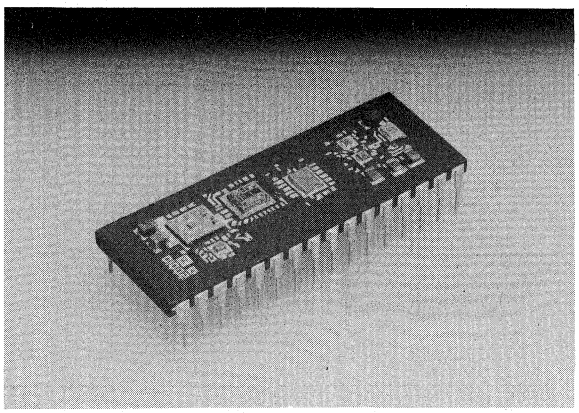
FEATURES

Performance

Complete 12-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 4μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max
Max Nonlinearity: ±0.012%
Low Power: 775mW
"Z" Models for ±12V Supplies
Hermetic Package Available

Versatility

Positive-True Parallel or Serial Logic Outputs
Short Cycle Capability
Precision +10V Reference for External Applications
Adjustable Internal Clock



PRODUCT DESCRIPTION

The AD578 is a high speed 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD578 include a maximum linearity error at +25°C of 0.012%, maximum gain temperature coefficient of ±30ppm/°C, typical power dissipation of 775mW and maximum conversion time of 4μs.

The fast conversion speeds of 4μs (K grade) and 6μs (J, S grades) makes the AD578 an excellent choice in a variety of applications where system throughput rates from 166kHz to 250kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD578 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD578 is available in three different versions. The AD578J and K grades are specified for a guaranteed maximum linearity error of ±3/4LSB over the 0 to +70°C temperature range. The S grade is guaranteed for ±3/4LSB linearity error over -25°C to +100°C, and ±2LSB's over the -55°C to +125°C temperature range. All commercial grade versions (J and K) are packaged in a 32-pin, epoxy sealed, ceramic DIP and the MIL version (S grade) in a solder sealed, hermetic, ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD578 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD578 makes it an excellent choice for high speed data acquisition and digital audio processing applications.
3. The internal buried zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typical T.C. The reference is available externally and can drive up to 1mA loads.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.

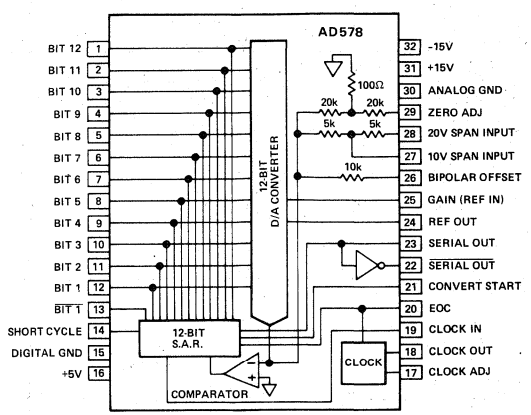


Figure 1. AD578 Functional Diagram and Pinout

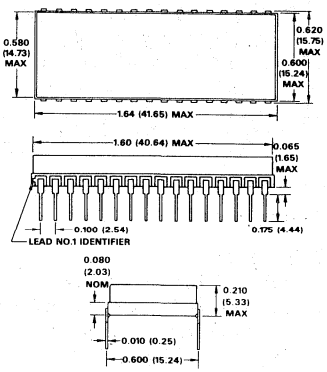
SPECIFICATIONS (typical @ +25°C; ±15V, and +5V unless otherwise noted).

Model	AD578J	AD578K	AD578S
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0V, ±10V	*	*
Unipolar	0 to +10V, 0 to +20V	*	*
Input Impedance			
0 to +10V, ±5V	5kΩ	*	*
±10V, 0 to +20V	10kΩ	*	*
DIGITAL INPUTS			
Convert Command[1]	1TTL Load	*	*
Clock Input	1TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[2,3]	±0.1% FSR, ±0.4% FSR max	*	*
Unipolar Offset[3]	±0.1% FSR, ±0.6% FSR max	*	*
Bipolar Offset[3,4]	±0.1% FSR, ±0.5% FSR max	*	*
Linearity Error			
+25°C	±1/2LSB max	*	*
0 to +70°C	±3/4LSB max	*	
−25°C to +100°C			±3/4LSB max
−55°C to +125°C			±2LSB max
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
+25°C	12 Bits	*	
0 to +70°C	12 Bits	*	
−25°C to +100°C			12 Bits
−55°C to +125°C			11 Bits
POWER SUPPLY SENSITIVITY			
+15V ±10%	3ppm/%ΔV_S typ	*	*
	10ppm/%ΔV_S max	*	*
−15V ±10%	15ppm/%ΔV_S typ	*	*
	25ppm/%ΔV_S max	*	*
+5V ±10%	2ppm/%ΔV_S typ	*	*
	10ppm/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±15ppm/°C typ	*	*
	±30ppm/°C max	*	*
Unipolar Offset	±3ppm/°C typ	*	*
	±10ppm/°C max	±5ppm/°C max	±15ppm/°C max
Bipolar Offset	±8ppm/°C typ	*	*
	±20ppm/°C max	±15ppm/°C max	±25ppm/°C max
Differential Linearity	±2ppm/°C typ	*	*
CONVERSION TIME[5]	6.0μs	4.0μs	6μs
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	5TTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive			
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8TTL Loads		
INTERNAL CLOCK[6]			
Output Drive	2TTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ± 10mV	*	*
External Current	±1mA max	*	*
POWER SUPPLY REQUIREMENTS[7]			
Voltages/Currents			
+15V ±10%	3mA typ, 8mA max	*	*
−15V ±10%	22mA typ, 35mA max	*	*
+5V ±10%	80mA typ, 110mA max	*	*
Power Dissipation	775mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	−55°C to +125°C
Storage	−55°C to +150°C	*	*

NOTES
[1] Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[2] With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.
[3] Adjustable to zero.
[4] With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).
[5] Specifications guaranteed at conversion time listed. To obtain 4μs conversion time for the AD578K, connect a 2k resistor between pins 17 and 18 or use an external clock.
[6] Externally adjustable by a resistor or capacitor.
[7] AD578Z grade available, ±12V ±5%.
*Specifications same as AD578J.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



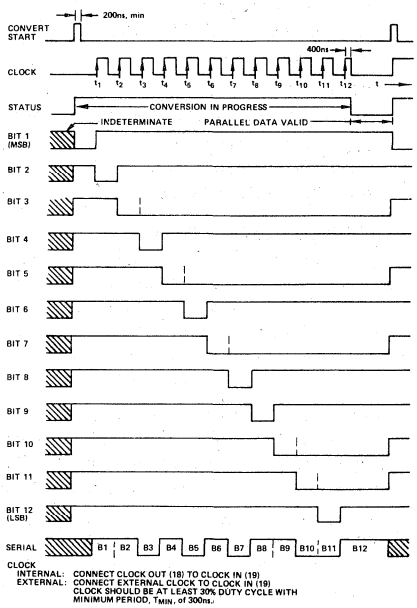


Figure 2. Timing Diagram (Binary Code 110101011001)

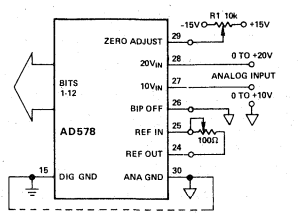


Figure 3. Unipolar Input Connections

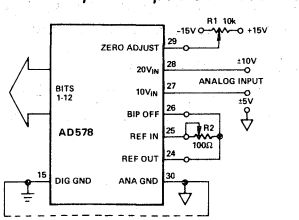


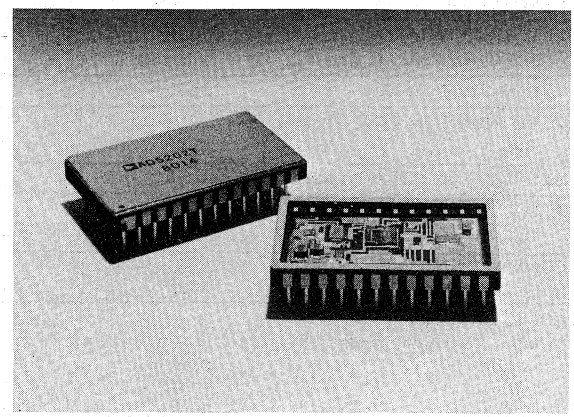
Figure 4. Bipolar Input Connections

ANALOG DEVICES

12-Bit Successive Approximation High Accuracy A/D Converter

AD5200 SERIES

PRELIMINARY TECHNICAL DATA



FEATURES

- True 12-Bit Operation: ±1/2LSB max Nonlinearity
- Totally Adjustment-Free
- Guaranteed No Missing Codes Over the Specified Temperature Range
- Hermetically-Sealed Package
- Standard Temperature Range: -25°C to +85°C
- Military Temperature Range: -55°C to +125°C
- MIL-STD-883 Processing Available
- Serial and Parallel Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count for High Reliability
- Industry Standard Pin Out
- Small 24-Pin DIP

GENERAL DESCRIPTION

The AD5200 series devices are 12-bit successive approximation analog-to-digital converters. The hybrid design utilizes MSI digital, linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide a totally adjustment free converter—no potentiometers are required for calibration.

The innovative design of the AD5200 series devices incorporates a monolithic 12-bit feedback DAC for reduced chip count and higher reliability. The exceptional temperature coefficients of the monolithic DAC guarantees ±1/2LSB linearity over the entire operating temperature range of -25°C to +85°C for the commercial grade and -55°C to +125°C for the military grade.

The AD5200 series converters are available in 2 input voltage ranges: ±5V (AD5201/AD5204) and ±10V (AD5202/AD5205). The converters are available either complete with an internal buried zener reference or with the option of an external reference for improved absolute accuracy.

The AD5200 series converters are available in four performance grades; the "A" and "B" are specified from -25°C to +85°C and the "S" and "T" are specified from -55°C to +125°C. The "S" and "T" grades are also available processed to MIL-STD-883 level B requirements. All units are available in a 24-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD5200 series devices are laser trimmed at the factory to provide a totally adjustment free converter—no potentiometers are required for 12-bit performance.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The AD5200 series directly replaces other devices of this type with significant increases in performance.
4. The devices offer true 12-bit accuracy and exhibits no missing codes over the entire operating temperature range.
5. The fast conversion rate of the AD5200 series makes it an excellent choice for applications requiring high system throughput rate.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

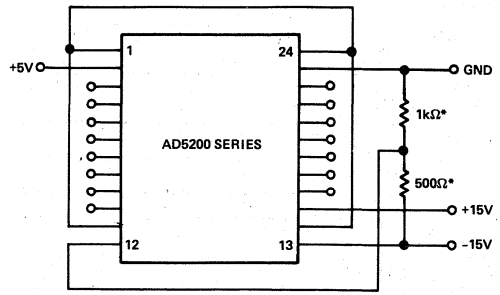
INPUT RANGE	INPUT IMPEDANCE				
-5V to +5V	5.0kΩ	AD5201A, S	AD5201B, T	AD5204A, S	AD5204B, T
-10V to +10V	10.0kΩ	AD5202A, S	AD5202B, T	AD5205A, S	AD5205B, T
REFERENCE		Internal	*	External -10.000V	External -10.000V
RESOLUTION		12 Bits	*	*	*
LINEARITY MAX		1LSB	1/2LSB	*	**
No Missing Codes T_{min} to T_{max}		Guaranteed	*	*	*
ZERO ERROR, MAX		2LSB	1LSB	*	**
ZERO ERROR, MAX T_{min} to T_{max}		4LSB	2LSB	*	**
ABSOLUTE ACCURACY, MAX		4LSB	2LSB	*	**
ABSOLUTE ACCURACY, MAX T_{min} to T_{max}		±0.4% FSR[1]	±0.2 of FSR[1]	**	±0.1% FSR[1]
CONVERSION TIME, MAX Clock = 260kHz		50μs	*	*	*
LOGIC RATINGS					
Input Logic Commands					
Logic "0"		0.8V max	*	*	*
Logic "1"		+2.0V min	*	*	*
Loading		0.5TTL Load	*	*	*
CLOCK INPUT PULSE WIDTH		100ns min	*	*	*
OUTPUT LOGIC					
Logic "0"		0.4V max	*	*	*
Logic "1"		3.6V (2.4 min)	*	*	*
FANOUT - HIGH		8TTL Loads	*	*	*
FANOUT - LOW		2TTL Loads	*	*	*
POWER SUPPLY REQUIREMENTS					
V_{LOGIC}		+5V±10%	*	*	*
V_{CC}		+15V±10%	*	*	*
V_{DD}		-15V±10%	*	*	*
OPERATING CURRENT					
V_{LOGIC}		25mA (42mA max)	*	*	*
V_{CC}		10mA (25mA max)	*	*	*
V_{DD}		25mA (35mA max)	*	*	*
V_{REF}				0.5mA max	0.5mA max
POWER SUPPLY REJECTION					
V_{CC}		±0.005%/%	*	*	*
V_{DD}		±0.005%/%	*	*	*
POWER CONSUMPTION		725mW	*	*	*
OPERATING TEMPERATURE RANGE					
-25°C to +85°C		"A" Version	"B" Version	*	**
-55°C to +125°C		"S" Version	"T" Version	*	**

*Same specifications as AD5201/2A, S.
**Same specifications as AD5201/2B, T.
[1] FSR is Full Scale Range and is equal to the peak to peak input signal.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Positive Supply	+18V
Negative Supply	−18V
Logic Supply	+7V
Analog Input	±25V
Digital Outputs	Logic Supply
Digital Inputs	+5.5V
Reference Supply	−15V



Burn In Circuit

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all models of the AD5200 receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Stabilization Bake	24 hours @ +150°C
3. Seal Test, Gross	In-House Criteria
4. Operating Burn-In	48 hours @ +125°C

PROCESSING TO MIL-STD-883

All models ordered to the requirements of MIL-STD-883, Method 5008, Class B are identified with a /883 suffix, and receive the following processing:

1. Pre-Cap Visual Inspection	2010, Test Condition B
2. Stabilization Bake	1008, 24 hours @ +150°C
3. Temperature Cycling	1010, Test Condition C, 10 cycles, −65°C to +150°C
4. Constant Acceleration	2001, Y_1 plane, 5000G
5. Seal Test, Fine and Gross	1014, Test Condition A and C
6. Operating Burn-In	1015, Test Condition B, 160 hours @ +125°C
7. Final Electrical Testing	Performed at max and min operating temperatures
8. External Visual Inspection	2009

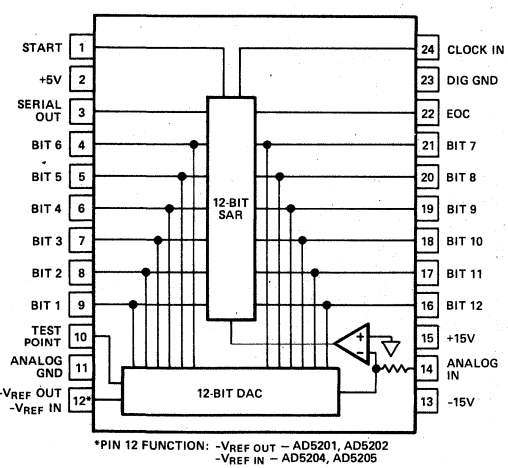
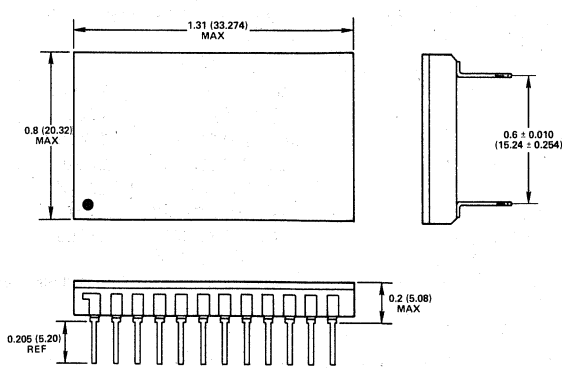


Figure 1. Pin Designations

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



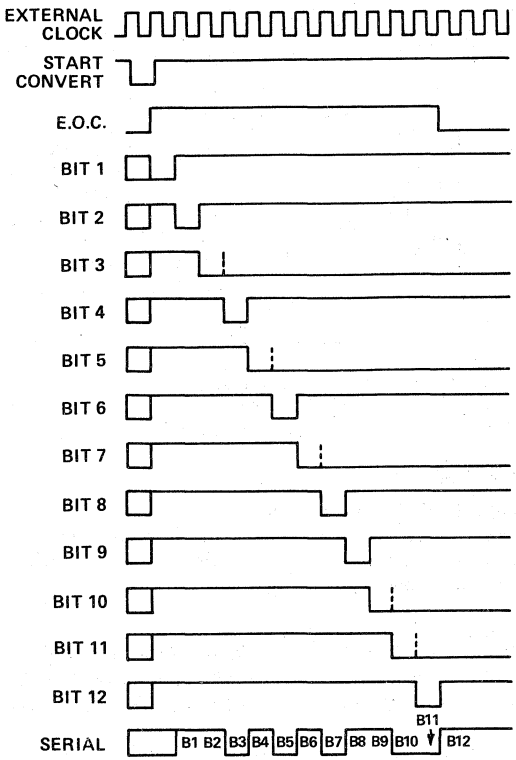


Figure 2. Timing Diagram

TIMING

The timing diagram is shown in Figure 2. A conversion is initiated by holding the start convert low during a rising edge of the clock. The start convert transition must occur at a minimum of 25ns prior to the clock transition. The end of conversion (E.O.C.) signal will be set simultaneously with the initiation of conversion. The actual conversion will not start until the first rising edge of the clock after the start convert is again set high.

Parallel data is valid on the falling edge of the E.O.C. and it will remain valid until the next conversion is initiated. The serial data is in the Non-Return To Zero format and it is valid on the same transition as the parallel data.

An external clock of 260kHz will yield 50μs conversion time. Increasing the clock frequency will decrease the conversion time; the linearity error, however, will increase. Refer to Figure 3 for the acceptable minimum conversion time.

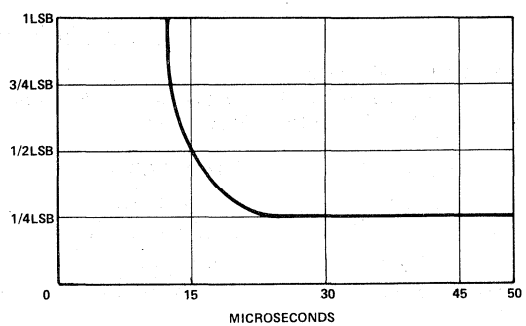


Figure 3. Linearity Error vs. Conversion Time (Normalized)

AD5201/AD5204	AD5202/AD5205	MSB LSB
+5.0000V	+10.000V	0000000000
0.0000V	0.000V	1000000000
-4.9976V	- 9.995V	1111111111

Table 1. Logic Coding (Complementary Offset Binary)

AD5200 SERIES ORDERING GUIDE

Model	Linearity	Absolute Accuracy	Temperature Range
AD520*AD	1LSB	4LSB	-25°C to +85°C
AD520*BD	1/2LSB	2LSB	-25°C to +85°C
AD520*SD	1LSB	4LSB	-55°C to +125°C
AD520*TD	1/2LSB	2LSB	-55°C to +125°C
AD520*SD/883	1LSB	4LSB	-55°C to +125°C
AD520*TD/883	1/2LSB	2LSB	-55°C to +125°C

*Insert number according to desired input voltage range.

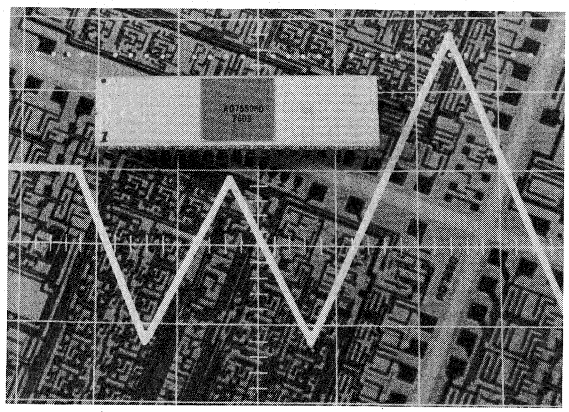
ANALOG DEVICES

CMOS 13-Bit Monolithic A/D Converter

AD7550

FEATURES

- Resolution: 13 Bits, 2's Complement
- Relative Accuracy: ±1/2 LSB
- "Quad Slope" Precision
  - Gain Drift: 1ppm/°C
  - Offset Drift: 1ppm/°C
- Microprocessor Compatible
- Ratiometric
- Overrange Flag
- Very Low Power Dissipation
- TTL/CMOS Compatible
- CMOS Monolithic Construction



GENERAL DESCRIPTION

The AD7550 is a 13-bit (2's complement) monolithic CMOS analog-to-digital converter on a 118 x 125 mil die packaged in a 40-pin ceramic DIP. Outstanding accuracy and stability (1ppm/°C) is obtained due to its revolutionary integrating technique, called "Quad Slope" (Analog Devices patent No. 3872466). This conversion consists of four slopes of integration as opposed to the traditional dual slope and provides much higher precision.

The AD7550 parallel output data lines have three-state logic and are microprocessor compatible through the use of two enable lines which control the lower eight LSB's (low byte enable) and the five MBS's (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

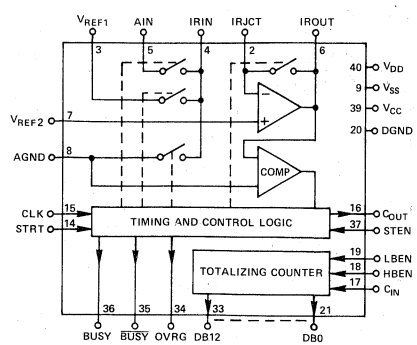
The AD7550 conversion time is about 40ms with a 1MHz clock. Clock can be externally controlled or internally generated by simply connecting a capacitor to the clock pin. A positive start pulse can be self-generated by having a capacitor on the start pin or can be externally applied.

For most applications, the AD7550 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

A wide range of power supply voltages (±5V to ±12V) with minuscule current requirements make the AD7550 ideal for low power and/or battery operated applications. Selection of the logic (V_{CC}) supply voltage (+5V to V_{DD}) provides direct TTL or CMOS interface on the digital input/output lines.

The AD7550 uses a high density CMOS process featuring double layer metal and silicon nitride passivation to ensure high reliability and long-term stability.

FUNCTIONAL DIAGRAM



SPECIFICATIONS (VDD = +12V, VSS = -5V, VCC = +5V, VREF1 = +4.25V unless otherwise noted)[2]

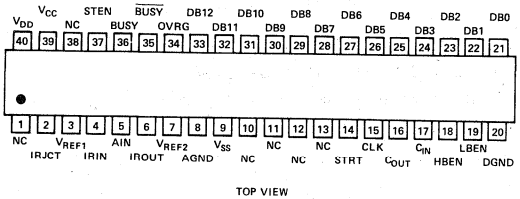
PARAMETER	TA = +25°C	OVER SPECIFIED TEMPERATURE RANGE	TEST CONDITIONS
ACCURACY			
Resolution		13 Bits 2's Comp min	
Relative Accuracy	±1LSB max	±1 LSB max	f_{CLK} = 500kHz, R_1 = 1MΩ,
Gain Error	±1LSB max		C_1 = 0.01μF, IRJCT Voltage
Gain Error Drift	1ppm/°C typ		Adjusted to $\frac{V_{REF1}}{2}$ ±0.6%
Offset Error	±0.5LSB max		
Offset Error Drift	1ppm/°C typ		
ANALOG INPUTS			
AIN Input Resistance[1]	R1MΩ min		
V_{REF1} Input Resistance[1]	R1MΩ min		
V_{REF2} Leakage Current	10pA typ		
DIGITAL INPUTS			
CIN, LBEN, HBEN, STEN			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+2.4V min	+2.4V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}, I_{INH}	5nA typ		
START			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V to V_{DD}
V_{INH}	+2.4V min	+2.4V min	
I_{INL}	−1μA typ		V_{CC} = +5V to V_{DD}, BUSY = Low
I_{INH}	+150μA typ		V_{CC} = +5V to V_{DD}, BUSY = High
CLOCK			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+3V min	+3V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}	−100μA typ		$V_{IN} \neq V_{INL}$; V_{CC} = +5V to +12V
I_{INH}	+100μA typ		$V_{IN} = V_{INH}$; V_{DD} = +5V to +12V
DIGITAL OUTPUTS			
V_{OUTL}	+0.5V max	+0.8V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OUTH}	+2.4V min	+2.4V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OUTL}	+1.2V max	+1.2V max	V_{CC} = +12V, I_{SINK} = 1.6mA
V_{OUTH}	+10.8V min	+10.8V min	V_{CC} = +12V, I_{SOURCE} = 0.6mA
Capacitance (Floating State) (OVRG, BUSY, BUSY, and DB0–DB12)	5pF typ		
I_{LKG} (Floating State) (OVRG, BUSY, BUSY, and DB0–DB12)	±5nA typ		V_{CC} = +5V to +12V V_{OUT} = 0V and V_{CC}
DYNAMIC PERFORMANCE			
Conversion Time	90ms typ		$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 500kHz
	40ms typ		$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 1MHz
STEN, HBEN, LBEN Propagation Delay t_{ON}, t_{OFF}	250ns typ, 500ns max		V_{IN}(STEN, HBEN, LBEN) 0 to +3V
External STRT Pulse Duration	800ns min		$V_{IN(STRT)}$ = 0 to +3V
POWER SUPPLIES			
V_{DD} Range	+10V min, +12V max		
V_{SS} Range	−5V min, −12V max		
V_{CC} Range	+5V min, V_{DD} max		
I_{DD}	0.6mA typ, 2mA max		
I_{SS}	0.3mA typ, 2mA max		f_{CLK} = 1MHz
I_{CC}	0.06mA typ, 2mA max		

[1] The equivalent input circuit is the integrator resistor R_1 (1MΩ min, 10MΩ max) in series with a voltage source $\frac{V_{REF1}}{2}$, (see Figure 1).

[2] Full Scale Voltage = ±VREF1 ÷ 2.125. For VREF1 = +4.25V, FS voltage is ±2.000V.

Specifications subject to change without notice.

PIN CONFIGURATION



TOP VIEW

ORDERING INFORMATION

Model	Temperature Range	Package
AD7550BD	−25°C to +85°C	Ceramic

ABSOLUTE MAXIMUM RATINGS

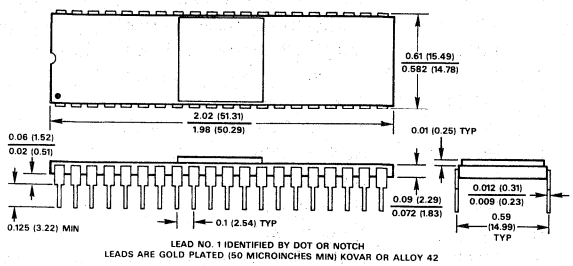
V_{DD} to AGND . . . . . 0V, +14V
V_{DD} to DGND . . . . . 0V, +14V
V_{SS} to AGND . . . . . 0V, −14V
V_{SS} to DGND . . . . . 0V, −14V
AGND to DGND . . . . . 0V, +14V
V_{CC} to DGND . . . . . .0V, V_{DD}
V_{REF1} . . . . . V_{SS}, V_{DD}
V_{REF2} . . . . . AGND, V_{DD}
AIN . . . . . V_{SS}, V_{DD}
IRIN . . . . . V_{SS}, V_{DD}
IRJCT . . . . . AGND, V_{DD}
IROUT . . . . . V_{SS}, V_{DD}
Digital Input Voltage
HBEN, LBEN, STEN, C_{IN} . . . . . DGND, (DGND +27V)
CLK, START . . . . . DGND, V_{DD}
Digital Output Voltage
DB0–DB12, OVRG, BUSY, $\overline{BUSY}$, C_{OUT} . . . DGND, V_{CC}
Power Dissipation (Package)
Up to +50°C 1000mW
Derates above +50°C by . . . . . 10mW/°C
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . −25°C to +85°C

CAUTION:

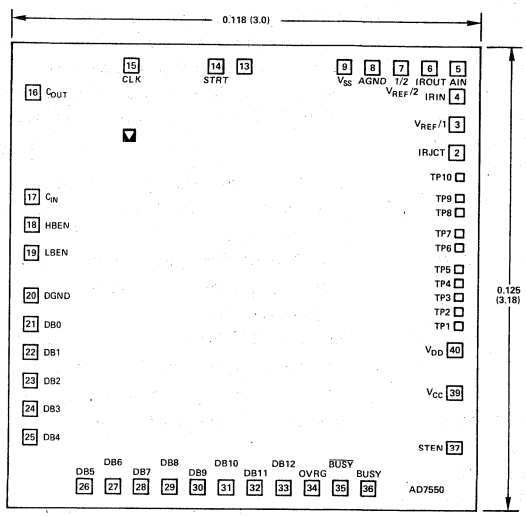
1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.
2. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



40-Pin Ceramic Dip



Bonding Diagram

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V_{REF1}	Voltage REFerence Input
4	IRIN	IntegratoR INput. External integrator input R is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Fullscale AIN equals $V_{REF}/2.125$.
6	IROUT	IntegratoR OUTput. External integrating capacitor C_I is connected between IROUT and IRJCT.
7	V_{REF2}	Voltage REFerence ÷ 2 Input
8	AGND	Analog GrouND
9	V_{SS}	Negative Supply (-5V to -12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1," the AD7550's digital logic is set up and BUSY is latched "high." When STRT returns "low," conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 800 nanoseconds to ensure proper set-up of the AD7550 logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C_{OUT}	Count OUT provides a number (N) of gated clock pulses given by: $N = \left[\frac{AIN}{V_{REF1}} \; 2.125 + 1\right] \; 4096$
17	C_{IN}	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C_{OUT} is connected to C_{IN}.
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8-DB12 data outputs. When HBEN is low, the DB8–DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0–DB7. When LBEN is "low," DB0–DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVerRange indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2 LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$, and OVRG.
38	NC	No Connection
39	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible if V_{CC} = +5V, CMOS compatible for V_{CC} = +10V to V_{DD}.
40	V_{DD}	Positive Supply +10V to +12V.

PRINCIPLES OF OPERATION

BASIC OPERATION

The essence of the quad slope technique is best explained through Figures 1 and 2.

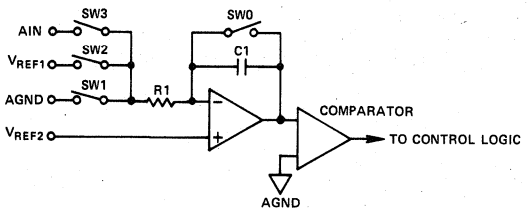


Figure 1. Quad Slope Integrator Circuit

The inputs AGND (analog ground), V_{REF1}, AIN (analog input) and V_{REF2} are applied in sequence to an integrator (Figure 1), creating four slopes (phases 1 through 4, Figure 2) at the integrator output. Voltage V_{REF2} is normally equal to $\frac{V_{REF1}}{2}$, but if not, will create an error count "n" that will be minimized by the "quad-slope" conversion process. V_{REF1} and V_{REF2} must be positive voltages.

The equivalent integrator input voltages and their integration times are shown in Table 1.

TABLE 1
INTEGRATOR EQUIVALENT INPUT VOLTAGES AND INTEGRATION TIMES

Phase	Input Voltage	Integration Time
1	$AGND-V_{REF2}$	$t_1 = K_1t$
2	$V_{REF1}-V_{REF2}$	$t_2 = (K_1 + n)t$
3	$AIN-V_{REF2}$	$t_3 = (2K_1 - n)t$
4	$V_{REF1}-V_{REF2}$	$t_4 = (K_3 - 2K_1 + n - 2N)t$

where:
- t = The CLK period
- n = System error count
- K_1 = A fixed count equal to 4352 counts
- K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
- K_3 = A fixed count equal to 25600 counts
- N = Digital output count corresponding to the analog input voltage, AIN

PHASE 0

After the start pulse is applied, switch SW2 is closed (all other switches open) and the integrator output is ramped to comparator zero crossing. Phase 0 can be considered the reset phase of the converter, and always has a duration $t_0 = R_1C_1$ (integrator time constant). Upon zero crossing, counters K_1 and K_2 are started, switch SW2 is opened and SW1 is closed.

PHASE 1

Phase 1 integrates ($AGND - V_{REF2}$) for a fixed period of time (by counter K_1) equal to $t_1 = K_1t$. At the end of phase 1, switch SW1 is opened and SW2 is closed.

PHASE 2

The integrator input is switched to ($V_{REF1}-V_{REF2}$) and the output ramps down until zero crossing is achieved. The integration time $t_2 = (K_1 + n)t$ includes the error count "n" due to offsets, etc. At the end of phase 2, switch SW2 is opened, SW3 is closed, and a third counter (K_3) is started.

PHASE 3

Phase 3 integrates the analog input ($AIN - V_{REF2}$) until counter K_2 counts $4K_1t$. At this time SW3 is opened and SW2 is closed again.

PHASE 4

Phase 4 integrates ($V_{REF1}-V_{REF2}$) and the comparator output ramps down until zero crossing once again is achieved. Since the comparator always approaches zero crossing from the same slope, propagation delay is constant and hysteresis effect is eliminated.

Notes
1. $t = 1/f_{CLK}$
2. Time periods shown in BOLD are unaffected by n since they are determined by counters K_1, K_2, or K_3
3. STEN = LOGIC 1. If STEN = 0, BUSY and $\overline{BUSY}$ are in floating state

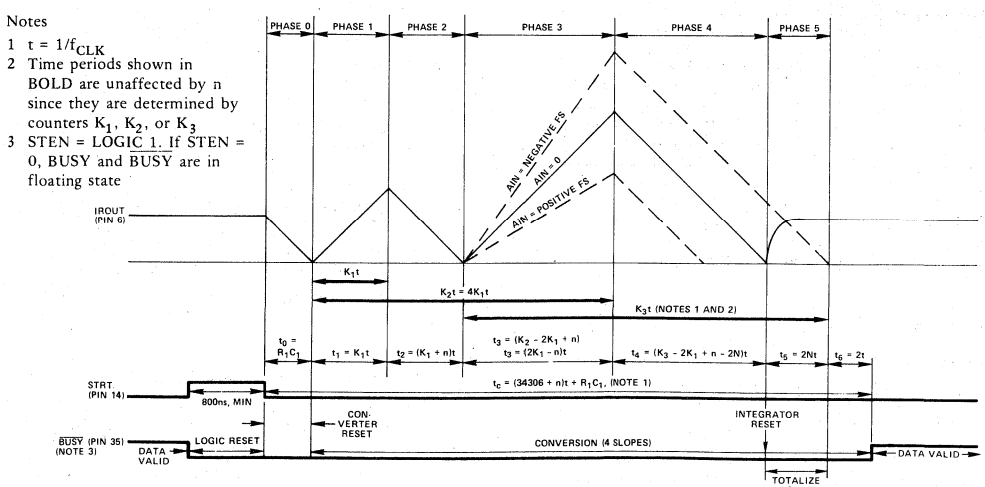


Figure 2. Quad Slope Timing Diagram

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the C_{OUT} terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

(EQN 1)

$$N = \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal transfer function}} + \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot \left[\frac{AGND}{V_{REF1}}(1 + 2\alpha) - \alpha^2\right] \cdot 2K_1}_{\text{error term}}$$

where:

$$\alpha = \frac{2V_{REF2} - V_{REF1}}{V_{REF1}}$$

The ideal case assumes:

$AGND = 0V$

$V_{REF2} = \frac{V_{REF1}}{2}$, therefore $\alpha = 0$

Then (EQN 1) simplifies to:

$$N = \frac{AIN}{V_{REF1}} \cdot 8704 + 4096 \qquad \text{(EQN 2)}$$

or

$$N = \frac{AIN}{V_{FS}} \cdot 4096 + 4096 \qquad \text{(EQN 3)}$$

where:

V_{FS} = full scale input voltage = $\frac{V_{REF1}}{2.125}$

The parallel output (DB0–DB12) of the AD7550 represents the number N in binary 2's complement coding when the C_{OUT} pin is connected to the C_{IN} pin (see Table II).

TABLE II
OUTPUT CODING (Bipolar 2's Complement)

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)			
		OVRG	DB12		DB0
+Overrange	–	1	0	1111 1111 1111	
+VFS ($1-2^{-12}$)	8191	0	0	1111 1111 1111	
+VFS (2^{-12})	4097	0	0	0000 0000 0001	
0	4096	0	0	0000 0000 0000	
-VFS (2^{-12})	4095	0	1	1111 1111 1111	
-VFS	0	0	1	0000 0000 0000	
-Overrange	–	1	1	0000 0000 0000	

Notes
1 $V_{FS} = \frac{V_{REF1}}{2.125}$
2 N = number of counts at C_{OUT} pin
3 C_{OUT} strapped to C_{IN}; LBEN and HBEN = Logic 1

ERROR ANALYSIS

Equation 1 shows that only α and AGND generate error terms. Their impact can be analyzed as follows:

Case 1: $AGND = 0, \alpha \neq 0$

Error sources such as capacitor-leakage (I_L) and op amp offset (e) cause α to be different from zero.

Under this condition,

$$\alpha = \frac{2(e + I_L R_1)}{V_{REF1}}$$

where $I_L R_1$ is the equivalent error voltage generated by leakage I_L.

The evaluation of this error term is best demonstrated through the following example:

Assume:

$e = 5mV$, $I_L = 5nA$, $R_1 = 1M\Omega$ and $V_{REF1} = 4.25V$.

Then:

$\alpha = 4.7 \times 10^{-3}$

and:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \times 8704 + 12800 - \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \times 22.1 \times 10^{-6} \times 8704}_{\text{error term } N_\epsilon}$$

Therefore, the error count N_ϵ is as follows:

For AIN = $-V_{FS}$: N_ϵ = 0.28 counts = 0.28LSB
AIN = 0: N_ϵ = 0.19 counts = 0.19LSB
AIN = $+V_{FS}$: N_ϵ = 0.09 counts = 0.09LSB

The above example shows the strong reduction of the circuit errors because of the α^2 term in (EQN 1). Another consequence of this effect is that N_ϵ is always positive, regardless of the polarity of the circuit errors.

Case 2: $AGND \neq 0, \alpha = 0$

When AGND is different from the signal ground, then this error will come through on a first-order basis. Indeed:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \cdot 8704 + 12800 + \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \cdot \frac{AGND}{V_{REF1}}}_{\text{error term } N_\epsilon}$$

The following example demonstrates the impact of AGND.

Let AGND = 1mV and $V_{REF1} = 4.25V$.

For AIN = $-V_{FS}$, then N_ϵ = 3.01 counts
AIN = 0, then N_ϵ = 2.05 counts
AIN = + V_{FS}, then N_ϵ = 1.08 counts

Therefore, ground loops should be minimized because a 330μV difference between AGND and signal ground will cause 1 count (1 LSB) of error when the analog input is at minus full scale. An optimized ground system is shown in Figure 7.

OPERATING GUIDELINES

The following steps, in conjunction with Figure 3, explain the calculations of the component values required for proper operation.

1. DETERMINATION OF V_{REF1}

When the full scale voltage requirement (VFS) has been ascertained, the reference voltage can be calculated by:

$V_{REF1} = 2.125\ (V_{FS})$

V_{REF1} must be positive for proper operation.

2. SELECTION OF C_3 (INTERNAL CLOCK OPERATION)

For internal clock operation, connect capacitor C_3 to the clock pin as shown in Figure 3. The clock frequency versus capacitor C_3 is shown in Figure 4.

The clock frequency must be limited to 1.3MHz for proper operation.

3. SELECTION OF INTEGRATOR COMPONENTS (R_1 AND C_1)

To ensure that the integrator's output doesn't saturate to its bound (V_{DD}) during the phase (3) integration cycle, the integrator time constant (R_1C_1) should be approximately equal to:

$$\tau = R_1C_1 = \frac{V_{REF}\ (9 \times 10^3)}{f_{CLK}\ (V_{DD} - 4V)}$$

The integrator components R_1 and C_1 can be selected by referring to Figure 5 and/or Figure 6. Figure 5 plots the time constant (R_1C_1) versus clock frequency for different reference voltages. Figure 6 is a direct plot of the required C_1 versus f_{CLK} for R_1 values of 1MΩ and 10MΩ.

R_1 can be a standard 10% resistor, but must be selected between 1MΩ to 10MΩ.

The integrating capacitor "C_1" must be a low leakage, low dielectric absorption type such as teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C_1 must be connected to IR_{OUT}.

4. CONVERSION TIME

As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

$$t_{convert} = t_{STRT} + \frac{34306}{f_{CLK}} + R_1C_1$$

where:

t_{STRT} = STRT pulse duration
R_1C_1 = Integrator Time Constant
f_{CLK} = CLK Frequency

For example, if $V_{REF1} = 4.25V$, $R_1 = 1M\Omega$, $C_1 = 400pF$ and CLK = 1MHz, the conversion time (not including t_{STRT}, which is normally only microseconds in duration) is approximately 40 milliseconds.

5. EXTERNAL OR AUTO STRT OPERATION

The STRT pin can be driven externally, or with the addition of C_2, made to self-start.

The size of C_2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

$t_{DAV} \approx (1.7 \times 10^6\Omega)\ C_2 + 20\mu s$

When first applying power to the AD7550, a 0V to V_{DD} positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation.

6. INITIAL CALIBRATION

Trim R_4 (Figure 3) so that pin 2 (IRJCT) equals 1/2 V_{REF1} ±0.6%. When measuring the voltage on IRJCT, apply a Logic "1" to the STRT terminal.

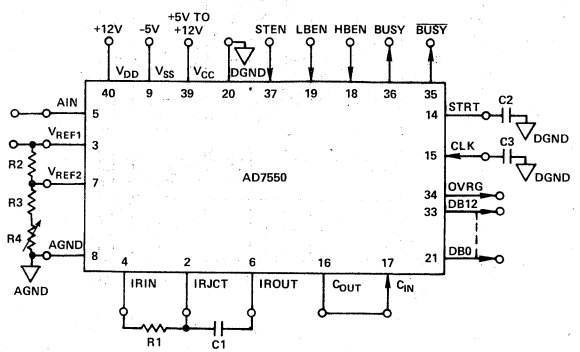


Figure 3. Operation Diagram

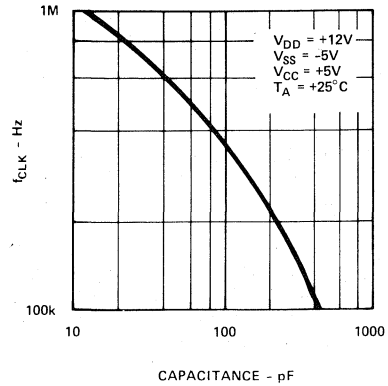


Figure 4. f_{CLK} vs. C_3

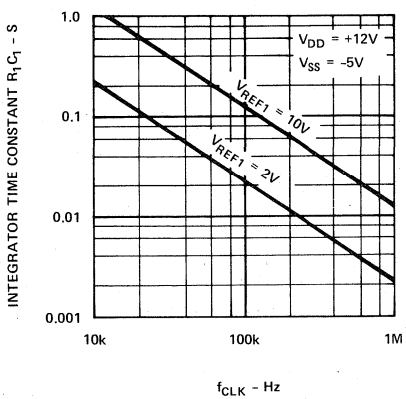


Figure 5. Integrator Time Constant (R_1C_1) vs. f_{CLK} for Different Reference Voltages

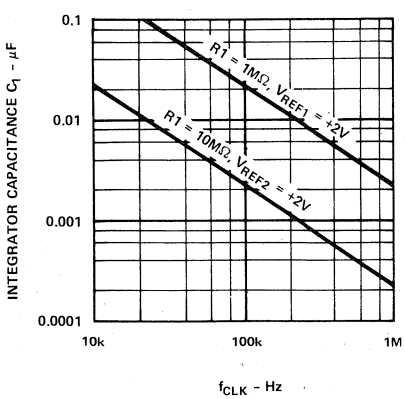


Figure 6. Integrator Capacitance (C_1) vs. f_{CLK} for Different Integrator Resistances (R_1)

APPLICATION HINTS

When operating at f_{CLK} greater than 500kHz, the following steps are recommended to minimize errors due to noise coupling (see Figure 7).

1. Decouple AIN (pin 5), V_{REF1} (pin 3) and V_{REF2} (pin 7) through 0.01µF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R_1 and C_1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C_1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying $\overline{\text{STEN}}$ to the 1 state and driving HBEN and LBEN with $\overline{\text{BUSY}}$. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.

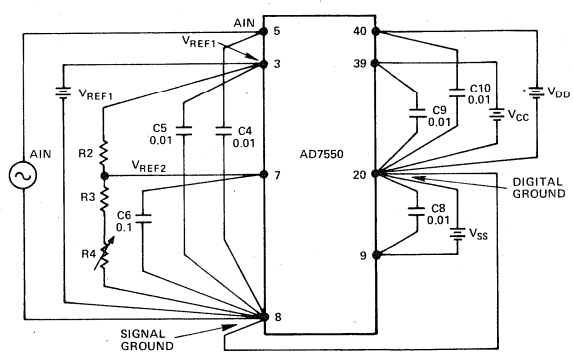


Figure 7. Ground System

ANALOG DEVICES

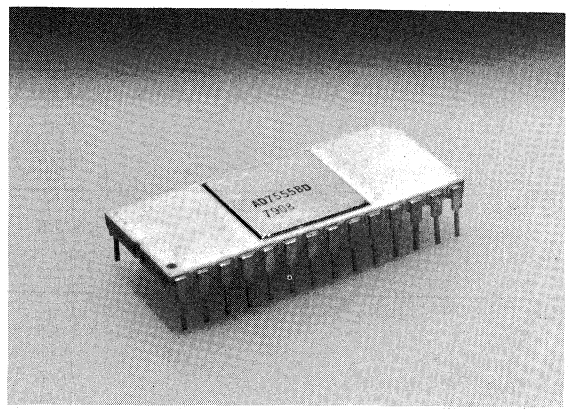
CMOS 4½ / 5½ Digit ADC Subsystem

AD7555

PRELIMINARY TECHNICAL DATA

FEATURES

- **Resolution: ±4 1/2 Digits BCD or ±20k Count Binary Capability for 5 1/2 Digit Resolution or Custom Data Formats**
- **Data Format: Multiplexed BCD (for Display) and Serial Count (for External Linearization, Data Reformatting, or Microprocessor Interface)**
- **Accuracy: ±1 Count in ±20k Counts**
- **Scale Factor Drift: 0.2ppm/°C Using Only Medium-Precision Op Amps**
- **Requires only a Single Positive Reference**
- **Overrange Display**
- **Auto Calibration Capability**
- **Interfaces to TTL or 5V CMOS**
- **$\overline{\text{HOLD}}$ Input and SCC (System Conversion Complete) Output for Interface Flexibility**

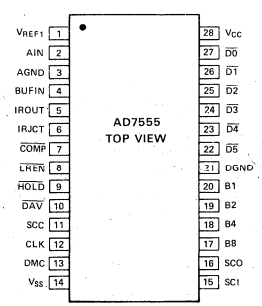


GENERAL DESCRIPTION

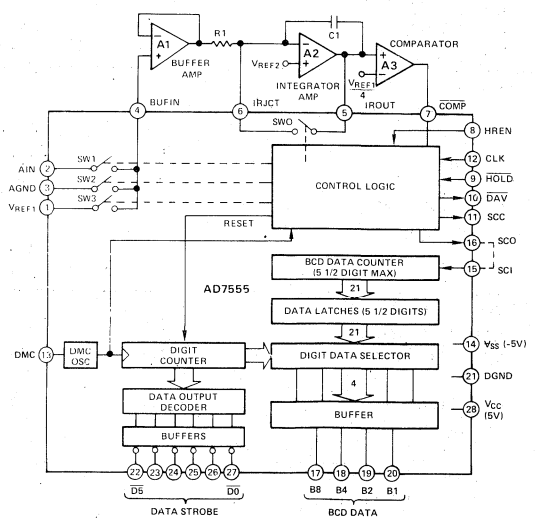
The AD7555 is a 4 1/2 digit, monolithic CMOS, quad slope integrating ADC subsystem designed for display or microprocessor interface applications. Use of the high resolution enable input expands the display format to 5 1/2 digits BCD. With SCO (Serial Count Out) connected to SCI (Serial Count In), the output data format is multiplexed BCD suitable for visual display purposes. As an added feature, SCO can also be used with rate multipliers for linearization, or with BCD or binary counters for data reformatting (up to 200k binary counts).

The quad slope conversion algorithm (Analog Devices patent No. 3872466) converts the external amplifier's input drift errors to a digital number and subsequently reduces the total system drift error to a second order effect. Using only inexpensive, medium-precision amplifiers a scale factor drift of 0.2ppm/°C is achieved.

PIN CONFIGURATION



AD7555 FUNCTIONAL DIAGRAM



ORDERING INFORMATION

Model	Package	Operating Temperature Range
AD7555BD	28 Pin Side Brazed Ceramic	-25°C to +85°C
AD7555KN	28 Pin Molded Plastic	0 to +70°C

SPECIFICATIONS (V_{CC} = +5V, V_{SS} = -5V, V_{REF1} = +4.0960V, F_{CLK} = 614.4kHz, AGND = 0V)

PARAMETER	LIMIT AT T_A = +25°C	LIMIT AT T_A = T_{min}, T_{max}	UNITS	CONDITIONS/COMMENTS
ANALOG SWITCHES				
R_{ON} (Switch 1-3)	800	1200	Ω max	-2V ≤ AIN ≤ +2V Refer to Functional Diagram
ΔR_{ON} (Switch 1) versus AIN	300	500	Ω typ	-2V ≤ AIN ≤ +2V
Mismatch Between Any Two Switches (excluding SW0)	300	500	Ω typ	-2V ≤ AIN ≤ +2V
I_{LKG} (Switch OFF)				
SW0 (pin 6)	1	70	nA max	IRJCT (pin 5) = +2.048V 0V ≤ IROUT (pin 5) ≤ +10V
SW1 (pin 2)	1	70	nA typ	AIN = +2V to -2V, BUFIN = 0V and +4.096V
SW2 (pin 3)	1	70	nA typ	AGND = 0V, BUFIN = -2V to +2V, +4.096V
SW3 (pin 1)	1	70	nA typ	V_{REF1} = +4.096V, BUFIN = -2V to +2V
I_{LKG} (BUFIN, pin 4)	3	200	nA typ	Any 1 of SW1, 2, 3 on
CONTROL INPUTS (pins 7, 8, 9, 15)				
V_{INH}	3.0	3.0	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} or I_{INL}	1	10	µA max	V_{IN} = 0V or V_{CC}
CLOCK INPUTS (pin 12 and 13)				
V_{INH} (CLK)	3.5	3.5	V min	
V_{INL} (CLK)	0.8	0.8	V max	
V_{INH} (DMC)	3.0	3.0	V min	
V_{INL} (DMC)	0.8	0.8	V max	
I_{INH} (CLK)	1.0	1.5	mA max	
I_{INL} (CLK)	-1.0	-1.5	mA max	
I_{INH} (DMC)	200	300	µA max	
I_{INL} (DMC)	-100	-150	µA max	
DIGITAL OUTPUTS				
$\overline{D0}$ - $\overline{D5}$ (pins 22-27)				
V_{OH}	4.5	4.5	V min	I_{SOURCE} = 40µA
V_{OL}	4.0	4.0	V max	I_{SINK} = 5mA (Display Driver Load)
V_{OL}	0.5	0.8	V max	I_{SINK} = 1.6mA (TTL Load)
B1, B2, B4, B8, $\overline{DAV}$, SCC, SCO (pins 20, 19, 18, 17, 10, 11, 16)				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 40µA
V_{OL}	0.5	0.8	V max	I_{SINK} = 1.6mA
DYNAMIC PERFORMANCE				
DMC Pulse Width	5	5	µs min	See Figure 3
DMC Frequency	100	100	kHz max	Typical f_{DMC} is 1.5kHz with C_{DMC} = 0.01µF
CLK Frequency	1.5	1.5	MHz max	
Propagation Delays				
DMC HIGH to $\overline{DAV}$ HIGH	5	7	µs max	See Figure 3
DMC HIGH to $\overline{DAV}$ LOW	5	7	µs max	
DMC HIGH to BCD Data on B8, B4, B2, B1	5	5	µs max	
DMC LOW to Digit Strobe (D0 - D5) LOW	5	5	µs max	
POWER SUPPLY				
I_{CC}	5	5	mA max	During Conversion
I_{SS}	5	5	mA max	During Conversion
V_{CC} Range	+5 to +17	+5 to +17	V	See Absolute Maximum Ratings
V_{SS} Range	-5 to -17	-5 to -17	V	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to DGND . . . . . +17V
V_{SS} to DGND . . . . . -17V
V_{CC} to V_{SS} . . . . . +22V
Digital Outputs . . . . . V_{CC}, DGND
Digital Inputs
DMC (Pin 13), CLK (Pin 12) . . . . . V_{SS}, V_{CC}
All other Logic Inputs . . . . . DGND, +17V
Analog Inputs/Outputs
AGND to DGND (Positive Limitation) . . . . V_{CC} or V_{IROUT}*
AGND to DGND (Negative Limitation). V_{SS} or V_{IROUT} -20V†
AIN (Pin 2), V_{REF1} (Pin 1),
BUFIN (Pin 4) . . . . . V_{CC}, V_{SS}
IRJCT (Pin 6), IROUT (Pin 5) . . . . . +27V, AGND
Operating Temperature Range
AD7555KN (Plastic) . . . . . 0 to +70°C
AD7555BD (Ceramic) . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . +300°C

Power Dissipation (package)
Plastic (AD7555KN)
To +50°C. 1200mW
Derate above +50°C by. . . . . 12mW/°C
Ceramic (AD7555BD)
To +50°C. 1000mW
Derate above +50°C by. . . . . 10mW/°C

*Whichever is the least positive.
†Whichever is the least negative.

NOTE:
Do not apply voltages to any AD7555 digital output, AIN or V_{REF1} before V_{CC} and V_{SS} are applied. Additionally, the voltages at AIN, V_{REF1} or any digital output must never exceed V_{CC} and V_{SS} (if an op amp output is used to drive AIN it must be powered by the AD7555 V_{CC} and V_{SS} supply voltages). Do not allow any digital input to swing below DGND.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

SYSTEM ELECTRICAL CHARACTERISTICS (T_A = 0 to +45°C)
Characteristics refer to the system of Figures 6a and 6b. V_{CC} = +5V, V_{SS} = -5V, V_{REF1} = +4.096V, error count n calibrated to zero at T_A = +25°C as per procedure on page 10-65 unless otherwise noted. Switch leakages and limitations in temperature performance of auxiliary components (such as the integrating capacitor) cause performance degradations above +45°C.

CHARACTERISTIC	LIMIT	CONDITIONS/COMMENTS
Resolution	4 1/2 Digit BCD 5 1/2 Digit BCD	±20,000 Counts ±200,000 Counts (See Note 1)
Relative Accuracy	±1 Count max ±10 Count max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Notes 1 and 2)
Count Uncertainty Due to Noise (Flicker)	±1/2 Count max ±2 Counts max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Note 1)
Conversion Time	610ms max 1,760ms max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Note 1)

NOTES:
[1] 4 1/2 digit mode; f_{CLK} = 614.4kHz, HREN = LOW, R_1 = 360kΩ, C_1 = 0.22μF
5 1/2 digit mode; f_{CLK} = 1.024MHz, HREN = HIGH, R_1 = 750kΩ, C_1 = 0.22μF
[2] Assumes voltage reference (V_{REF1}) TC of 0ppm/°C.

Applying the AD7555

AD7555 PIN DESCRIPTION		
ANALOG FUNCTIONS		
V_{REF1}	(Pin 1):	+4.096V Reference Input
AIN	(Pin 2):	Analog Input Voltage (±2V Full Scale)
AGND	(Pin 3):	Analog Signal Common Ground
BUFIN	(Pin 4):	To External Buffer Amplifier Input
IROUT	(Pin 5):	From Integrator Amplifier Output
IRJCT	(Pin 6):	To Integrator Amplifier Summing Junction
LOGIC INPUTS		
$\overline{COMP}$	(Pin 7):	Input from the external comparator.
HREN	(Pin 8):	High Resolution Enable, determines converter resolution HREN = LOGIC LOW, Full Scale = ±1.9999V (100μV resolution) HREN = LOGIC HIGH, Full Scale = ±1.99999V (10μV resolution)
$\overline{HOLD}$	(Pin 9):	Hold Input $\overline{HOLD}$ = LOGIC HIGH, the ADC converts and updates the displays continuously as per the timing diagram of Figure 3. $\overline{HOLD}$ = LOGIC LOW, the ADC is reset and conversion is disabled. Data from the last complete conversion continues to be displayed. To ensure most recent data is displayed, $\overline{HOLD}$ should not be taken LOW when $\overline{DAV}$ is HIGH. When $\overline{HOLD}$ returns HIGH, the next leading edge of DMC initiates a new conversion.
DMC	(Pin 13):	Display Multiplexer Clock, can be driven from an external logic source, or with the addition of an external capacitor, will self oscillate. With an external capacitor of 10,000pF, DMC oscillates at approximately 1.5kHz at a 5% to 10% duty cycle, suitable for display purposes.
CLK	(Pin 12):	Clock Input for maximum line rejection in the 4 1/2 digit mode; 50Hz: f_{CLK} = 512kHz (= 4.096MHz ÷ 8) 60Hz: f_{CLK} = 614.4kHz (= 4.915MHz ÷ 8) 50/60Hz: f_{CLK} = 409.6kHz (= 3.2768MHz ÷ 8) For maximum line rejection in the 5 1/2 digit mode; 50/60Hz, f_{CLK} = 1.024MHz (= 4.096MHz ÷ 4)
SCI	(Pin 15):	Serial Count In. Input to totalizing counter in the AD7555. SCI is normally connected to SC0 for direct count totalization.
SUPPLY INPUTS		
V_{CC}	(Pin 28):	Positive Supply Input (+5V)
V_{SS}	(Pin 14):	Negative Supply Input (-5V)
DGND	(Pin 21):	Digital Ground

LOGIC OUTPUTS		
B8 - B1	(Pins 17 - 20)	BCD8 - BCD1 output, Active HIGH (See table 1)
$\overline{D5}$	(Pin 22):	10^{-5} digit output, Active LOW in 5 1/2 digit mode, stays HIGH in 4 1/2 digit mode
$\overline{D4}$ - $\overline{D1}$	(Pins 23-27)	10^{-4} - 10^{-1} digit outputs, Active LOW
$\overline{D0}$	(Pin 27):	10^{0} /overflow/polarity output, Active LOW
SCC	(Pin 11):	System conversion complete, goes HIGH when conversion is complete, returns LOW on comparator crossing at end of phase 0 integration period.
SCO	(Pin 16):	Serial Count Out, a serial output pulse train proportional in length to the magnitude of AIN. SCO can be externally pulled HIGH while $\overline{DAV}$ = HIGH to display the error count "n" for calibration purposes (see page 9).
$\overline{DAV}$	(Pin 10):	Data Valid – When low, $\overline{DAV}$ indicates that the data being presented on the BCD output bus is valid. $\overline{DAV}$ goes high on the first positive edge of DMC after a conversion is complete and returns low two DMC pulses later. When it returns low, the digit counter is reset to $\overline{D0}$. This is termed the MASTER RESET.

DATA		B8	B4	B2	B1	LED DISPLAY WHEN USING 7447 SEGMENT DECODER
0		0	0	0	0	0
1		0	0	0	1	1
2		0	0	1	0	2
3		0	0	1	1	3
4		0	1	0	0	4
5		0	1	0	1	5
6		0	1	1	0	6
7		0	1	1	1	7
8		1	0	0	0	8
9		1	0	0	1	9
OVERFLOW		1	1	0	0	[
DIGIT 0 ONLY	+1	0	0	0	0	=
	-1	0	0	1	0	-
	+	1	1	0	0	+
	-	0	1	1	1	-

Table 1. Output Coding

Component limitations such as switch leakage, as well as operational amplifier offset voltage and bias current (and the temperature dependency of these errors), are major obstacles when designing high resolution integrating A/D converters.

The AD7555 however, utilizes a patented *quad slope* conversion technique (Analog Devices Patent No. 3872466) to reduce the effects of such errors to second order effects.

Figure 1 shows a simplified quad slope integrator circuit. The various inputs AGND (Analog Ground), V_{REF1}, and AIN (Analog Input) are applied in sequence to the integrator via switches 1-3 (see Table 2), creating four slopes at the integrator output (phase 1-4 of Figure 2). If the equivalent summing junction voltage V_S is precisely $0.5V_{REF1}$, the phase 1 and phase 2 integration times are equal, indicating there are no input errors. If $V_S \neq 0.5V_{REF1}$ (due to amplifier offset voltage, bias current, etc.), an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts, depending on whether the error was positive or negative.

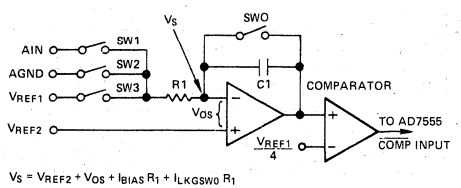
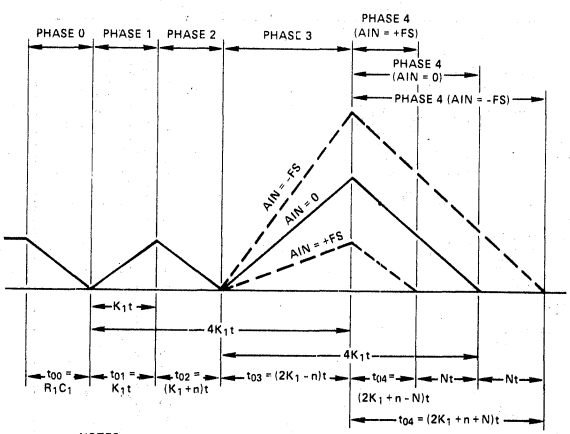


Figure 1. Simplified Quad Slope Integrator Circuit



NOTES:
1. FOR 4 1/2 DIGIT MODE, K_1 = 10,240
   $t = 4 \times 1/f_{CLK}$, WHERE f_{CLK} IS CLOCK FREQUENCY AT PIN 12
2. FOR 5 1/2 DIGIT MODE, K_1 = 102,400
   $t = 2/f_{CLK}$, WHERE f_{CLK} IS CLOCK FREQUENCY AT PIN 12
3. n = ERROR COUNT DUE TO AMPLIFIER OFFSETS ETC. AND CAN BE POSITIVE OR NEGATIVE.

Figure 2. Quad Slope Integrator Output

The final effect is to reduce the analog input error terms to second order effects. This can be proven by solving the differential equations obtained during the phase 1 through phase 4 integration periods. Barring third (and higher) order effects, the solutions are given in equations 1 and 2.

$$N_{(AIN\geq 0)} = \underbrace{-K_T\left[\frac{AIN}{V_{REF1}}\right]}_{\text{IDEAL TERM}} \underbrace{+K_T\left[\frac{AIN}{V_{REF1}} - 1\right]\left[-a^2 + \frac{AGND}{V_{REF1}}(1+2a)\right]}_{\text{ERROR TERM}} \quad \text{EQN1}$$

$$N_{(AIN<0)} = \underbrace{-K_T\left[\frac{AIN}{V_{REF1}}\right]}_{\text{IDEAL TERM}} \underbrace{-K_T\left[\frac{AIN}{V_{REF1}} - 1\right]\left[-a^2 + \frac{AGND}{V_{REF1}}(1+2a)\right]}_{\text{ERROR TERM}} \quad \text{EQN2}$$

WHERE:

N = Number of counts appearing at AD7555 Serial Count Out pin corresponding to the analog input voltage, AIN.

AIN = Analog Input Voltage to be digitized

K_T = 40960 counts (4 1/2 Digit Mode)
409600 counts (5 1/2 Digit Mode)

AGND = Voltage at AD7555 pin 3 (AGND) measured with respect to V_{REF1} and AIN signal common ground. (Ideally, AGND = 0V)

a is an error term equal to $\frac{2V_S - V_{REF1}}{V_{REF1}}$

Ideally $a = 0$ when $V_S = 0.5V_{REF1}$.

NOTE:
$V_S = V_{REF2} + V_{OS1} + V_{OS2} + I_{B2}R_1 + I_{SW0}R_1$

WHERE:

$V_{REF2} = 0.5V_{REF1}$ if no error is present

V_{OS1} = Offset voltage of buffer amplifier A1 (required to buffer the effect of ΔR_{ON} of SW1 - SW2)

V_{OS2} = Offset voltage of integrator amplifier A2

$I_{B2}R_1$ = Equivalent integrator amplifier offset voltage due to bias current of A2

$I_{SW0}R_1$ = Equivalent integrator amplifier offset voltage due to SW0 leakage current.

If AGND = 0, then the error terms of EQN 1 and 2 contain only second order effects due to $a \neq 0$. Thus, the AD7555 is a powerful tool which allows high precision system performance to be obtained when using only moderate precision op amps.

Other advantages of the quad slope technique include bipolar operation using a single positive voltage reference, and the fact that since the comparator propagation delay is constant hysteresis effects are eliminated. (This is because the comparator always approaches the zero crossing from the same direction).

Phase	Switch Closed (Figure 1)	Equivalent Input Voltage	Integration Time
0	SW3	$V_{REF1} - V_S$	$t_{00} = R_1C_1$
1	SW2	$AGND - V_S$	$t_{01} = K_1t$
2	SW3	$V_{REF1} - V_S$	$t_{02} = (K_1 + n)t$
3	SW1	$AIN - V_S$	$t_{03} = (2K_1 - n)t$
4	SW3	$V_{REF1} - V_S$	$t_{04} = (2K_1 + n \pm N)t$
5	SW0	RESET INTEGRATOR	

Table 2. Integrator Equivalent Input Voltages and Integration Times

TIMING AND CONTROL

Figure 3 shows the AD7555 timing. SCC goes HIGH at the end of SCO indicating conversion is complete. DAV goes HIGH on the 1st leading edge of DMC after conversion is complete. New data is strobed into the data latches (see functional diagram) on the leading edge of the 2nd DMC. DAV returns low on the leading edge of the 3rd DMC.

BCD data is placed on B1, B2, B4, B8 on the positive edge of DMC while the digit counter is incremented on the negative edges of DMC.

A reset phase (phase 0) is initiated on the 4th DMC after conversion is complete. SCC returns low at the phase 0 comparator crossing indicating a conversion start.

If the DMC oscillator is set up to free run (C8 in Figure 6b causes DMC to run at about 1.5kHz), the AD7555 will continuously convert and update the displays.

Externally controlling the generation of DMC pulses provides a means of controlling data outputting for computer interface applications. Pages 10-66 and 10-67 illustrate how to use this feature to interface the AD7555 to a microprocessor.

DISPLAY

The output data format of the AD7555 is multiplexed BCD as per the Timing Diagram of Figure 3. The output code format is shown in Table 1.

Overflow causes digit 1 through digit 4 (digit 1 through digit 5 in 5 1/2 digit mode) to output a BCD 12 (1100). Overflow does not affect digit 0. Therefore, a positive overflow is displayed as $+1$ and a negative overflow as -1, when using the 7447 seven-segment decoder.

PRINTED CIRCUIT LAYOUT

To ensure performance with the system specifications Figures 5a and 5b show the recommended P.C. board layout for the AD7555. Figure 4 shows the component overlay for Figure 5a.

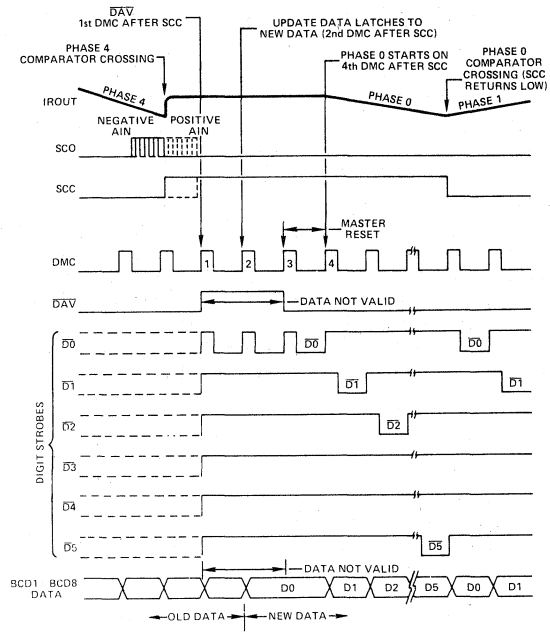


Figure 3. Timing Diagram (Self Start DPM Mode)

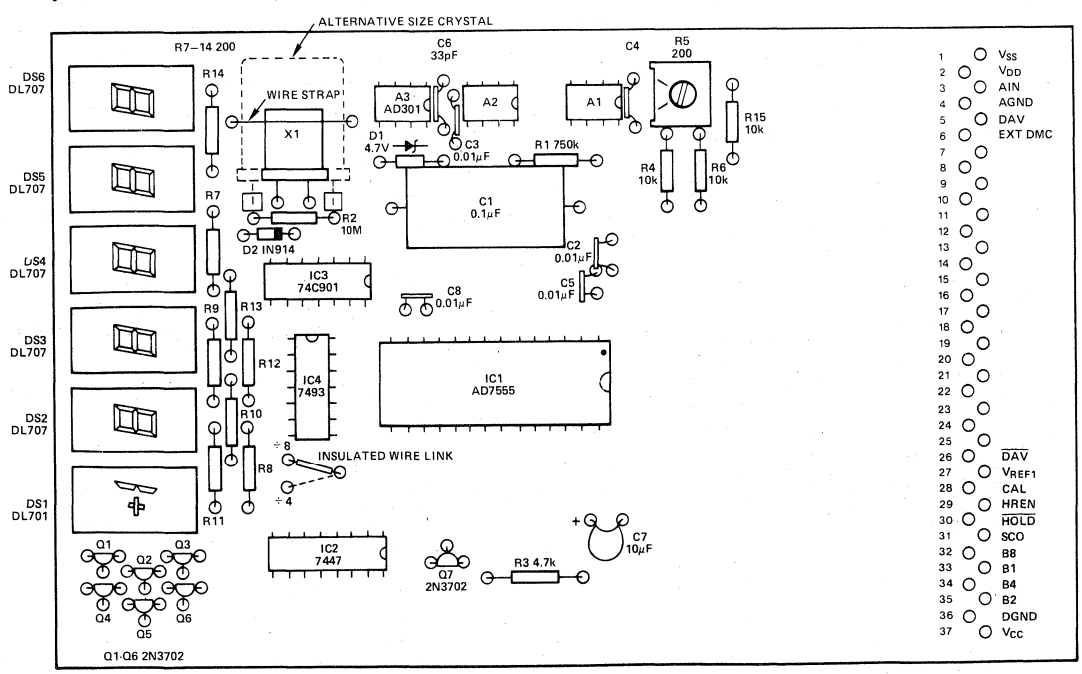


Figure 4. Component Overlay for Figure 5a

PCB Layout is reproduced on a one to one scale. Note that a pad already exists on the PCB layout for an AD584LH voltage reference, suitable for 4 1/2 digit operation.

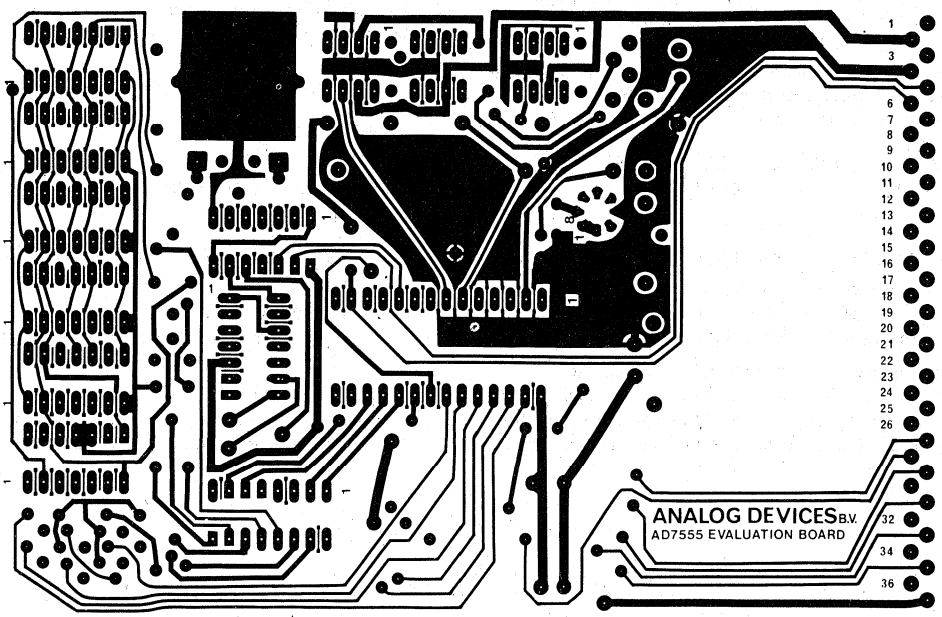


Figure 5a. Component Side

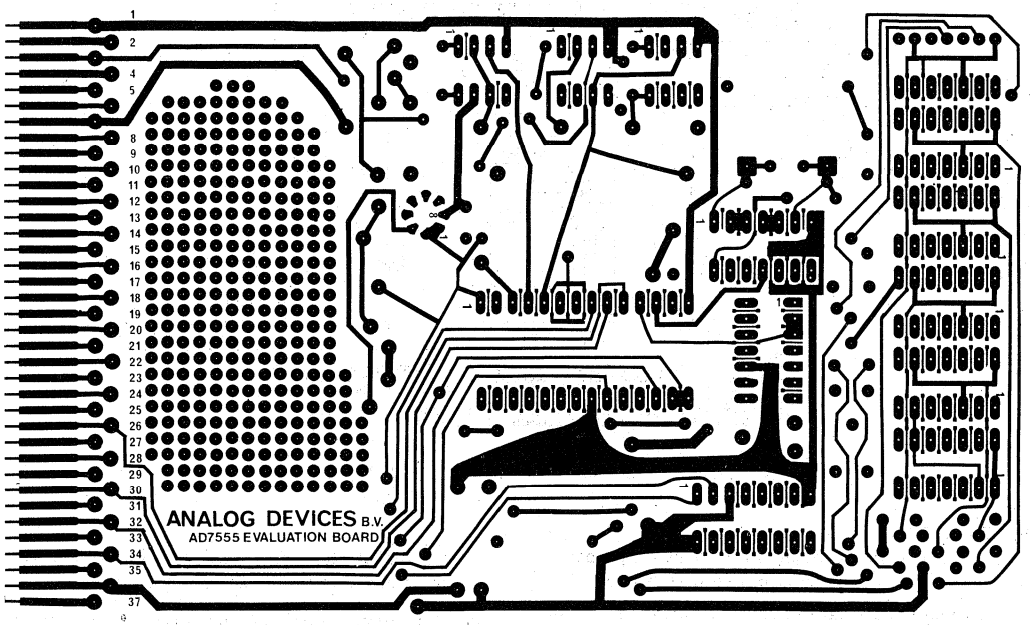


Figure 5b. Foil Side

ANALOG CIRCUIT SET-UP AND OPERATION

The following steps, in conjunction with the analog circuitry of Figure 6a explain the selection of the various component values required for proper operation.

1. **Selection of Integrator Components R_1 and C_1**
   Improper selection of the integrator time constant (time constant = R_1C_1) may cause excessive noise due to the integrator output level being too low, or may cause non-linear operation if the integrator output attempts to exceed the rated output voltage of the amplifier. The integrator time constant R_1C_1 must be:

$$\frac{(V_{REF1})(K_a)}{(f_{CLK})(7V)} \geq R_1C_1 \geq \frac{(V_{REF1})(K_a)}{(f_{CLK})(V_{DD}-5V)}$$

   Where:

   V_{DD} is the integrator amplifier positive supply voltage
   f_{CLK} is the clock frequency at pin 12
   $K_a = 8.2 \times 10^4$ (4 1/2 digit mode)
   or 4.0×10^5 (5 1/2 digit mode)

   The integrating capacitor must be a low leakage, low dielectric absorption type such as teflon (5 1/2 digit mode), polystyrene or polypropylene (4 1/2 digit mode). To minimize noise injection, the outside foil of C1 must be connected to the output of the integrating amplifier, not to its summing junction.

   The recommended maximum value for R1 in both the 4 1/2 digit and 5 1/2 digit mode is 750kΩ. Higher values may cause noise injection.

2. **Determing Conversion Time**
   Maximum conversion time occurs when A_{IN} = -FS and is given by

   4 1/2 DIGIT MODE

   $t_{CONVERT} = (325{,}760)(t_{CLK}) + R_1C_1$

   5 1/2 DIGIT MODE

   $t_{CONVERT} = (1{,}628{,}800)(t_{CLK}) + R_1C_1$

   Where:

   t_{CLK} = Period of CLK as measured at pin 12
   R_1C_1 = Integrator Time Constant

3. **Initial Calibration**
   a. Adjust V_{REF1} so that the voltage at pin 1 (V_{REF1}) of the AD7555 is +4.0960V.
   b. Apply 0V to AIN and adjust R5 (V_{REF2} Adjust) for display 0.0000. (See optional calibration procedure on the next page for more precise calibration.)

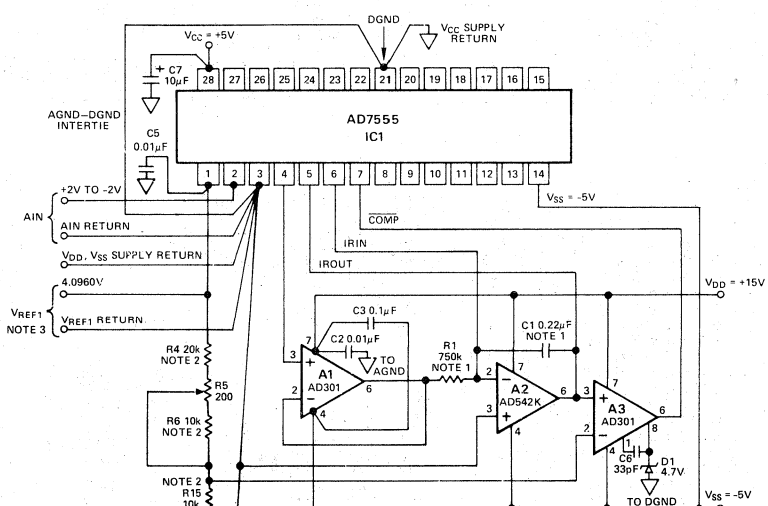


Figure 6a. Analog Circuit Diagram

APPLICATION HINTS

1. See Note under Absolute Maximum Ratings for proper power sequencing and input/output voltage ratings.
2. For linear operation the absolute magnitude of AIN cannot exceed 1/2 V_{REF1}. In no case must AIN be more negative than V_{SS}.
3. Do not leave unused CMOS inputs floating.
4. Check that integrator components R1 and C1 are chosen as per paragraph 1 of the setup and operation section on this page and that initial calibration as per paragraph 3 has been accomplished. A resistor value no larger than 750k is recommended to minimize noise pickup.
5. For optimum normal mode noise rejection, use the crystal frequencies shown on page 10-60.
6. In order for the calibrate mode (on the next page) to display the error count properly it can be shown that
   $V_{REF2} \geq V_{REF1} \times 0.4883$
   Specifically, for V_{REF1} = 4.0960V
   $V_{REF1} \geq 2V$

LOGIC AND DISPLAY CIRCUITRY

The AD7555 possesses 4 1/2 digit accuracy with potential for 5 1/2 digit resolution. Figure 6b shows the logic and display circuitry when operating the AD7555 with this high resolution.

MODIFYING THE FULL SCALE DISPLAY

Availability of the SCO and SCI terminals on the AD7555 provides flexibility for range-switching and modified data-format applications.

For example, in the 5 1/2 digit mode, inserting a ÷5 counter between SCO and SCI provides a full scale count at SCI of 39,999 counts (199,999 ÷5).

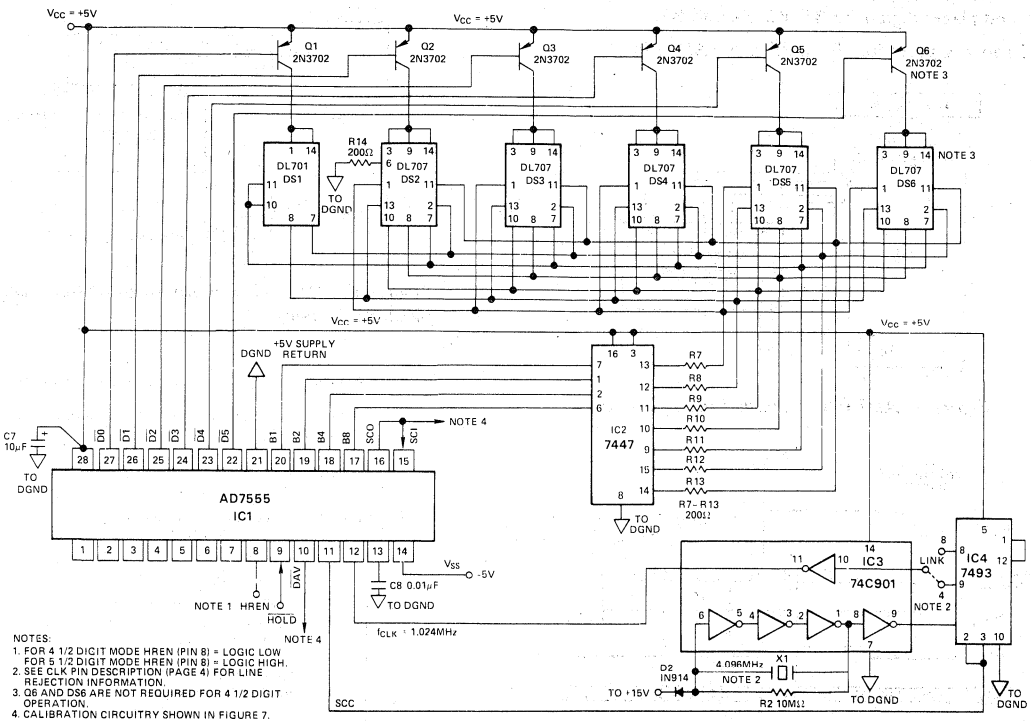


Figure 6b. Logic and Display Circuitry (for 5 1/2 Digit Resolution)

CALIBRATING THE AD7555

When the AD7555 is placed in the *calibrate* mode, any resulting error voltage in V_S (summing junction voltage), due to drift, etc., will be contained in the resulting display. To display the error SC1 and SC0 must be taken HIGH (only allowable when $\overline{DAV}$ is HIGH). In the *calibrate* mode the display indicates +b.0480 ±n (+b.04800 ±n in 5 1/2 digit mode) where b indicates a blanked digit and n is a number representing the reference input errors. This gives the change required in V_{REF2} ($\pm\Delta V_{REF2}$) for proper calibration (ie., $n \approx 0$). The exact relationship between n and ΔV_{REF2} can be shown to be equal to:

$$\Delta V_{REF2} = \frac{(V_{REF1})n}{40{,}960 + n} \quad \text{(4 1/2 digit operation)}$$

$$\Delta V_{REF2} = \frac{(V_{REF1})10n}{40{,}960 + 10n} \quad \text{(5 1/2 digit operation)}$$

For this capability to operate, $|V_{REF2}|$ must be $1/2\ V_{REF1}$ ±2%.

Figure 7 shows the hardware connections for manual calibration. With the switch in the *calibrate* mode, adjust V_{REF2} (potentiometer R5 as shown in Figure 6a) until the display reads +b.0480 (+b0.04800 in 5 1/2 digit mode). The AD7555 is now calibrated to the center of its error correcting range.

Return the switch to *normal* to resume normal conversion.

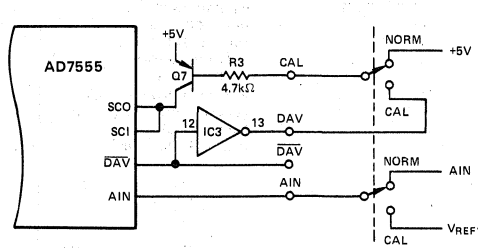


Figure 7. Hardware Requirements for Manual Calibration of n = 0

Microprocessor Interfacing

AD7555 AS A POLLED INPUT DEVICE (MCS-85 SYSTEM)

Figure 8 shows an AD7555/8085 interface. The DMC clock input of the AD7555 is controlled by the microcomputer via an output port of the 8155.

Typical timing for this interface mode is shown in Figure 9. $\overline{DAV}$ goes HIGH on the 1st DMC leading edge after SCC goes HIGH. It returns LOW on the rising edge of the 3rd DMC pulse. Digit zero is availabe on B1, B2, B4 and B8 at this time. The leading edge of the 4th DMC pulse initiates a new conversion and places digit 1 on B1, B2, B4 and B8.

Table 3 shows a procedure for polling the AD7555.

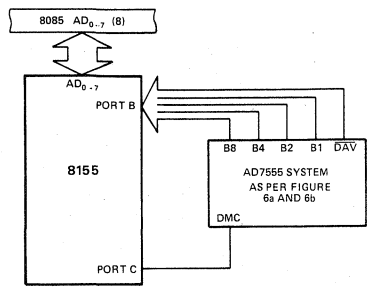


Figure 8. AD7555 as a Polled Input Device

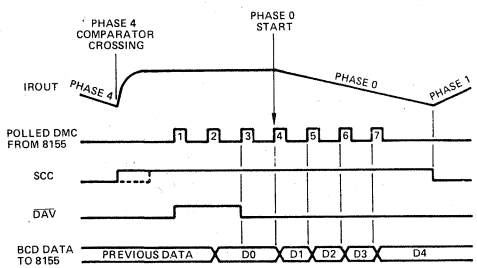


Figure 9. Timing Diagram for Operation as a Polled Input Device (8085/AD7555)

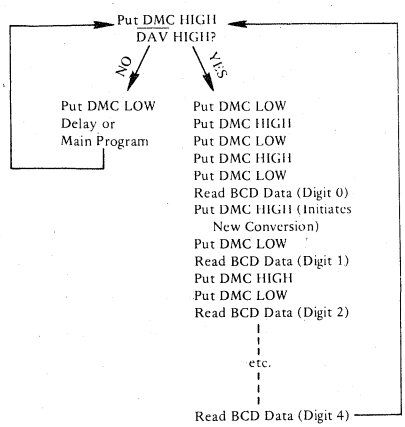


Table 3. Procedure for Interfacing the AD7555 as a Polled Input Device

AD7555 AS AN INTERRUPTING INPUT DEVICE (MCS-85 SYSTEM)

The AD7555 DMC oscillator provides DMC pulses until SCC (System Conversion Complete) goes high. This causes an interrupt on the RST 7.5 line whereby the three-state buffer is activated and the microprocessor takes control of DMC. Table 4 shows a procedure for using the AD7555 in this mode. Figure 10 shows the basic hookup.

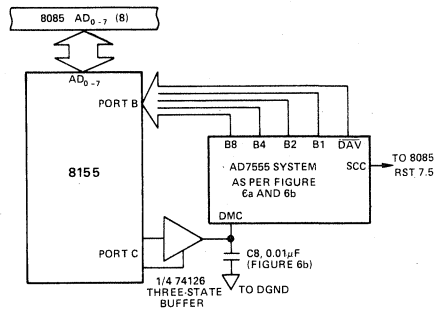


Figure 10. AD7555 as an Interrupting Input Device (MCS-85 System)

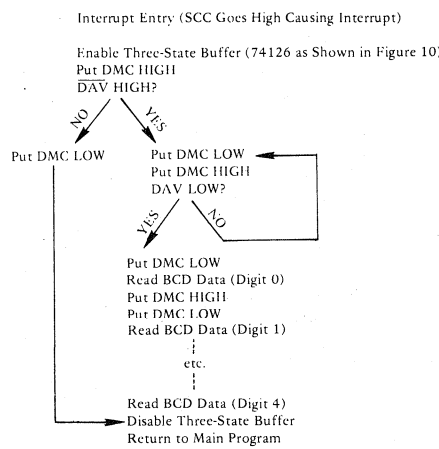


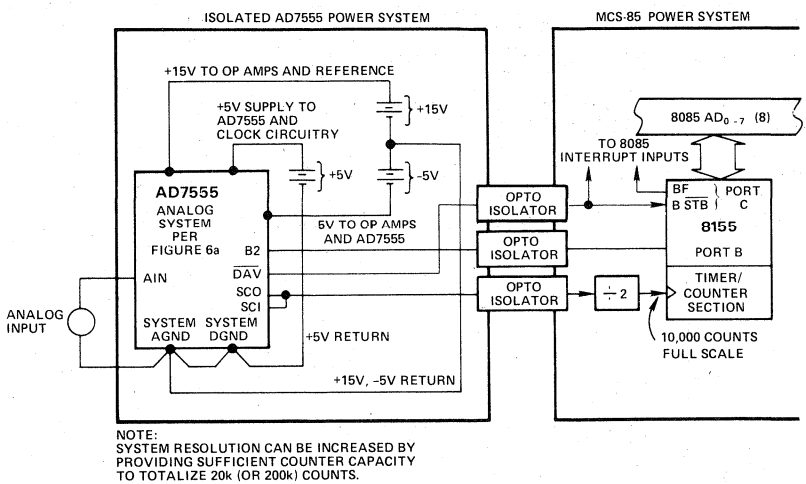
Table 4. Procedure for Interfacing the AD7555 as an Interrupting Input Device

OPTO-ISOLATED SERIAL INTERFACE

Figure 11 shows a serial interface to the MCS-85 system. This system can accommodate a remote interface where a common-mode voltage is expected to exist between system grounds. The 8155 counter/timer is only 14 bits long, i.e., it can only count down from 2^{14}; therefore SCO output from the AD7555 (20k counts full scale) has to be divided by 2 with consequent reduction in system resolution.

Port C of the 8155 is configured as a control port. Port B is an input port. This port configuration is necessary if sign information is required. Magnitude information is obtained by interrogating the 8155 counter value. The rising edge of $\overline{DAV}$ is used to cause an interrupt on the RST 7.5 line. The value $\left(2^{14} - \left|\frac{SCO}{2}\right|\right)$ in the 8155 counter should now be read.

When $\overline{DAV}$ returns low the 8155 counter is reset to FF_H. Sign information is checked at this time since $\overline{D_0}$ BCD data is present and stable on the BCD bus (see Figure 9). The B2 line of the BCD bus is latched into port B by the signal on $\overline{B\ STB}$ i.e. the falling edge of $\overline{DAV}$. This causes a rising edge signal on BF (buffer full) to call the 8085 CPU to read the B2 bit. B2 bit is HIGH for negative data, LOW for positive data.



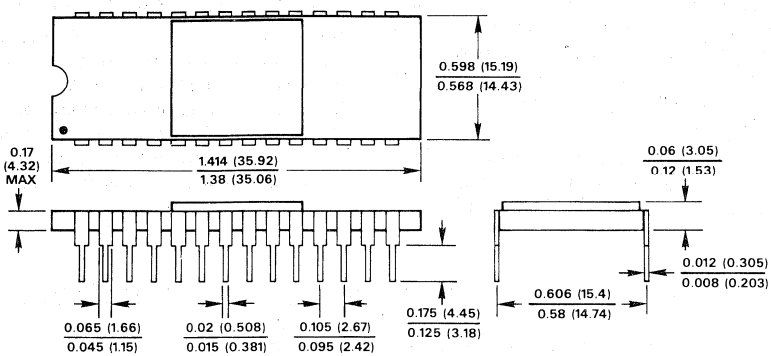
NOTE:
SYSTEM RESOLUTION CAN BE INCREASED BY PROVIDING SUFFICIENT COUNTER CAPACITY TO TOTALIZE 20k (OR 200k) COUNTS.

Figure 11. Optically Isolated Serial AD7555/MCS-85 Interface (Full Scale = 10,000 Counts)

OUTLINE DIMENSIONS

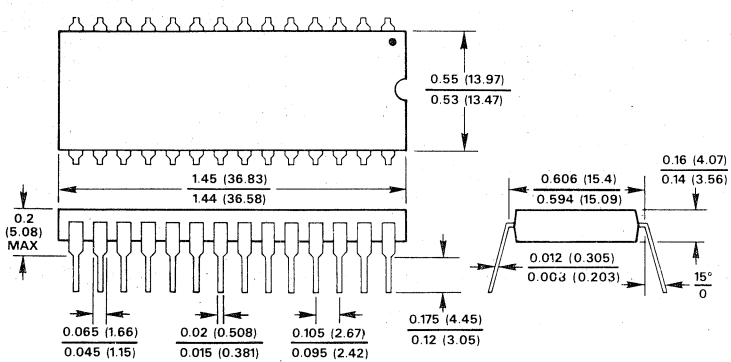
Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (SUFFIX D)



NOTES:
LEAD NO. 1 IS IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42.

28-PIN PLASTIC DIP (SUFFIX N)



NOTES:
LEAD NO. 1 IS IDENTIFIED BY DOT OR NOTCH.
LEADS ARE GOLD-PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42.
CAVITY LID IS ELECTRICALLY ISOLATED.

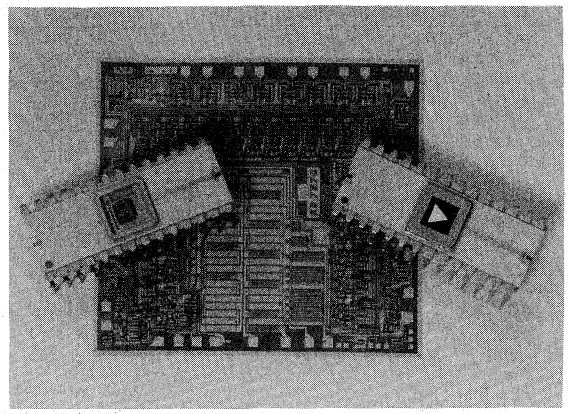
ANALOG DEVICES

CMOS 10-Bit Monolithic A/D Converter

AD7570

FEATURES

- 8- and 10-Bit Resolution
- 20μs Conversion Time
- Microprocessor Compatibility
- Very Low Power Dissipation
- Parallel and Serial Outputs
- Ratiometric Operation
- TTL/DTL/CMOS Logic Compatibility
- CMOS Monolithic Construction



GENERAL DESCRIPTION

The AD7570 is a monolithic CMOS 10-bit successive approximation A/D converter on a 120 by 135 mil chip, requiring only an external comparator, reference and passive clocking components. Ratiometric operation is inherent, since an extremely accurate multiplying DAC is used in the feedback loop.

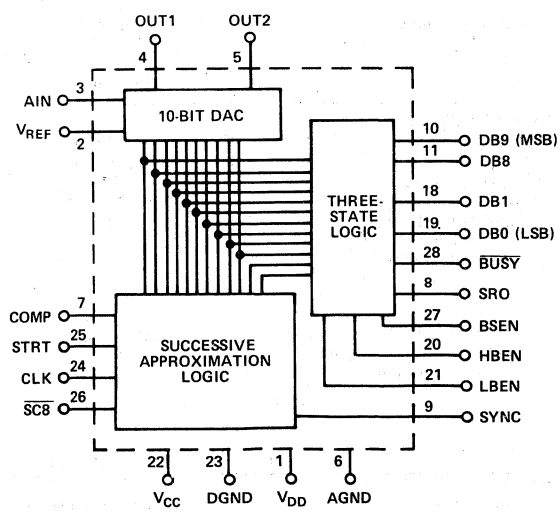
The AD7570 parallel output data lines and Busy line utilize three-state logic to permit bussing with other A/D output and control lines or with other I/O interface circuitry. Two enables are available: one controls the two MSBs; the second controls the remaining 8 LSBs. This feature provides the control interface for most microprocessors which can accept only an 8-bit byte.

The AD7570 also provides a serial data output line to be used in conjunction with the serial synchronization line. The clock can be driven externally or, with the addition of a resistor and a capacitor, can run internally as high as 0.6MHz allowing a total conversion time (8 bits) of typically 20μs. An 8-bit short cycle control pin stops the clock after exercising 8 bits, normally used for the "J" version (8-bit resolution).

The AD7570 requires two power supplies, a +15V main supply and a +5V (for TTL/DTL logic) to +15V (for CMOS logic) supply for digital circuitry. Both analog and digital grounds are available.

The AD7570 is a monolithic device using a proprietary CMOS process featuring a double layer metal interconnect, on-chip thin-film resistor network and silicon nitride passivation ensuring high reliability and excellent long term stability.

FUNCTIONAL DIAGRAM



SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V unless otherwise noted)

PARAMETER[1]	VERSIONS	T_A = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ACCURACY				
Resolution	J	8 Bits min	8 Bits min	$\overline{SC8}$ = Logic "0"
	L	10 Bits min	10 Bits min	$\overline{SC8}$ = Logic "1"
Relative Accuracy	J, L	±1/2LSB max	±1/2LSB max	f_{CLK} = 100kHz
Differential Nonlinearity	J, L	1LSB max	1LSB max	See Figure 5
Gain Error	J, L	0.3% Reading typ		
Gain Temperature Coefficient	J, L	5ppm Reading per °C typ	10ppm Reading per °C max	
ANALOG INPUTS				
Analog Input Resistance	J, L	10kΩ typ	5kΩ min, 20kΩ max	
Analog Input Resistance Tempco	J, L	−150ppm/°C typ		
Reference Input Resistance	J, L	10kΩ typ	5kΩ min, 20kΩ max	
Reference Input Resistance Tempco	J, L	−150ppm/°C typ		
ANALOG OUTPUTS				
Output Leakage Current (OUT1, OUT2)	J, L	10nA typ	200nA max	$V_{OUT1, 2}$ = 0V DB0 through DB9 = Logic "1"
Output Capacitance OUT1	J, L	120pF typ		
OUT2	J, L	40pF typ		
OUT1	J, L	40pF typ		DB0 through DB9 = Logic "0"
OUT2	J, L	120pF typ		
DIGITAL INPUTS				
V_{INL}[2]	J, L	+1.4V typ, +0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}[2]	J, L	+2.4V min, +1.4V typ	+2.4V min	
V_{INL}[2]	J, L	+1.5V max	+1.5V max	V_{CC} = +15V
V_{INH}[2]	J, L	+13.5V min	+13.5V min	
I_{INL}, I_{INH}[3]	J, L	±0.1μA typ, ±10μA max		V_{IN} = 0 to V_{CC}
CLK Input Current	J, L	+0.4mA typ, +1mA max		During Conversion V_{CC} = +5V; 2.4V ≤ V_{IN} ≤ V_{CC}
CLK Input Current	J, L	+1.7mA typ, +3mA max		During Conversion V_{CC} = +15V; 10V ≤ V_{IN} ≤ V_{CC}
CLK Input Current	J, L	±1μA typ		V_{CC} = +5V to +15V Conversion Complete or CLK IN ≤ V_{INL}
C_{IN}	J, L	2pF typ		
DIGITAL OUTPUTS				
V_{OUTL}	J, L	+0.5V max	+0.8V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OUTH}	J, L	+2.4V min	+2.4V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OUTL}	J, L	+1.5V max	+1.5V max	V_{CC} = +15V, I_{SINK} = 3mA
V_{OUTH}	J, L	+13.5V min	+13.5V min	V_{CC} = +15V, I_{SOURCE} = 1mA
C_{OUT} (Floating) (SYNC, SRO, $\overline{BUSY}$, and DB0 through DB9)	J, L	5pF typ		V_{CC} = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0"
I_{LKG} (Floating) (SYNC, SRO, $\overline{BUSY}$ and DB0 through DB9)		±5nA typ		V_{CC} = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0" V_{OUT} = 0V and V_{CC}
DYNAMIC PERFORMANCE				
Conversion Time	J	20μs typ, 40μs max	40μs max	See Figure 5
	L	40μs typ, 120μs max	120μs max	
Internal CLK Frequency	J, L	100kHz typ		V_{CC} = +5V; CLK Duty Cycle = 50%, R = 33k, C = 760pF
(See Figure 2, and Section 6 of Pin Function Description)	J, L	100kHz typ		V_{CC} = +15V, CLK Duty Cycle = 50%, R = 10k; C = 2500pF
LBEN, HBEN Propagation Delay				V_{CC} = +5V
t_{ON}	J, L	650ns typ		LBEN, HBEN = 0V to +3V
t_{OFF}	J, L	200ns typ		Data Bit Load = 5k, 16pF Measured from 50% of Enable Input to 50% Point of Data Bit Output
BSEN Propagation Delay				V_{CC} = +5V
t_{ON}	J, L	450ns typ		BSEN = 0V to +3V
t_{OFF}	J, L	200ns typ		$\overline{BUSY}$ Load = 5k, 16pF Measured from 50% Point of BSEN Input Waveform to 50% Point of $\overline{BUSY}$ Output Waveform
Convert Start (STRT)[4] Pulse Duration Requirement	J, L	0.5μs min		

PARAMETER[1]	VERSIONS	T_A = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
POWER SUPPLIES				
V_{DD}	J, L	+5V to +15V typ		See Figures 3 and 4
V_{CC}	J, L	+5V to V_{DD} typ		
I_{DD}	J, L	0.2mA typ, 2mA max		V_{DD} = +15V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)
I_{CC}	J, L	0.02mA typ, 2mA max		V_{CC} = +5V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)
	J, L	0.1mA typ, 2mA max		V_{CC} = +15V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)

[1] "J" version parameters specified for $\overline{SC8}$ = 0.
[2] V_{INL} and V_{INH} specifications applicable to all digital inputs except COMP. COMP terminal must be driven with CMOS levels (i.e., comparator output pullup must be tied to V_{CC}).
[3] I_{INL}, I_{INH} specifications not applicable to CLK terminal. See "CLK input current" in specifications table.
[4] STRT falling edge should not coincide with CLK in falling edge.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V
V_{CC} to GND. . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
V_{REF} to GND. . . . . ±25V
Analog Input to GND. . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND

I_{OUT1}, I_{OUT2} . . . . . -0.3V, V_{DD}
Power Dissipation (package)
up to +50°C. 1000mW
Derate above +50°C by. . . . . 10mW/°C
Operating Temperature. . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

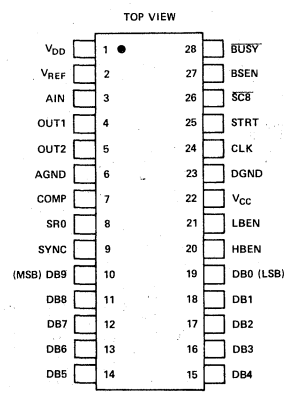
1. Do not apply voltages higher than V_{CC} or less than GND to any input/output terminal except V_{REF} or AIN.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
3. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

ORDERING INFORMATION

Resolution	Temperature Range
	-25°C to +85°C
8-Bit	AD7570J
10-Bit	AD7570L

Suffix D: Ceramic Package

PIN CONFIGURATION



TYPICAL PERFORMANCE CHARACTERISTICS

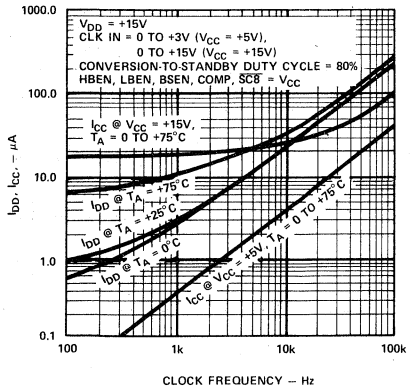


Figure 1. I_{DD}, I_{CC} vs. f_{CLK} at Different Temperatures

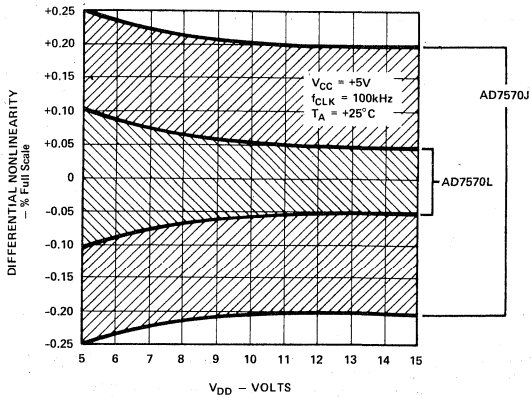


Figure 3. Differential Nonlinearity vs. V_{DD}

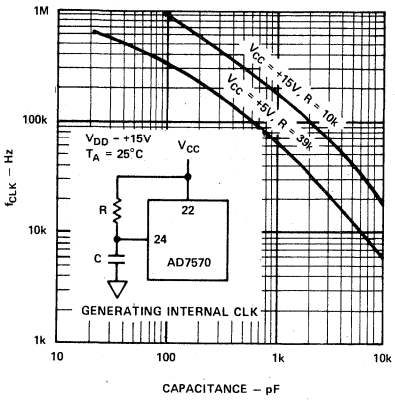


Figure 2. f_{CLK} vs. R and C at V_{CC} = +5V, +15V

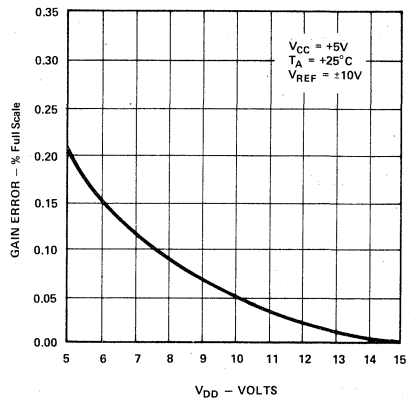


Figure 4. Gain Error vs. V_{DD} (Normalized for V_{DD} = 15V)

TEST CIRCUITS

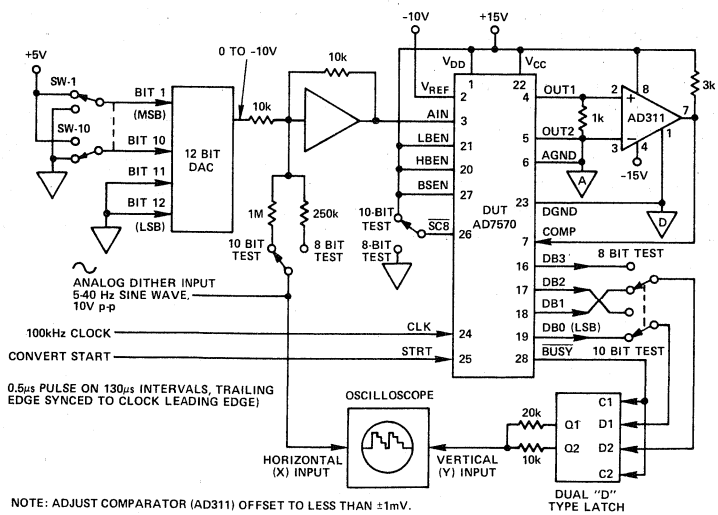
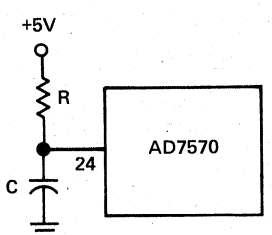


Figure 5. Dynamic Crossplot Accuracy Test

PIN FUNCTION DESCRIPTION

INPUT CONTROLS

1. Convert Start (pin 25 – STRT)
   When the start input goes to Logical "1", the MSB data latch is set to Logic "1" and all other data latches are set to Logic "0". When the start input returns low, the conversion sequence begins. The start command must remain high for at least 500 nanoseconds. If a start command is reinitiated *during* conversion, the conversion sequence starts over.
2. High Byte Enable (pin 20 – HBEN)
   This is a three-state enable for the bit 9 (MSB) and bit 8. When the control is low, the output data lines for bits 9 and 8 are floating. When the control is high, digital data from the latches appears on the data lines.
3. Low Byte Enable (pin 21 – LBEN)
   Same as High Byte Enable pin, but controls bits 0 (LSB) through 7.
4. Busy Enable (pin 27 – BSEN)
   This is an interrogation input which requests the status of the converter, i.e., conversion in process or convert complete. The converter status is addressed by applying a Logic "1" to the Busy Enable. (See Busy under Output Functions.)
5. Short Cycle 8 Bits (pin 26 – $\overline{SC8}$)
   With a Logic "0" input, the conversion stops after 8 bits reducing the conversion time by 2 clock periods. This control should be exercised for proper operation of the "J" version. When a Logic "1" is applied, a complete 10-bit conversion takes place ("L" version).
6. Clock (pin 24 – CLK)
   With an external RC connected, as shown in the figure below, clock activity begins upon receipt of a Convert-Start command to the A/D and ceases upon completion of conversion. An external clock (CMOS or TTL/DTL levels) can directly drive the clock terminals, if required. Figure 2 shows the internal CLK frequency versus R and C. If V_{CC} is <4.75V, the internal CLK will not operate.



Generating Internal Clock Frequency

7. V_{DD} (pin 1)
   V_{DD} is the positive supply for all analog circuitry plus some digital logic circuits that are not part of the TTL compatible input/output lines (back-gates to the P-channel devices). Nominal supply voltage is +15V.
8. V_{CC} (pin 22)
   V_{CC} is the logic power supply. If +5V is used, all control inputs/outputs (with the exception of comparator terminal) are DTL/TTL compatible. If +15V is applied, control inputs/outputs are CMOS compatible.

OUTPUT FUNCTIONS

1. Busy (pin 28 – $\overline{BUSY}$)
   The Busy line indicates whether conversion is complete or in process. Busy is a three-state output and floats until the Busy-Enable line is addressed with a Logic "1". When addressed, Busy will indicate either a "1" (conversion complete) or a "0" (conversion in process).
2. Serial Output (pin 8 – SRO)
   Provides output data in serial format. Data is available only during conversion. When the A/D is not converting, the Serial Output line "floats." The Serial Sync (see next function) *must* be used, along with the Serial Output terminal to avoid misinterpreting data.
3. Serial Synchronization (pin 9 – SYNC)
   Provides 10 positive edges, which are synchronized to the Serial Output pin. Serial Sync is floating if conversion is not taking place.

Note that all digital inputs/outputs are TTL/DTL compatible when V_{CC} is +5V, and CMOS compatible when V_{CC} is +15V.

PIN NO.	MNEMONIC	FUNCTION
1	V_{DD}	Positive Supply (+15V)
2	V_{REF}	Voltage REFerence (±10V)
3	AIN	Analog INput
4	OUT1	DAC Current OUTput 1
5	OUT2	DAC Current OUTput 2
6	AGND	Analog GrouND
7	COMP	COMParator
8	SRO	SeRial Output
9	SYNC	Serial SYNChronization
10	DB9	Data Bit 9 (MSB)
11	DB8	Data Bit 8
12	DB7	Data Bit 7
13	DB6	Data Bit 6
14	DB5	Data Bit 5
15	DB4	Data Bit 4
16	DB3	Data Bit 3
17	DB2	Data Bit 2
18	DB1	Data Bit 1
19	DB0	Data Bit 0 (LSB)
20	HBEN	High Byte ENable
21	LBEN	Low Byte ENable
22	V_{CC}	Logic Supply (+5V to +15V)
23	DGND	Digital GrouND
24	CLK	CLocK
25	$\overline{STRT}$	STaRT
26	$\overline{SC8}$	Short Cycle 8 Bits
27	$\overline{BSEN}$	BuSy ENable
28	$\overline{BUSY}$	BUSY

Table 1. Function Table

FUNCTIONAL ANALYSIS

BASIC DESCRIPTION

The AD7570 is a monolithic CMOS A/D converter which uses the successive approximations technique to provide up to 10 bits of digital data in a serial and parallel format. Most A/D applications require the addition of only a comparator and a voltage or current reference.

In the successive approximations technique, successive bits, starting with the most significant bit (DB9) are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage (AIN) using a zero crossing detector (comparator). If the DAC output is greater than AIN, the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than AIN, the trial data bit stays in the "1" state, and the next smaller data bit is tried.

Each successive bit is tried, compared to AIN, and set or reset in this manner until the least significant bit (DB0) decision is made. At this time, the AD7570 output is a valid digital representation of the analog input, and will remain in the data latches until another convert start (STRT) is applied.

TIMING DESCRIPTION

Figure 6 is the AD7570 timing diagram, showing the successive trials and decisions for each data bit. When convert start (STRT) goes HIGH, the MSB(DB9) is set to the Logic "1" state, while DB0 through DB8 are reset to the "0" state.

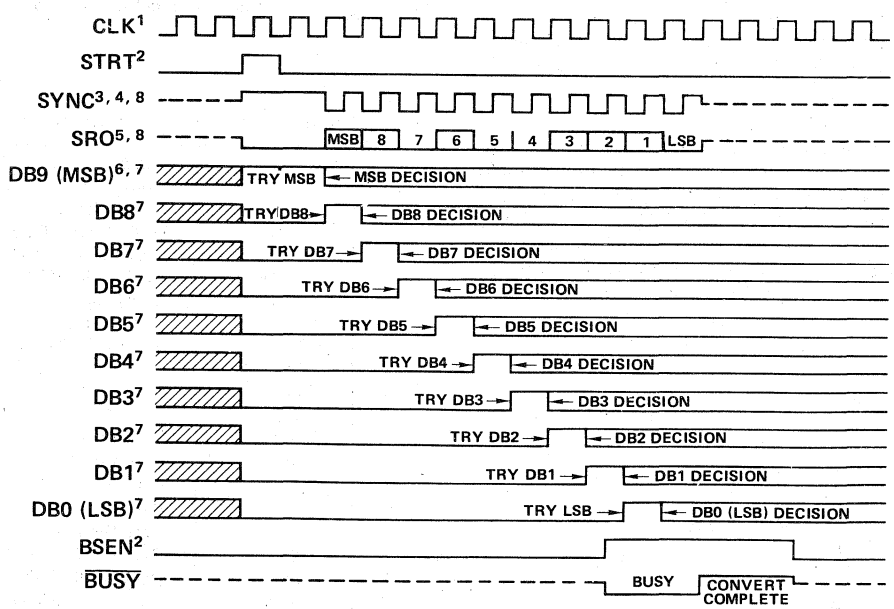
Two clock *pulses* plus 200ns after STRT returns LOW, the MSB decision is made, and DB8 is tried. Each succeeding trial and decision is made at t_{CLK} + 200ns.

Serial NRZ data is available during conversion at the SRO terminal. SYNC provides 10 positive edges which occur in the middle of each serial output bit. SYNC out must be used in conjunction with SRO to avoid misinterpretation of data. Both SYNC and SRO "float" when conversion is not taking place.

8-BIT SHORT CYCLE NOTES

If the AD7570 is short cycled to 8 bits ($\overline{SC8}$ = 0V), the following will occur:

1. The SYNC terminal will provide 8, instead of 10, positive output pulses.
2. DB1 goes "high" coincident with the LSB (DB2 is the LSB when short cycled to 8 bits) decision, and remains high until another STRT is initiated. DB0 remains in the "0" state.
3. $\overline{BUSY}$ goes "high" one clock period after the DB2 (DB2 is the LSB when short cycled) decision is made.



NOTES:
1. INTERNAL CLOCK RUNS ONLY DURING CONVERSION CYCLE (EXTERNAL CLOCK SHOWN).
2. EXTERNALLY INITIATED.
3. SERIAL SYNC LAGS $\overline{CLOCK}$ BY ≈ 200ns.
4. DOTTED LINES INDICATE "FLOATING" STATE.
5. FOR ILLUSTRATIVE PURPOSES, SERIAL OUT SHOWN AS 1101001110.
6. CROSS HATCHING INDICATES "DON'T CARE" STATE.
7. SET AND RESET OF OUTPUT DATA BITS LAGS CLOCK POSITIVE EDGE BY ≈ 200ns.
8. SHOWN FOR $\overline{SC8}$ = 1.

Figure 6. AD7570 Conversion Timing Sequence

DYNAMIC PERFORMANCE

The upper clock frequency limitation (hence the conversion speed limitation) of the AD7570 is due to the output settling characteristics of the current weighting DAC in conjunction with the propagation delay of the comparator, not to speed limitations in the digital logic.

DAC EQUIVALENT CIRCUIT

The D/A converter section of the AD7570 is a precision 10-bit multiplying DAC. The simplified DAC circuit, shown in Figure 7, consists of ten single-pole-double-throw current steering switches and an "inverted" R-2R current weighting network. (For a complete description of the DAC, refer to the AD7520 data sheet.)

The output resistance and capacitance at OUT1 (and OUT2) are code dependent, exhibiting resistive variations from 0.5 "R" to 0.75 "R", and capacitive variations from 40pF to 120pF.

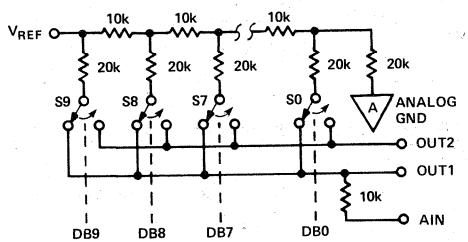


Figure 7. DAC Circuit

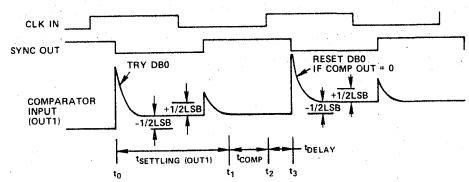
SETTLING TIME ANALYSIS

Due to the changing C_{OUT1} and R_{OUT1}, the time constant on OUT1 falls anywhere between 250 and 900ns, depending on the instantaneous state of the AD7570 digital output code.

Worst case settling requirements occur when a trial bit causes the OUT1 terminal to charge towards a final value which is precisely 1/2 LSB beyond zero crossing. When this occurs, the trial bit must settle and remain within 1/2 LSB of final value, or an incorrect decision will be made by the comparator.

For 10-bit accuracy, the first MSB must settle to within 0.1% of final value; the second MSB to within 0.2%. The LSB settling requirement is only 50% of the LSB value. Figure 8 illustrates the settling time available during a given clock period. The pulse shown on the OUT1 terminal falling midway between t_0 and t_3 is a feedthrough from internal clock mechanisms and is due primarily to bonding wire and header capacitance. Two methods may be used to reduce the OUT1 settling time:

1. Load OUT1 with a 1k resistor. This reduces the time constant by a factor of 10. Further reduction of the 1kΩ load reduces the amount of comparator overdrive, thus increasing the comparator propagation delay, resulting in a reduction of available settling time (t1 - t0 on Figure 8).
2. Use a zero input impedance comparator. Figure 9 illustrates a comparator circuit which has an input impedance of approximately 26Ω. Proper circuit layout will provide 10-bit accuracy for clock frequencies >500kHz.



NOTES:
1. "$t_{SETTLING}$" ($t_1 - t_0$) IS THE TIME REQUIRED FOR THE OUT1 TERMINAL TO SETTLE WITHIN ±1/2LSB OF THE FINAL VALUE.
2. "t_{COMP}" ($t_2 - t_1$) IS THE COMPARATOR SWITCHING TIME.
3. "t_{DELAY}" ($t_3 - t_2$) IS AN INTERNALLY GENERATED TIME DELAY EQUAL TO APPROXIMATELY 400 NANOSECONDS.
4. COMPARATOR OUTPUT IS LATCHES AT TIME t_2.

Figure 8. Expanded Timing Diagram

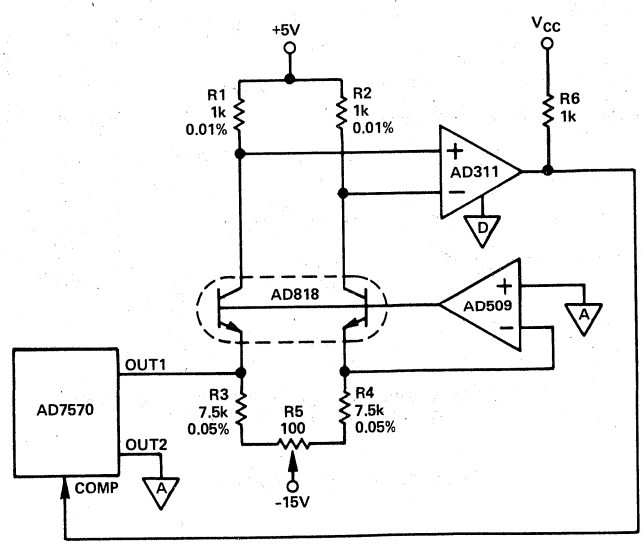


Figure 9. Current Comparator With Low Input Impedance

OPERATION GUIDELINES

UNIPOLAR BINARY OPERATION

Figure 10 shows the circuit connections required for unipolar analog inputs. If *positive* analog inputs are to be quantized, V_{REF} must be *negative*, and the OUT1 (pin 4) terminal of the AD7570 must be connected to the "+" comparator input. For *negative* analog inputs, V_{REF} must be *positive*, and the OUT1 terminal connected to the "–" input of the comparator.

For clarity, the digital control functions have been omitted from the diagram. For proper use of the digital input/output control functions, refer to the pin function description.

The input voltage/output code relationship for unipolar operation is shown in Table 2. Due to the inherent multiplying capability of the internal D/A converter, the AD7570 can accurately quantize full scale ranges of 10V to 1V. It should be noted, however, that for smaller full scale ranges, the resolution and speed limitations of the comparator impose a limitation on the maximum conversion rate.

BIPOLAR (OFFSET BINARY) OPERATION

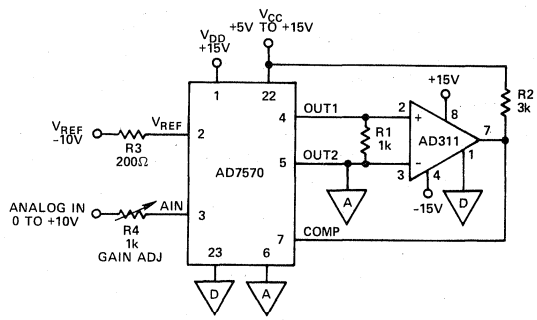
Figure 11 shows the AD7570 configured for offset binary (modified 2's complement) operation. Input voltage/output codes are shown in Table 3.

Amplifier A1, in conjunction with resistors R1, R2, and R3, offsets the bipolar analog input by full scale, and reduces its gain by a factor of 2. The analog signal applied to the AIN terminal is, therefore, a unipolar signal of 0 to +V or 0 to −V, depending on the polarity of V_{REF}.

ADJUSTMENT PROCEDURES UNIPOLAR OPERATION

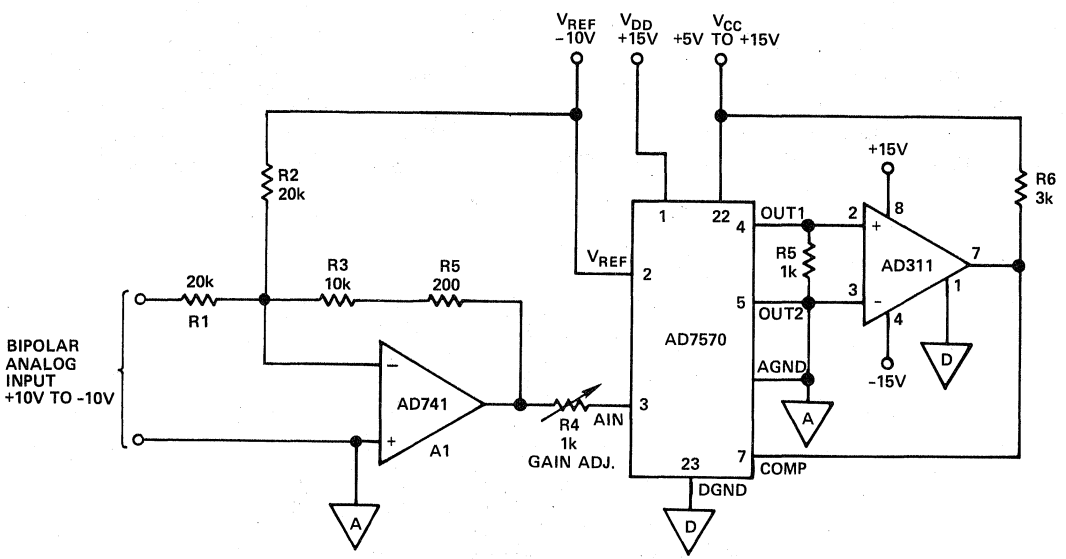
Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply full scale minus 1-1/2LSB to AIN.
3. Observe the SRO terminal as described under zero offset procedure above, and adjust the gain potentiometer (R4) until the LSB flickers between 0 and 1, and all other data bits equal "1". An alternate method is to adjust V_{REF} instead of using R4.



NOTE:
IF POSITIVE V_{REF} IS USED, THE ANALOG INPUT RANGE IS 0 TO $-V_{REF}$, AND THE COMPARATOR'S (–) INPUT SHOULD BE CONNECTED TO OUT1 (PIN 4) OF THE AD7570.

Figure 10. Unipolar Operation



NOTE: IF POSITIVE V_{REF} IS USED, CONNECT MINUS INPUT OF COMPARATOR TO OUT1 (PIN 4) OF THE AD7570.

Figure 11. Bipolar Operation

Table 2. Unipolar Operation

Analog Input (AIN) Notes 1, 2, 3	Digital Output Code MSB LSB
FS - 1LSB	1 1 1 1 1 1 1 1 1 1
FS - 2LSB	1 1 1 1 1 1 1 1 1 0
3/4 FS	1 1 0 0 0 0 0 0 0 0
1/2 FS + 1LSB	1 0 0 0 0 0 0 0 0 1
1/2 FS	1 0 0 0 0 0 0 0 0 0
1/2 FS - 1LSB	0 1 1 1 1 1 1 1 1 1
1/4 FS	0 1 0 0 0 0 0 0 0 0
1LSB	0 0 0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale, i.e., $(-V_{REF})$.
3. For 8-bit operation, 1LSB equals $(-V_{REF})$ (2^{-8}); for 10-bit operation, 1LSB equals $(-V_{REF})$ (2^{-10}).

Table 3. Bipolar Operation

Analog Input (AIN) Notes 1, 2, 3	Digital Output Code MSB LSB
+(FS - 1LSB)	1 1 1 1 1 1 1 1 1 1
+(FS - 2LSB)	1 1 1 1 1 1 1 1 1 0
+(1/2 FS)	1 1 0 0 0 0 0 0 0 0
+(1LSB)	1 0 0 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0 0 0 0
-(1LSB)	0 1 1 1 1 1 1 1 1 1
-(1/2 FS)	0 1 0 0 0 0 0 0 0 0
-(FS - 1LSB)	0 0 0 0 0 0 0 0 0 1
-FS	0 0 0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale; i.e., (V_{REF}).
3. For 8-bit operation, 1LSB equals $(-V_{REF})$ (2^{-7}); for 10-bit operation, 1LSB equals $(-V_{REF})$ (2^{-9}).

ADJUSTMENT PROCEDURES BIPOLAR OPERATION

Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply 1-1/2LSB less than positive full scale (FS = V_{REF}) to the bipolar analog input of Figure 11.
3. **Trim the gain potentiometer R4 for a flickering LSB, and all other data bits equal to Logic "1". Observe the SRO terminal, as described in zero offset procedure above.**

APPLICATION HINTS

1. Unused CMOS digital inputs should be tied to their appropriate logic level and not left floating. Open digital inputs may cause undesired digital activity in the presence of noise.
2. Analog and digital grounds should have separate returns.
3. Load the OUT1 terminal with a 1k resistor to reduce the time constant when operating at clock frequencies >50kHz.
4. For 10-bit operation, the comparator offset should be adjusted to less than 1mV. Each millivolt of comparator offset will cause approximately 0.015% of differential nonlinearity when a 10V reference is used.
5. The comparator input and output should be isolated to prevent oscillations due to stray capacitance. (See layout on the next page).
6. If an external clock is used, the negative transition of STRT should not coincide with the trailing edge of the clock input.

OPERATING PRECAUTIONS

1. Do not allow V_{CC} to exceed V_{DD}. In cases where V_{CC} could exceed V_{DD}, the diode protection scheme in Figure 12 is recommended.
2. Do not apply voltages greater than V_{CC} or lower than ground to any digital *output* from sources which can supply >20mA.
3. Do not apply voltages (from a source which can supply more than 5mA) lower than ground to the OUT1 or OUT2 terminal (see Figure 12).

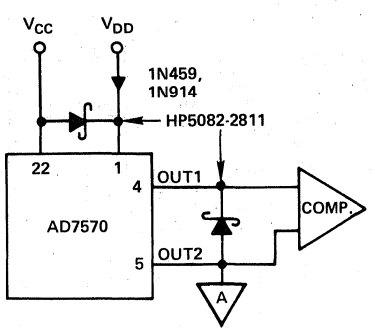
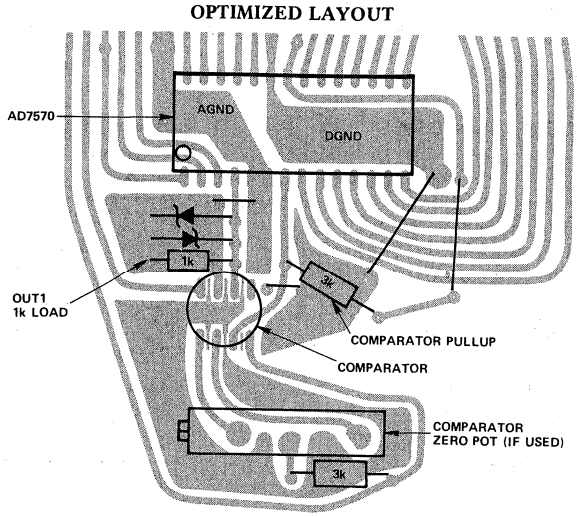


Figure 12. Diode Protection Scheme



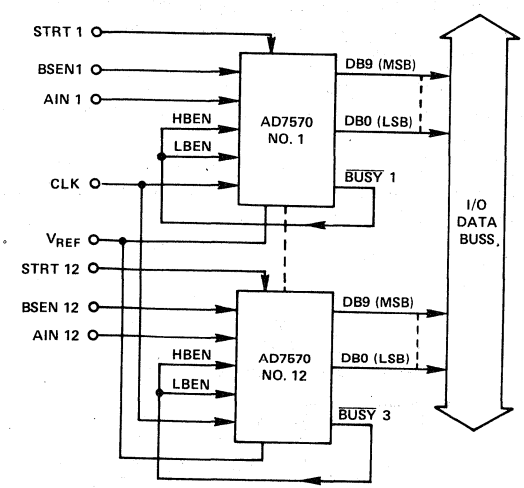
NOTES:
1. ALL PC TRACES ON BOTTOM OF BOARD.
2. LAYOUT SHOWN TERMINATES OUT1 INTO + INPUT OF AD311 TYPE COMPARATOR. (V_{REF} = -10V, AIN = 0 TO +10V).

Figure 13. PC Layout (Top View)

BUSING MULTIPLE AD7570 OUTPUTS

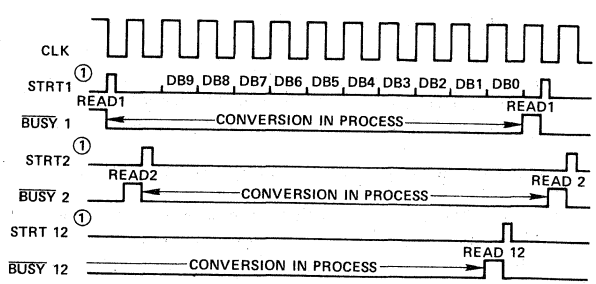
Several AD7570's may be paralleled to a data bus to provide an A/D converter per analog channel, this providing increased system throughput rate. For example, Figure 14 shows such a system for 12 AD7570's in parallel.

The three-state output logic enables of each AD7570 is controlled by its own BUSY (status) outputs. Thus, data is available at the A/D output only after conversion is complete, and until another "convert start" is initiated. The timing diagram of Figure 15 illustrates how the STRT signals of the twelve AD7570's might be staggered to provide a total system throughput twelve times as great as the classic method of data acquisition (an analog multiplexer feeding multichannel analog data to a single A/D converter).



NOTE: BSEN ON EACH AD7570 IS "ENABLED" (LOGIC 1).

Figure 14. Busing Multiple AD7570's



NOTE: STRT SIGNAL 0.5μs PULSE WIDTH, LEADING EDGE SYNCHRONIZED TO CLK TRAILING EDGE.

Figure 15. Timing Diagram

MICROPROCESSOR INTERFACE

Since most 8-bit microprocessors utilize a bidirectional data bus, each input peripheral (such as the AD7570) must be capable of isolating itself from the data bus when other I/O devices, memory, or the CPU takes control of the bus. The AD7570 output data and status (BUSY) lines all utilize three-state logic to provide this requirement.

Figure 16 illustrates a method of interfacing a TTY keyboard and printer to the AD7570, using an 8080 microprocessor as the interface controller.

The program (stored in Read Only Memory) waits for a keystroke on the TTY keyboard. When a keystroke is detected, an A/D conversion is started. When conversion is complete, the 8080 reads in the binary data from the AD7570, converts it to ASCII, and prints out the decimal number (preceded by a carriage return and line feed) on the teletype printer.

More specifically, the main sequence of events would be as follows:

1. When a TTY keystroke is detected by the CPU (via the UAR/T Receiver), a "convert start" (STRT) is applied to the AD7570.
2. BSEN is enabled, placing $\overline{\text{BUSY}}$ (conversion status) on the data bus. When the 8080 detects $\overline{\text{BUSY}} = 1$, conversion is complete, and BSEN is disabled, causing $\overline{\text{BUSY}}$ to return to its floating state.
3. LBEN is enabled, and the eight least significant data bits (DB0-DB7) are applied to the data bus for subsequent transfer to the 8080. When the data transfer is complete, LBEN is disabled, and DB0-DB7 return to their floating state.
4. HBEN is enabled, and the two most significant AD7570 data bits (DB8 and DB9) are applied to the data bus for subsequent transfer to the 8080. When the data transfer is complete, HBEN is disabled, and DB8 and DB9 return to their floating state.
5. The 8080 (in conjunction with the programmed Read Only Memory) performs a binary to decimal conversion.
6. $\overline{\text{SWE}}$ (Status Word Enable) on the UAR/T transmitter is enabled, applying XBMT (Transmitter Buffer Empty) to the data bus. When a Logic "1" is detected by the 8080, $\overline{\text{SWE}}$ is disabled, and XBMT returns to a floating state.
7. TDS (Transmitter Data Strobe) strobes the converted decimal number into the UAR/T transmitter for subsequent serial clocking into the keyboard.

The interface scheme shown below is only one example of a myriad of possible data acquisition/control systems which could conveniently use the AD7570 to provide digital data to a microprocessor or minicomputer bus.

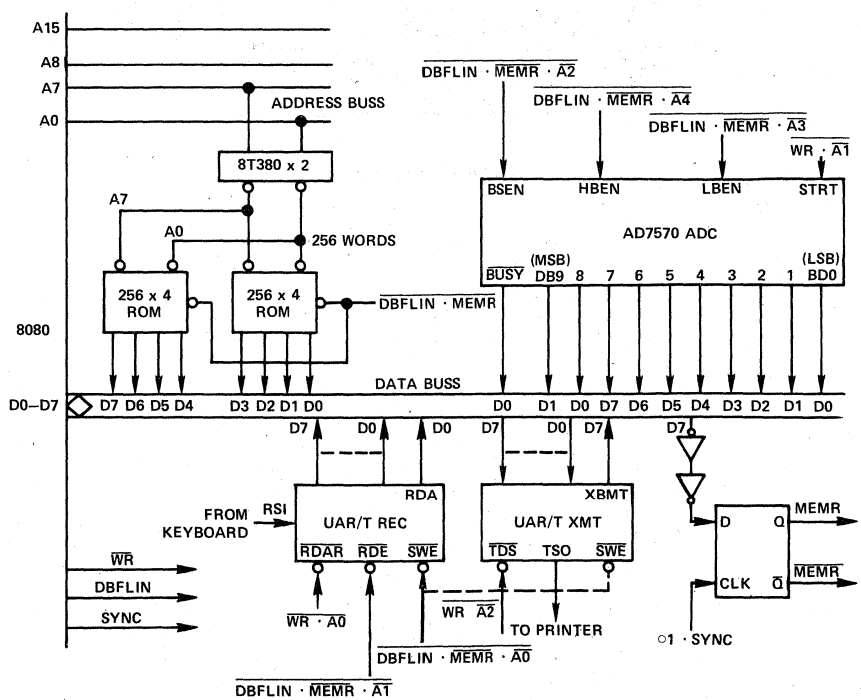


Figure 16. Microprocessor Controlled TTY/ADC Interface

TERMINOLOGY

Resolution
Resolution is the relative value of the LSB, or 2^{-n} for binary devices, for n-bit converters. It may be expressed as 1 part in 2^n, as a percentage, in parts-per-million, or simply by "n bits."

Relative Accuracy
Relative accuracy error is the difference between the nominal and actual ratios to full scale of the analog value corresponding to a given digital input, independently of the full-scale calibration. This error is a function of the linearity of the converter, and is usually specified at less than ±1/2LSB.

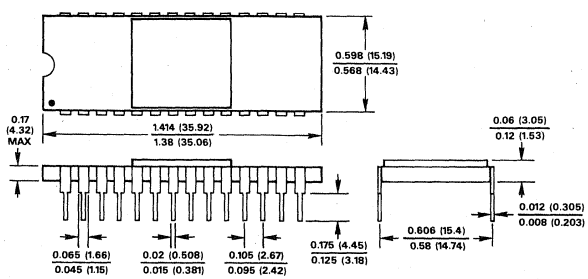
Gain Error
The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is adjusted either by setting the feedback resistor of a DAC, the input resistor in a current-comparing ADC, or the reference (voltage or current).

Differential Nonlinearity
In a converter, differential linearity error describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital input or output. If each transition is equal to its neighbors (i.e., 1LSB), the *differential nonlinearity* is zero. If a transition differs from one of its neighbors by more than 1LSB (e.g., if, at the transition 011. .11 to 100. . .00, the MSB is low by 1.1LSB), a D/A converter can be *non-monotonic,* or an A/D converter using it may miss one or more codes. A specified maximum differential nonlinearity of 1LSB ensures that monotonic behavior exists.

Output Leakage Current
Current which appears at the OUT1 terminal when all digital output (DB0 through DB9) are LOW, or on the OUT2 terminal when all digital outputs are HIGH. The effect of output leakage current will be on the offset of the A/D converter.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



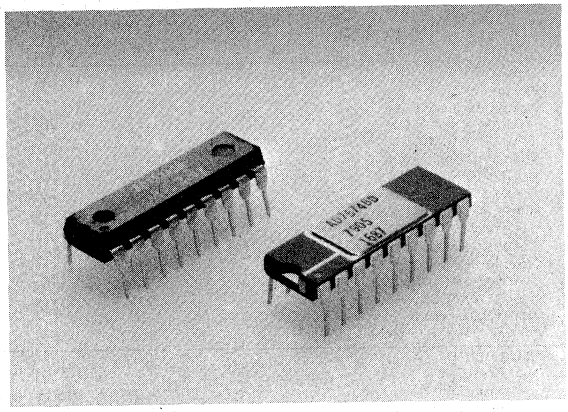
28 Pin Ceramic Dip

ANALOG DEVICES

CMOS µP Compatible 8-Bit ADC

AD7574

PRELIMINARY TECHNICAL DATA



FEATURES

- 8-Bit Resolution
- No Missed Codes over Full Temperature Range
- Fast Conversion Time: 15µs
- Interfaces to µP like RAM, ROM or Slow-Memory
- Low Power Dissipation: 30mW
- Ratiometric Capability
- Single +5V Supply
- Low Cost
- Internal Comparator and Clock Oscillator

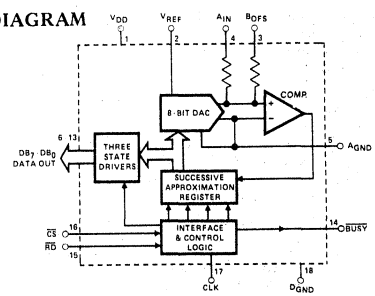
GENERAL DESCRIPTION

AD 7574 is a low-cost, 8-bit µP compatible ADC which uses the successive-approximations technique to provide a conversion time of 15µs.

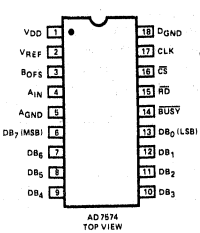
Designed to be operated as a memory mapped input device, the AD7574 can be interfaced like static RAM, ROM, or slow memory. It's $\overline{CS}$ (decoded device address) and $\overline{RD}$ ($\overline{READ}/\overline{WRITE}$ control) inputs are available in all µP memory systems. These two inputs control all ADC operations such as starting conversion or reading data. The ADC output data bits use three-state logic, allowing direct connection to the µP data bus or system input port.

Internal clock, +5V operation, on-board comparator and interface logic, as well as low power dissipation (30mW) and fast conversion time make the AD7574 ideal for most ADC/µP interface applications. Small size (18-pin DIP) and monolithic reliability will find wide use in avionics, instrumentation, and process automation applications.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

Differential Nonlinearity	Temperature Range and Package		
	Plastic 0°C to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
±7/8 LSB	AD7574JN	[1] AD7574AD	[1] AD7574SD
±3/4 LSB	AD7574KN	[1] AD7574BD	[1] AD7574TD

Note 1: Available 100% screened to MIL-STD-883, Class B. To order, add "/883B" to part number shown. See note 1, next page for details.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

DC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = -10V, Unipolar Configuration, R_{CLK} = 180kΩ, C_{CLK} = 100pF, unless otherwise noted)

PARAMETER	LIMITS T_A = +25°C	LIMITS T_{min}, T_{max}[1]	UNITS	CONDITIONS/COMMENTS
ACCURACY				
Resolution	8	8	Bits	
Relative Accuracy Error				
AD7574JN, AD, SD	±¾	±¾	LSB max	
AD7574KN, BD, TD	±½	±½	LSB max	Relative Accuracy and Differential Nonlinearity are measured dynamically using the external clock circuit of Fig. 7b.
Differential Nonlinearity				
AD7574JN, AD, SD	±⅞	±⅞	LSB max	Clock frequency is 500kHz (conversion time 15μs)
AD7574KN, BD, TD	±¾	±¾	LSB max	
Full Scale Error (Gain Error)				Full Scale Error is measured after calibrating out offset error. See
AD7574JN, AD, SD	±5	±6.5	LSB max	Fig. 8a and associated calibration procedure for offset. Max Full
AD7574KN, BD, TD	±3	±4.5	LSB max	Scale change from +25°C to T_{min} or T_{max} is ±2 LSB.
Offset Error[2]				
AD7574JN, AD, SD	±60	±80	mV max	Maximum Offset change from +25°C to
AD7574KN, BD, TD	±30	±50	mV max	T_{min} or T_{max} is ±20mV.
Mismatch Between B_{OFS} (pin 3) and A_{IN} (pin 4) Resistances[3]	±1.5	±1.5	%	
ANALOG INPUTS				
Input Resistance				
At V_{REF} (pin 2)	5/10/15	5/10/15	kΩ min/typ/max	
At B_{OFS} (pin 3)	10/20/30	10/20/30	kΩ min/typ/max	
At A_{IN} (pin 4)	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (for specified performance)	-10	-10	V	±5% for specified transfer accuracy.
V_{REF} Range[4]	-5 to -15	-5 to -15	V	Degraded transfer accuracy.
Nominal Analog Input Range				
Unipolar Mode	0 to +$\|V_{REF}\|$		V	
Bipolar Mode	-$\|V_{REF}\|$ to +$\|V_{REF}\|$		V	
LOGIC INPUTS				
RD (pin 15), CS (pin 16)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW Input Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	1	10	μA max	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	5	5	pF max	
CLK (pin 17)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW Input Voltage	+0.4	+0.4	V max	
I_{INH} Logic HIGH Input Current	+2	+3	mA max	During Conversion: $V_{IN(CLK)} \geq V_{INH(CLK)}$
I_{INL} Logic LOW Input Current	1	10	μA max	During Conversion: $V_{IN(CLK)} \leq V_{INL(CLK)}$ (see circuit of Fig. 7b if external clock operation is required).
LOGIC OUTPUTS				
BUSY (pin 14), DB_7 to DB_0 (pins 6-13)				
V_{OH} Output HIGH Voltage	+4.0	+4.0	V min	I_{SOURCE} = 40μA
V_{OL} Output LOW Voltage	+0.4	+0.8	V max	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating Stage Leakage	1	10	μA max	V_{OUT} = 0V or V_{DD}
Floating State Output Capacitance (DB_7 to DB_0)[5]	7	7	pF max	
Output Code	Unipolar Binary, Offset Binary			See Figs. 8a, 9a, 10a and 8b, 9b, 10b.
POWER REQUIREMENTS				
V_{DD}	+5	+5	V	±5% for specified performance.
I_{DD} (STANDBY)	5	5	mA max	A_{IN} = 0V, ADC in RESET condition.
I_{REF}	V_{REF} divided by 5kΩ		max	Conversion complete, prior to RESET.

Notes:

1. Temperature ranges as follows: JN, KN (0°C to +70°C)
   AD, BD (-25°C to +85°C)
   SD, TD (-55°C to +125°C)
   Screening to MIL-STD-883 is available. /883B versions are 100% screened to method 5004 for a class B device. Final electrical tests are performed at +25°C and +85°C (AD, BD versions) or +25°C and +125°C (SD, TD versions).
2. Typical offset temperature coefficient is ±150μV/°C.
3. R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive Full Scale. The effect is an offset and a gain term when using the circuit of Figure 9a.
4. Typical value, not guaranteed or subject to test.
5. Guaranteed but not tested

Specifications subject to change without notice.

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 180kΩ unless otherwise noted)

SYMBOL	SPECIFICATION	LIMIT at T_A = +25°C	LIMIT at $T_A = T_{min}$	LIMIT at $T_A = T_{max}$	CONDITIONS
STATIC RAM INTERFACE MODE (See Figure 1 and Table 1)					
t_{CS}	$\overline{CS}$ Pulse Width Requirement	100ns min	150ns min	150ns min	
t_{WSCS}	$\overline{RD}$ to $\overline{CS}$ Setup Time	0 min	0 min	0 min	
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	90ns typ 120ns max	70ns typ 120ns max	150ns typ 180ns max	$\overline{BUSY}$ Load = 20pF
		120ns typ 150ns max	100ns typ 150ns max	180ns typ 200ns max	$\overline{BUSY}$ Load = 100pF
t_{BSR}	$\overline{BUSY}$ to $\overline{RD}$ Setup Time	0 min	0 min	0 min	
t_{BSCS}	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0 min	0 min	0 min	
t_{RAD}	Data Access Time	120ns typ 150ns max	100ns typ 150ns max	180ns typ 220ns max	DB_0 - DB_7 Load = 20pF
		240ns typ 300ns max	220ns typ 300ns max	300ns typ 400ns max	DB_0 - DB_7 Load = 100pF
t_{RHD}	Data Hold Time	80ns typ 50ns min 120ns max	40ns typ 30ns min 80ns max	120ns typ 80ns min 180ns max	
t_{RHCS}	$\overline{CS}$ to $\overline{RD}$ Hold Time	250ns max	200ns max	500ns max	
t_{RESET}	Reset Time Requirement	3μs min	3μs min	3μs min	
$t_{CONVERT}$	Conversion Time using internal clock oscillator	See typical data of Figure 7a			
$t_{CONVERT}$	Conversion Time using external clock	15μs	15μs	15μs	f_{CLK} = 500kHz circuit of Figure 7b
ROM INTERFACE MODE (See Figure 2 and Table 2)					
t_{RAD}	Data Access Time	Same as RAM Mode			
t_{RHD}	Data Hold Time	Same as RAM Mode			
t_{WBPD}	$\overline{RD}$ HIGH to $\overline{BUSY}$ Propagation Delay	400ns typ 1.5μs max	350ns typ 1.0μs max	1μs typ 2.0μs max	$\overline{BUSY}$ Load = 20pF
t_{BSR}	$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	$\overline{RD}$ can go LOW prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table 2			
$t_{CONVERT}$	Conversion Time using internal clock oscillator	See typical data of Figure 7a. Add 2μs to data shown in Figure 7a for ROM Mode			
SLOW – MEMORY INTERFACE MODE (See Figure 3 and Table 3)					
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	Same as RAM Mode			
t_{RESET}	Reset Time Requirement	Same as RAM Mode			
t_{RAD}	Data Access Time	Same as RAM Mode			
t_{RHD}	Data Hold Time	Same as RAM Mode			
$t_{CONVERT}$	Conversion Time	Same as RAM Mode			

ABSOLUTE MAXIMUM RATINGS

V_{DD} to A_{GND} . . . . . 0V, +7.0V
V_{DD} to D_{GND} . . . . . 0V, +7.0V
A_{GND} to D_{GND} . . . . . -0.3V, V_{DD}
Digital Input Voltage to D_{GND}
(pins 15 and 16) . . . . . -0.3V, +15.0V
Digital Output Voltage to D_{GND}
(pins 6 - 14) . . . . . -0.3V, V_{DD}
CLK Input Voltage (pin 17) to D_{GND} . . . . . -0.3V, V_{DD}
V_{REF} (pin 2) . . . . . ±20V
V_{BOFS} (pin 3) . . . . . ±20V
V_{AIN} (pin 4) . . . . . ±20V

Operating Temperature Range
JN, KN . . . . . 0°C to +70°C
AD, BD . . . . . -25°C to +85°C
SD, TD . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 secs.) . . . . . +300°C
Power Dissipation (Package)
Plastic (suffix N)
to +70°C 670mW
Derate above +70°C by . . . . . 8.3mw/°C
Ceramic (suffix D)
to +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C

TERMINOLOGY

RESOLUTION: Resolution is a measure of the *nominal* analog change required for a 1-bit change in the A/D converter's digital output. While normally expressed in a number of bits, the analog resolution of an n-bit unipolar A/D converter is $(2^{-n})(V_{REF})$. Thus the AD7574, an 8-bit A/D converter, can resolve analog voltages as small as $(1/256)(V_{REF})$ when operated in a unipolar mode. When operated in a bipolar mode, the resolution is $(1/128)(V_{REF})$. Resolution does not imply accuracy. *Usable* resolution is limited by the differential nonlinearity of the A/D converter.

RELATIVE ACCURACY: Relative accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the device's measured zero and measured full scale transition points. Relative accuracy, therefore, is a measure of code *position*.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity in an ADC is a measure of the size of an analog voltage range associated with any digital output code. As such differential nonlinearity specifies code width (usable resolution). An ADC with a specified differential nonlinearity of ±n bits will exhibit codes ranging in width from 1LSB - nLSB to 1LSB + nLSB. A specified differential nonlinearity of less than ±1LSB guarantees no-missing-codes operation.

TIMING & CONTROL OF THE AD7574

STATIC RAM INTERFACE MODE

Table 1 and Figure 1 show the truth table and timing requirements for AD7574 operation as a static RAM.

A convert start is initiated by executing a memory WRITE instruction to the address location occupied by the AD7574 (once conversion has started, subsequent memory WRITES have no effect). A data READ is performed by executing a memory READ instruction to the AD7574 address location.

$\overline{BUSY}$ must be HIGH before a data READ is attempted, i.e. the total delay between a convert start and a data READ must be at least as great as the AD7574 conversion time. The delay can be generated by inserting NOP instructions (or other program instructions) between the WRITE (start convert) and READ (read data) operations. Once $\overline{BUSY}$ is HIGH (conversion complete), a data READ is performed by executing a memory READ instruction to the address location occupied by the AD7574. The data readout is destructive, i.e. when RD returns HIGH, the converter is internally reset.

The RAM interface mode uses distinctly different commands to start conversion (memory WRITE) or read the data (memory READ). This is in contrast to the ROM mode where a memory READ causes a data READ *and* a conversion restart.

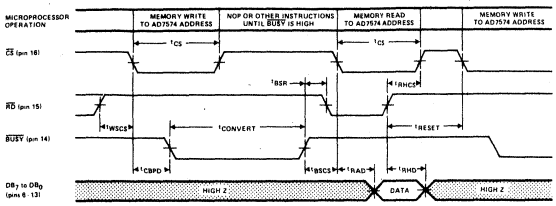


Figure 1. Static RAM Mode Timing Diagram

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB_7 - DB_0	
L	H	H	HIGH Z	WRITE CYCLE (START CONVERT)
L	⌐	H	HIGH Z → DATA	READ CYCLE (DATA READ)
L	⌐	H	DATA → HIGH Z	RESET CONVERTER
H	X[1]	X	HIGH Z	NOT SELECTED
L	H	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	⌐	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	⌐	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

Note 1: If $\overline{RD}$ goes LOW-to-HIGH, the ADC is internally reset, regardless of the state of $\overline{CS}$ or $\overline{BUSY}$.

Table 1. Truth Table, Static RAM Mode

ROM INTERFACE MODE

Table 2 and Figure 2 show the truth table and timing requirements for interfacing the AD7574 like Read Only Memory.

$\overline{CS}$ is held LOW and converter operation is controlled by the $\overline{RD}$ input. The AD7574 $\overline{RD}$ input is derived from the decoded device address. MEMRD should be used to enable the address decoder in 8080 systems. VMA should be used to enable the address decoder in 6800 systems. A data READ is initiated by executing a memory READ instruction to the AD7574 address location. The converter is automatically restarted when $\overline{RD}$ returns HIGH. As in the RAM mode, attempting a data READ before $\overline{BUSY}$ is HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is relatively poorly defined in time inasmuch as executing a data READ automatically starts a new conversion. This problem can be overcome by executing two READs separated by NO-OPS (or other program instructions) and using only the data obtained from the second READ.

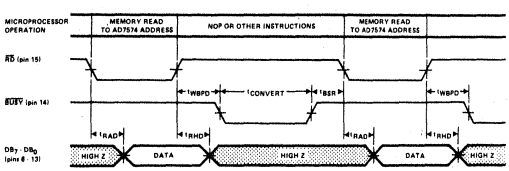


Figure 2. ROM Mode Timing Diagram ($\overline{CS}$ Held LOW)

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB_7 - DB_0	
L	⌐	H	HIGH Z → DATA	DATA READ
L	⌐	⌐	DATA → HIGH Z	RESET AND START NEW CONVERSION
L	⌐	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	⌐	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

Table 2. Truth Table, ROM Mode

SLOW-MEMORY INTERFACE MODE

Table 3 and Figure 3 show the truth table and timing requirements for interfacing the AD7574 as a slow-memory. This mode is intended for use with processors which can be forced into a WAIT state for at least 12μs (such as the 8080, 8085 and SC/MP). The major advantage of this mode is that it allows the μP to start conversion, WAIT, and then READ data with a single READ instruction.

In the slow-memory mode, $\overline{CS}$ and $\overline{RD}$ are tied together. It is suggested that the system ALE signal (8085 system) or SYNC signal (8080 system) be used to latch the address. The decoded device address is subsequently used to drive the AD7574 $\overline{CS}$ and $\overline{RD}$ inputs. $\overline{BUSY}$ is connected to the microprocessor READY input.

When the AD7574 is NOT addressed, the $\overline{CS}$ and $\overline{RD}$ inputs are HIGH. Conversion is initiated by executing a memory READ to the AD7574 address. $\overline{BUSY}$ subsequently goes LOW (forcing the μP READY input LOW) placing the μP in a WAIT state. When conversion is complete ($\overline{BUSY}$ is HIGH) the μP completes the memory READ.

Do not attempt to perform a memory WRITE in this mode, since three-state bus conflicts will arise.

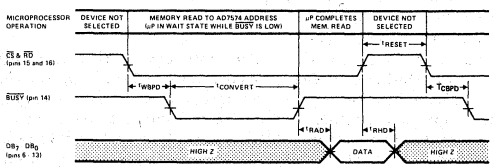


Figure 3. Slow Memory Mode Timing Diagram (CS and RD Tied Together)

AD7574 INPUTS	AD7574 OUTPUTS		AD7574 OPERATION
CS & RD	BUSY	DB_7 - DB_0	
H	H	HIGH Z	NOT SELECTED
⌐	H→L	HIGH Z	START CONVERSION
L	L	HIGH Z	CONVERSION IN PROGRESS, μP IN WAIT STATE
L	⌐	HIGH Z→DATA	CONVERSION COMPLETE, μP READS DATA
⌐	H	DATA→HIGH Z	CONVERTER RESET AND DESELECTED
H	H	HIGH Z	NOT SELECTED

Table 3. Truth Table, Slow Memory Mode

GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7574 uses the successive approximations technique to provide an 8-bit parallel digital output. The control logic was designed to provide easy interface to most microprocessors. Most applications require only passive clock components (R & C), a -10V reference, and +5V power.

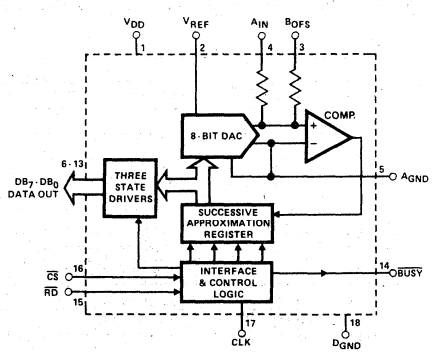


Figure 4. AD7574 Functional Diagram

Figure 4 shows the AD7574 functional diagram. Upon receipt of a start command either via the $\overline{CS}$ or $\overline{RD}$ pins for Control Logic and Timing Details), $\overline{BUSY}$ goes low indicating conversion is in progress. Successive bits, starting with the most significant bit (MSB), are applied to the input of a DAC. The comparator determines whether the addition of each successive bit causes the DAC output to be greater than or less than the analog input, A_{IN}. If the sum of the DAC bits is less than A_{IN}, the trial bit is left ON, and the next smaller bit is tried. If the sum is greater than A_{IN}, the trial bit is turned OFF and the next smaller bit is tried.

Each successively smaller bit is tried and compared to A_{IN} in this manner until the least significant bit (LSB) decision has been made. At this time $\overline{BUSY}$ goes HIGH (conversion is complete) indicating the successive approximation register contains a valid representation of the analog input. The $\overline{RD}$ control (see the previous page for details) can then be exercised to activate the three-state buffers, placing data on the DB_0 - DB_7 data output pins. $\overline{RD}$ returning HIGH causes the clock oscillator to run for 1 cycle, providing an internal ADC reset (i.e. the SAR is loaded with code 10000000).

DAC CIRCUIT DETAILS

The current weighting D/A converter is a precision multiplying DAC. Figure 5 shows the functional diagram of the DAC as used in the AD7574. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted, i.e. the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the DAC logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

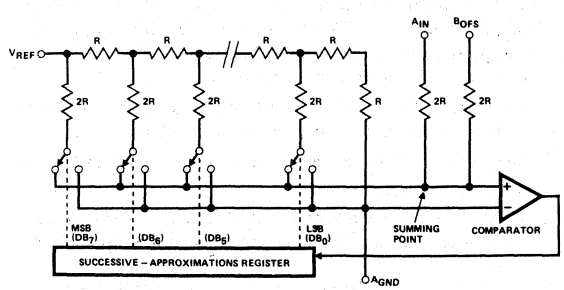


Figure 5. D/A Converter As Used In AD7574

OPERATING THE AD7574

APPLICATION HINTS

1. TIMING & CONTROL
   Failiure to observe the timing restrictions of figures 1, 2 or 3 may cause the AD7574 to change interface modes. For example, in the RAM mode, holding $\overline{CS}$ LOW too long after $\overline{RD}$ goes HIGH will cause a new convert start (i.e. the converter moved into the ROM mode).
2. LOGIC DEGLITCHING IN uP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7574 $\overline{CS}$ or $\overline{RD}$ terminals. These glitches can cause unwanted convert starts, reads, or resets. The best way to avoid glitches is to gate the address decoding logic with RD or WR (8080) or VMA (6800) when in the ROM or RAM mode. When in the slow-memory mode, the ALE (8085) or SYNC (8080) signal should be used to latch the address.
3. INPUT LOADING AT V_{REF}, A_{IN} AND B_{OFS}
   To prevent loading errors due to the finite input resistance at the V_{REF}, A_{IN} or B_{OFS} pins, low impedance driving sources must be used (i.e. op amp buffers or low output-Z reference).
4. RATIOMETRIC OPERATION
   Ratiometric performance is inherent to A/D converters such as the AD7574 which use a multiplying DAC weighting network. However, the user should recognize that comparator limitations such as offset voltage, input noise and gain will cause degradation of the transfer characteristics when operating with reference voltages less than -10V in magnitude.
5. OFFSET CORRECTION
   Offset error in the transfer characteristic can be trimmed by offsetting the buffer amplifier which drives the AD7574 A_{IN} pin (pin 4). This can be done either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between V_{DD} and V_{REF} and applying the tap voltage to the amplifier's positive input (an example of a resistive tap offset adjust is shown in Figure 10a where R_8, R_9 and R_{10} can be used to offsct the ADC).
6. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7574. In systems where the A_{GND}-D_{GND} intertie is not local, connect back-to-back diodes (IN914 or equivalent) between the AD7574 A_{GND} and D_{GND} pins.
7. INITIALIZATION AFTER POWER – UP
   Execute a memory READ to the AD7574 address location, and subsequently ignore the data. The AD7574 is internally reset when reading out data, i.e. the data readout is destructive.

CLOCK OSCILLATOR

The AD7574 has an internal asynchronous clock oscillator which starts upon receipt of a convert start command, and ceases oscillating when conversion is complete.

The clock oscillator requires an external R and C as shown in figure 6. Nominal conversion time versus R_{CLK} and C_{CLK} is shown in Figure 7a. The curves shown in Figure 7a are applicable when operating in the RAM or slow-memory interface modes. When operating in the ROM interface mode, add 2μs to the typical conversion time values shown.

The AD7574 is guaranteed to provide transfer accuracy to published specifications for conversion times down to 15μs, as indicated by the unshaded region of Figure 7a. Conversion times faster than 15μs can cause transfer accuracy degradation.

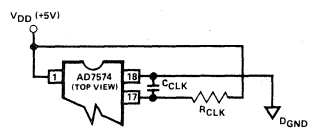


Figure 6. Connecting R_{CLK} and C_{CLK} To CLK Oscillator

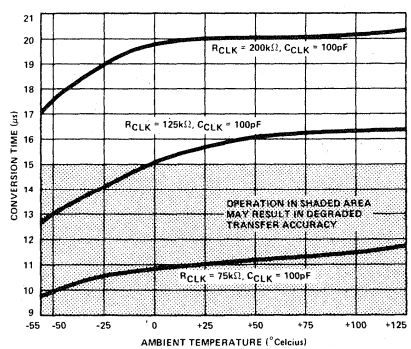


Figure 7a. Typical Conversion Time vs. Temperature For Different R_{CLK} and C_{CLK} (Applicable to RAM and Slow-Memory Modes. For ROM Mode add 2μs to values shown)

OPERATION WITH EXTERNAL CLOCK

For applications requiring a conversion time close to or equal to 15μs, an external clock is recommended. Using an external clock precludes the possibility of converting faster than 15μs (which can cause transfer accuracy degradation) due to temperature drift – as may be the case when using the internal clock oscillator.

Figure 7b shows how the external clock must be connected. The $\overline{BUSY}$ output of the AD7574 is connected to the three-state enable input of a 74125 three-state buffer. R_1 is used as a pullup, and can be between 6kΩ and 100kΩ. A 500kHz clock will provide a conversion time of 15μs.

The external clock should be used only in the static-RAM or slow-memory interface mode, and *not* in the ROM mode.

Timing constraints for external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.
2. A data READ can be initiated any time after BUSY = 1.

SLOW-MEMORY MODE

1. When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.

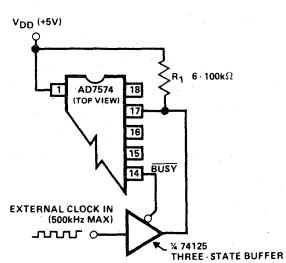


Figure 7b. External Clock Operation (Static RAM and Slow-Memory Mode)

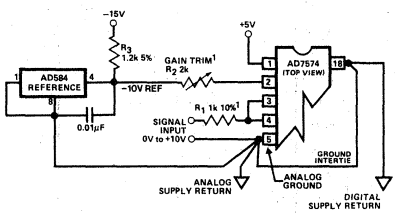
UNIPOLAR BINARY OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar operation. An AD584 is used as the -10V reference.

Calibration is as follows:

OFFSET

Offset must be trimmed out in the signal conditioning circuitry used to drive the signal input terminals shown in Figure 8a. An example of an offset trim is shown in Figure 10a, where R_8, R_9 and R_{10} comprise a simple voltage tap which is applied to the amplifier's positive input.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

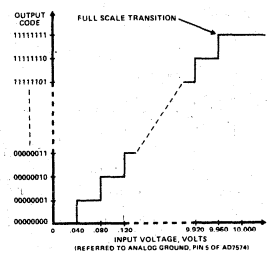
Figure 8a. AD7574 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

1. Apply -39.1mV (1 LSB) to the input of the buffer amplifier used to drive R_1 (i.e. +39.1mV at R_1).
2. While performing continuous conversions, adjust the offset potentiometer (described above) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

Offset adjustment must be performed before gain adjustment.

1. Apply -9.961V to the input of the buffer amplifier used to drive R_1 (i.e. +9.961V at R_1).
2. While performing continuous conversions, adjust trim pot R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers.



Note: Approximate bit weights are shown for illustration. Nominal bit weight for a -10V reference is ≈ 39.1mV

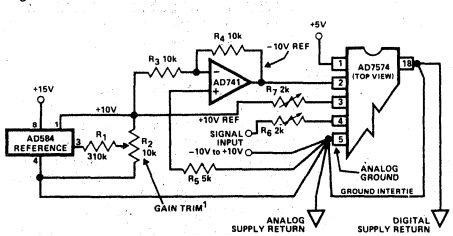
Figure 8b. Nominal Transfer Characteristic For Unipolar Circuit of Figure 8a

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for bipolar operation. Output coding is offset binary. As in unipolar operation, offset correction can be performed at the buffer amplifier used to drive the signal input terminals of Figure 9a (Resistors R_8, R_9 and R_{10} in Figure 10a show how offset trim can be done at the buffer amplifier).

Calibration is as follows:

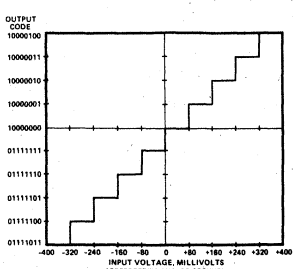
1. Adjust R_6 and R_7 for minimum resistance across the potentiometers.
2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at R_6).
3. While performing continuous conversions, trim R_6 or R_7 (whichever required) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

Figure 9a. AD7574 Bipolar (-10V to +10V) Operation (Output Code is Offset Binary)

4. Apply 0V to the buffer amplifier used to drive the signal input terminals.
5. Doing continuous conversions, trim the offset circuit of the buffer amplifier until the ADC output code flickers between 01111111 and 10000000.
6. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to R_6).
7. Doing continuous conversions, trim R_2 until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.
8. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of R_6).
9. If the ADC output code is not 11111110 ±1 bit, repeat the calibration procedure.



Note: Approximate bit weights are shown for illustration. Nominal bit weight for ± 10V full scale is ≈ 78.1mV

Figure 9b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

OPERATING THE AD7574

BIPOLAR (COMPLEMENTARY OFFSET BINARY) OPERATION

Figure 10a shows the analog connections for complementary offset binary operation. The typical transfer characteristic is shown in Figure 10b. In this bipolar mode, the ADC is fooled into believing it is operated in a unipolar mode - i.e. the +10V to -10V analog input is conditioned into a 0 to +10V signal range. R_2 is the gain adjust, while R_9 is the offset adjust.

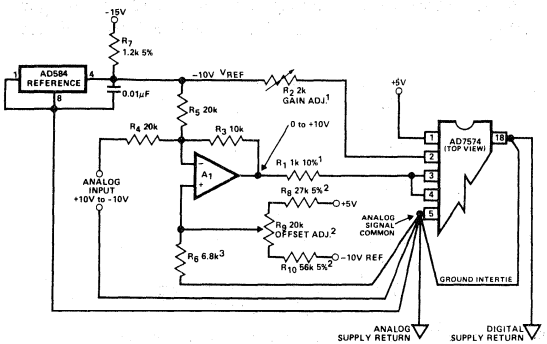
Calibration is as follows (adjust offset before gain):

OFFSET

1. Apply OV to the analog input shown in Figure 10a.
2. While performing continuous conversions, adjust R_9 until the converter output flickers between codes 01111111 and 10000000.

GAIN (FULL SCALE)

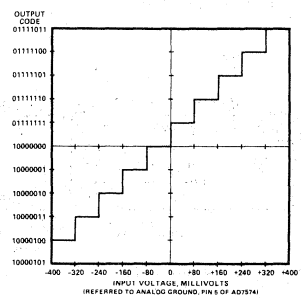
1. Apply -9.922V across the analog input terminals shown in Figure 10a.
2. While performing continuous conversions, adjust R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers between HIGH and LOW.



Notes:

1. R_1 and R_2 can be omitted if gain trim is not required
2. R_8, R_9 and R_{10} can be omitted if offset trim is not required
3. $R_6 \| R_8 \| R_{10} = 5k\Omega$. If R_8, R_9 and R_{10} not used, make $R_6 = 5k\Omega$

Figure 10a. AD7574 Bipolar Operation (-10V to +10V) (Output Code is Complementary Offset Binary)

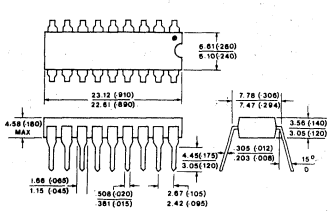


Note: Approximate bit weights are shown for illustration. Nominal bit weight for ±10V full scale is ≈78.1mV

Figure 10b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 10a

MECHANICAL INFORMATION

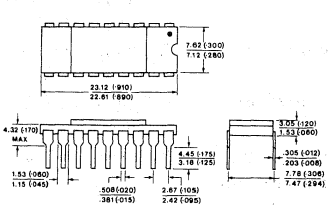
18 PIN PLASTIC DIP



Notes:

1. Lead no.1 identified by dot or notch.
2. Dimensions in mm (in.).
3. Leads are solder plated KOVAR or ALLOY 42.

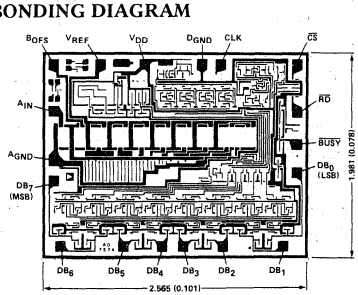
18 PIN CERAMIC DIP



Notes:

1. Lead no. 1 identified by dot or notch.
2. Leads are gold plate (50µin. min.) over Nickel (100µin. nominal). Base material is KOVAR or ALLOY 42.
3. Cavity lid is electrically isolated.

BONDING DIAGRAM



Notes:

1. Bond D_{GND} first to minimize ESD hazard.
2. Die dimensions are in mm. (in.), and may vary from nominal shown on layout by ±0.076mm (±0.003in.).
3. Die thickness is 0.508mm ±0.025mm (0.020in. ±0.001in.).
4. Gold backing is not available.
5. Passivation covers all topside surface area except bonding pads, test pads and scribe lines.
6. Surface matallization is Al, 10kÅ min.
7. Bonding pads are 0.102mm x 0.102mm (0.004in. x 0.004in.). Passivation window is 0.089mm x 0.089mm min. (0.0035in. x 0.0035in. min.).

ANALOG DEVICES

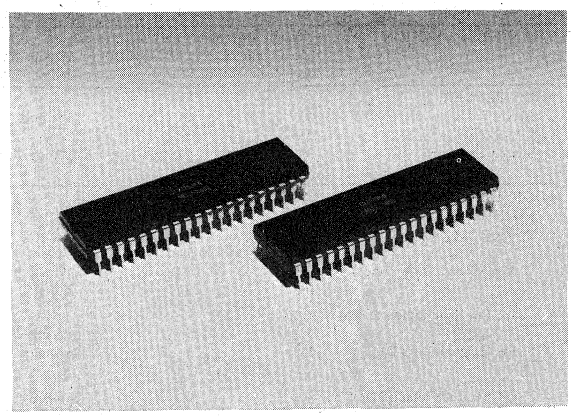
CMOS Single Supply, 9-Channel, 8-Bit ADC

AD7583

PRELIMINARY TECHNICAL DATA

FEATURES

- 8-Bit Resolution and Accuracy
- 9-Channel Analog Input (Expandable)
- Single Supply +5V to +15V Operation
- Easily Interfaced to Most μP's via an I/O Port
- Low Power Consumption
- Ratiometric
- TTL/CMOS Compatible



GENERAL DESCRIPTION

The AD7583 is a monolithic CMOS, 9-channel (expandable), 8-bit A/D converter designed for single supply operation (+5V to +15V), making it highly suited to battery operation. It provides accuracy with stability using a patented integrating technique (ADI patent No. 3872466) called "quad slope".

Most applications require the addition of only a few passive components and two general purpose operational amplifiers.

Digital information (channel address input, converted output data) is passed to and from the AD7583 via an 8-bit bidirectional I/O bus under command of control signals $\overline{I/O}$ (Input/Output) and IOS (IO Strobe).

The A/D converter responds to analog inputs ranging from $0.15V_{REF}$ to $0.85V_{REF}$. In single supply applications, this precludes the necessity for signal conditioning circuitry whose output swings to the supply rails. It also facilitates connection to ratiometric transducers whose zero output may not be at "true zero".

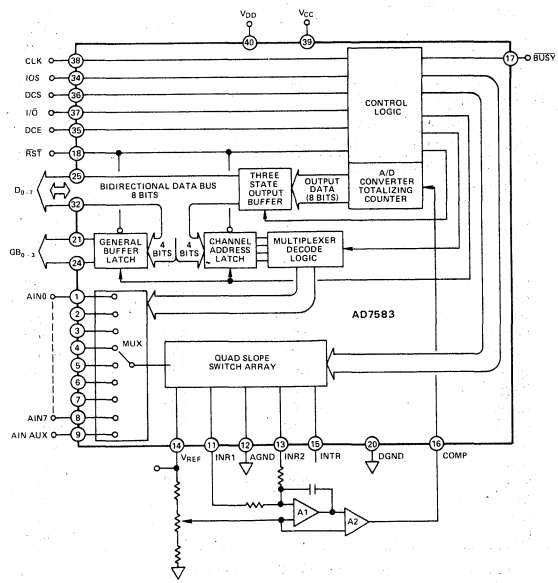
Direct TTL input/output interface is provided when V_{CC} = +5V. Putting V_{CC} equal to the CMOS logic supply voltage provides CMOS compatibility.

Single supply operation, low power consumption and easy hardware interface to μP's make the AD7583 useful in a wide variety of data-acquisition and process-control applications.

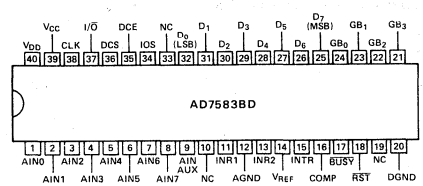
ORDERING INFORMATION

Model	Temperature Range	Package
AD7583KN	0 to +70°C	40 pin plastic DIP

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



SPECIFICATIONS

(V_{REF} = V_{DD} = 12V, V_{CC} = 5V, f_{CLK} = 1.28MHz, R_1 = R_2 = 2MΩ, R_3 = R_4 = 10kΩ, C_1 = 0.001μF unless otherwise noted. Amplifier A_1 has input error less than 1.4% of V_{REF}. See page 10-94, Selecting an Integrator Amplifier).

PARAMETER	T_A = 25°C	T_A = T_{min}/T_{max}	UNITS	CONDITIONS	COMMENTS
ACCURACY					The AD7583 rounds down to the nearest integer value. At reduced V_{DD} typical values for Relative Accuracy, Full Scale Error and Zero Scale Error are: For 9≤V_{DD}≤15, ±1 count; for 7≤V_{DD}≤9, ±2 counts; for 5≤V_{DD}≤7, ±4 counts.
Resolution	8	8	Bits		
Relative Accuracy	±1	±1	Counts max		
Differential Nonlinearity	±1	±1	Counts max		
Full Scale Error	±1	±1	Counts max	AIN = 0.85V_{REF}	
Zero Scale Error	±1	±1	Counts max	AIN = 0.15V_{REF}	
TRANSFER FUNCTION	Straight unipolar binary see Table 2. Zero scale output (00000000) at AIN≤0.15V_{REF} Full scale output (11111111) at AIN≥0.85V_{REF}				
MULTIPLEXER					
R_{ON}	2	2	kΩ max	0.15V_{REF} ≤ AIN ≤ 0.85V_{REF}	
$\Delta R_{ON}/AIN$[1]	30	30	% typ		
Switch Leakage[1]	±1	±1	μA max	Multiplexer 'common' at GND Multiplexer input at V_{DD}	
LOGIC INPUTS (CLK, IOS, DCS, I/$\overline{O}$, DCE, $\overline{RST}$, D_{0-7})					
V_{INH} (Logic High Input)	2.4	2.4	V min	V_{CC} = 5V	
	11.5	11.5	V min	V_{CC} = 12V	
V_{INL} (Logic Low Input)	0.8	0.8	V max	V_{CC} = 5V	
	0.5	0.5	V max	V_{CC} = 12V	
I_{IN} (all logic inputs except D_{0-7})	5	5	μA max	V_{IN} = 0, 5V, 12V	
I_{IN} (Logic inputs D_{0-7})	5	5	μA max	V_{IN} = 0, 5V, 12V measured when 3-state bus is disabled.	
C_{IN} (Input Capacitance)[2]	8	8	pF typ		
LOGIC OUTPUTS (D_{0-7}, $\overline{BUSY}$ GB_{0-3})					
V_{OH} (Logic High Output)	2.8	2.8	V min	V_{CC}= 5V I_{SOURCE} = 40μA	
	11.5	11.5	V min	V_{CC} = 12V I_{SOURCE} = 0.6mA	
V_{OL} (Logic Low Output)	0.4	0.4	V max	V_{CC} = 5V I_{SINK} = 1.6mA	
	0.5	0.5	V max	V_{CC} = 12V I_{SINK} = 1.0μA	
I_L, 3-State Output Leakage	10	10	μA max		
POWER SUPPLY CURRENT					
I_{CC} (V_{CC} Supply Current)	2	2	mA max	f_{CLK} = 1.28MHz	
I_{DD} (V_{DD} Supply Current)	20	20	mA max		
DYNAMIC PERFORMANCE[3]					
Conversion Time	4	4	ms max	f_{CLK} = 1.28MHz	See "Conversion Time" Page 10-94
f_{CLK}	1.28	1.28	MHz max		
t_{BSIO}	1100	1100	ns min		$\overline{BUSY}$ to IOS Set Up Time Figure 6
t_{IOS}	500	500	ns min		IOS Pulse Width Figure 6
t_{AD}	650	650	ns min		Data Access Time Figure 6
t_{HD}	300	300	ns min		Data Hold Time Figure 6
t_{IO}	1200	1200	ns min		I/$\overline{O}$ Pulse Width Figure 5
t_{WOS}	500	500	ns min		I/$\overline{O}$ Setup Time Figure 5
t_{WOH}	200	200	ns min		I/O Hold Time Figure 5
t_{DS2}	200	200	ns min		Data Setup Time Figure 5
t_{DH2}	200	200	ns min		Data Hold Time Figure 5
t_{IDPD}	1450	1450	ns max		IOS to $\overline{BUSY}$ Propagation Delay Figure 5
t_{IGPD}	650	650	ns max		IOS to General Buffer Latched Delay Figure 5
t_{DCE}	750	750	ns min		DCE Pulse Width Figure 4
t_{DDS}	250	250	ns min		DCE Setup Time
t_{PCS}	500	500	ns min		DCS Pulse Width
t_{DDH}	0	0	ns min		DCE Hold Time
t_{DSI}	200	200	ns min		Device Address Setup Time
t_{DHI}	500	500	ns min		Device Address Hold Time

[1] Typical values not guaranteed or subjected to production test.
[2] Guaranteed not tested.
[3] AC parameters sample tested at +25° C to ensure specification compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND . . . . . 0V, +17V
V_{CC} to DGND . . . . . .0V, V_{DD}
Digital Input Voltage to DGND
CLK, IOS, DCS, I/$\overline{O}$, DCE, $\overline{RST}$ . . . . . .-0.3V, V_{CC}
Digital Output Voltage to DGND
$\overline{BUSY}$, GB_{0-3} . . . . . -0.3V, V_{CC}
I/O Bus (D_{0-7}) to DGND. . . . . -0.3V, V_{CC}
AGND to DGND. . . . . .-0.3V, V_{DD}
Analog Inputs/Outputs to AGND
COMP, AIN0 - AINAUX, V_{REF}, INTR, INR1 INR2
. . . . . .-0.3V, V_{DD}
Power Dissipation (Package)
Up to +50°C. 1000mW
Derates Above +50° by. . . . . 10mW/°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (soldering, 10s) . . . . . +300°C
Operating Temperature Range . . . . . -25°C to +85°C

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	FUNCTION
1	AIN0	Analog Input Channel 0
2-8	AIN1-AIN7	Analog Input Channels 1-7
9	AIN AUX	Auxiliary Analog Input - Can be used for channel expansion as shown in Figure 8.
10	NC	Not Connected
11	INR1	Integrator Resistor 1 (see Figure 7)
12	AGND	Analog Ground
13	INR2	Integrator Resistor 2 (see Figure 7)
14	V_{REF}	Reference Voltage Input. The reference voltage must be a positive voltage $\leq V_{DD}$.
15	INTR	Integrator reset pin, normally should be connected to AGND.
16	COMP	Input to AD7583 from output of the external comparator (A2 in Figure 7)
17	$\overline{BUSY}$	Status Output. When HIGH, indicates conversion is complete and that data can be read-out.
18	$\overline{RST}$	RESET Input (active low); resets control logic, general buffer latch, channel address latch, and device enable latch.
19	NC	Not Connected
20	DGND	Digital Ground
21-24	GB_3-GB_0	General Buffer Outputs. When writing a channel address (and convert start command), data at D_{4-7} is strobed into the general buffers on the positive edge of IOS. (D_4 is latched into GB_0, D_5 into GB_1, D_6 into GB_2 and D_7 into GB_3)
25	D_7	I/O Bus (MSB)
26-31	D_{6-1}	I/O Bus
32	D_0	I/O Bus (LSB)
33	NC	Not Connected
34	IOS	I/O Strobe Input. If the device enable latch is *SET* and I/$\overline{O}$ is High, analog channel address data on D_{0-3} is latched into the channel address latch on the positive edge of IOS. The phase 0 integration cycle begins within 1 clock period *after* the leading edge of IOS. If the device enable latch is *SET*, if $\overline{BUSY}$ is HIGH and if I/$\overline{O}$ is LOW; the 3-state output buffers are activated, placing converted data on D_{0-7} during the time IOS is held HIGH.
35	DCE	Decode Enable Input. If DCE is HIGH, and if code XXX11001 is placed on D_{0-7}, strobing DCS *SETs* the Device Enable Latch. If DCS is strobed when DCE is LOW, the device enable latch is *RESET*.
36	DCS	Decode Strobe Input. See DCE above.
37	I/$\overline{O}$	I/O control input. When I/$\overline{O}$ is HIGH, the AD7583 is in a data Input mode (write channel address and convert start). When I/$\overline{O}$ is LOW, the AD7583 is in a data Output mode (data READ).
38	CLK	Clock Input
39	V_{CC}	Logic Supply Input, range +5V to V_{DD}. For TTL output levels, put V_{CC} = +5V.
40	V_{DD}	Main Supply input, range +5V to +15V.

A/D CONVERTER OPERATION

Figures 1 and 2 show the basic converter circuit and its corresponding timing diagram. The inputs AGND (Analog GrouND), V_{REF} (Voltage REFerence) AIN (Analog INput) and INTR (INTegrator Reset) are applied to the integrator via switches 1 to 6, creating two reset phases (phases 0 and 5) and four measurement phases (phases 1 through 4). If the junction voltage of the integrator ("V_S" in Figure 1) is precisely $0.5V_{REF}$ (and AGND = 0V), then the phase 1 and phase 2 integration times are equal, indicating no input errors. If the junction voltage is different from $0.5V_{REF}$ (due to op amp offset voltage, bias current, etc.) and/or AGND $\neq$ 0, an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts. The effect is to eliminate the error term from the final output-count N_0 on a first order basis. The errors remaining in N_0 are negligible.

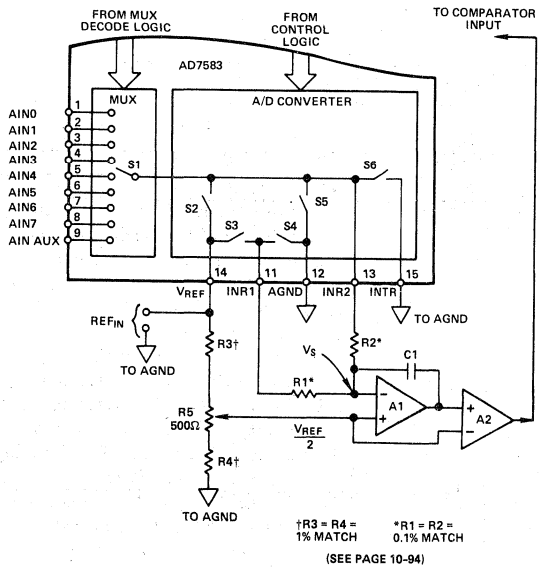


Figure 1. Functional Diagram of AD7583 Analog Circuitry

The time difference between the last comparator crossing and the termination of counter K3 represents the output count N_0. This count is divided by two and fed to an output totalizing counter which is preset in such a manner as to give a transfer function per table 1.

Phase	Input Voltage	Integration Time
0	$V_{REF} - V_S$	$\left(\frac{2V_{DD}}{V_{REF}} - 1\right) \cdot \left(\frac{R_1 R_2}{R_1 + R_2}\right) \cdot C_1$
1	$AGND - V_S$	$K_1 t$
2	$V_{REF} - V_S$	$(K_1 + n)t$
3	$\frac{AIN}{2} - V_S$	$(2K_1 - n)t$
4	$V_{REF} - V_S$	$(2K_1 + n - N_0)t$
5	$AGND - V_S$	$\left(\frac{2V_{DD}}{V_{REF}} - 1\right) \cdot \left(\frac{R_1 R_2}{R_1 + R_2}\right) \cdot C_1$

Where:
t = clock period
n = system error count (±)
K_1 = fixed count = 364
K_2 = fixed count = $4K_1$ = 1456
K_3 = fixed count = $4K_1$ = 1456
N_0 = internal count corresponding to the analog input voltage

Table 1. Integrator Equivalent Input Voltages and Integration Times

Analog Input Voltage	Internal Count Representation, N_0	Digital Output D_7 (MSB) . . . . . D_0 (LSB)
0 to $0.15V_{REF1}$	$N_0 = 0$	00000000
(0.15 to 0.85) V_{REF1}	$N_0 = \frac{255}{0.7}\left(\frac{AIN}{V_{REF1}} - 0.15\right)$	00000000 to 11111111
$0.85V_{REF1}$ to V_{REF1}	$N_0 = 255$	11111111

Note: V_{REF1} and the Analog Input must both be positive voltages ($0 \leq AIN \leq V_{REF}$).

Table 2. Code Relationship

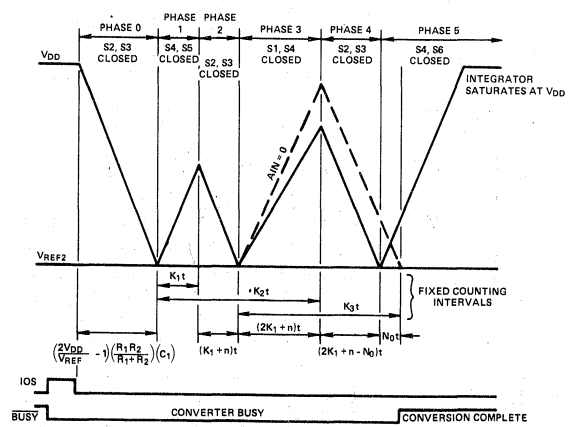


Figure 2. Quad Slope Timing Diagram

TIMING AND CONTROL OF THE AD7583

INTERFACE LOGIC

Figure 3 shows the functional diagram of the AD7583 Input/Output Logic. Digital information is communicated to and from the AD7583 via a bidirectional 8-bit data bus (D_{0-7}) under command of control inputs I/$\overline{O}$ (INPUT/$\overline{OUTPUT}$) and IOS (INPUT/OUTPUT STROBE).

With $\overline{RST}$ high, before the AD7583 will respond to commands placed on the I/$\overline{O}$ and IOS inputs, the device must be *enabled* by setting the Device Enable Latch. This is a one-time requirement which is accomplished by putting D_{0-7} equal to XXX11001, putting DCE (Decode Enable) HIGH, and strobing DCS (Decode Strobe). The AD7583 will remain *enabled* until a specific *disable* command is issued. Once the internal Device Enable Latch's "Q" output is HIGH, the internal READ and WRITE gates are enabled, control of these gates thus passes to the I/$\overline{O}$ and IOS inputs.

I/$\overline{O}$ controls data direction while IOS activates either the internal READ or WRITE signal. The 3-state output buffer is activated when READ is high. The General Buffer Latch and Channel Address Latch is loaded on the positive edge of the internal WRITE signal.

OPERATION

The AD7583 responds to 4 basic operation commands:

- ☐ Enable Command to bring the AD7583 out of its standby state.
- ☐ Disable Commands to place the AD7583 in standby.
- ☐ Channel Select and Start Command.
- ☐ Data READ Command.

1. ENABLE COMMAND (See Figure 4)
   Place code XXX11001 binary on D_{0-7}, put DCE HIGH, and strobe DCS. Timing requirements are shown in Figure 4.

2. DISABLE COMMAND (See Figure 4)
   There are 3 ways to place the AD7583 in a standby (disabled) mode:
   1. Put data bus D_{0-7} to a code *other than* XXX11001, put DCE HIGH, and strobe DCS.
      or
   2. Put DCE LOW and strobe DCS (D_{0-7} are "don't care")
      or
   3. Put $\overline{RST}$ momentarily LOW.

3. CHANNEL SELECT and START COMMAND (See Figure 5)
   Assuming the AD7583 has been *enabled* as per paragraph 1 above, the AD7583 will accept a Channel Select and Start Command. Put the channel address (per table 3) on Data Bus inputs D_{0-3}, put I/$\overline{O}$ HIGH (INPUT mode) and strobe IOS as per Figure 5.

   The positive edge of IOS strobes D_{0-3} into the Channel Address Latch, strobes data on D_{4-7} into the General Buffer Latch, resets all internal control logic, and causes $\overline{BUSY}$ (status output) to go LOW. In addition, within one clock period after IOS goes HIGH, phase 0 of the A/D conversion cycle begins (see Figure 2). Note: Attempting to execute a convert start when $\overline{BUSY}$ is LOW can cause an erroneous conversion.

4. DATA READ COMMAND (Figure 6)
   Prior to issuing a READ command, the AD7583 should have been enabled (as per paragraph 1) and $\overline{BUSY}$ must be HIGH.

   Failure to observe this precaution will cause erroneous data to be read.

   A DATA READ COMMAND is as follows: Put I/$\overline{O}$ LOW (OUTPUT mode) and put IOS HIGH. (The 3-state buffers are activated when IOS is HIGH). Timing is shown in Figure 6.

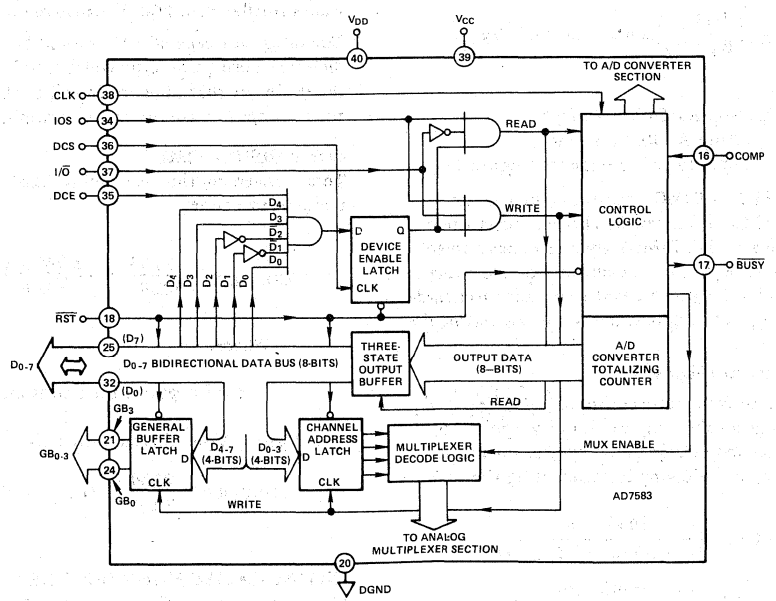


Figure 3. AD7583 Logic Section Functional Diagram

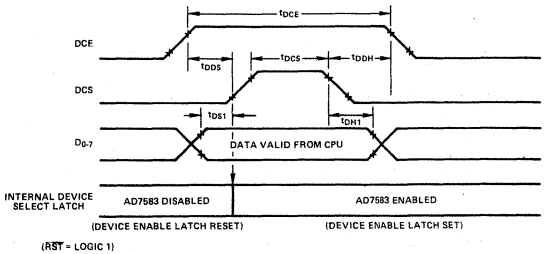


Figure 4. Setting the Device Enable Latch (Enabling the AD7583)

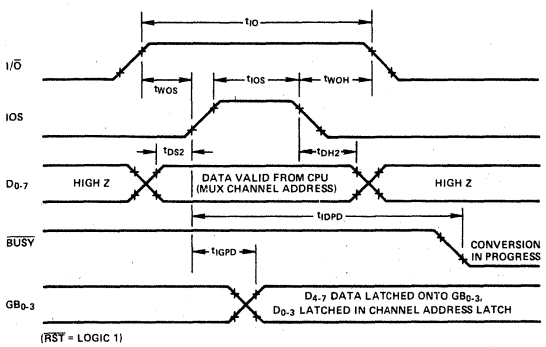


Figure 5. Writing Analog Channel Address and Convert Start

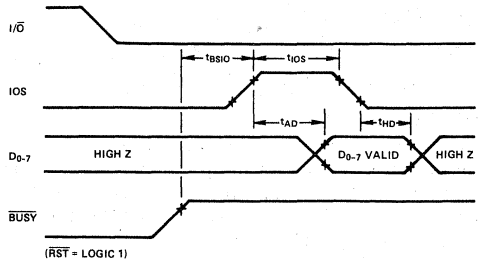


Figure 6. Data Read Timing

Channel Address				Selected Channel
D3	D2	D1	D0	
0	0	0	0	AIN0
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	X	X	X	AIN AUX

Note: 1 is Logic HIGH
0 is Logic LOW
X is "DON'T CARE"

Table 3. Channel Address Codes

ANALOG CIRCUIT SETUP

Selecting an Integrator Amp (A1 in Figure 7)

Integrator amplifier A1 (Figure 7) must be chosen such that its total equivalent input error voltage e_{eq} over the temperature range of interest is

$$e_{eq} = V_{OS} + I_{BIAS}\left(\frac{R_1R_2}{R_1+R_2}\right) \text{ is less than } 1.4\%\ V_{REF}$$

Where:

V_{OS} = Op Amp A1 Offset Voltage
I_{BIAS} = Op Amp A1 Bias Current
R1 and R2 are integrator resistors (Figure 7)

General purpose BIFET or BIMOS op amps (such as the AD544J, TL081 or CA3160) meet the above criteria when using a V_{REF} of at least +6V. BIMOS amplifiers have an advantage over BIFET types in that the output voltage swing can be virtually rail-to-rail. This precludes the necessity to guardband the integrator's peak output swing when calculating the integrator time constant.

Integrator Time Constant (Figure 7)

Proper selection of integrator time constant $\left(\frac{R_1R_2}{R_1+R_2}\right)\cdot C_1$ is important. Too large a value may cause noisy operation, while too small a value may cause the integrator output to saturate to V_{DD}. Use the following for calculating the time constant τ:

$$\tau = \left(\frac{R_1R_2}{R_1+R_2}\right)\cdot C_1 = \frac{364V_{REF}}{(f_{CLK})(V_{DD}-0.5V_{REF})}$$

if $V_{REF} = V_{DD}$, this simplifies to

$$\tau = \left(\frac{R_1R_2}{R_1+R_2}\right)\cdot C_1 = \frac{728}{f_{CLK}}$$

The integrator resistors R1 and R2 must match and track to within 0.1% over the temperature range of interest. Their absolute value; however, may be between 200kΩ to 2MΩ. Values larger than 2MΩ may cause noisy operation, whereas values smaller than 200kΩ cause relative accuracy degradation.

The integrator capacitor C1 should be a low leakage, low dielectric absorption type (teflon, polypropylene or polystyrene). Ensure that the outside foil of the capacitor is connected to the *output* of amplifier A1 to minimize noise injection.

CONVERSION TIME

Total conversion time is equal to 2184 clock periods plus the phase 0 reset time.

$$t_{CONVERT} = \frac{2184}{f_{CLK}} + \tau\left(\frac{2V_{DD}}{V_{REF}}\right) - 1$$

Where:

τ = Integrator time constant

If $V_{REF} = V_{DD}$, this simplifies to

$$t_{CONVERT} = \frac{2184}{f_{CLK}} + 2\tau$$

INITIAL CALIBRATION (FIGURE 7)

Short circuit integrating capacitor C1 (with the AD7583 powered but not converting) and adjust trimpot R5 for amplifier A1 output equal to $0.5V_{REF}$ to within 1.4%.

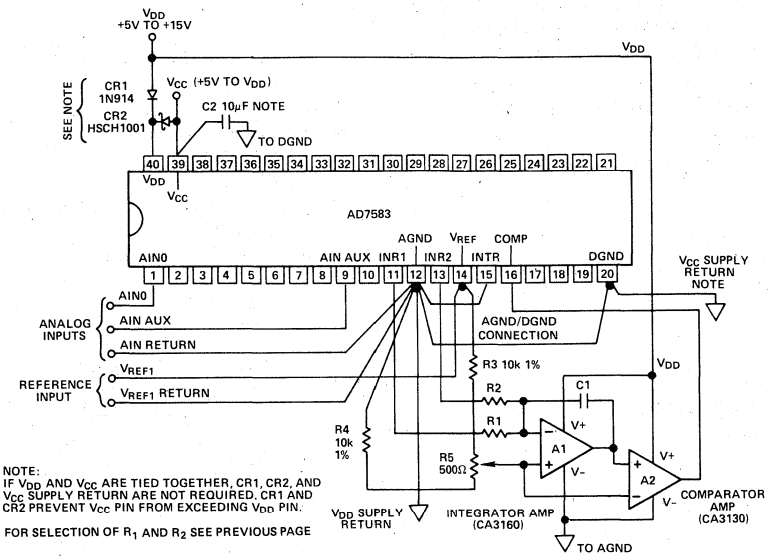


Figure 7. Analog Circuit Connections (Logic Input/Output Connections Omitted for Clarity)

APPLICATION HINTS

1. The AGND/DGND connection should be made at the AD7583, as shown in Figure 7. In systems where the connection must be remote, connect back-to-back diodes (1N914 or equivalent) between pin 12 and 20 of the AD7583.
2. Failure to observe correct grounding techniques can introduce conversion error and/or noise. System analog common must be located directly at pin 12 of the AD7583, as shown in Figure 7.
3. A major advantage of the AD7583 is the fact that the ADC does not respond to analog inputs less than $0.15V_{REF}$ or greater than $0.85V_{REF}$ (see table 1). A signal buffer amplifier used to drive the AIN inputs can therefore be powered from AGND and V_{DD} since its output will not have to swing to either rail. This is a particular advantage in single supply systems. For +5V single supply applications, we recommend BIMOS amplifiers (such as the CA3160) because of their rail-to-rail output voltage capability.
4. Do not apply V_{CC} before V_{DD}. Additionally, V_{CC} must never exceed V_{DD}. Failure to observe this precaution may cause device failure.
5. Attempting to write a convert start command when $\overline{BUSY}$ is LOW may result in an erroneous conversion.
6. To prevent loading errors due to the finite input impedance at any AIN input ($R_{IN} \approx R_1$), AIN should be driven from a source impedance lower then 0.1% R1.
7. For proper operation, ensure that the correct values for the integrator components have been selected and resistance tolerance and capacitor type are as recommended on the previous page.

CHANNEL EXPANSION

Figure 8 shows the AD7583 expanded to 24 channel operation using a single supply CD4067 16-channel analog multiplexer. The AD7583 General Buffer Outputs (GB_{0-3}) are used as the multiplexer address. The ON resistance of the CD4067 is buffered by amplifier A1.

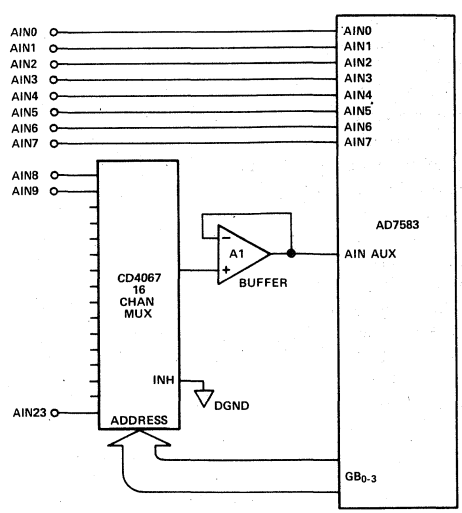


Figure 8. Channel Expansion Scheme

MICROPROCESSOR INTERFACE

Figure 9 shows how to interface the AD7583 to a MCS-85 microprocessor via an I/O port.

Port A of the 8155 is used as a bidirectional bus for sending channel address data to the AD7583, and for reading converted data into the MCS-85 system. Port B is used to control the strobes IOS, DCS, I/$\overline{O}$, and DCE.

The $\overline{BUSY}$ output is used as an interrupt, while $\overline{RST}$ is tied to the MCS-85 system reset.

A typical operating procedure is as follows:

Initilization

1. Power ON
2. $\overline{RST}$ (System Reset)
3. Put Port B as follows:
   DCS = LOW
   DCE = HIGH
   IOS = LOW
   I/$\overline{O}$ = Don't Care
4. Put Port A to Code XXX11001
5. Put Port B as follows:
   DCS = HIGH
   DCE = HIGH
   (AD7583 is now "enabled")
   IOS = LOW
   I/$\overline{O}$ = Don't Care
6. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW
   I/$\overline{O}$ = HIGH

Channel Address and Convert Start

1. Output desired Channel address to Port A (as per table 3).
2. Put Port B as follows:
   DCS = LOW
   DCE = HIGH
   IOS = LOW
   I/$\overline{O}$ = LOW
3. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = HIGH
   I/$\overline{O}$ = HIGH
   (Latches in channel address, $\overline{BUSY}$ goes LOW)
4. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW
   I/$\overline{O}$ = HIGH
5. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW
   I/$\overline{O}$ = LOW

Interrupt Service (Reading Converted Data)

1. Enter Interrupt when $\overline{BUSY}$ goes HIGH (ie, valid data is available)
2. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = HIGH (activates three-state buffers)
   I/$\overline{O}$ = LOW
3. READ Port A (converted data)
4. Put Port B as follows:
   DCS = LOW
   DCE = LOW
   IOS = LOW (deactivates three-state buffers)
   I/$\overline{O}$ = HIGH
5. Return to Main Program

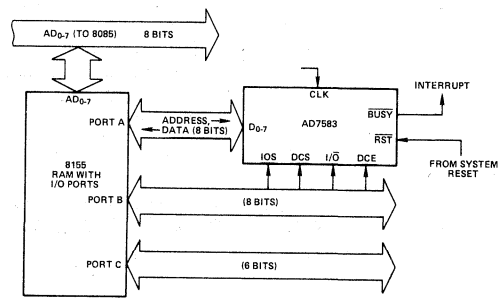
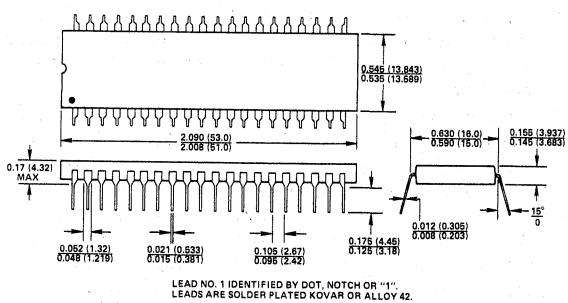


Figure 9. Interfacing the AD7583 to MCS-85 VIA an I/O PORT (Analog Circuitry Not Shown for Clarity)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

40 PIN DIP PLASTIC



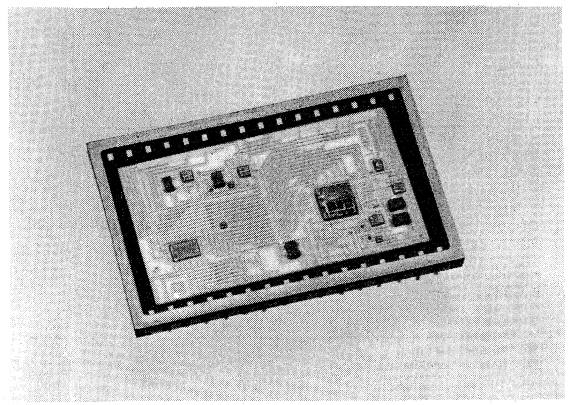
ANALOG DEVICES

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD ADC80

FEATURES

True 12-Bit Operation: Max Nonlinearity ±0.012%
Low Gain T.C.: ±30ppm/°C max
Low Power: 800mW
Fast Conversion Time: 25μs
Precision 6.3V Reference for External Application
Short-Cycle Capability
Serial or Parallel Data Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count—High Reliability
Industry Standard Pinout
"Z" Models for ±12V Supplies



PRODUCT DESCRIPTION

The AD ADC80 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at +25°C of ±0.012%, max gain T.C. of 30ppm/°C, typical power dissipation of 800mW and max conversion time of 25μs. Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of -25°C to +85°C.

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of ±2.5, ±5.0, ±10, 0 to +5 or 0 to +10 volts. The 6.3V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data may be read in both serial and parallel form.

The AD ADC80 is available in two performance grades, the AD ADC80-12 (0.012% of FSR max) and the AD ADC80-10 (0.048% of FSR max). Both grades are specified for use over the -25°C to +85°C temperature range and both are available in a 32-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried zener reference is laser trimmed to 6.3 volts. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Every AD ADC80 is subject to stabilization bakes and receives a powered burn-in at +125°C.
6. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
7. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
8. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

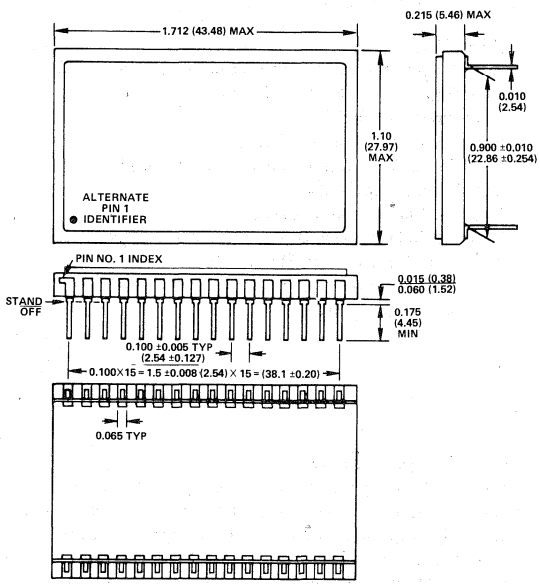
MODEL	AD ADC80-12	AD ADC80-10
RESOLUTION	12 Bits	10 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	
Unipolar	0V to +5V, 0V to +10V	
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ	*
0V to +10V, ±5V	5kΩ	*
±10V	10kΩ	*
DIGITAL INPUTS[1]		
Convert Command	Positive Pulse 100ns Wide (min) ("0" to "1" Initiates Conversion)	
Logic Loading	1TTL Load	
External Clock	1TTL Load	
TRANSFER CHARACTERISTICS ERROR		
Gain Error[2]	±0.1% of FSR[3]	*
Offset Error[2]		
Unipolar	±0.05% of FSR	*
Bipolar	±0.1% of FSR	*
Linearity Error (max)[4]	±0.012% of FSR	±0.048% of FSR
Inherent Quantization Error	±1/2LSB	*
Differential Linearity Error	±1/2LSB	*
No Missing Codes Temperature Range	-25°C to +85°C	*
Power Supply Sensitivity		
±15V	±0.0030% of FSR/% V_S	*
+5V	±0.0015% of FSR/% V_S	*
DRIFT		
Specification Temperature Range	-25°C to +85°C	*
Gain (max)	±30ppm/°C	*
Offset		
Unipolar	±3ppm of FSR/°C	*
Bipolar (max)	±15ppm of FSR/°C	*
Linearity (max)	±3ppm of FSR/°C	*
Monotonicity	GUARANTEED	*
CONVERSION SPEED[5]	22μs typ, 25μs max	21μs max
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[6]		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	2TTL Loads	
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Status Output Drive	2TTL Loads	
Internal Clock		
Clock Output Drive	2TTL Loads	
Frequency[7]	575kHz	
INTERNAL REFERENCE VOLTAGE	6.3V	
Max. External Current (with no degradation of specifications)	1.5mA	
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	
POWER REQUIREMENTS		
Rated Voltages	±15V, +5V	
Range for Rated Accuracy	4.75V to 5.25V and ±14.0V to ±16.0V	
Z Models[8]	4.75V to 5.25V and ±11.4V to ±16.0V	
Supply Drain +15V	+10mA	
-15V	-20mA	
+5V	+70mA	
TEMPERATURE RANGE		
Specification	-25°C to +85°C	
Operating (Derated Specs)	-55°C to +100°C	
Storage	-55°C to +125°C	

NOTES:
[1] DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital inputs, Logic "0" = +0.4V max and "1" = 2.4V min digital outputs.
[2] Adjustable to zero with external trimpots.
[3] FSR means Full Scale Range- for example, unit connected for ±10V range has 20V FSR.
[4] Error shown is the same as ±1/2LSB max for resolution of A/D converter.
[5] Conversion time with internal clock.
[6] See Table 1. CSB – Complementary Straight Binary
COB – Complementary Offset Binary
CTC – Complementary Two's Complement
[7] For conversion speeds specified.
[8] For Z models order AD ADC80Z-12 or AD ADC80Z-10.
*Specifications same as AD ADC80-12.

Specifications subject to change without notice.

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



NOTES
1. GOLD PLATING 60 MICROINCHES MINIMUM THICKNESS OVER 100 MICROINCHES NOMINAL THICKNESS OF NICKEL.
2. COLOR: OPAQUE-STANDARD ACCEPTABLE. BLACK, DARK BROWN, DARK VIOLET.
3. TOP SURFACE MATERIAL MAY BE EITHER CERAMIC OR BARE METAL. REMAINDER OF PACKAGE IS CERAMIC WITH METAL LEADS.

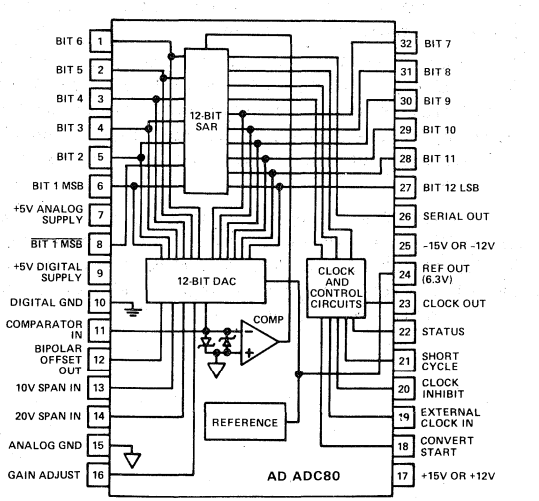
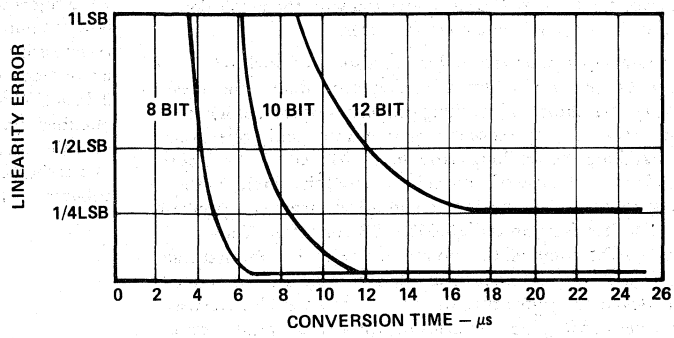


Figure 1. AD ADC80 Functional Diagram and Pinout

Figure 2. Linearity Error vs. Conversion Time (Normalized)



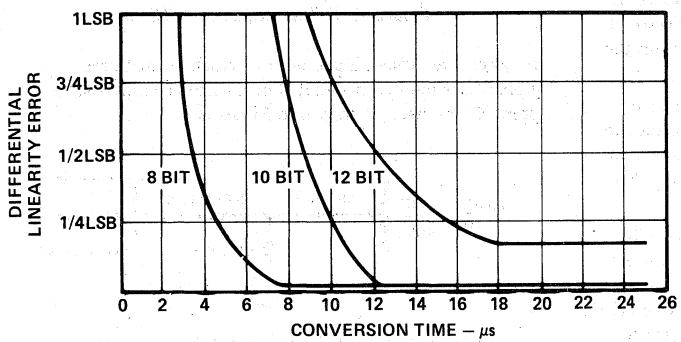
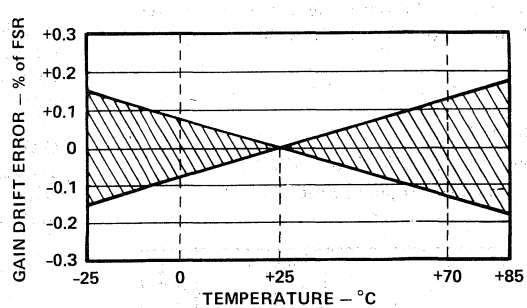


Figure 3. Differential Linearity Error vs. Conversion Time (Normalized)

Figure 4. Maximum Gain Drift Error – % of FSR vs. Temperature



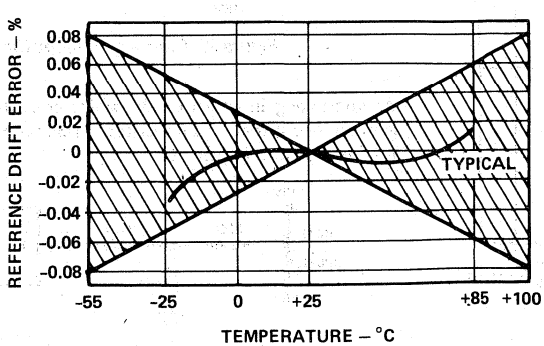


Figure 5. Reference Drift – % Error vs. Temperature

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the AD ADC80 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 7 and 9. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 6).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC80 is specified as having no missing codes over the entire temperature range from -25°C to +85°C.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

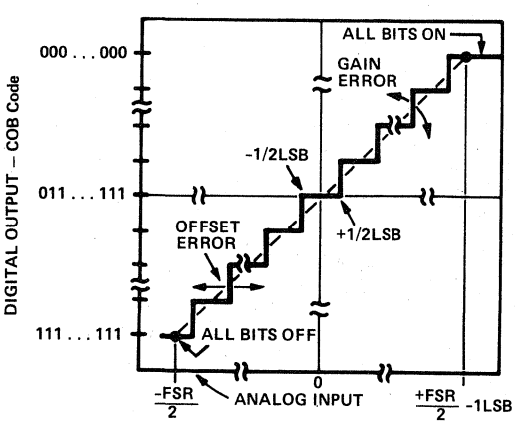


Figure 6. Transfer Characteristic for an Ideal Bipolar A/D

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 11 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

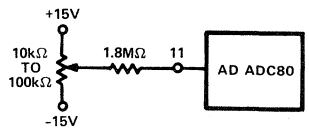


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 8.

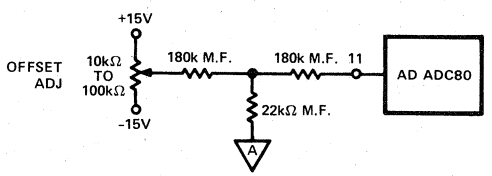


Figure 8. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 11 should be located close to this pin to keep the pin 11 connection runs short (Comparator Input pin 11 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 16 as shown in Figure 9.

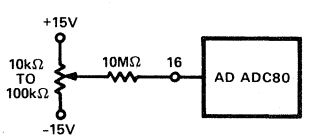


Figure 9. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 10.

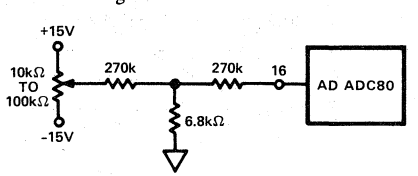


Figure 10. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

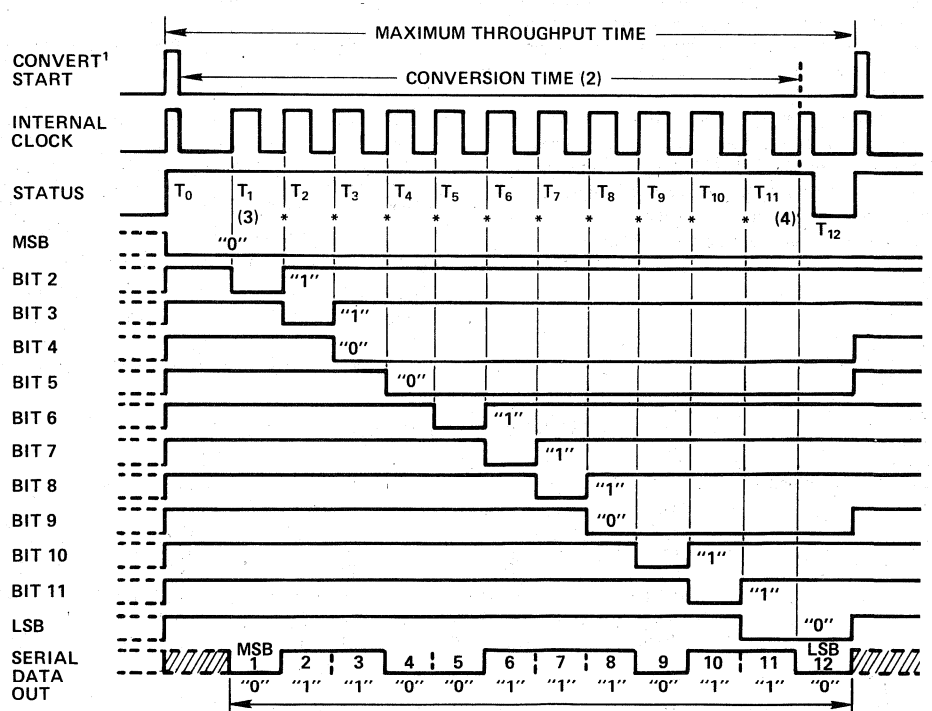
On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 11. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 11).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND.
2. 25μs FOR 12 BITS AND 21μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 11. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 6) or its logical inverse $\overline{\text{BIT 1}}$ (pin 8) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 11. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 11. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 21, permits the timing cycle shown in Figure 11 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 21 is connected to +5V (pin 9). When 10-bit resolution is desired, pin 21 is connected to Bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 11). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table 1.

Connect Short Cycle Pin 21 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t_{12} +40ns
28	10	0.100	21	t_{10} +40ns
30	8	0.390	17	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 12 for circuit details.

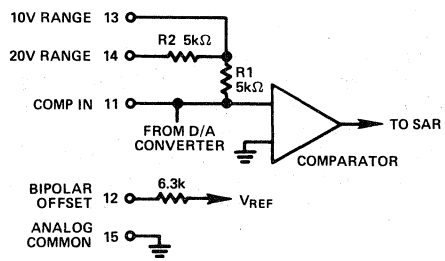


Figure 12. AD ADC80 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0V to +5V	CSB	15	Pin 11	13
0V to +10V	CSB	15	Open	13

Table II. AD ADC80 Input Scaling Connections

Binary (BIN) Output / Analog Input Voltage Range	Defined As:	INPUT VOLTAGE RANGE AND LSB VALUES ±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available on pin 8.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definitions

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

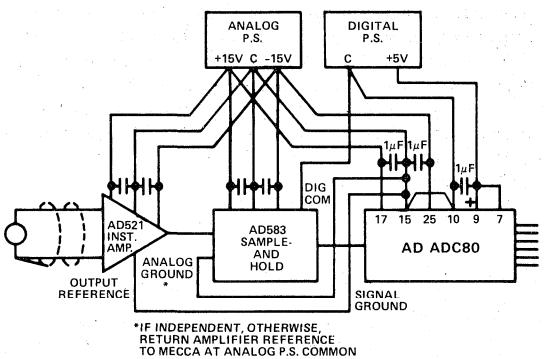


Figure 13. Basic Grounding Practice

CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 14–17.

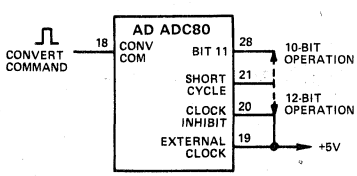


Figure 14. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

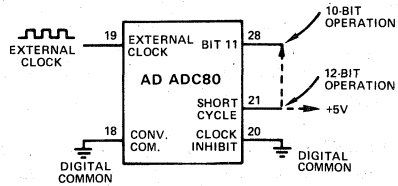


Figure 15. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock runs Continuously.

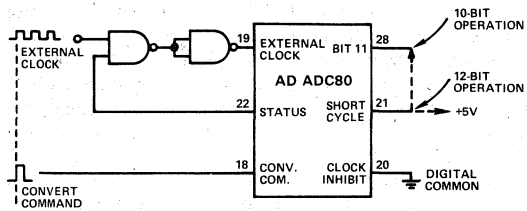


Figure 16. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command must be Synchronized with Clock.

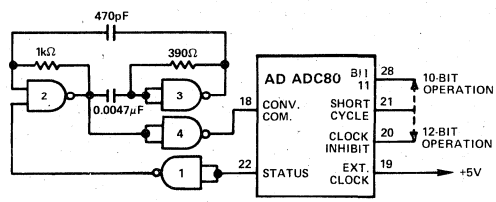


Figure 17. Continuous Conversion with Internal Clock. Conversion is Initiated by the 14th Clock Pulse. Clock Runs Continuously. The Oscillator Formed by Gates 2 and 3 Insures that the Conversion Process will Start When Logic Power is First Turned On.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 18 and 19, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and –FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR –2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

–10V to +10V Range: Set analog input to –9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and –10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, –2.5V to +2.5V and –5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and –10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

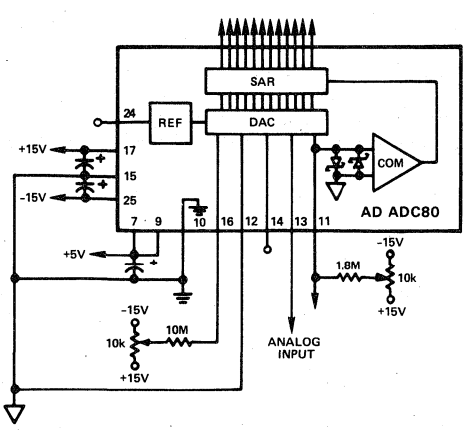


Figure 18. Analog and Power Connections for Unipolar 0–10V Input Range

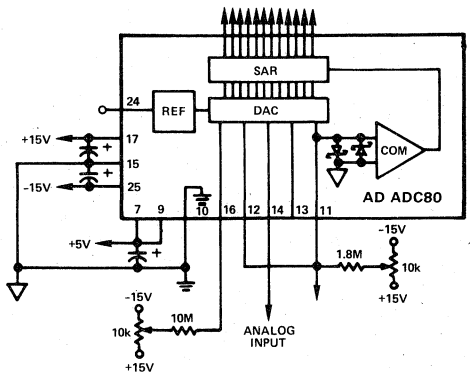


Figure 19. Analog and Power Connections for Bipolar ±10V Input Range

MULTICHANNEL CONVERSION

In multichannel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system.

The data acquisition system shown in Figure 20 is a low cost solution to digitizing data from many analog channels. For most efficient use of time, the multiplexer is acquiring the next channel to be converted while the sample-hold is holding the previous output level for conversion. When conversion is complete, the status line from the converter causes the S/H to return to the sample mode and acquire the new data. After the acquisition time is completed, the sample hold can be switched to hold. A conversion can then begin and the multiplexer can be switched to the next channel.

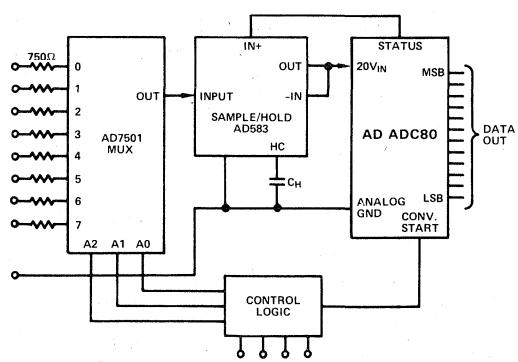


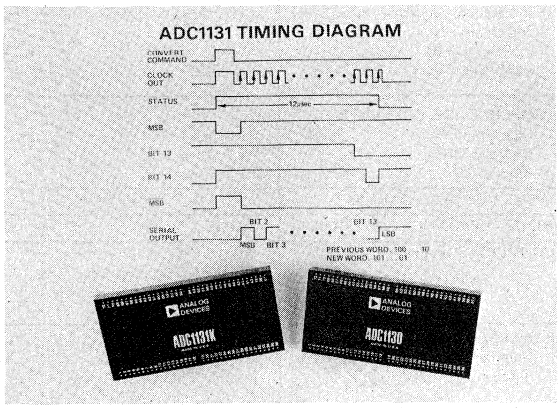
Figure 20. Data Acquisition System

14-Bit High Speed Analog to Digital Converters

ADC1130, ADC1131

FEATURES
- **14-BIT Resolution and Accuracy**
- **Fast 12μs Conversion Time (ADC1131J/K)**
- **Low 10ppm/°C Maximum Gain TC**
- **User Choice of Input Range**
- **No Missing Codes**

APPLICATIONS
- **Wide Band Data Digitizing**
- **Multi-Channel Computer Interface**
- **High Accuracy Data Acquisition**
- **X-Ray Tomography**
- **Nuclear Accelerator Instrumentation**



GENERAL DESCRIPTION

The ADC1130 and ADC1131 are high speed analog-to-digital converters packaged in a small 2" x 4" x 0.4" (51 x 102 x 10mm) module, which perform complete 14-bit conversions in 25μs and 12μs respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 14 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.

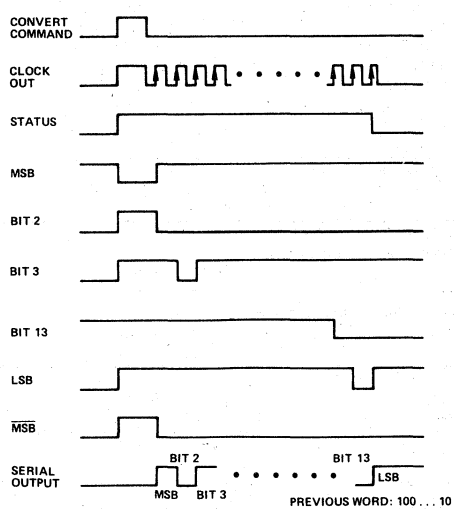


Figure 1. Timing Diagram

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	HIGH SPEED 12μs ADC1131 J	K	MEDIUM SPEED 25μs ADC1130
RESOLUTION, BITS	14	14	14
CONVERSION TIME (max)	12μs	12μs	25μs
ACCURACY			
Integral Nonlinearity Error (LSB)	±1/2 (max)	*	*
Differential Nonlinearity			
Error (LSB)	±1/2 (1 max)	±1/2 (max)	±1/2 (1 max)
Missing Codes	No missing codes	*	*
TEMPERATURE COEFFICIENTS			
Gain ppm/°C	±12 (max)	±7 (+10 max)	±12 max
Unipolar Offset	±0.7 (±3 max)	*	*
Bipolar Offset	±3 (±7 max)	*	*
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V	*	*
INPUT IMPEDANCE (10V RANGE)	2500Ω	*	*
CONVERT COMMAND	Positive Pulse, 200ns min, 400ns max Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible	*	*
PARALLEL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary, Two's Complement	*	*
SERIAL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
STATUS OUTPUT	"1" During Conversion. Complement also available TTL/DTL Compatible.	*	*
LOGIC FANOUTS AND LOADINGS			
Convert Command Input	1TTL Unit Load	*	*
Clock Input	3TTL Unit Loads	*	*
Short Cycle Input	1TTL Unit Load	*	*
Parallel Data Outputs	3TTL Unit Loads/Bit	*	*
Serial Data Output	8TTL Unit Loads	*	*
STATUS Output	2TTL Unit Loads	*	*
$\overline{\text{STATUS}}$ Output	12TTL Unit Loads	*	*
Clock Output	4TTL Unit Loads	*	*
POWER REQUIREMENTS	+15V ±5% @ 40mA	*	*
	−15V ±5% @ 60mA	*	*
	+5V ±5% @ 250mA	*	*
POWER SUPPLY SENSITIVITY			
To ±15V Tracking Supplies			
Gain	$\pm 4.5 ppm/\%\Delta V_S$	*	*
Zero	$\pm 4.5 ppm/\%\Delta V_S$	*	*
To ±15V Non-Tracking Supplies			
Gain	$\pm 10 ppm/\%\Delta V_S$	*	*
Zero	$\pm 7 ppm/\%\Delta V_S$	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	−55°C to +85°C	*	*

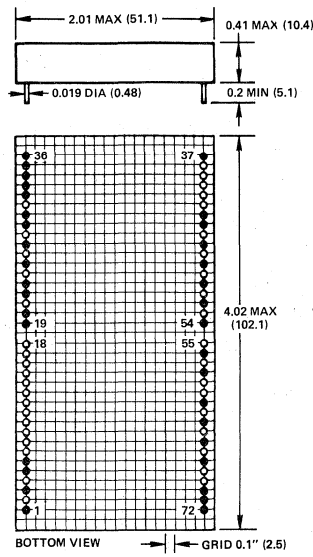
*Same Specifications as ADC1131J.

NOTES:
[1] Offset (zero) and gain errors are adjustable to zero by means of external potentiometers. See Figure 5 for proper connection.
[2] Recommended power supply: Analog Devices model 902 and model 906.

Specifications subject to change without notice.

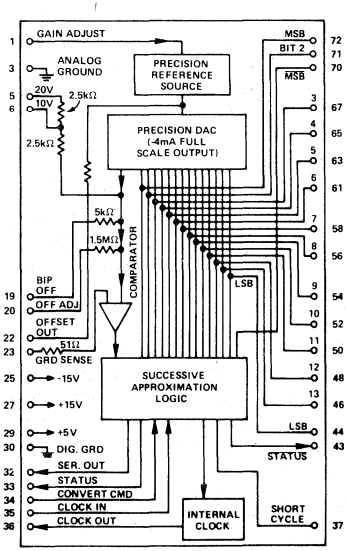
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 3.5 ounces (99.3 grams).

BLOCK DIAGRAM AND PIN DESIGNATIONS



ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1130 and ADC1131 are shown in block diagram form.

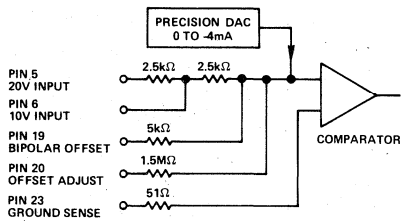


Figure 2. Input Circuit Block Diagram

When the converters are connected as a unipolar device, Pin 19 is left open circuit and, thus, no offset current is applied to the comparator input. The 0 to +10V input signal applied to Pin 6 (or the 0 to +20V input signal applied to Pin 5) develops a 0 to +4mA current which is compared to the 0 to -4mA output of the D/A converter. A voltage between +15V and -15V can be applied to Pin 20 from the wiper of a 100kΩ potentiometer to adjust the zero point by ±40LSB. To reduce the range of this trim padding resistors should be used.

With the offset output, Pin 22, connected to Pin 19, a +2mA offset current is applied to the comparator input. The ADC1130 and ADC1131 will then accept bipolar inputs of ±5V at Pin 6, or ±10V at Pin 5 and compare the 0 to +4mA sum of the offset and input signal currents to the 0 to -4mA D/A converter output. The offset adjustment potentiometer is once again used as described in the preceding paragraph.

Signal ground sense, Pin 23, should normally be jumpered to analog ground, Pin 3. In the event that an offset voltage is developed in the ground wiring, it may be possible to eliminate its effect by connecting Pin 23 directly to the signal or analog ground of the device feeding the analog input signal to the ADC. In any case, Pin 23 must not be left open.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer.

PARALLEL DATA OUTPUT

These converters produce natural Binary Coded outputs when configured as a unipolar device. As a bipolar device, they can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by Pin 72 (MSB output) for Binary and Offset Binary codes, or by Pin 70 ($\overline{\text{MSB}}$ output) for the Two's Complement code. Tables I and II illustrate the relationship between analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT
0 to +10V Range	0 to +20V Range	Binary Code
+9.9994V	+19.9988V	11111111111111
+5.0000V	+10.0000V	10000000000000
+1.2500V	+2.5000V	00100000000000
+0.0006V	+0.0012V	00000000000001
+0.0000V	+0.0000V	00000000000000

Table 1. Nominal Unipolar Input-Output Relationships

±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.9994V	+9.9988V	11111111111111	01111111111111
+2.5000V	+5.0000V	11000000000000	01000000000000
+0.0006V	+0.0012V	10000000000001	00000000000001
+0.0000V	+0.0000V	10000000000000	00000000000000
-5.0000V	-10.0000V	00000000000000	10000000000000

Table 2. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUT

The serial data output, available on Pin 32, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the converter.

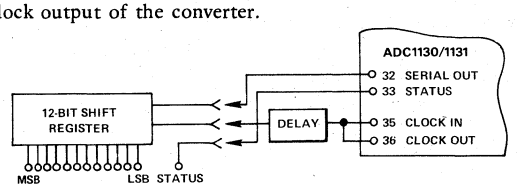


Figure 3. Serial Data Transmission

The timing diagram presented in Figure 4 shows that the converter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 20ns clock output to serial output delay.

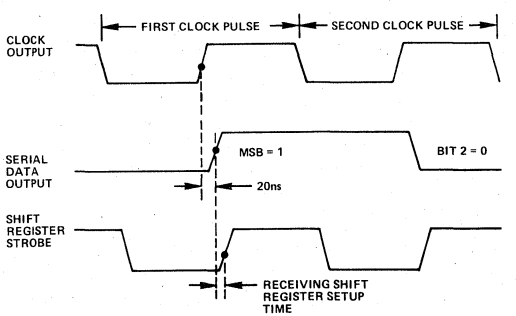


Figure 4. Serial Data Timing Diagram

The 50ns span between the time that the last serial output bit is available and the time that the STATUS output returns to zero insures that the data in the shift register will be valid on the "1" to "0" transition of the STATUS signal.

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 5. Note that a jumper

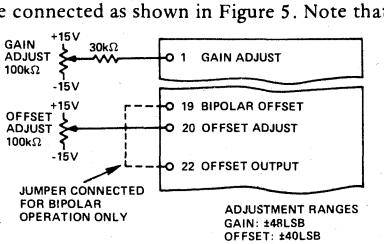


Figure 5. Adjustment Connections

is connected between Pin 19 and Pin 22 for bipolar operation; these pins *must* be left open for unipolar operation.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the output of the converter to be on the verge of switching from one digital value to the adjacent digital value, the unit can be calibrated so that it does change values at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D and D/A converters.

OFFSET CALIBRATION

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V; for 0 to +20V units set it to +0.0006V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00 . . . . 0 to 00 . . . . 1.

For the ±5V bipolar range set the input voltage precisely to -4.9997V; for ±10V units set it to -9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . 0 to 00 . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely to +19.9982V for 0 to +20V units, +9.9991V for 0 to +10V units, +4.9991V for ±5V units, or +9.9982V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . 0 to 11 . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.

POWER SUPPLY AND GROUNDING CONNECTIONS

These converters do not have an internal connection between analog power ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. One suggested approach is shown in Figure 6.

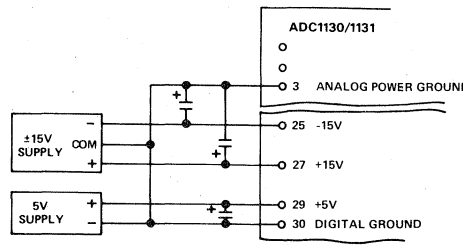


Figure 6. Power Supply and Grounding Connections

The ±15V and +5V power supplies must be externally bypassed with 15μF (+35V tantalum) capacitors. These capacitors should be connected between Pin 27 and Pin 3, between Pin 25 and Pin 3, and between Pin 29 and Pin 30. Capacitor connections should be made as close to the module pins as possible.

CLOCK CONNECTIONS

When the converters are used with their own internal clock, Pin 36 is simply jumpered to Pin 35. When the internal clock is not used, Pin 36 is grounded and an external clock capable of driving three TTL loads is connected to Pin 35. The convert command should be synchronized with the external clock.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command may be initiated any time after the "1" to "0" transition of the STATUS output. The STATUS output may not, however, be connected directly to the CONVERT COMMAND input for the purpose of automatically generating convert command pulses.

SHORT CYCLE CONNECTIONS

When the converters are operated as a 14-bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 14 bits, Pin 37 is connected to the N + 1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is T_C x N/14 where T_C is the conversion time of the particular model when operated at 14-bit resolution.

ANALOG DEVICES

Ultra-Fast Hybrid Analog to Digital Converters

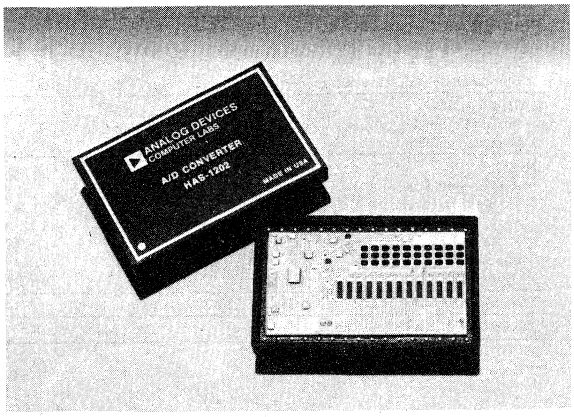
HAS-0802/1002/1202

FEATURES

- Conversion Times as Low as 1.2μs
- Resolution: 8, 10 and 12 Bits
- Exceptional Accuracy, 0.012% of F.S.
- Low Power
- Contained in Glass or Metal 32-Pin DIP
- Adjustment-Free Operation

APPLICATIONS

- Waveform Analysis
- Fast Fourier Transforms
- Radar



GENERAL DESCRIPTION

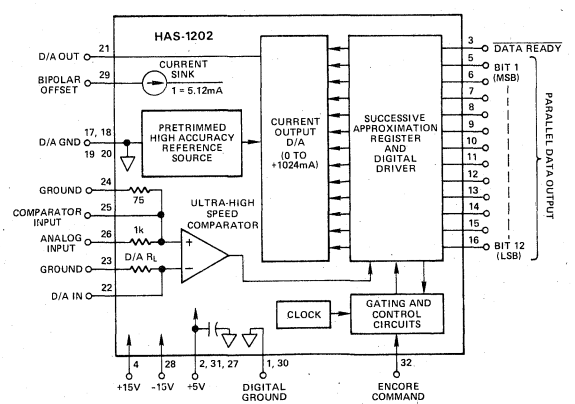
With a typical conversion time of only 2.2μs for complete 12-bit conversion, the Analog Devices' HAS series hybrid A/D converters are the fastest, smallest, most complete successive-approximation A/D's available. Housed in 32-pin DIP packages, these converters feature laser trimming for accuracy and linearity surpassing the best modular competitive A/D's. This series offers a unique combination of flexibility and simplicity which allows them to be used as stand-alone A/D converters requiring no additional external potentiometers and needing only an analog input signal and encode command for operation.

The HAS-1202 A/D features an accuracy of 0.012% and when combined with an HTC-0300 track-and-hold, forms an A/D conversion system capable of up to 350kHz sampling rates.

The HAS series A/D's are ideally suited for applications requiring excellent performance characteristics, small size, low power consumption and adjustment-free operation. Some of these applications include radar, PCM, data-acquisition, and digital-signal-processing systems where FFT's and other digital processing techniques are to be performed on analog input data.

For the ultra-high reliability requirements of military and aerospace applications these A/D's are optionally available with hermetically sealed metal cases and with MIL-STD-883 processing.

Extreme care in circuit layout should be exercised when using these hybrids in order to obtain rated performance. In particular, input and output runs should be as short as possible, a ground plane should be used to tie all ground pins together, and power supplies should be bypassed as close to the hybrid circuit power supply pins as possible. Do not allow input or other analog signal lines to be in close proximity to or cross over any digital output line.



NOTES: 1. FUNCTIONAL CONFIGURATION SHOWN IS FOR THE HAS-1202. FOR THE HAS-1002 PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY. FOR HAS-0802 PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.
2. FOR BIPOLAR OPERATION, CONNECT PINS 21, 22 AND 29. FOR UNIPOLAR OPERATION, CONNECT PIN 21 TO PIN 22 AND GROUND PIN 29.

Block Diagram — HAS Series

SPECIFICATIONS (typical @ +25°C with nominal voltages unless otherwise noted)

MODEL	UNITS	HAS-0802	HAS-1002	HAS-1202
RESOLUTION	BITS	8	10	12
LSB Weight	% Full Scale	0.4	0.1	0.025
	mV	40	10	2.5
RELATIVE ACCURACY (INCLUDING LINEARITY)	% Full Scale	0.05	0.025	0.012
Quantization Error	LSB	±1/2	*	*
LINEARITY VS. TEMPERATURE	ppm/°C	3	*	*
		(No Missing Codes over Temperature Range)		
INPUT OFFSET VOLTAGE				
Initial (Trimmable to Zero)	mV	10	*	*
Zero Offset vs. Temperature	µV/°C	15	*	*
Bipolar Offset vs. Temperature	µV/°C	100	*	*
GAIN ERROR				
Initial (Trimmable to Zero)	% Full Scale	0.1	*	*
Gain vs. Temperature	ppm/°C	30	*	*
INPUT				
Ranges (Full Scale)				
"Built-In" Standard Unipolar	V ±0.1%	+10.24	*	*
Bipolar	V ±0.05%	±5.12	*	*
Resistor Programmable (See Figure 3)	V, 0 to:	+5, +7.5, +15, +20, ±2.5, ±3.75, ±7.5, ±10		
Impedance	Ω min	1000	*	*
Overvoltage	V	Two Times Full Scale + or −		
CONVERSION TIME (COMPLETE CYCLE TIME)	µs max (typ)	1.5 (1.2)	1.7 (1.4)	2.8 (2.2)
CONVERSION RATE	kHz max	667	588	357
ENCODE COMMAND – TTL LOGIC INPUT				
Logic Levels (Positive Logic)	V	"0" = 0 to +0.4, "1" = +2 to +5		
Function[1]		Logic "1" Resets Converter Logic "0" Starts Conversion		
Loading		1 Standard TTL Load: "0" = −1.6mA, max "1" = 40µA, max		
Pulse Width	ns min	100	*	*
Repetition Rate		0 to Maximum Conversion Rate		
LOGIC OUTPUTS				
Data Ready ($\overline{DR}$)				
Function		Signals conversion is complete when low. After $\overline{DR}$ goes low, data is valid. A new conversion may be initiated at this time. $\overline{DR}$ may be used to strobe data into external register if adequate register setup time is allowed.		
Timing		See Figure 1		
Loading		5 Standard TTL Loads, max		
Parallel Data				
Format		8-, 10-, or 12-bits parallel data. Valid from time $\overline{DR}$ output goes low until 20ns after receipt of next encode command.		
Logic Levels		TTL Compatible: "0" = 0V to +0.4V "1" = +2.4V to +5V		
Loading		Will drive up to 5 Standard TTL Loads or 2 TTL "S" or "H" Loads.		
Coding[2]		Offset Binary (BIN) for Unipolar Inputs: +10.24V = 1111....1 0V = 0000....0 Offset Binary (OBN) for Bipolar Inputs: +5.12V = 1111....1 0V = 0111....1 −5.12V = 0000....0		
POWER REQUIREMENTS				
+14.5V to +15.5V (+18V Absolute Max)	mA	40	*	*
−14.5V to −15.5V (−18V Absolute Max)	mA	15	*	*
+4.75V to +5.25V (+7V Absolute Max)	mA	200	*	*
TEMPERATURE RANGE				
Operating (Case)	°C	0 to +70	*	*
Storage	°C	−55 to +125	*	*

NOTES:
[1] After converter is reset, all other logic signals, including clock, are internally generated.
[2] When HAS series A/D's are used with HTC-0300 track/hold, output coding is complementary binary (CBN) for unipolar inputs and complementary offset binary (COB) for bipolar inputs (see Table 1).

*Specifications same as model HAS-0802.
Specifications subject to change without notice.

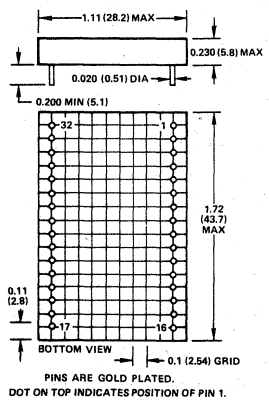
*Table 1. Output Coding**

SCALE	INPUT OF HTC-0300	INPUT OF HAS-1202	DIGITAL OUTPUT
UNIPOLAR OPERATION			
FS-1LSB	-10.2375V	+10.2375V	111111111111
3/4 FS	- 7.6800V	+ 7.6800V	110000000000
1/2 FS	- 5.1200V	+ 5.1200V	100000000000
1/4 FS	- 2.5600V	+ 2.5600V	010000000000
+1LSB	- 0.0025V	+ 0.0025V	000000000001
0	0.0000V	0.0000V	000000000000
BIPOLAR OPERATION			
+FS-1LSB	- 5.1175V	+ 5.1175V	111111111111
0	0.0000V	0.0000V	100000000000
-FS+1LSB	+ 5.1175V	- 5.1175V	000000000001
-FS	+ 5.1200V	- 5.1200V	000000000000

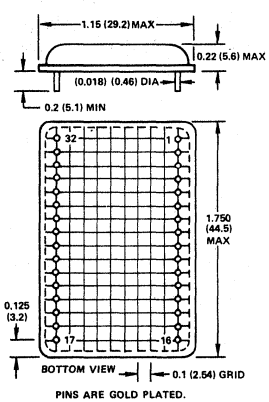
*Coding and input levels shown are for HAS-1202. For 8- and 10-bit A/D's the input levels are less by the values of the LSB weight for each type, and the digital output will show only 8 or 10 bits, respectively.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



GLASS PACKAGE



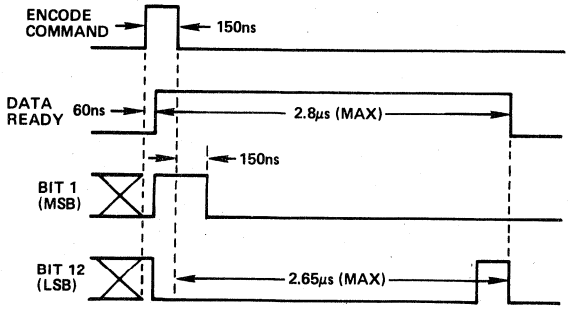
METAL PACKAGE (M)
(OPTIONAL)

PIN DESIGNATIONS

HAS-1202*

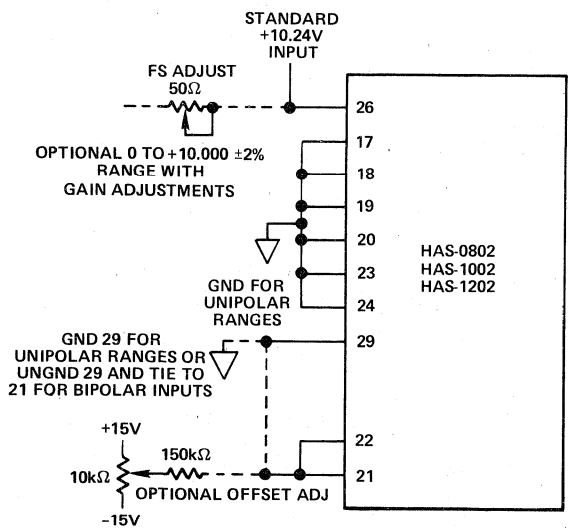
PIN	FUNCTION
1, 30	DIGITAL GROUND
2, 27, 31	+5V
3	DATA READY
4	+15V
5	BIT 1 OUTPUT (MSB)
6	BIT 2 OUTPUT
7	BIT 3 OUTPUT
8	BIT 4 OUTPUT
9	BIT 5 OUTPUT
10	BIT 6 OUTPUT
11	BIT 7 OUTPUT
12	BIT 8 OUTPUT
13	BIT 9 OUTPUT
14	BIT 10 OUTPUT
15	BIT 11 OUTPUT
16	BIT 12 OUTPUT (LSB)
17, 18, 19	ANALOG GROUND
20, 23, 24	ANALOG GROUND
21	D/A OUT
22	D/A IN
25	COMP INPUT
26	ANALOG INPUT
28	-15V
29	BIPOLAR OFFSET
32	ENCODE COMMAND

***HAS-1002, PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY. HAS-0802, PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.**



TIMING SHOWN FOR HAS-1202. TIMING IS SIMILAR FOR HAS-1002 AND HAS-0802 EXCEPT LSB IS BIT 10 AND 8, RESPECTIVELY, AND TOTAL TYPICAL CONVERSION TIME IS 1.4μs AND 1.2μs, RESPECTIVELY.

Figure 1. Timing Diagram (Typical)



NOTES:
1. THIS CIRCUIT SHOWN FOR UNIPOLAR (0 TO +10.24V) INPUT. 0V INPUT = 000000000000; +10.24 INPUT = 111111111111.
2. FOR BIPOLAR (±5.12V) INPUT, UNGROUND PIN 29 AND CONNECT PIN 29 TO PIN 21.
3. FOR EXTRA-PRECISE GAIN (FULL-SCALE) ADJUSTMENT, CONNECT A 50Ω VARIABLE RESISTANCE IN SERIES WITH PIN 20 OF HAS-1202. THIS WILL RESULT IN 0 TO +10.000V INPUT WITH ADJUSTMENT RANGE OF ±2% OF FULL SCALE.
4. FOR EXTRA-PRECISE ZERO OFFSET ADJUSTMENT, CONNECT 150k RESISTOR FROM PIN 21 TO THE TAP OF A 10k POTENTIOMETER. END TERMINATIONS OF POTENTIOMETER CONNECT TO +15V AND -15V. THIS ZERO OFFSET ADJUSTMENT WILL HAVE A RANGE OF APPROXIMATELY ±100mV.

Figure 2. Input Connections For Standard Input Ranges

INPUT RANGE	R1	R2	Z_{IN}	ABSOLUTE MAXIMUM SIGNAL
0 to +5V, ±2.5V	SHORT	1000	500	±10V
0 to +7.5V, ±3.75V	SHORT	3000	750	±15V
0 to +15V, ±7.5V	500	OPEN	1500	±30V
0 to +20V, ±10V	1000	OPEN	2000	±40V

Input Connections For Optional Input Ranges

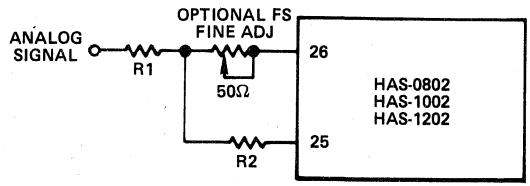


Figure 3. Full Scale Trim

APPLICATION CIRCUIT

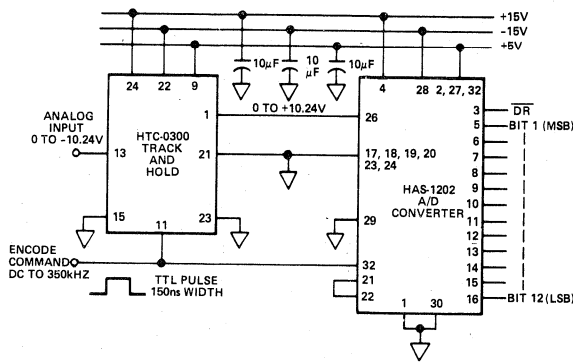


Figure 4. DC to 350kHz, 12-Bit, A/D Conversion System

ORDERING INFORMATION

Order model number HAS-0802, HAS-1002, or HAS-1202 for 8-, 10-, or 12-bit operation, respectively. Mating connector for the HAS series A/D's is model number HSA-2. Metal cased versions of this A/D with extended operating temperature range, and MIL-STD processing are also available. Consult the factory or nearest Analog Devices' sales office for further information.

ANALOG DEVICES

Ultra High Speed 8- and 10-Bit A/D Converters

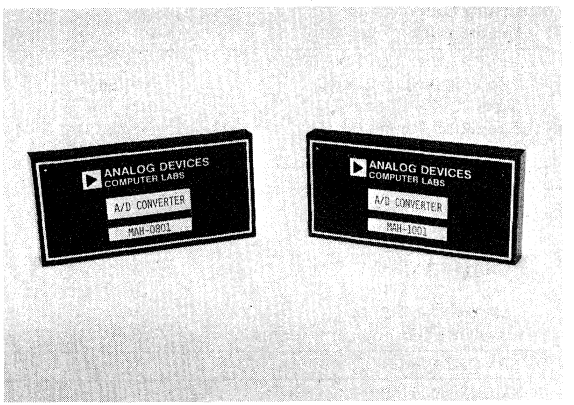
MAH-0801, -1001

FEATURES

High Speed at Low Cost
8-Bits @ 750ns max
10-Bits @ 1μs max
Monotonic Over Temperature
Differential Nonlinearity ±1/4LSB typ
Parallel and Serial Outputs
Pin and Function Compatible with 4130, 4131

APPLICATIONS

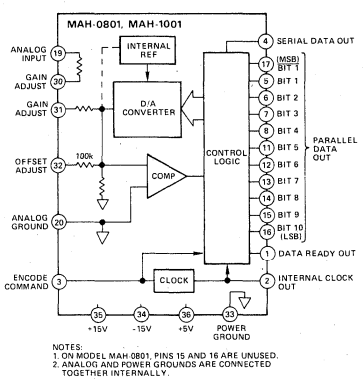
High Speed Data Acquisition
Real Time Waveform Analysis
Radar Signal Processing
Analytical Instruments



GENERAL DESCRIPTION

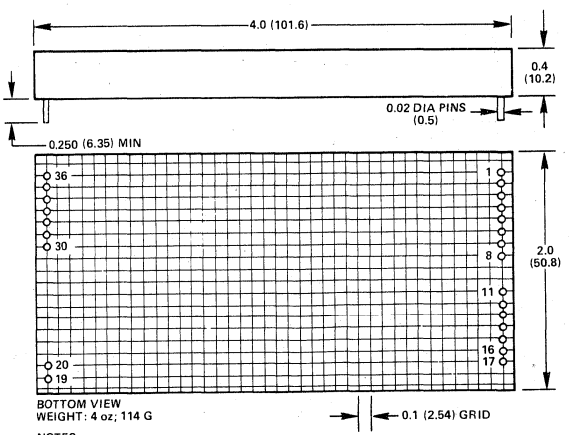
The MAH series of high-speed analog-to-digital converters represent the latest "state-of-the-art" in high speed successive approximation technology. They are the fastest and most accurate complete converters of their type, featuring internal reference, clock, timing, encoding, and control logic functions. The MAH series A/D's should be considered in applications where completeness of design function, ease of interface, and speed are required. These modules make maximum use of the latest monolithic and hybrid parts to minimize total parts complexity and increase reliability. They are designed to be form, fit, and function compatible with the T.P. 4130 and 4131, with advantages over the latter in overall accuracy without any sacrifice in speed.

In almost all applications, these A/D's require the use of a fast sample-and-hold. Depending upon the application, either the ADI THC or THS series of ultra-fast sample-and-holds are recommended.



NOTES:
1. ON MODEL MAH-0801, PINS 15 AND 16 ARE UNUSED.
2. ANALOG AND POWER GROUNDS ARE CONNECTED TOGETHER INTERNALLY.

MAH-0801 and MAH-1001 Block Diagram



NOTES:
SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.
PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

MATING CONNECTOR: MSA-1

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	UNITS	MAH-0801	MAH-1001
RESOLUTION FS @ Full Scale	Bits	8	10
ACCURACY (Relative to Full Scale)	±% FS	0.02	*
Quantization Error	LSB	±1/2	*
Nonlinearity	LSB (max)	±1/4	±1/2
Differential Nonlinearity	LSB (max)	±1/4	±1/2
	LSB (typ)	±1/8	±1/4
Missing Codes		No Missing Codes 0 to +70°C	
Monotonicity		Monotonic 0 to +70°C	
TEMPERATURE COEFFICIENTS			
Differential Nonlinearity	±ppm/°C	3	*
Gain	±ppm/°C	20	*
Zero Offset (Unipolar)	±μV/°C	10	*
Zero Offset (Bipolar)	±ppm/°C	15	*
INPUT			
Ranges (Full Scale)			
MAH-XXXX-1	V	0 to -5	*
MAH-XXXX-2	V	0 to -10	*
MAH-XXXX-3	V	±5	*
MAH-XXXX-4	V	±10	*
MAH-XXXX-5	V	±1.024	*
Impedance (Function of Option)	Ω/V	100	*
OVERVOLTAGE	V	To Twice Peak Input FS Without Damage.	
CONVERSION TIME[1]	ns max	750	1000
	ns typ	700	950
ENCODE COMMAND			
Logic Levels (1 Standard TTL Load)	V	"0" = 0 to +0.4, "1" = +2 to +5.5	
Function		Positive-going edge resets converter. Trailing edge starts conversion.	
Duration (Width)	ns min (max)	50 (150)	*
Rise and Fall Times	ns max	20	*
Repetition Rate	kHz max	1333	1000
LOGIC OUTPUTS			
Levels TTL (Same as Encode Command)			
Drive Capability		Data and Data Ready—10 Std TTL Loads, Clock—10 TTL Loads	
Parallel Data		8 or 10 lines of data held until start of next Encode Command	
Coding (Unipolar)		CBN	*
(Bipolar)		COB/C2SC	*
Serial Data		MSB first, successive pulse output during conversion, NRZ.	
Coding		Same as parallel output except 2SC not available.	
Clock		Pulse train of 9 or 11 internal clock pulses, gated on during the conversion period.	
POWER REQUIREMENTS			
+14.5V to +15.5V	mA max	50	*
-14.5V to -15.5V	mA max	30	*
+5V ±5%	mA max	250	*
TEMPERATURE RANGE			
Operating	°C	0 to +70	*
Storage	°C	-55 to +85	
PHYSICAL CHARACTERISTICS			
Case		Diallyl Phthalate per MIL-M-14 Type SDG-F	

NOTE:
[1] Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.
*Specifications same as MAH-0801.
Specifications subject to change without notice.

OUTPUT CODING

The logic output coding is shown true relative to the analog input to the A/D. If an inverting track and hold—such as the Analog Devices THC series—or an inverting op amp is used ahead of the A/D, the true logic coding is inverted relative to the system input. This yields the systemic coding as follows:

Scale	Input Voltage	Complementary Straight Binary
-FS -1LSB	-9.9900V	1111 1111 11
-3/4 FS	-7.5000V	1100 0000 00
-1/2 FS	-5.0000V	1000 0000 00
-1/4 FS	-2.5000V	0100 0000 00
-1LSB	-0.0010V	0000 0000 01
0	0.0000V	0000 0000 00

NOTE
(0 to -10V) for MAH-1001-2; LSB = 10mV for MAH-1001-1, apply input voltage factor of 1/2.

Table 1. MAH-0801 and MAH-1001 Unipolar Operation for Options 1 and 2

Binary (BIN) in place of Complementary Binary (CBN) for options 1 and 2; Offset Binary (OBN) in place of Complementary Offset Binary (COB) for options 3, 4 and 5; Two's Complement (2SC) in place of Complementary Two's Complement (C2SC).

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-4.9900V	1111 1111 11	0111 1111 11
-3/4 FS	-3.7500V	1110 0000 00	0110 0000 00
-1/2 FS	-2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
+1/2 FS	+2.5000V	0100 0000 00	1100 0000 00
+3/4 FS	+3.7500V	0010 0000 00	1010 0000 00
+FS -1LSB	+4.9900V	0000 0000 01	1000 0000 01
+FS	+5.0000V	0000 0000 00	1000 0000 00

NOTES:
(-5V to +5V) for MAH-1001-3; LSB = 10mV for MAH-1001-4 apply input voltage factor of 2.

Table 2. MAH-0801 and MAH-1001 Bipolar Operation for Options 3 and 4

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-1.022V	1111 1111 11	0111 1111 11
-1/2 FS	-0.512V	1100 0000 00	0100 0000 00
0	-0.000V	1000 0000 00	0000 0000 00
+1/2 FS	+0.512V	0100 0000 00	1100 0000 00
+FS	+1.024V	0000 0000 00	1000 0000 00

NOTE
(-1.024V to +1.024V) for MAH-1001-5; LSB = 2mV.

Table 3. MAH-0801 and MAH-1001 Bipolar Operation for Option 5

CALIBRATION AND ADJUSTMENT

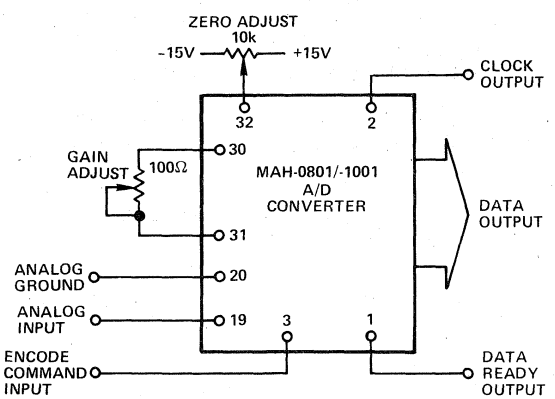


Figure 1. MAH-0801 and MAH-1001 Hookup

PROCEDURE:
1. APPLY ENCODE COMMAND PULSE TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE FOR +1/2LSB. VARY THE ZERO ADJUST POTENTIOMETER FOR AN LSB FLUTTER (THIS WILL APPEAR AS AN EQUAL UNCERTAINTY AT THE OUTPUT BETWEEN THE CODES 0000 .... 0000 AND 0000 .... 0001).
3. WITH THE PRECISION VOLTAGE SOURCE ADJUSTED TO -FS +1/2LSB, ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN CODES 1111 .... 1110 AND 1111 .... 1111.

Unipolar Operation

PROCEDURE:
1. APPLY AN ENCODE COMMAND TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE TO +FS -1/2LSB. THE ZERO ADJUST POTENTIOMETER FOR A FLUTTER BETWEEN VARY CODES 0000 .... 0000 AND 0000 .... 0001.
3. ADJUST THE VOLTAGE SOURCE TO -FS +1/2LSB. ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN THE CODES 1111 .... 1110 AND 1111 .... 1111.

Bipolar Operation

TIMING DIAGRAM

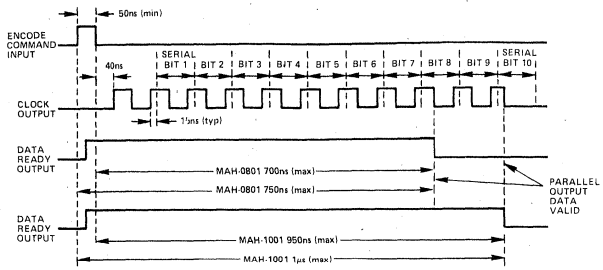


Figure 2. MAH-0801 and MAH-1001 Timing Diagram

APPLICATIONS

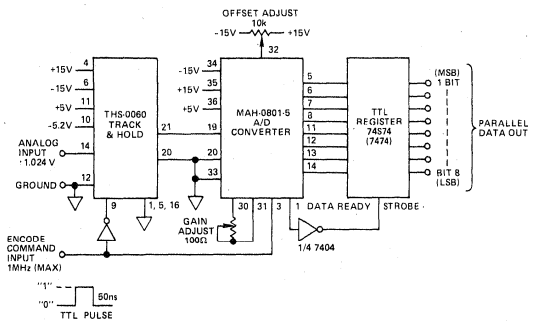


Figure 3. Depicts a Complete 8-Bit, 1MHz Conversion System Using the THS-0060 Track-and-Hold and the MAH-0801-5 Low-Voltage Input A/D Converter

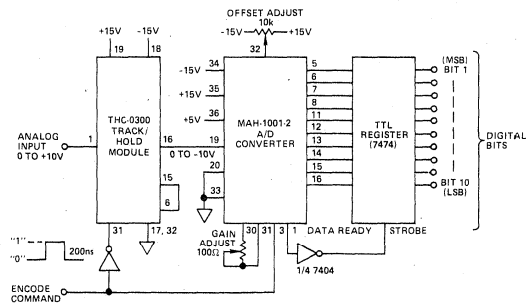


Figure 4. Depicts the MAH-1001-2 A/D Converter Used with the THC-0300 Track-and-Hold

NOTES ON USAGE

The use of a large ground plane is highly recommended. Tie all grounds for both the ADC and T&H together. Make the distance from the ADC to the system ground as short as possible with as low an impedance as possible. Bypass each power supply run with a ceramic (0.1μF) and tantalum (3.3μF) capacitor. Keep the analog input as far away from the digital outputs as practical. Avoid the use of twisted pair cables for digital outputs wherever possible. The use of coax cable for analog inputs is recommended wherever practical to avoid digital feedback.

PIN DESIGNATIONS
MAH-0801, MAH-1001

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY OUT	15	BIT 9 OUT
2	INTERNAL CLOCK OUT	16	BIT 10 OUT (LSB)
3	ENCODE COMMAND IN	17	BIT 1 OUT (MSB)
4	SERIAL OUTPUT	19	ANALOG INPUT
5	BIT 1 OUT (MSB)	20	ANALOG GROUND
6	BIT 2 OUT	30	GAIN ADJUST
7	BIT 3 OUT	31	GAIN ADJUST
8	BIT 4 OUT	32	OFFSET ADJUST
11	BIT 5 OUT	33	POWER GROUND
12	BIT 6 OUT	34	-15V POWER IN
13	BIT 7 OUT	35	+15V POWER IN
14	BIT 8 OUT	36	+5V POWER IN

NOTES:
On Model MAH-0801, Pins 15 and 16 are deleted.
Power and Analog grounds are internally connected.

ORDERING INFORMATION

The 8- and 10-bit versions of the MAH series may be ordered with various options according to the chart below.

MAH-0801 **-1**

RESOLUTION AND ACCURACY	ANALOG INPUT RANGE
MAH-0801 = 8 Bits	-1 0 to -5V FS
MAH-1001 = 10 Bits	-2 0 to -10V FS
	-3 ±5V FS
	-4 ±10V FS
	-5 ±1.024V FS

Ultra High Speed 8-, 10-, and 12-Bit A/D Converters

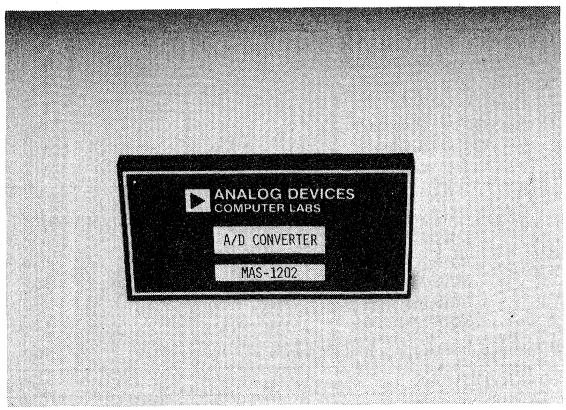
MAS-0801, -1001, -1202

FEATURES

- High Speed at Low Cost
  - 8 Bits 1μs max
  - 10 Bits 1.5μs max
  - 12 Bits 2μs max
- No Missing Codes Over Temperature
- Low Power
- Industry Standard Pin Out
- Parallel and Serial Outputs

APPLICATIONS

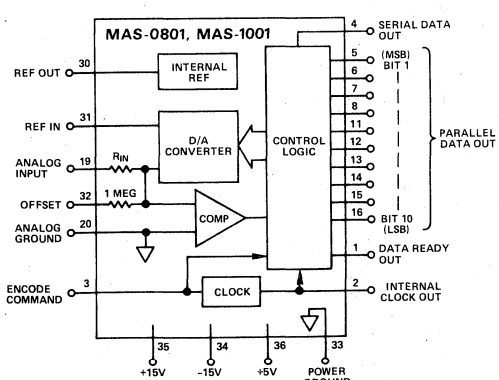
- High Speed Data Acquisition
- Real Time Waveform Analysis
- Radar Signal Processing
- Analytical Instruments



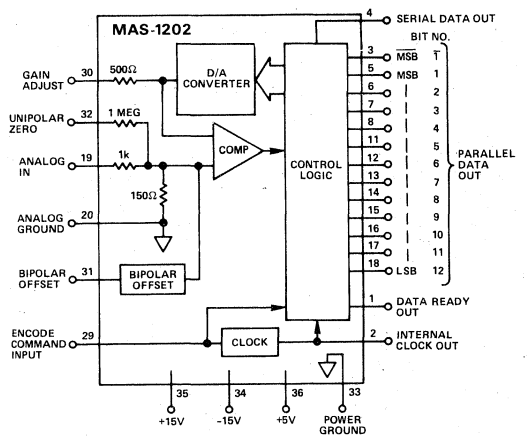
GENERAL DESCRIPTION

The MAS series of high speed analog to digital converters represent the "state of the art" in application of the successive approximation conversion technique by providing highest speed at lowest cost. With monotonicity guaranteed over temperature these reliable modules are form, fit and function compatible with popular industry standards from Datel and Philbrick (for new designs consider the HAS series of hybrid converters).

In most applications these A/D's should be used with a fast sample hold such as the THS/THC series.



MAS-0801 and MAS-1001 Block Diagram



MAS-1202 Block Diagram

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Units	MAS-0801	MAS-1001	MAS-1202
RESOLUTION FS = Full Scale	Bits	8	10	12
ACCURACY (Relative to Full Scale)	±% FS	0.2	0.05	0.012
Quantization Error	LSB	±1/2	*	*
Nonlinearity	LSB (max)	±1/2	*	*
Differential Nonlinearity	LSB (max)	±1/2	*	*
Missing Codes		No Missing Codes 0 to +70°C		
TEMPERATURE COEFFICIENTS				
Differential Nonlinearity	±ppm/°C	3	*	*
Gain	±ppm/°C	20	*	30
Gain (Option-P)	±ppm/°C	5	*	NA
Zero Offset (Unipolar)	±μV/°C	10	*	100
Zero Offset (Bipolar)	±ppm/°C	15	*	*
Zero Offset (Option-P)	±ppm/°C	5	*	NA
INPUT				
Ranges (Full Scale)		Options MAS-0801 and MAS-1001 ONLY		STANDARD
MAS-XXXX-1	V	0 to -5	*	0 to +10/±5
MAS-XXXX-2	V	0 to -10	*	NA
MAS-XXXX-3	V	±5	*	NA
MAS-XXXX-4	V	±10	*	NA
MAS-XXXX-5	V	±1.024	*	NA
Impedance (Function of Option)	Ω/V	100	*	1150Ω
OVERVOLTAGE	V	To Twice Peak Input FS Without Damage.		
CONVERSION TIME[1]	μs max	1	1.5	2
	μs typ	0.8	1.3	1.8
ENCODE COMMAND				
Logic Levels (1 Standard TTL Load)	V	"0" = 0 to +0.4, "1" = +2 to +5.5		
Function		Positive-going edge resets converter, Trailing edge starts conversion for 8- and 10-bit versions.		
Duration (Width)	ns min	50	*	100
Rise and Fall Times	ns max	20	*	*
Repetition Rate	kHz max	1000	666	500
LOGIC OUTPUTS				
Levels TTL (Same as Encode Command)				
Drive Capability		Data and Data Ready – 4 Std TTL Loads, Clock – 6TTL Loads		
Parallel Data		8, 10 or 12 lines of data held until next Encode Command		
Coding (Unipolar)		CBN	*	BIN
(Bipolar)		COB/2SC	*	OBN/2SC
Serial Data		MSB first, successive pulse output during conversion, NRZ.		
Coding		Same as parallel output except 2SC not available.		
Clock		Pulse train of 9, 11 or 13 internal clock pulses, gated on during the conversion period.		
POWER REQUIREMENTS				
+14.5V to +15.5V	mA	70	*	80
-14.5V to -15.5V	mA	30	*	20
+5V ±5%	mA	150	*	*
TEMPERATURE RANGE				
Operating	°C	0 to +70	*	*
Storage	°C	-55 to +85	*	*
PHYSICAL CHARACTERISTICS				
Case		Diallyl Phthalate per MIL-M-14 Type SDC-F		

NOTE:

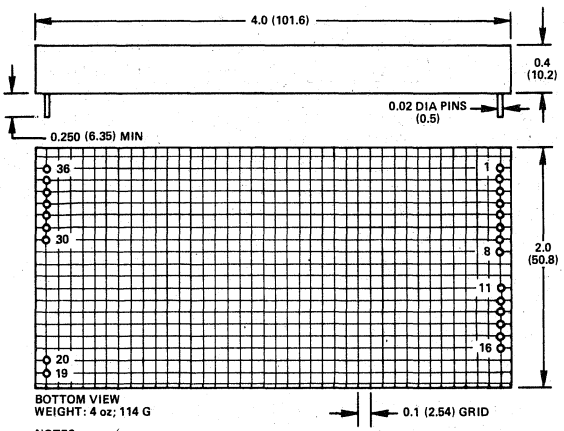
[1] Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.

*Specifications same as MAS-0801.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

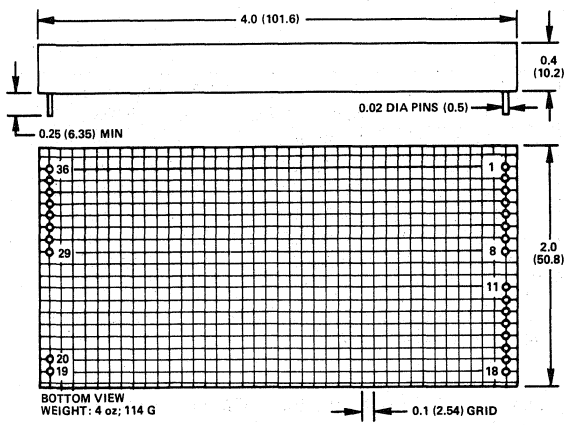
Dimensions shown in inches and (mm).



NOTES:
SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.
PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

PIN DESIGNATIONS
MAS-0801, MAS-1001

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY OUT	15	BIT 9 OUT
2	INTERNAL CLOCK OUT	16	BIT 10 OUT (LSB)
3	ENCODE COMMAND IN	19	ANALOG INPUT
4	SERIAL OUTPUT	20	ANALOG GROUND
5	BIT 1 OUT (MSB)	30	REFERENCE OUT
6	BIT 2 OUT	31	REFERENCE INPUT
7	BIT 3 OUT	32	OFFSET
8	BIT 4 OUT	33	POWER GROUND
11	BIT 5 OUT	34	-15V POWER IN
12	BIT 6 OUT	35	+15V POWER IN
13	BIT 7 OUT	36	+5V POWER IN
14	BIT 8 OUT		

PIN DESIGNATIONS
MAS-1202

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY	16	BIT 10 OUT
2	INTERNAL CLOCK OUT	17	BIT 11 OUT
3	BIT 1 OUT ($\overline{\text{MSB}}$)	18	BIT 12 OUT (LSB)
4	SERIAL DATA OUT	19	ANALOG INPUT
5	BIT 1 OUT (MSB)	20	ANALOG GROUND
6	BIT 2 OUT	29	ENCODE COMMAND IN
7	BIT 3 OUT	30	GAIN ADJUST
8	BIT 4 OUT	31	BIPOLAR OFFSET
11	BIT 5 OUT	32	UNIPOLAR ZERO
12	BIT 6 OUT	33	POWER GROUND
13	BIT 7 OUT	34	-15V POWER IN
14	BIT 8 OUT	35	+15V POWER IN
15	BIT 9 OUT	36	+5V POWER IN

ORDERING INFORMATION

The 8- and 10-bit versions of the MAS series may be ordered with various options according to the chart below.

MAS-0801	P	-1	-CBN
RESOLUTION AND ACCURACY	TEMPCO	ANALOG INPUT RANGE	LOGIC OUTPUT CODING (See Note 1)
MAS-0801 = 8 Bits MAS-1001 = 10 Bits	For ±5ppm/°C tempco at slightly higher cost, add "P". For standard tempco, leave blank.	-1 0 to -5V FS -2 0 to -10V FS -3 ±5V FS -4 ±10V FS -5 ±1.024V FS	CBN = Complementary Binary (Options 1 and 2) COB = Complementary Offset Binary (Options 3, 4 and 5) C2SC = Complementary Two's Complement (Options 3, 4 and 5)

NOTES:
For 12-bit performance order the MAS-1202 which has no options.
The mating connector for the MAS series is the MSA-1.

OUTPUT CODING

The logic output coding is shown true relative to the analog input to the A/D. If an inverting track and hold—such as the Analog Devices THC series—or an inverting op amp is used ahead of the A/D, the true logic coding is inverted relative to the system input. This yields the systemic coding as follows:

Scale	Input Voltage	Complementary Straight Binary
-FS -1LSB	-9.9900V	1111 1111 11
-3/4 FS	-7.5000V	1100 0000 00
-1/2 FS	-5.0000V	1000 0000 00
-1/4 FS	-2.5000V	0100 0000 00
-1LSB	-0.0010V	0000 0000 01
0	0.0000V	0000 0000 00

NOTE
(0 to -10V) for MAS-1001-2; LSB = 10mV for MAS-1001-1, apply input voltage factor of 1/2.

Table 1. MAS-0801 and MAS-1001 Unipolar Operation for Options 1 and 2

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-1.022V	1111 1111 11	0111 1111 11
-1/2 FS	-0.512V	1100 0000 00	0100 0000 00
0	-0.000V	1000 0000 00	0000 0000 00
+1/2 FS	+0.512V	0100 0000 00	1100 0000 00
+FS	+1.024V	0000 0000 00	1000 0000 00

NOTE
(-1.024V to +1.024V) for MAS-1001-5; LSB = 2mV.

Table 3. MAS-0801 and MAS-1001 Bipolar Operation for Option 5

Binary (BIN) in place of Complementary Binary (CBN) for options 1 and 2; Offset Binary (OBN) in place of Complementary Offset Binary (COB) for options 3, 4 and 5; Two's Complement (2SC) in place of Complementary Two's Complement (C2SC).

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-4.9900V	1111 1111 11	0111 1111 11
-3/4 FS	-3.7500V	1110 0000 00	0110 0000 00
-1/2 FS	-2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
+1/2 FS	+2.5000V	0100 0000 00	1100 0000 00
+3/4 FS	+3.7500V	0010 0000 00	1010 0000 00
+FS -1LSB	+4.9900V	0000 0000 01	1000 0000 01
+FS	+5.0000V	0000 0000 00	1000 0000 00

NOTES:
(-5V to +5V) for MAS-1001-3; LSB = 10mV for MAS-1001-4 apply input voltage factor of 2.

In Table 2, complementary 2SC is accomplished by factory option.

Table 2. MAS-0801 and MAS-1001 Bipolar Operation for Options 3 and 4

Scale	Input Voltage	Straight Binary
+FS -1LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4 FS	+2.5000V	0100 0000 0000
+1LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

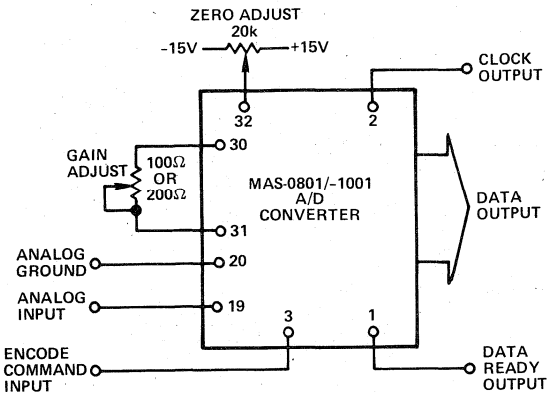
NOTE
Unipolar Operation (0 to +10V)

Table 4. MAS-1202 Unipolar Operation (0 to +10V)

Scale	Input Voltage	Straight Binary	Two's Complement
+FS -1LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS +1LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

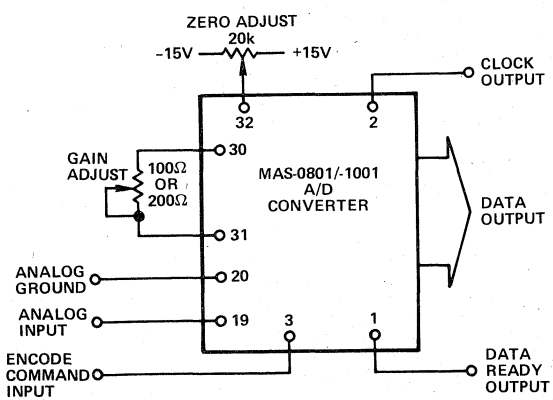
NOTE
In Table 5, TWO'S COMPLEMENT (2SC) is accomplished by using the MSB output for Bit 1.

Table 5. MAS-1202 Bipolar Operation (-5V to +5V)



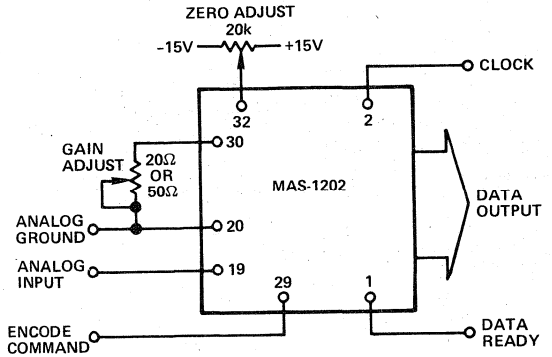
PROCEDURE:
1. APPLY ENCODE COMMAND PULSE TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE FOR +1/2LSB (+1.2mV). VARY THE ZERO ADJUST POTENTIOMETER FOR AN LSB FLUTTER (THIS WILL APPEAR AS AN EQUAL UNCERTAINTY AT THE OUTPUT BETWEEN THE CODES 0000 .... 0000 AND 0000 .... 0001).
3. WITH THE PRECISION VOLTAGE SOURCE ADJUSTED TO -FS +1/2LSB, ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN CODES 1111 .... 1110 AND 1111 .... 1111.

Figure 1. MAS-0801 and MAS-1001 Unipolar Operation



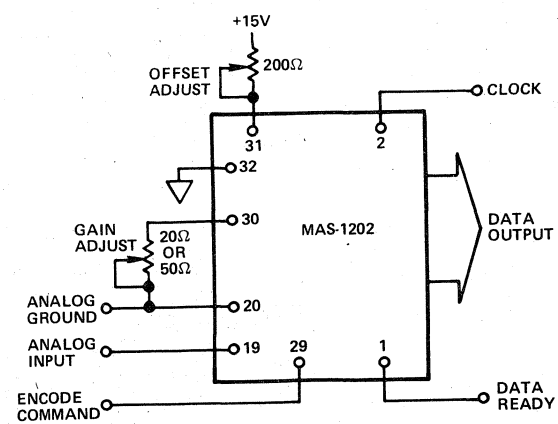
PROCEDURE:
1. APPLY AN ENCODE COMMAND TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE TO +FS -1/2LSB. THE ZERO ADJUST POTENTIOMETER FOR A FLUTTER BETWEEN VARY CODES 0000 .... 0000 AND 0000 .... 0001.
3. ADJUST THE VOLTAGE SOURCE TO -FS +1/2LSB. ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN THE CODES 1111 .... 1110 AND 1111 .... 1111.

Figure 2. MAS-0801 and MAS-1001 Bipolar Operation



PROCEDURE:
1. APPLY ENCODE COMMAND PULSE TO THE ENCODE COMMAND INPUT (PIN 29).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE FOR +1/2LSB (+1.2mV). VARY THE ZERO ADJUST POTENTIOMETER FOR BIT 12 FLUTTER (THIS WILL APPEAR AS AN EQUAL UNCERTAINTY AT THE OUTPUT BETWEEN THE CODES 0000 0000 0000 AND 0000 0000 0001).
3. WITH THE PRECISION VOLTAGE SOURCE ADJUSTED TO +FS -1 1/2LSB (+9.9964V), ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN CODES 1111 1111 1110 AND 1111 1111 1111.

Figure 3. MAS-1202 Unipolar Operation



PROCEDURE:
1. APPLY AN ENCODE COMMAND TO THE ENCODE COMMAND INPUT (PIN 29).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE TO -FS +1/2LSB (-4.9988V). ADJUST THE OFFSET POTENTIOMETER FOR A FLUTTER BETWEEN CODES 0000 0000 0000 AND 0000 0000 0001.
3. ADJUST THE VOLTAGE SOURCE TO +FS -1 1/2LSB (+4.9964V). ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN THE CODES 1111 1111 1110 AND 1111 1111 1111.

Figure 4. MAS-1202 Bipolar Operation

APPLICATIONS

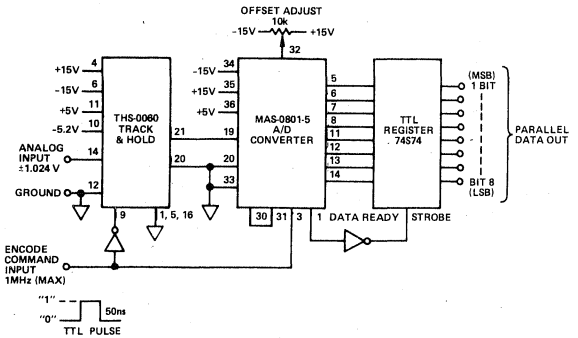


Figure 5. Depicts a Complete 8-Bit, 1MHz Conversion System Using the THS-0060 Track-and-Hold and the MAS-0801-5 Low-Voltage Input A/D Converter

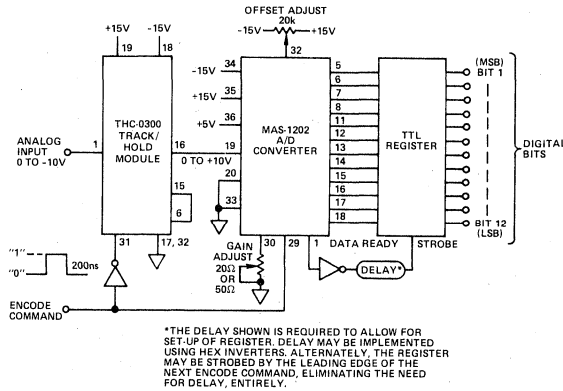


Figure 6. Depicts the MAS-1202 A/D Converter used with the THC-0300 Track-and-Hold

TIMING DIAGRAMS

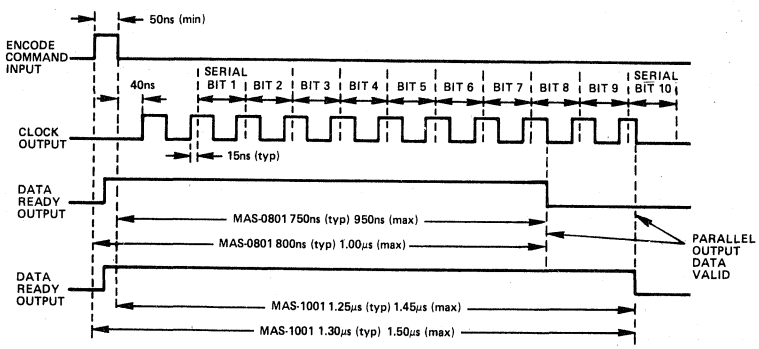


Figure 7. MAS-0801 and MAS-1001 Timing Diagram

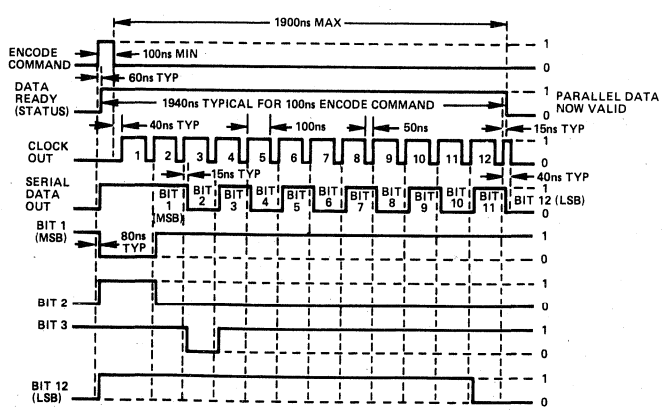


Figure 8. MAS-1202 Timing Diagram

8-Bit Video Analog-to-Digital Converter

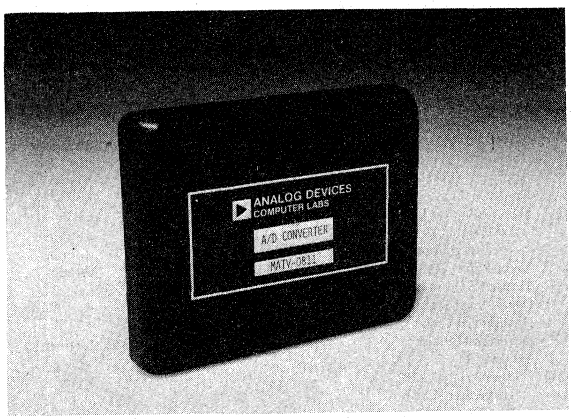
MATV-0811, -0816, -0820

FEATURES

8-Bit Accuracy — Guaranteed Monotonic
Ultra-High Speed — dc to 20MHz Word Rates
Most Economical Video A/D
Smallest Available Complete A/D — 5.5″ X 4.38″ X 0.85″
Self Contained — Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

APPLICATIONS

Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies
Video Time Base Correction and Frame Synchronization
Radar Signal Processing
Real Time Transient and Continuous Spectrum Analysis

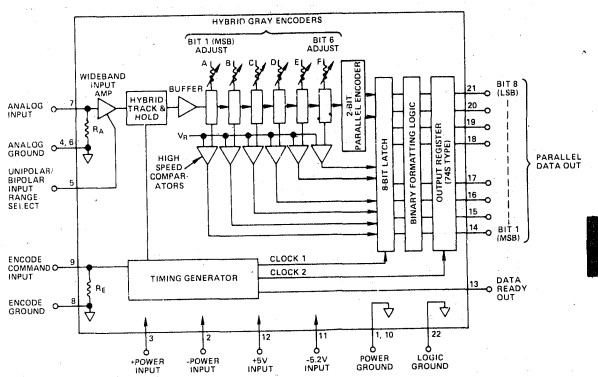


GENERAL DESCRIPTION

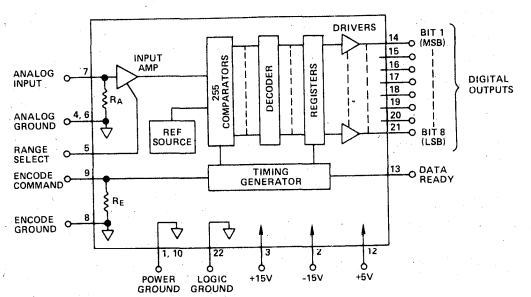
The Analog Devices' MATV series of A/D converters represent a major breakthrough in high-speed A/D technology. Providing conversion word rates from dc to 11MHz, 16MHz and 20MHz the MATV-0811, MATV-0816 and MATV-0820 are the lowest cost A/D converters in their performance class. As complete devices, they require only the addition of external power to accomplish precision video A/D conversion.

The use of internal hybrid microcircuit construction allows these modular A/D's to occupy a volume of only 21 cubic inches—about 1/5 the volume of available comparable devices. They are housed in metal cases which not only shield the circuits from external RF interference, but aid in efficient heat dissipation. A choice of analog input voltages is available, including the industry standard 0 to +1V at 75Ω. The encode command input, data ready output, and the digital bit outputs are all TTL compatible. Designed to operate from either ±12V or ±15V analog and +5V digital supplies (MATV-0811 and MATV-0816 also require -5.2V), the MATV series dissipate less than 8 watts. Their weight is < 10 ounces due to enclosure rather than encapsulation. This technique facilitates rapid, inexpensive factory repair and aids in reliable printed circuit board mounting by the customer without extensive mechanical constraints or system engineering.

Relative dc accuracy is 0.2% of full scale ±1/2LSB when operating over the frequency range of dc to 20MHz. The MATV series is designed to digitize color television signals at rates up to 20MHz and is also ideally suited for other analog to digital conversion requirements, such as radar signal processing, laser pulse analysis, transient analysis, and medical electronics applications where real-time analysis and display of large quantities of information are required.



MATV-0811, MATV-0816 Block Diagram



R_A AND R_E ARE DETERMINED BY THE ANALOG INPUT IMPEDANCE AND ENCODE COMMAND INPUT IMPEDANCE, RESPECTIVELY.

MATV-0820 Block Diagram

SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	UNITS	MATV-0811	MATV-0816	MATV-0820
RESOLUTION (FS = Full Scale)	Bits/% FS	8/0.4	*	*
LSB Weight	% FS	0.4	*	*
ACCURACY (relative) at dc	typ	±0.15% ±1/2LSB	*[1]	*
	max	±0.2% ±1/2LSB	*[1]	*
Monotonicity		GUARANTEED	*	*
Differential Nonlinearity vs Temperature	% FS/°C	0.01	*	0.005
Linearity and Gain vs Temperature	% FS/°C	0.02	*	0.01
DYNAMIC CHARACTERISTICS				
AC Linearity @ Encode Rate[2]	MHz	11	15	20
Analog Input Frequency				
DC to 3.6MHz	Spurious Signals are			
	> dB below FS	50	*	*
3.6MHz to 5.5MHz		45	*	*
Conversion Rate (Encode Word Rate)	MHz max	11	16[1]	20
Conversion Time[3]	ns	150±20	120±20	35 ±10 + 1/Encode Rate
Aperture Uncertainty (Jitter)	ps max	±30	*	*
Aperture Time	ns	3	*	12
Signal to Noise Ratio				
(rms signal to rms noise)	dB min	48	*	*
(peak signal to rms noise)	dB min	58	*	*
Noise Power Ratio[4]	dB min	37	*	*
Transient Response[5]	ns	50	*	*
Overvoltage Recovery Time[6]	ns	60	*	*
Differential Gain[7]	%	3	*	*
Differential Phase	Degrees	1	*	*
Bandwidth				
Small Signal 3dB	MHz	20	*	*
Large Signal 3dB	MHz	15	*	*
Flat ±0.1dB, dc through	MHz	5.5	*	*
INPUT[8]				
Voltage Range				
Unipolar (Pin 5 Grounded)	V	0 to 1	*	*
Bipolar (Pin 5 open)	V	±0.5	*	*
Impedance (Terminated to Ground)	Ω	75	*	*
ENCODE COMMAND INPUT[8]				
Logic Levels, TTL Compatible		"0" = 0 to +0.4V	*	*
		"1" = +2.4V to +5V	*	*
Impedance (terminated to ground)	Ω	75 ±5%	*	*
Rise and Fall Times (10% to 90%) max	ns	10	*	*
Duration/Width 50% points (see timing diagram)	ns min	10	*	20
	ns max	50% duty cycle	40	*
Frequency (random or periodic)	dc to MHz	11	16	20
DIGITAL DATA OUTPUT[8]				
Format		Eight Parallel Bits NRZ		
Logic Levels, TTL		(Same as Encode Command)		
Drive Capability (not short circuit protected)	TTL Loads	10 Std	10 Schottky	
Time Skew	ns max	15	10	10
Coding		Straight Binary (BIN)		
DATA READY OUTPUT				
Format[9]		RZ	*	*
Logic Levels, TTL		(Same as Encode Command)		
Drive Capability		10 Std	10 Schottky	
Width	ns	40±10	35±5	25±5
POWER REQUIREMENTS[10]				
MATV-0811, MATV-0816/MATV-0820				
+15V ±2%/+11.8V to +15.5V	mA max	210	*	70
−15V ±2%/−11.8V to −15.5V	mA max	180	*	400
+5V ±5%/+5V +5%	mA max	450	540	200
−5.2V ±5%	mA max	280	*	N/A
TEMPERATURE RANGE[11]				
Operating (case)	°C	0 to +70	*	*
Storage	°C	−55 to +85	*	*

*Same as MATV-0811.

NOTES:

[1] Applies to a customer specified operating frequency, ±10%. Outside this range, accuracy may degrade to ±0.3% ±1/2LSB.

[2] AC linearity expressed in terms of spurious in-band signals generated at specified encode rates.

[3] Pipeline delay not related to encode rate.

[4] DC to 5MHz while noise BW with slot frequency at 500kHz.

[5] Time to achieve 8-bit (0.2%) accuracy after F.S. step input.

[6] For signals not exceeding 10% overvoltage, the A/D will recover to 8-bit accuracy within 60ns after the signal returns to the specified range. Overvoltage inputs greater than 150% of F.S. may damage input circuits and should be avoided.

[7] At maximum encode rate, 20 IRE unit subcarrier, not including quantization effects.

[8] Consult factory for other voltage, impedance and logic level options.

[9] The leading edge of the data ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

[9] For MATV-0811, the leading edge of the Data Ready pulse occurs approximately 15ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0816, the leading edge of the Data Ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0820, the leading edge of the Data Ready pulse occurs approximately simultaneously with output data changes. The trailing edge is recommended for strobing data into external circuits. This provides a minimum of 20ns set-up time for external registers.

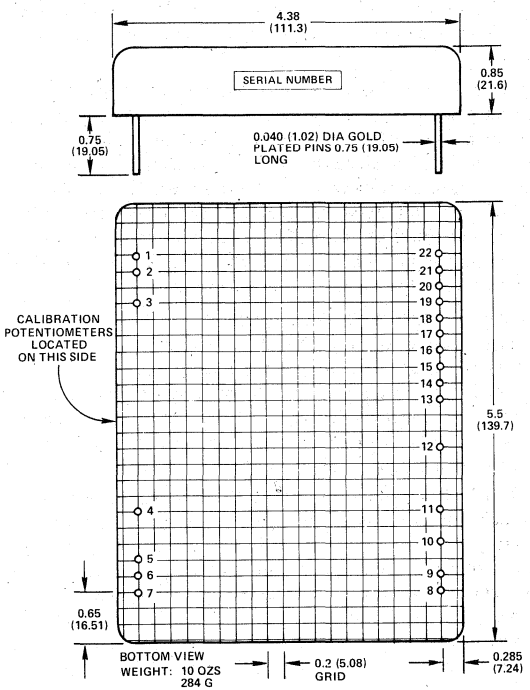
[10] The A/D's are calibrated at the factory at either ±12V or ±15V as a no-cost option. Other operating voltages within this range may be specified by the user at slight additional cost. See application section for more information.

[11] See Thermal Considerations for operating temperature considerations.

Specifications subject to change without notice.

MECHANICAL OUTLINE AND DIMENSIONS

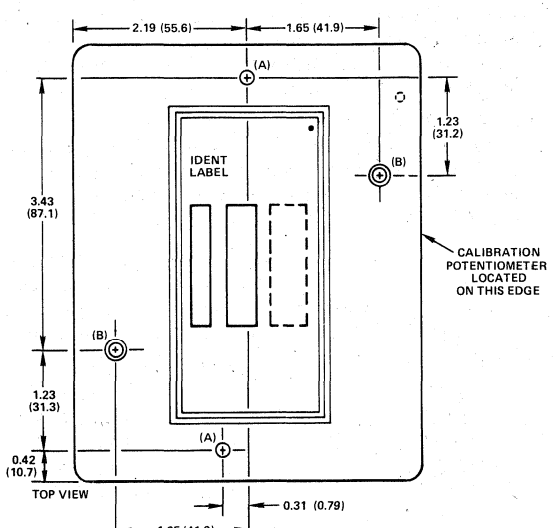
Dimensions shown in inches and (mm)



PINS ARE GOLD PLATED PER MIL-G-5204, TYPE II

NOTES:
DIMENSIONS AND LOCATION OF HOLD DOWN HOLES FOR MATV-0820 ARE SHOWN ON THE MECHANICAL OUTLINE FIGURE BELOW. NOT AVAILABLE ON MATV-0811 AND -0816.

DOT ON TOP INDICATES POSITION OF PIN 1.



(A) LOCATIONS ARE HOLES (0.16" TO 0.18" DIA.) THRU THE A/D SUITABLE FOR SECURING THE UNIT TO A MOTHER BOARD, ETC.
(B) LOCATIONS ARE EQUIPPED WITH #6X32 CLINCH NUTS (0.3" DEEP) SUITABLE FOR ATTACHING HEAT SINK, ETC.

DOT ON TOP INDICATES POSITION OF PIN 1.

MATV SERIES
PIN DESIGNATIONS

PIN	FUNCTION	COMMENTS
1	POWER GROUND	*
2	- POWER INPUT	-11.8V (MIN); -16.5V (MAX)
3	+ POWER INPUT	+11.8V (MIN); +16.5V (MAX)
4	ANALOG GROUND	*
5	RANGE SELECT	UNIPOLAR = GROUND BIPOLAR = OPEN
6	ANALOG GROUND	*
7	ANALOG INPUT	OPTIONAL
8	ENCODE GROUND	*
9	ENCODE COMMAND	TTL, +5V (MAX)
10	POWER GROUND	*
11	NO CONNECTION 0820 -5.2V POWER INPUT 0811, 0816	 -5V (MIN), -5.5V (MAX)
12	+5V POWER INPUT	+4.75V (MIN); +5.25V (MAX)
13	DATA READY OUTPUT	TTL LEVELS
14	BIT 1 OUTPUT (MSB)	TTL LEVELS
15	BIT 2 OUTPUT	TTL LEVELS
16	BIT 3 OUTPUT	TTL LEVELS
17	BIT 4 OUTPUT	TTL LEVELS
18	BIT 5 OUTPUT	TTL LEVELS
19	BIT 6 OUTPUT	TTL LEVELS
20	BIT 7 OUTPUT	TTL LEVELS
21	BIT 8 OUTPUT (LSB)	TTL LEVELS
22	DIGITAL LOGIC GND.	*

*ALL GROUNDS ARE INTERNALLY CONNECTED

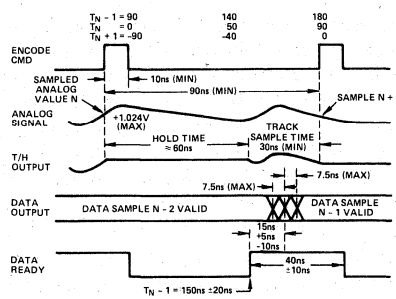


Figure 1. MATV-0811 Timing Diagram at Maximum Sample Rate of 11MHz

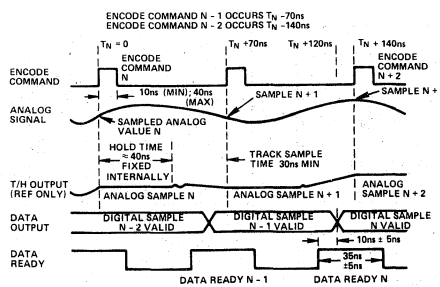
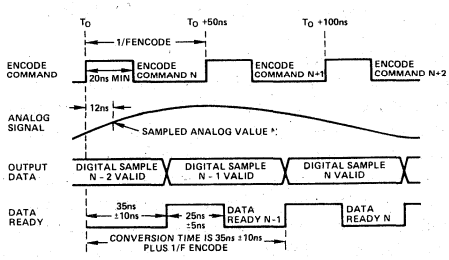


Figure 2. MATV-0816 Timing Diagram at Sample Rate of 14.3MHz



NOTE:
2 ENCODE COMMAND PULSES ARE REQUIRED TO OBTAIN FIRST "DATA READY".

Figure 3. MATV-0820 Timing Diagram Shown at an Encode Frequency of 20MHz

Applying the MATV-0811, -0816, -0820

REMOTE INTERFACE CONSIDERATIONS

In many applications, the user may wish to build up an A/D converter assembly using the MATV modular converter as a building block. The assembly would typically consist of a printed circuit card in a card nest, housed within an equipment enclosure. It could also be a chassis with coaxial inputs and outputs, and power supplies incorporated into the chassis to permit operation from ac line voltages.

This type of assembly generally includes provisions for converting remotely generated signals and driving transmission lines to the remote digital loads. The design of such an assembly must take into account the wideband, low level sensitivity of the A/D converter input, and the use of terminated coaxial input lines is recommended for analog and encode command inputs. The use of 75Ω coaxial transmission line is recommended. It is particularly important to isolate the A/D's digital outputs from the signal input, since digital feedback can seriously affect the conversion accuracy.

In order to maintain specified A/D conversion parameters, the power supplies must be fully decoupled from sources of noise and other signals. Total line and load regulation should be better than 15mV at the MATV power supply terminals.

The output circuit of the MATV is a "74" register and is capable of driving up to 10 local TTL loads. When driving distant loads and terminations are required, line drivers should be used. For twisted pair lines, the 9614 driver is recommended. For coaxial lines, the 2614 is recommended.

Figure 4 shows the recommended circuit for the A/D assembly used in applications where the signal source and digital load are remote from the A/D converter.

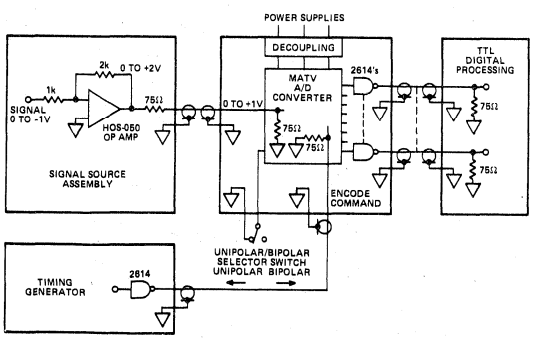


Figure 4. Typical System Application

THERMAL CONSIDERATIONS

The MATV series A/D converters are specified to operate over a temperature range of 0 to +70°C. The temperature referred to is the module case temperature, and operation outside of this range can seriously damage the converter. The temperature limitations that Analog Devices has placed on this converter are necessitated by the published temperature limits of the commercially available components used within the device. Nowhere in the device are unreliable semiconductor junction temperature limits approached.

Generally, the A/D module must have forced air cooling when in operation. The only exceptions are when the unit is operated in free air ambients of <+40°C (as during bench test, for example), or if the case is in contact with a heat sink or cold plate which will maintain the temperature of the case at +70°C or less.

Whenever the A/D module is confined in a closed space or operated at ambient temperatures above +40°C, Analog Devices recommends an air flow of 500 linear feet per minute across the top of the case. Since the A/D is a metal encased device, this amount of air flow will keep the case temperature within 10°C of the air temperature, and thus permit operation at ambient temperatures of up to +60°C. This amount of air flow can be easily supplied by a 20 or 30 CFM fan if the air flow is directed across the top surface of the module.

POWER SUPPLY CONSIDERATIONS

The MATV-0820 A/D is designed to operate from standard analog and digital power supplies. The digital supply is +5V ±5% the industry standard. The analog supplies may be any symmetrical voltages between ±11.8 and ±15.5 volts. Thus the modules may be operated on either of the two industry standard analog-supply voltages (±12V or ±15V).

The MATV-0811 and MATV-0816 also require -5.2V +5%, and their calibration is affected somewhat by power supply changes. So the A/D must be readjusted whenever the analog supply voltages are changed by more than 300mV. The MATV-0811 and MATV-0816 units supplied by Analog Devices are normally calibrated and tested at ±15V ±0.1% power supply voltages. The customer may at time of purchase specify other power supply voltages between ±12V and ±15V, and the A/D's will be calibrated and tested at the specified power supply voltages.

CALIBRATION INFORMATION – MATV-0811, MATV-0816

The MATV series A/D converters are calibrated at the factory at either ±12V or ±15V and do not normally require recalibration more often than every year (depending on severity of service). The following calibration procedures are provided to aid the user in long term maintenance. Recalibration should not be started unless it has been determined that the A/D is definitely out of calibration.

DC CALIBRATION

Using appropriate power supply voltages and encode rates, adjust potentiometers A through F shown in Figure 5 as indicated below. Use a test set-up similar to that shown in Figure 6.

Unipolar DC Input Voltage	Adjustment Point	Adjust for Flutter Zone of Bit Given	Correct Output "X" Denotes Flutter or Uncertainty
+1/2 FS	A	1	XXXXXXXX
+1/4 FS	B	2	0XXXXXXX
+3/8 FS	C	3	01XXXXXX
+7/16 FS	D	4	011XXXXX
+15/32 FS	E	5	0111XXXX
+31/64 FS	F	6	01111XXX

Table 1.

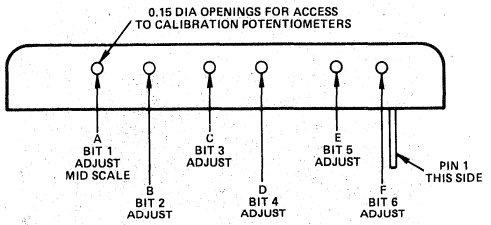


Figure 5. Location of Calibration Potentiometers

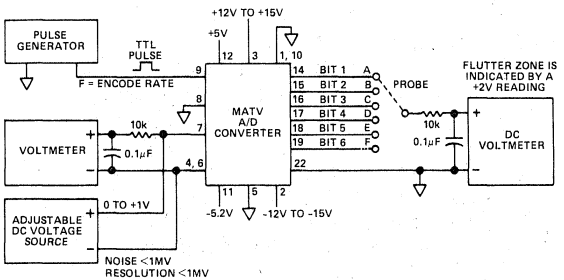


Figure 6. DC Calibration Set-Up

DYNAMIC LINEARITY ADJUSTMENT

If the need arises for recalibration of an MATV series A/D, the simple dc procedure just described may be used, or the following dynamic adjustment may be performed. In general, the dc procedure gives satisfactory results for most applications, but by its nature, is an approximation. When the best possible linearity is required, the following dynamic linearity adjustment may be used. In this procedure, the output of the A/D is converted back into an analog signal by a D/A converter and then subtracted from the input. The result is an error display, and the A/D calibration potentiometers are used to reduce the error pattern to the minimum possible error.

The equipment is set-up and adjusted as shown in Figure 7. The A/D adjustments F through B (see Figure 5) are adjusted in that order to obtain minimum error, which is indicated by the least vertical deflection on the oscilloscope error display.

Adjustment B controls the linearity at mid-scale of the A/D. Mid-scale (1/2 scale) is approximately in the horizontal center of the display. Adjustment C controls the linearity at 1/4 scale, 1/2 scale and 3/4 scale. Adjustment D controls the linearity at 1/8 scale, 1/4 scale, 3/8 scale . . . . 7/8 scale. Adjustment E controls linearity in 1/16 scale segments across the range, and adjustment F controls linearity in 1/32 scale segments across the range.

Note that adjustment F interacts with B, C, D and E. Adjustment E interacts with adjustments B, C and D, etc. Therefore the highest letter adjustment pot requiring adjustment must be varied first. For example, if nonlinearities are observed at 1/4, 1/2 and 3/4 scale, adjustment C is first varied to correct the errors at 1/4 and 3/4 scale. Then adjustment B is used to correct the error at mid-scale.

After adjustment, the error display should be less than 4mV p-p.

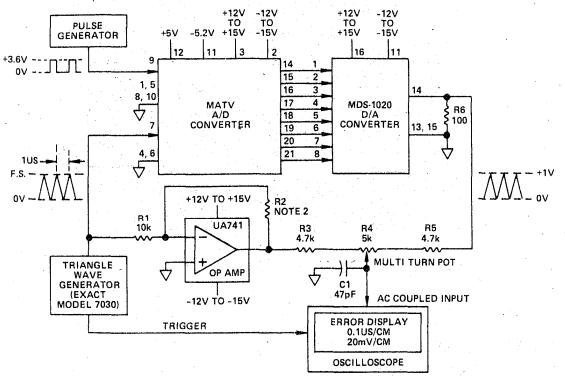


Figure 7. Dynamic Linearity Adjustment Set-Up

CALIBRATION INFORMATION – MATV-0820

Two internal calibration potentiometers are provided for the adjustment of offset and gain of the MATV-0820. These potentiometers are accessible from the exterior of the MATV-0820, and Figure 8 shows the location of these potentiometers.

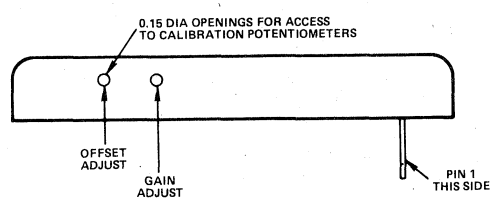


Figure 8. Location of Calibration Potentiometers

OFFSET ADJUSTMENT

The OFFSET ADJUST control shifts the range of the A/D without affecting gain or linearity. It is normally adjusted for an output of 0000000X (X signifies an uncertainty or flutter zone for the indicated bit) with an input analog dc voltage of +1/2LSB for the unipolar input option, and –FS +1/2LSB for the bipolar input option. The user, however, may set this potentiometer to any point in its range to obtain a different offset. The range of the offset potentiometer is approximately ±10% of FS.

GAIN ADJUSTMENT

The GAIN ADJUST control affects the full scale range of the A/D by varying the gain of the A/D front end. It is normally adjusted to give an output of 1111111X for an input dc analog voltage of +FS –1/2LSB. The user may adjust this potentiometer anywhere in its range to provide for different input full scale requirements. The range of this potentiometer is approximately ±5% of the nominal input FS range.

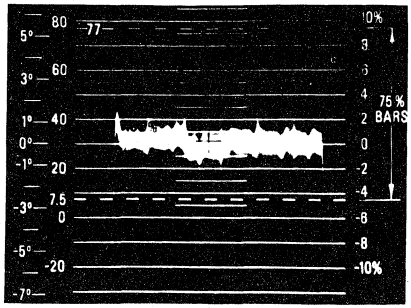


Figure 9. Typical Differential Gain of MATV-0816 Operating at 15MHz Word Rates

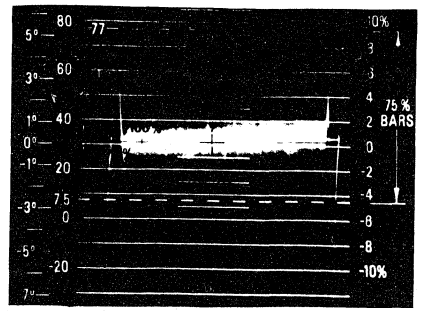


Figure 10. Typical Differential Phase of MATV-0816 Operating at 15MHz Word Rates

ORDERING INFORMATION

Each MATV series A/D converter will be calibrated at ±15V as a standard. Order by model number either MATV-0811, MATV-0816 or MATV-0820.

Optional Versions

The MATV series A/D's are available with a variety of options, including analog input range and impedance, encode command input impedance, encode word rate, power supply voltage calibration, etc. Any option other than what is shown on the data sheet will have longer delivery, since each non-standard device is built on a per order basis.

A complete listing of optional designators is available from either the factory or your local Analog Devices' sales office.

Device Marking

The MATV series A/D that you order will be marked with a series of alphanumerics which specifically designate the options built into the device. For the standard devices, these will be as follows:

MATV-0811 will be marked MATV-0811-1-BIN-15 for older devices, or MATV-0811-AA150 for newer devices.

MATV-0816 will be marked MATV-0816-0175 BIN 75143150 for older devices, or MATV-0816 ABBA143150 for newer devices.

MATV-0820 will be marked MATV-0820-0175 BIN 75 for older devices, or MATV-0820 ABAA for newer devices.

This information is provided so that there will be no confusion as to why information other than the basic model number appears on the device identification label, which might cause problems at a customers' incoming inspection.

10-Bit Video Analog to Digital Converter

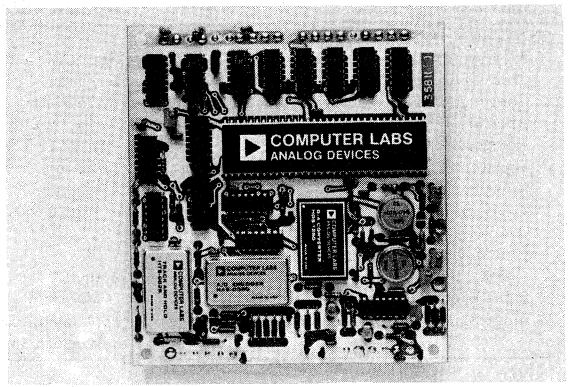
MOD-1005

FEATURES

10 Bits @ 5MHz Word Rate
One-27 Sq. In. PC Board
Built-In Track-and-Hold — 25ps Aperture Uncertainty
20MHz Analog Input Bandwidth
TTL Compatible
Low (10-Watt) Power Dissipation
Signal-To-Noise Ratio Greater Than 58dB
Noise Power Ratio Greater Than 49dB
Completely Repairable

APPLICATIONS

Radar Digitizing
Digital Communications
Real Time Spectrum Analysis
High Resolution TV



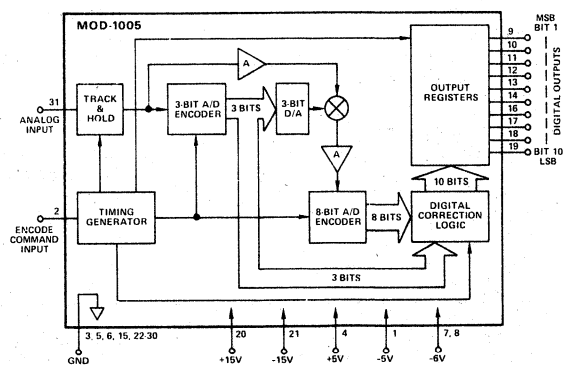
GENERAL DESCRIPTION

Analog Devices' model MOD-1005 is a very high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1005 is truly a breakthrough in high-speed A/D technology. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

The MOD-1005 is constructed on a single printed circuit card which is intended for mounting on a system mother-board, and occupies only 27 square inches. Within this A/D is the required sample/track and hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. NO external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1005 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1005 is backed by Analog Devices' limited one year warranty.



Block Diagram

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

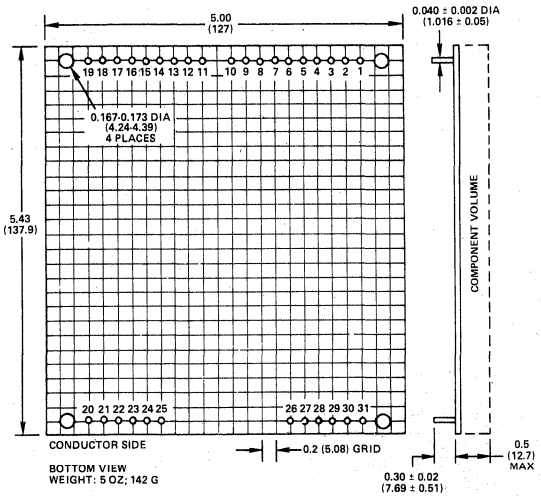
MODEL	MOD-1005
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)
LSB WEIGHT	4mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Full Scale ±1/2LSB
Monotonicity	Guaranteed
Differential Nonlinearity vs. Temperature	0.0005% of FS/°C
Gain vs. Temperature	0.01% of FS/°C
DYNAMIC CHARACTERISTICS	
AC Linearity[1]	Spurious Signals >59dB below FS
Conversion Time	See Text
Conversion Rate (Word Rate)	dc to 5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time	45ns (±10ns from unit to unit)
Signal to Noise Ratio (rms signal to rms noise)	58dB min at 500kHz analog input
Noise Power Ratio[2]	49dB min
Transient Response (Full Scale Step Input)	10-Bit (0.05%) Accuracy within 50ns
Overvoltage Recovery Time	
Recovers to 10-bit accuracy after	
2 X FS input overvoltage in	200ns
Input Bandwidth (small signal, 3dB)	20MHz min
Input Bandwidth (large signal, 3dB)	15MHz min flat within ±0.1dB, dc through 5MHz
INPUT	
Voltage Range	±2.048V FS
	±4V Absolute max
Impedance	50Ω
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.01% Full Scale/°C
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration Min/Max	20ns/60% of Duty Cycle
Frequency (Random or Periodic)	dc to 5MHz
Sample Delay	45ns (unit to unit tolerance is ±10ns)
DIGITAL DATA OUTPUT	
Format	10 Parallel Bits, NRZ
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or 2 Standard TTL Loads
Time Skew	10ns max
Coding	2's Complement (2SC)
Conversion Time	See Text on the Next Page
POWER REQUIREMENTS	typ/max
+15V ±5%	150/170mA
-15V ±5%	150/170mA
-6V ±4%	300/350mA
+5V ±5%	350/400mA
-5V ±5%	500/550mA
Power Consumption	10 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	100 Linear Feet Per Min (LFPM)
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:
[1] AC linearity expressed in terms of spurious in-band signals generated as specified encode rates, with dc to 2.5MHz analog input.
[2] DC to 2.4MHz white noise BW with Slot frequency of 512kHz.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches (mm).



PIN DESIGNATIONS

PIN	FUNCTION
1	-5V
2	ENCODE COMMAND
3	GND*
4	+5V
5	GND*
6	GND*
7	-6V
8	-6V
9	BIT 1 MSB
10	BIT 2
11	BIT 3
12	BIT 4
13	BIT 5
14	BIT 6
15	GND*

PIN	FUNCTION
16	BIT 7
17	BIT 8
18	BIT 9
19	BIT 10 LSB
20	+15V
21	-15V
22	GND*
23	GND*
24	GND*
25	GND*
26	GND*
27	GND*
28	GND*
29	GND*
30	GND*
31	ANALOG INPUT

*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1005

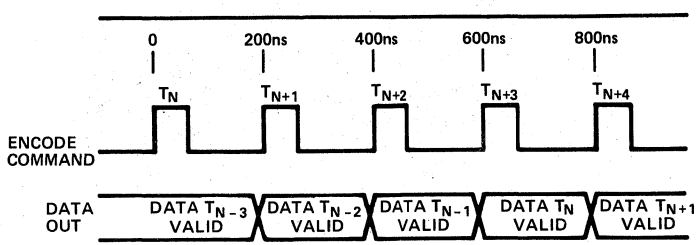
ORDERING INFORMATION

Order model number MOD-1005 A/D converter. Mating pin sockets for the MOD-1005 are model number MSB-2 (31 required per A/D).

CONVERSION TIME

Output data is valid two encode command clock periods plus 200ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid 600ns after the application of the first encode command pulse – assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA T_N (THE RESULT OF ENCODE COMAND T_N) OCCURS TWO CONVERSION PERIODS PLUS 200ns AFTER ENCODE COMMAND T_N. FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 200ns AFTER THE THIRD ENCODE COMMAND PULSE OR T_N + 600ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

Figure 1. MOD-1005 Timing Diagram

GROUND CONNECTIONS

It should be noted that the MOD-1005 PC board has 13 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

CALIBRATION PROCEDURE (MOD-1005)

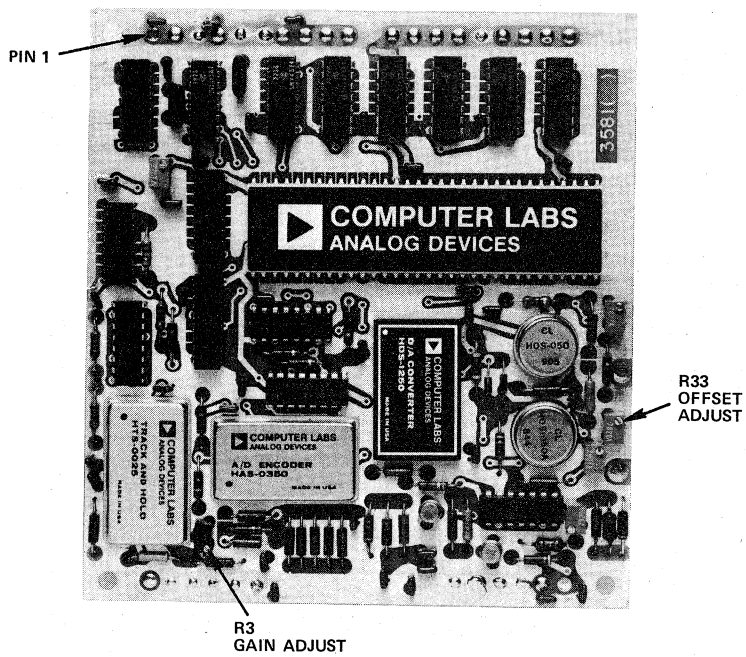
The MOD-1005 A/D is precisely calibrated at the factory before shipment, and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. It should be remembered that the output coding of this A/D is 2SC.

Offset Adjustment

The offset is adjusted by varying potentiometer R33 with 0 volts applied to the analog input. To obtain the proper output code, observe that the digital output is changing between 1 1 1 1 1 1 1 1 1 1 and 0 0 0 0 0 0 0 0 0 0 at this adjustment level. When properly adjusted a digital code of 0 0 0 0 0 0 0 0 0 0 will represent analog input 1LSB above zero volts, and a digital code of 1 1 1 1 1 1 1 1 1 1 will represent an analog input of 1LSB below zero volts.

Gain Adjustment

The gain is adjusted by varying potentiometer R3. This adjustment is made by applying +2.042V (FS –1 1/2LSB) to the analog input and while monitoring the digital output, adjust R3 for the output code varying between 0 1 1 1 1 1 1 1 1 0 and 0 1 1 1 1 1 1 1 1 1 (FS). If the user needs to offset the entire range of the A/D, this can be accomplished by readjusting R33 as required. However, in this procedure, the offset should always be adjusted first.



A/D Converter Assembly

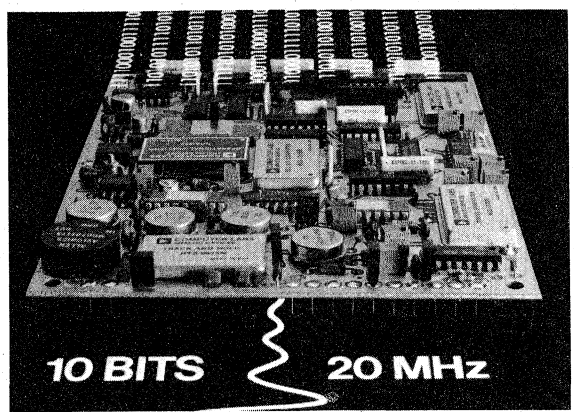
ANALOG DEVICES

10-Bit Video Analog to Digital Converter

MOD-1020

FEATURES
10-Bits @ 20MHz Word Rates
One 35 Sq. In. PC Board
Built-In Track-and-Hold – 25ps Aperture
15MHz Large-Signal Input Bandwidth
ECL Compatible
Signal-to-Noise Ratio Greater Than 56dB
Noise Power Ratio Greater Than 45dB

APPLICATIONS
Television Digitizing
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis
Sonar Digitizing



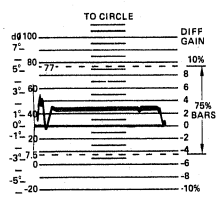
GENERAL DESCRIPTION

The Analog Devices' model MOD-1020 is an ultra-high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at word rates through 20MHz. The MOD-1020 is another in the series of state-of-the-art A/D converters from Analog Devices that employs the unique digital correcting subranging (DCS) conversion technique to virtually eliminate errors normally associated with subranging type A/D converters. No other A/D converter commercially available offers the user the speed and accuracy attainable with the MOD-1020.

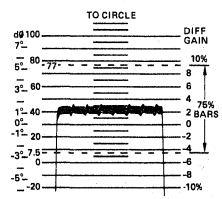
The MOD-1020 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 35 square inches. The A/D is complete with internal track-and-hold, encoder, timing circuitry, references, and latched output. It produces a true all-parallel digital output.

The encode command input, digital outputs, and data ready output are balanced ECL compatible. The A/D requires only an external encode command input pulse and external power supplies for operation. The analog input impedance is at least 500Ω, so that the user can easily terminate the A/D with lower impedances in his system. Gain and offset potentiometers are provided on the card so that the A/D can be operated in either the unipolar or bipolar modes. The A/D is fully repairable.

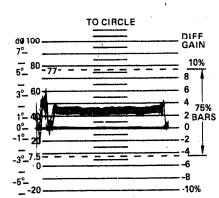
The MOD-1020 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications (baseband digitizing), composite color television digitizing, spectrum analysis, medical instrumentation, and many others. Each MOD-1020 is backed by Analog Devices' limited one-year warranty.



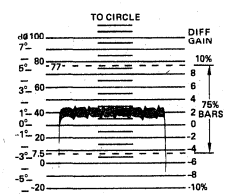
Differential Phase – Generator and Vectorscope Back-to-Back No A/D Conversion



Differential Gain – Generator and Vectorscope Back-to-Back No A/D Conversion



Differential Phase – Model MOD-1020 ADC and Model 4120E DAC Back-to-Back 14.4MHz Conversion (Word) Rate



Differential Gain – Model MOD-1020 and Model 4120E DAC Back-to-Back 14.4MHz Conversion (Word) Rate

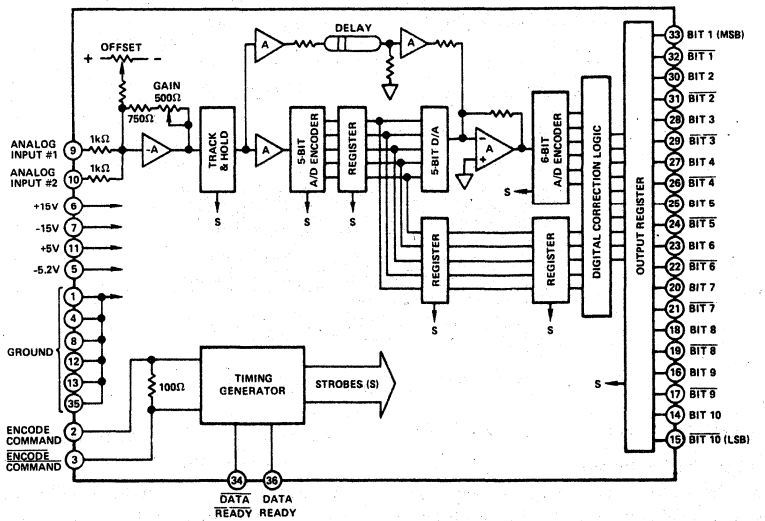
The above waveforms were obtained utilizing a Tektronix Model 149A N.T.S.C. Test Signal Generator with a 20 IRE unit TV test signal output. The display (output) was obtained using a Tektronix Model 520A Vectorscope.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1020
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)
LSB WEIGHT	1mV or 2mV Depending on Analog Input Range
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Full Scale ±1/2LSB
Monotonicity	Guaranteed 0 to +70°C
Nonlinearity vs. Temperature	0.0005% of FS/°C
Gain vs. Temperature	0.015% of FS/°C
DYNAMIC CHARACTERISTICS	
AC Linearity[1] (dc to 1MHz)	Spurious Signals ≥60dB below FS
(1MHz to 5MHz)	Spurious Signals ≥55dB below FS
(5MHz to 10MHz)	Spurious Signals ≥50dB below FS
Conversion Time	See Text and Timing Diagram
Conversion Rate[2]	dc to 20MHz (See Note and Ordering Information)
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time (Delay)	5ns (±2ns unit-to-unit tolerance)
Signal to Noise Ratio[3]	56dB min
Signal to Noise Ratio[4]	65dB min
Noise Power Ratio[5]	45dB min, 47dB typ
Transient Response[6]	50ns
Overvoltage Recovery[7]	50ns
Input Bandwidth (small signal, 3dB)[8]	30MHz
Input Bandwidth (large signal, 3dB)[9]	15MHz; Flat within 0.2dB, dc to 10MHz
Two-Tone Linearity (@ Input Frequency);	
60kHz; 62kHz	In-Band Spurious Signals ≥60dB below FS
4.998MHz; 5.000MHz	In-Band Spurious Signals ≥55dB below FS
9.996MHz; 9.998MHz	In-Band Spurious Signals ≥50dB below FS
Differential Gain[10]	1% with 20 IRE Unit Reference
Differential Phase[10]	0.5° with 20 IRE Unit Reference
ANALOG INPUT (See Notes on Input Range in Text)	
Voltage Range	1V p-p or 2V p-p, Depending on Hook-Up
	Either Unipolar or Bipolar
	±4V Absolute max Input
Impedance	1000Ω (2V Input Range)
	500Ω (1V Input Range)
Offset	Adjustable to Zero with On-Card Potentiometer (R4)
Offset vs. Temperature	0.01%/°C
ENCODE COMMAND INPUT	
Logic Levels, ECL Compatible	"0" = -1.7V
(Balanced Input)	"1" = -0.9V
Impedance	100Ω Line-to-Line
Rise and Fall Times	5ns max
Duration (min/max)	10ns/70% of Duty Cycle
Frequency	Specified by Customer, dc to 20MHz (See Ordering Information)
DIGITAL OUTPUT DATA	
Format	10 Parallel Bits, NRZ
Logic Levels, ECL Compatible	"0" = -1.7V
(Balanced Outputs)	"1" = -0.9V
Drive	75Ω to 100Ω, Line-to-Line
Time Skew	5ns max
Coding	Binary (BIN), 2's Complement (2SC)
DATA READY OUTPUT	
Logic Level, ECL Compatible	"0" = -1.7V
(Balanced Output)	"1" = -0.9V
Rise and Fall Times	5ns max
Duration	25ns ±3ns
Conversion Time	Output data is valid two clock perios plus 185 ±20ns after the application of an initial Encode Command pulse—assuming that two pulses occur after the first. Use of the trailing edge of the Data Ready pulses are required to shift the data to the output. For example, with a 20MHz encode rate, data is valid 285 ±20ns after the application of the first Encode Command pulse—assuming that two pulses occur after the first. Use of the trailing edge of the Data Ready pulse is recommended for strobing output data into external registers.
POWER REQUIREMENTS	
+15V ±5%	200mA
-15V ±5%	200mA
+5V ±5%	100mA
-5.2V ±5%	2.7A
Power Consumption	21 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	500 Linear Feet per Minute (LFPM)
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:
[1] AC linearity expressed in terms of spurious in-band signals generated at 20MHz encode rate at the analog frequencies ( ) shown.
[2] To be specified by the customer. See text and ordering information.
[3] RMS signal to rms noise ratio with 500kHz analog input.
[4] Peak-to-peak signal to rms noise ratio with 500kHz analog input.
[5] DC to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz and an encode rate of 20MHz.
[6] Recovers to 10-bit accuracy after 2 X FS input overvoltage in time specified.
[7] For full-scale step input, attains 10-bit accuracy in time specified.
[8] With analog input signal 40dB below FS.
[9] With FS analog input.
[10] Applies to devices optimized for video applications. Differential gain and phase are measured and optimized for ADC's which have the following encode rate optional designators (see Ordering Information): "107" (3 X NTSC subcarrier); "133" (3 X PAL); "143" (4 X NTSC); "177" (4 X PAL).

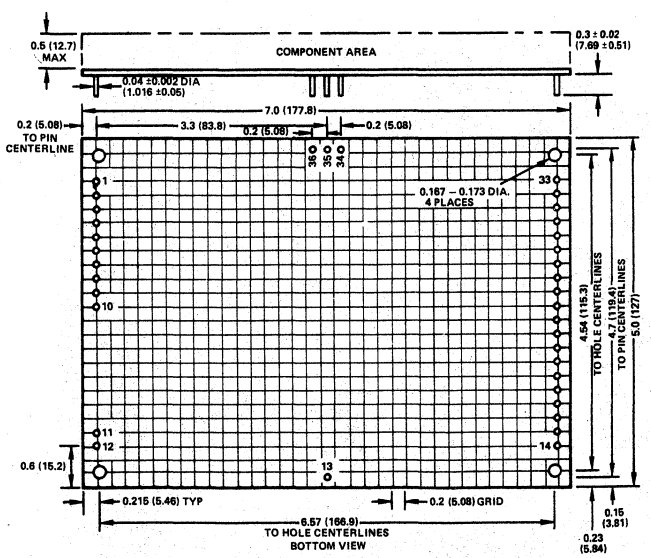
Specifications subject to change without notice.



MOD-1020 Block Diagram

OUTLINE DIMENSIONS

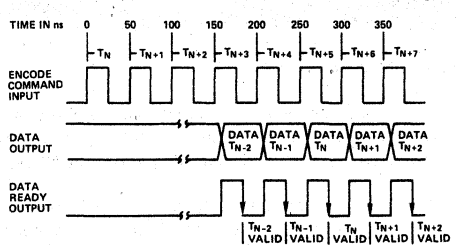
Dimensions shown in inches and (mm).



PIN DESIGNATIONS

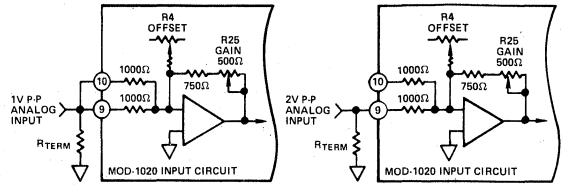
PIN	FUNCTION	PIN	FUNCTION
1	GROUND	19	$\overline{\text{BIT 8}}$
2	ENCODE COMMAND	20	BIT 7
3	$\overline{\text{ENCODE COMMAND}}$	21	$\overline{\text{BIT 7}}$
4	GROUND	22	$\overline{\text{BIT 6}}$
5	-5.2V	23	BIT 6
6	+15V	24	$\overline{\text{BIT 5}}$
7	-15V	25	BIT 5
8	GROUND	26	$\overline{\text{BIT 4}}$
9	ANALOG INPUT #1	27	BIT 4
10	ANALOG INPUT #2	28	BIT 3
11	+5V	29	$\overline{\text{BIT 3}}$
12	GROUND	30	BIT 2
13	GROUND	31	$\overline{\text{BIT 2}}$
14	BIT 10	32	$\overline{\text{BIT 1}}$
15	$\overline{\text{BIT 10}}$	33	BIT 1
16	BIT 9	34	DATA READY
17	$\overline{\text{BIT 9}}$	35	GROUND
18	BIT 8	36	DATA READY

ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE ADC.



OUTPUT DATA ARE VALID TWO CLOCK PERIODS PLUS 185 ±20ns AFTER THE APPLICATION OF AN INITIAL ENCODE COMMAND PULSE. DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D, A TOTAL OF THREE ENCODE COMMAND PULSES ARE REQUIRED TO SHIFT THE DATA TO THE OUTPUT. IN THIS EXAMPLE, WITH AN ENCODE RATE OF 20MHz, DATA ARE VALID 285 ±20ns AFTER THE APPLICATION OF THE FIRST ENCODE COMMAND PULSE. THIS ASSUMES THAT TWO ADDITIONAL ENCODE COMMAND PULSES OCCUR AFTER THE FIRST, AS SHOWN. THE OUTPUT DATA CHANGES STATE TWO ENCODE PERIODS PLUS 160 ±20ns AFTER THE APPLICATION OF THE FIRST ENCODE COMMAND PULSE. AS SHOWN, THE TRAILING EDGE OF THE DATA READY PULSE IS RECOMMENDED FOR STROBING OUTPUT DATA INTO EXTERNAL REGISTERS. IN THESE WAVEFORMS, THE ENCODE COMMAND AND DATA READY REFER TO THE POSITIVE "TRUE" INPUT AND OUTPUTS.

MOD-1020 Timing Diagram



FOR 1V P-P INPUT RANGE, CONNECT ANALOG INPUT TO PIN 9, AND CONNECT PINS 9 AND 10 TOGETHER. UNTERMINATED INPUT IMPEDANCE IS 500Ω. GAIN ADJUSTMENT RANGE (R25) IS ±20% MIN. FOR 2V P-P INPUT RANGE, CONNECT ANALOG INPUT TO PIN 9. PIN 10 IS LEFT DISCONNECTED. UNTERMINATED INPUT IMPEDANCE IS 1000Ω. GAIN ADJUSTMENT RANGE (R25) IS ±20%.

TO OBTAIN THE DESIRED TERMINATED INPUT IMPEDANCE, CONNECT THE APPROPRIATE EXTERNAL TERMINATING RESISTOR BETWEEN THE ANALOG INPUT PIN(S) AND GROUND, AS SHOWN IN THE ABOVE EXAMPLES. INPUT IMPEDANCES GREATER THAN 100Ω WILL RESULT IN LOSS OF INPUT BANDWIDTH AND SHOULD BE AVOIDED.

THE OFFSET POTENTIOMETER (R4) HAS SUFFICIENT RANGE TO ALLOW THE USER TO OPERATE THE ADC IN EITHER THE UNIPOLAR OR BIPOLAR MODE. THE ADC'S ARE CALIBRATED IN THE BIPOLAR CONFIGURATION AT THE FACTORY.

MOD-1020 Analog Input Range Options

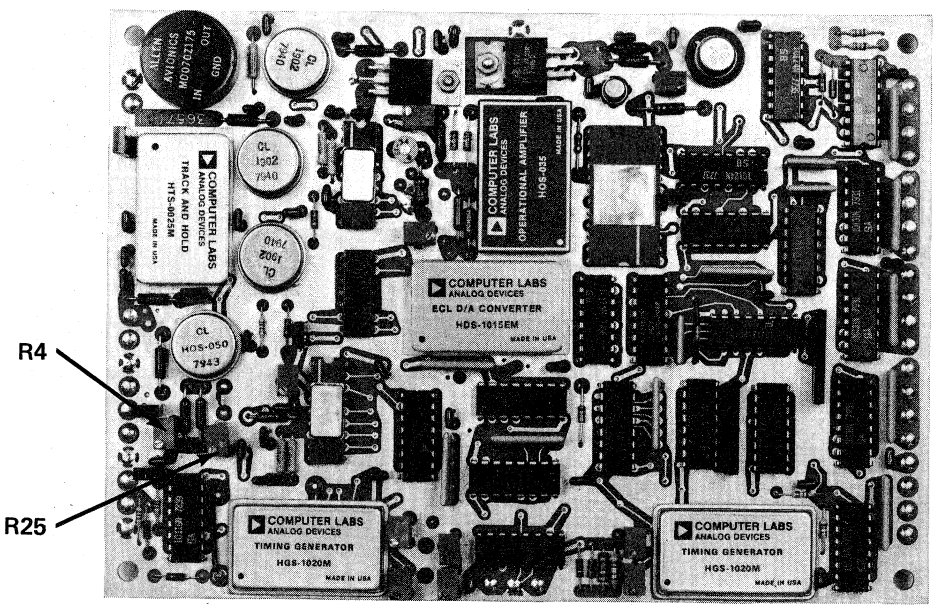
OFFSET AND GAIN ADJUSTMENT

The offset of the ADC is adjusted by varying potentiometer R4. Apply an input voltage to the analog input corresponding to positive full scale. Adjust R4 such that the digital output is changing between 1111111111 and 1111111110.

The gain of the ADC is adjusted by varying potentiometer R25. Apply an input voltage to the analog input that corresponds to negative full scale. Adjust R25 such that the digital output is changing between 0000000000 and 0000000001.

In the foregoing, the ADC is calibrated to have a unipolar positive transfer function. If bipolar input range is required, adjust R4 to offset the entire input by one-half of the full scale input.

In setting the gain, always adjust R4 first to obtain the correct setting for full scale positive input.



Location of Adjustment Potentiometers

ORDERING INFORMATION

IMPORTANT—THE ENCODE RATE OF THE MOD-1020 MUST BE SPECIFIED BY THE CUSTOMER AS SHOWN BELOW:

ORDER MODEL NUMBER: MOD-1020- "XXX", where "XXX" is to be specified by the customer. "XXX" represents the encode word rate in MHz with the decimal place assumed to be (but not shown) between the second and third places. Full 10-bit accuracy will be maintained within ±12% of this specified frequency, up to a maximum of 21MHz. For example, a device specified as MOD-1020-200 is for operation at 20.0MHz and will maintain accuracy from 17.6MHz to 21MHz.

For encode rates of 10MHz or less, the MOD-1020 will maintain full accuracy from dc to 10MHz. For encode frequencies of 10MHz or less, order MOD-1020-100.

Mating sockets for the MOD-1020 are model number MSB-2 (36 required per A/D).

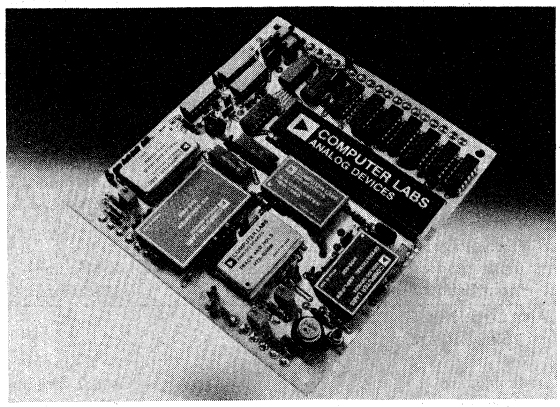
ANALOG DEVICES

12-Bit Video Analog to Digital Converter

MOD-1205

FEATURES
12 Bits @ 5MHz Word Rate
One-27 Sq. In. PC Board
Built-In Track-and-Hold – 25ps Aperture Uncertainty
15MHz Analog Input Bandwidth
TTL Compatible
Low (13-Watt) Power Dissipation
Signal-to-Noise Ratio Greater Than 66dB
Noise Power Ratio Greater Than 56dB
Completely Repairable

APPLICATIONS
Radar Digitizing
Digital Communications
Real Time Spectrum Analysis
Signature Analysis



GENERAL DESCRIPTION

Analog Devices' model MOD-1205 is a very high-speed A/D converter capable of digitizing video input signals to 12-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1205 is truly a breakthrough in high-speed A/D technology. It utilizes the latest state-of-the-art conversion technique called digital correcting subranging (DCS) to effectively eliminate errors normally associated with subranging type ADC's. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

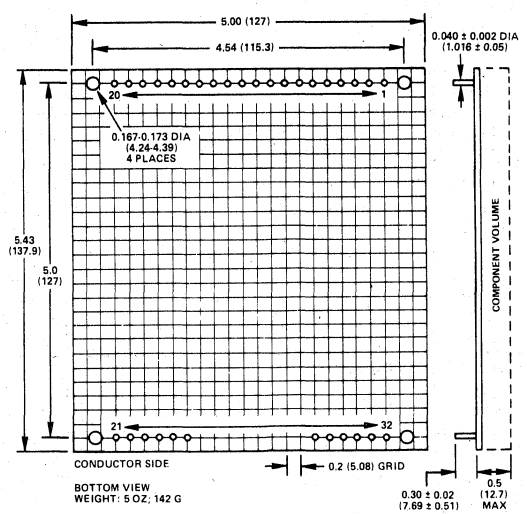
The MOD-1205 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 27 square inches. Within this A/D is the required sample/track-and-hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. NO external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1205 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1205 is backed by Analog Devices' limited one year warranty.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1205
RESOLUTION (FS = FULL SCALE)	12 Bits (0.024% FS)
LSB WEIGHT	1mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.0125% Full Scale ±1/2LSB
Monotonicity	Guaranteed (0 to +70°C)
Nonlinearity vs. Temperature	0.0005% of FS/°C, max
Gain vs. Temperature	0.002% of FS/°C, typ; 0.005% of FS/°C, max
DYNAMIC CHARACTERISTICS	
AC Linearity[1] (dc to 1MHz)	Spurious Signals >70dB below FS, max
(1MHz to 2.5MHz)	Spurious Signals >65dB below FS, max; >68dB, typ
Conversion Time	See Text and Timing Diagram
Conversion Rate (Word Rate)	dc to 5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time	30ns (±10ns from unit to unit)
Signal to Noise Ratio[2]	66dB min; 68dB, typ
Noise Power Ratio[3]	56dB min, 58dB typ
Transient Response[4]	12-Bit (0.0125%) Accuracy within 200ns
Overvoltage Recovery Time[5]	200ns
Input Bandwidth (small signal, 3dB)	15MHz min
Input Bandwidth (large signal, 3dB)	10MHz min; flat within ±0.1dB, dc through 5MHz
ANALOG INPUT	
Voltage Range	±2.048V FS
	±4V Absolute max
Impedance	400Ω with pin 30 open, 50Ω with pin 30 grounded
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.002% FS/°C, typ; 0.005% of FS/°C, max
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration min/max	25ns/50% of Duty Cycle
Frequency (Random or Periodic)	dc to 5MHz
DIGITAL DATA OUTPUT	
Format	12 Parallel Bits, NRZ
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or
	2 Standard TTL Loads
Time Skew	10ns max
Coding	Offset Binary (OBN) or 2's complement (2SC)
Conversion Time	See Text on the Next Page
POWER REQUIREMENTS	
+15V ±5%	200mA
-15V ±5%	150mA
-6V ±4%	700mA
+5V ±5%	800mA
Power Consumption	13 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	500 Linear Feet Per Min (LFPM) @ +70°C
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:
[1] AC linearity expressed in terms of spurious in-band signals generated at specified encode rates at analog input frequencies ( ).
[2] rms signal to rms noise at 500kHz analog input.
[3] dc to 2.4MHz white noise bandwidth with slot frequency of 512kHz.
[4] For full-scale step input, attains 12-bit accuracy in time specified.
[5] Recovers to 12-bit accuracy after 2 X FS input overvoltage in time specified.

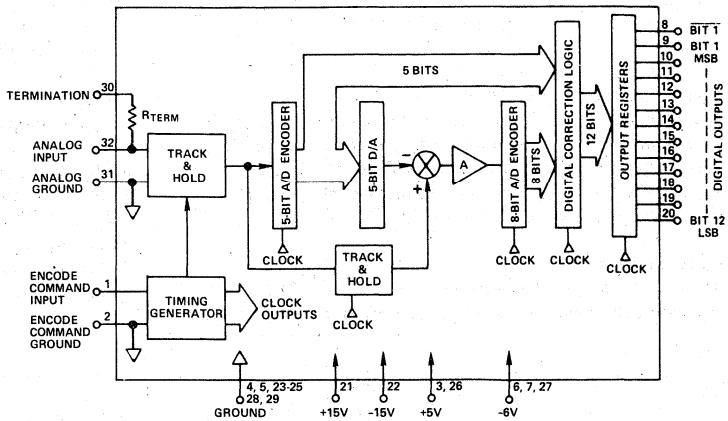
Specifications subject to change without notice.

PIN	FUNCTION
1	ENCODE COMMAND
2	GND*
3	+5V
4	GND*
5	GND*
6	-6V
7	-6V
8	$\overline{\text{BIT 1}}$
9	BIT 1 (MSB)
10	BIT 2
11	BIT 3
12	BIT 4
13	BIT 5
14	BIT 6
15	BIT 7
16	BIT 8

PIN	FUNCTION
17	BIT 9
18	BIT 10
19	BIT 11
20	BIT 12 (LSB)
21	+15V
22	-15V
23	GND*
24	GND*
25	GND*
26	+5V
27	-6V
28	GND*
29	GND*
30	TERMINATION
31	GND*
32	ANALOG INPUT

*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1205

Pin Designations



NOTE: WITH PIN 30 OPEN, ANALOG INPUT IMPEDANCE IS 400Ω. WITH PIN 30 GROUNDED, ANALOG IMPEDANCE IS 50Ω.

MOD-1205 Block Diagram

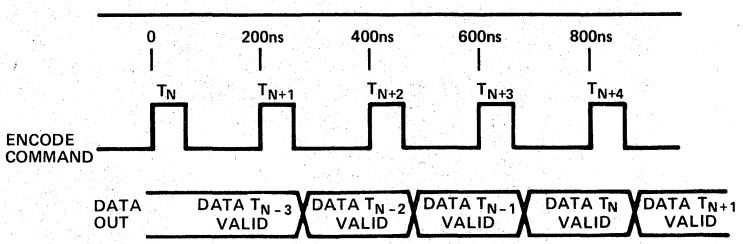
ORDERING INFORMATION

Order model number MOD-1205 A/D converter. Mating pin sockets for the MOD-1205 are model number MSB-2 (32 required per A/D).

CONVERSION TIME

Output data is valid two encode command clock periods plus 275ns ±25ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid 675ns ±25ns after the application of the first encode command pulse—assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA T_N (THE RESULT OF ENCODE COMMAND T_N) OCCURS TWO CONVERSION PERIODS PLUS 275ns ±25ns AFTER ENCODE COMMAND T_N. FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 275ns ±25ns AFTER THE THIRD ENCODE COMMAND PULSE OR T_N + 675ns ±25ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

Figure 1. MOD-1205 Timing Diagram

GROUND CONNECTIONS

It should be noted that the MOD-1205 PC board has 9 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

CALIBRATION PROCEDURE (MOD-1205)

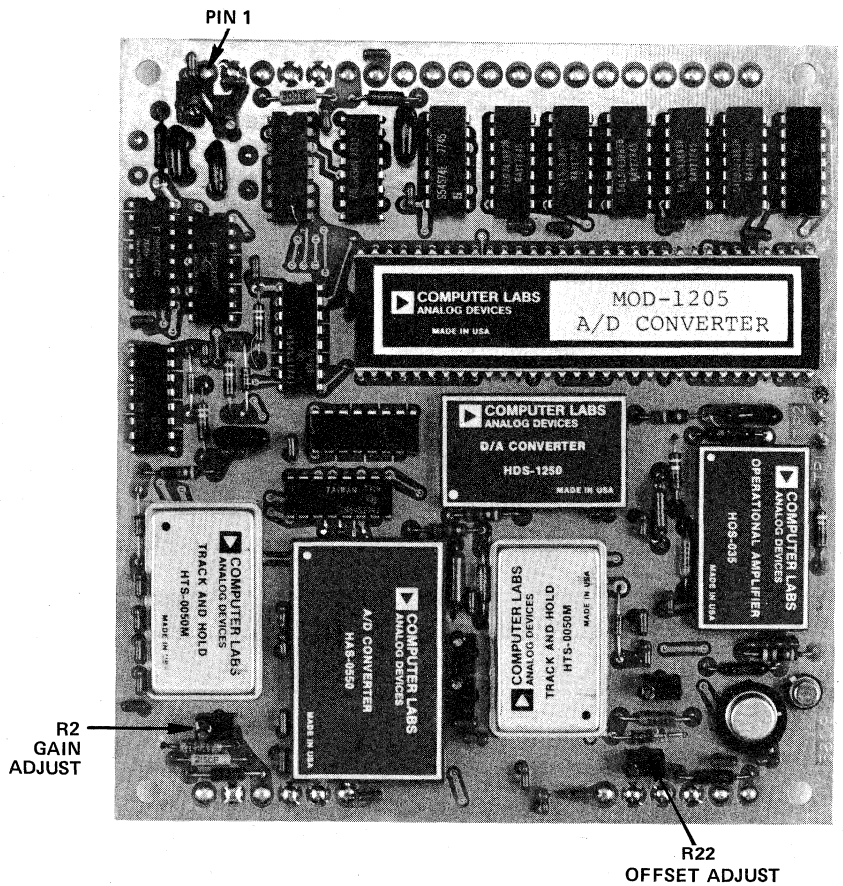
The MOD-1205 A/D is precisely calibrated at the factory before shipments and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. This procedure refers to a binary output.

Offset Adjustment

The offset is adjusted by varying potentiometer R22 with 0 volts applied to the analog input. To obtain the proper output code, observe that the digital output is changing between 1 0 0 0 0 0 0 0 0 0 0 0 and 0 1 1 1 1 1 1 1 1 1 1 1 at this adjustment level. When properly adjusted a digital code of 1 0 0 0 0 0 0 0 0 0 0 0 will represent analog input 1LSB above zero volts, and a digital code of 0 1 1 1 1 1 1 1 1 1 1 1 will represent an analog input of 1LSB below zero volts.

Gain Adjustment

The gain is adjusted by varying potentiometer R2. This adjustment is made by applying +2.0465V (FS -1 1/2LSB) to the analog input and while monitoring the digital output, adjust R2 for the output code varying between 1 1 1 1 1 1 1 1 1 1 1 0 and 1 1 1 1 1 1 1 1 1 1 1 1 (FS). If the user needs to offset the entire range of the A/D, this can be accomplished by a readjusting R22 as required. However, in this procedure, the offset should always be adjusted first.



Location of Adjustment Potentiometers

Voltage-to-Frequency & Frequency-to-Voltage Converters

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Selection Guide

Voltage-to-Frequency & Frequency-to-Voltage Converters

In this Selection Guide, V/F and F/V Converters are listed in separate tables, in order of increasing maximum frequency range. Complete descriptions, specifications, and applications information can be found in the data sheets. General information regarding VFCs and FVCs can be found in the following pages. Specifications are typical at rated supply voltage and load, and $T_A = +25^\circ C$, except where noted.

VOLTAGE-TO-FREQUENCY CONVERTERS

Max F.S. Frequency	Model	Brief Description	Page
10kHz	450	Module, 0.005% max nonlinearity, max tempcos: offset – 20μV/°C: gain – 25ppm/°C	11-15
10kHz	456	Module, 0.02% max nonlinearity, max tempcos: offset – 100μV/°C: gain – 80ppm/°C	11-15
20kHz	454	Module, 0.005% max nonlinearity, max tempcos: offset – 20μV/°C: gain – 25ppm/°C	11-15
100kHz	AD537#	Low-cost IC, 0.07% max nonlinearity, low power, max tempcos: offset – 1μV/°C (K): gain – 50ppm/°C (K)	11-7
100kHz	452	Module, 0.015% nonlinearity, max tempcos: offset – 30μV/°C: gain – 50ppm/°C	*
100kHz	458	Module, 0.01% nonlinearity, max tempcos: offset – 30μV/°C: gain – 5ppm/°C	11-19
1MHz	460	Module, 0.015% nonlinearity, max tempcos: offset – 30μV/°C: gain – 15ppm/°C	11-19

FREQUENCY-TO-VOLTAGE CONVERTERS

Max F.S. Frequency	Model	Brief Description	Page
100Hz–20kHz Adjustable	451	Module, 0.008% max nonlinearity, 30ms to full scale, max gain tempco – 50ppm/°C	11-23
1kHz–200kHz Adjustable	453	Module, 0.008% max nonlinearity, 4ms to full scale, max gain tempco – 50ppm/°C	11-23

#Monolithic chips available with guaranteed performance for precision hybrids. Chip catalog available upon request.
*Data sheet available upon request.

Orientation
Voltage-to-Frequency & Frequency-to-Voltage Converters

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters (VFC's) convert analog voltage or current levels to pulse trains or square waves in a logic-compatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external-clock synchronization is not required. V/f converters find applications in analog-to-digital converters with high resolution, long-term high-precision integrators, two-wire high-noise-immunity digital transmission, and digital voltmeters.

FREQUENCY-TO-VOLTAGE CONVERTERS

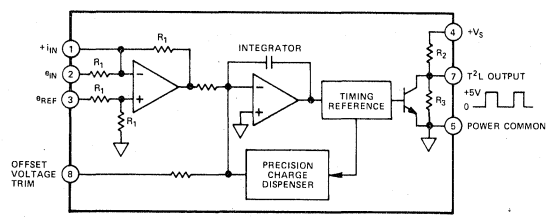
Frequency-to-voltage converters (FVC's) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain, and output offset with low linearity-error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors, and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

FACTORS IN CHOOSING VFC's AND FVC's

Voltage-to-frequency converters are available from Analog Devices in both module- and monolithic-IC- form. The output of modular types, ranging from 10kHz to 1MHz F.S., is a train of pulses of constant height and width, with very low duty cycle for small analog inputs. The output of the AD537, a monolithic integrated circuit, is unique in that its output is square-wave, an advantage in some applications. Apart from performance specifications, the tradeoffs between module and IC are as follows: modular VFCs have the advantages of completely specified performance; they do not rely on the specifications of critical external components, because the complete self-contained functional package requires no external components; trims are optional. IC's, on the other hand, have the advantages of lower cost and smaller size, and—in the case of the AD537—versatility of output and input connections, lower offset drift, flexibility of frequency range, low power, single-supply operation, low external-component count, plus built-in voltage—and temperature—references. Modules offer better linearity, lower gain drift, and higher full-scale frequencies.

The most-popular VFC designs (Figure 1) contain an integrator, which charges at a rate proportional to the value of the input signal. Each time the integrator's charge has been increased by a precisely metered increment, the threshold crossing produces a pulse of accurately known area. The pulse serves both as the output (via a buffer) and as a subtractive charge



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram — Models 458, 460 VFC's

increment to reduce the integrator's net charge. The next pulse is triggered when the net integral has again reached the threshold. The relationship between the pulse rate and the input level is linear. The AD537* operates on a somewhat different principle (Figure 2): an input current charges a capacitor between 2 threshold levels, first in one direction, then in the other, in an emitter-coupled astable multivibrator circuit. Since the time required to reach the switching threshold is inversely proportional to the analog input, the frequency is directly proportional. For constant analog input, the charging rate and the discharge rate are equal, so the output is a square wave.

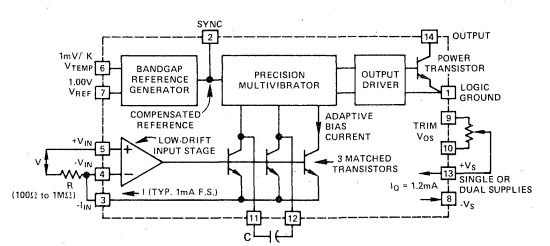
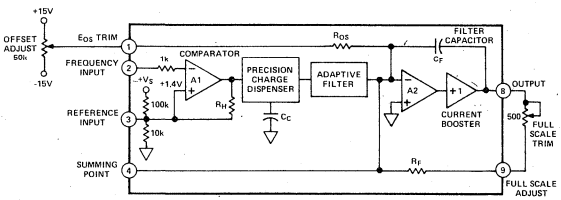


Figure 2. Block Diagram of the AD537

*A useful 20-page Application Note, "Applications of the AD537 IC Voltage-to-Frequency Converter", by Doug Grant, is available upon request.



MODEL	C_F	R_{OS}	R_H	R_F
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

Figure 3. Block Diagram – Models 451 & 453 FVC's

Frequency-to-voltage-converter modules (Figure 3) average a train of equal-area pulses that are generated internally by a precision charge dispenser, in response to each crossing of an input threshold. The analog output voltage is proportional to the sum of the pulse areas over a given period. F/V conversion can also be obtained by using the IC AD537 VFC in a phase-locked loop; the VFC's output frequency is forced by feedback to be equal to the input frequency, hence the VFC input must be proportional to frequency.

SPECIFICATIONS

The salient specifications for VFC's are *(non)linearity*, as a percentage of full-scale frequency; *frequency range*, the greater the frequency range, the greater the resolution for a given counting period; *full-scale-calibration error; gain-temperature coefficient*, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage, *input-offset temperature coefficient; overrange capability*, within rated specifications, and *step response*, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVC's, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated, and for versatility in interfacing various types of sensors directly), *hysteresis*, to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform, and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets.

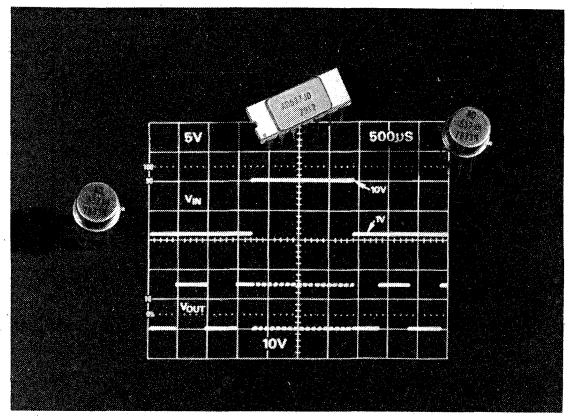
ANALOG DEVICES

Integrated Circuit Voltage to Frequency Converter

AD537

FEATURES

- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05% FS
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/K)
- F-V Applications



PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to ±30V. Linearity error is as low as ±0.05% for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, offset scales such as 0°C or 0°F can be generated.

The low drift (1μV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0 to 70°C range while the AD537S is specified for operation over the full military temperature range, -55°C to +125°C. MIL-STD-883, Level B processing is available.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ - 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristics are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 10.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.
5. Every AD537 is subjected to a 24-hour 150°C stabilization bake prior to final test to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted)

MODEL	AD537JH	AD537JD	AD537KD AD537KH	AD537SD[1] AD537SH[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 to 150kHz	*	*	*
Nonlinearity[2]				
f_{max} = 10kHz	0.15% max (0.1% typ)	*	0.07% max	**
f_{max} = 100kHz	0.25% max (0.15% typ)	*	0.1% max	**
Full Scale Calibration Error				
C = 0.01μF, I_{IN} = 1.000mA	±10% max	±7% max	±5% max	**
vs. Supply (f_{max} < 100kHz)	±0.1%/V max (0.01% typ)	*	*	*
vs. Temp. (T_{min} to T_{max})	±150ppm/°C max (50ppm typ)	*	50ppm/°C max (30ppm typ)[3]	150ppm/°C max
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to (+V_S - 4) Volts (min)	*	*	*
Dual Supply	-V_S to (+V_S - 4) Volts (min)	*	*	*
Input Bias Current				
(Either Input)	100nA	*	*	*
Input Resistance (Non-Inverting)	250MΩ	*	*	*
Input Offset Voltage				
(Trimmable in "D" Package Only)	5mV max	*	2mV max	**
vs. Supply	200μV/V max	100μV/V max	100μV/V max	**
vs. Temp. (T_{min} to T_{max})	5μV/°C	*	1μV/°C	10μV/°C max
Safe Input Voltage[4]	±V_S	*	*	*
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ±5% max	*	*	*
vs. Temp. (T_{min} to T_{max})	50ppm/°C	*	100ppm/°C max[3]	**
vs. Supply	±0.03%/V max	*	*	*
Output Resistance[5]	380Ω	*	*	*
Absolute Temperature Reference[6]				
Nominal Output Level	1.00mV/K	*	*	*
Initial Calibration @ +25°C	298mV (±5mV)	*	298mV (±5mV max)	**
Slope Error from 1.00mV/K	±0.02mV/K	*	*	*
Slope Nonlinearity	±0.1K	*	*	*
Output Resistance[5]	900Ω	*	*	*
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"				
V_{OUT} = 0.4V max, T_{min} to T_{max})	10mA min	20mA min	20mA min	10mA min
Output Leakage Current in Logic "1"				
(T_{min} to T_{max})	200nA max	*	*	2μA max
Logic Common Level Range	-V_S to (+V_S - 4) Volts	*	*	*
Rise/Fall Times (C_T = 0.01μF)				
I_{IN} = 1mA	0.2μs	*	*	*
I_{IN} = 1μA	1μs	*	*	*
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5V to 36V	*	*	*
Dual Supply	±5 to ±18V	*	*	*
Quiescent Current	1.2mA (2.5mA max)	*	*	*
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*

*Specifications same as AD537JH.
**Specifications same as AD537K.

Specifications subject to change without notice.

[1] The AD537S is available inspected and processed to the full requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request. Order part number AD537SD/883B or AD537SH/883B.

[2] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[3] Guaranteed not tested.

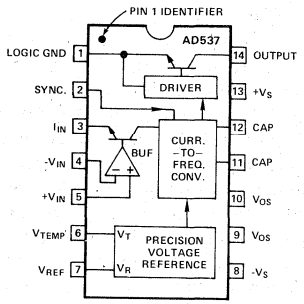
[4] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resisor (see Figure 4).

[5] Loading the 1.0 volt or 1mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the internal buffer or an external amplifier.

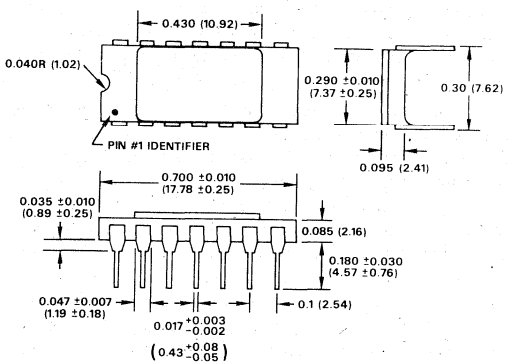
[6] Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, -55°C to +125°C for "S" model.

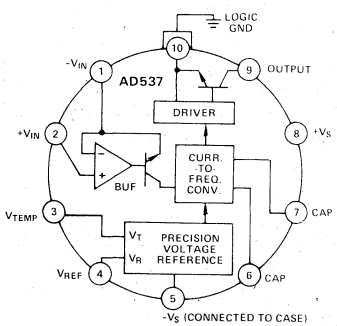
PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).



"D" PACKAGE – TO-116





"H" PACKAGE – TO-100

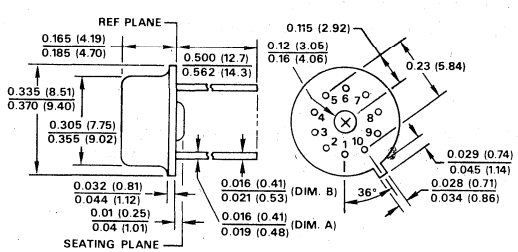


Figure 1. Block Diagram and Pin Connections

AD537 CHIPS

The AD537 is also available in passivated chip form. Consult the Chip Catalog for details. Figure 2 shows the chip metallization layout and bonding pads.

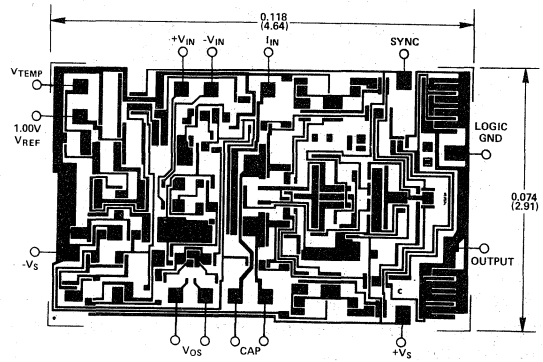


Figure 2. Chip Bonding Diagram

CIRCUIT OPERATION

A block diagram of the AD537 is shown in Figure 1. A versatile operational amplifier (BUF) serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 to 2000μA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than $-V_S$. The "SYNC" input ("D" package only) allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a band-gap circuit (this allows single-supply operation to 4.5 volts which is not possible with low T.C. zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the V_{TEMP} output which tracks absolute temperature at 1mV/K.

V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from $-V_S$ (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 3 provides a very high (250MΩ) input impedance. The input voltage is converted to the proper drive current at pin 3 by selecting a scaling resistor. The full scale current is 1mA, so, for example a 10 volt range would require a nominal 10kΩ resistor. The trim range required will depend on capacitor tolerance. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive.

As indicated by the scaling relationship in Figure 3, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. The maximum frequency is 150kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will degrade linearity. The capacitor should be wired very close to the AD537.

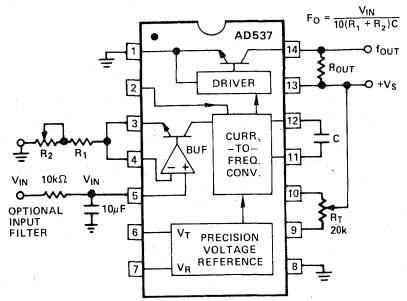


Figure 3. Standard V-F Connection for Positive Input Voltages

V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 4. This connection, unlike the buffered positive connection, is not high impedance since the 1mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 (HP5082-2811) is necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source, R_1 and R_2 are not used. Full scale calibration can be accomplished by connecting a 200kΩ pot in series with a fixed 27kΩ from pin 7 to $-V_S$ (see calibration section, below).

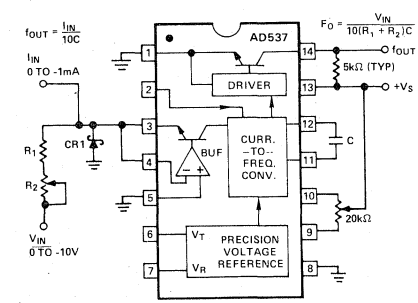


Figure 4. V-F Connections for Negative Input Voltage or Current

CALIBRATION

There are two independent adjustments: scale and offset. The first is trimmed by adjustment of the scaling resistor R and the second by the (optional) potentiometer connected to $+V_S$ and the V_{OS} pins ("D" package only). Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. *Every AD537 is automatically tested for linearity,* and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature and to ensure that the supply, source and load conditions are proper. Begin by setting the input voltage to 1/10,000 of full scale. Adjust the offset pot until the output frequency is 1/10,000 of full scale (for example 1Hz for FS of 10kHz). This is most easily accomplished using a frequency meter connected to the output. Then apply the FS input voltage and adjust the gain pot until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the input bias current of the buffer amplifier. A change of 1kΩ in R will affect the input by approximately 100μV, which is as much as 0.1% of a 100mV FS range. Therefore, it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input voltage drift after offset nulling is typically below 1μV/°C.

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 5. A resistor-potentiometer connected from the V_R output to $-V_S$ will alter the internal operating conditions in a predictable way, providing the necessary adjustment range. With the values shown, a range of ±4% is available; a larger range can be attained by reducing R1. This technique does not degrade the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

Unless it is required to set the input node at exactly ground potential, no offset adjustment is needed. The capacitor C is selected to be 5% below the nominal value; with R2 in its mid-position the output frequency is given by

$$f = \frac{I}{10.5 \times C}$$

where f is in kHz, I is in mA and C is in μF. For example, for a FS frequency of 10kHz at a FS input of 1mA, C = 9500pF. Calibration is effected by applying the full-scale input and adjusting R2 for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative-voltage mode. The scaling relationship is then

$$f = \frac{V}{R_{exact}} \cdot \frac{1}{10.5\ C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of R2.

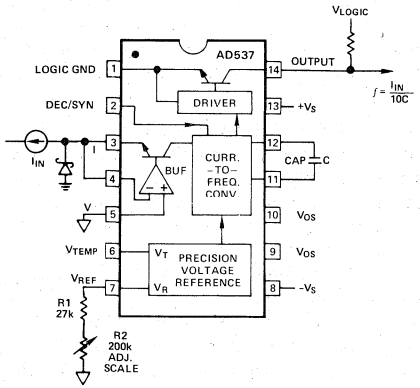


Figure 5. Scale Adjustment for Current Inputs

INPUT PROTECTION

The AD537 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions.

The $-V_{IN}$, $+V_{IN}$ and I_{IN} pins should not be driven more than 300mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below $-V_S$" inputs by a Schottky diode, CR1 (HP5082-2811) as shown in Figure 4. It is also desirable not to drive $+V_{IN}$, $-V_{IN}$ and I_{IN} above $+V_S$. In operation, the converter will become very nonlinear for inputs above ($+V_S$ -3.5V). Control currents above 2mA will also cause nonlinearity.

The 80dB dynamic range of the AD537 guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, the -80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter. For a FS of 10kHz a single-pole filter with a time-constant of 100ms (Figure 3) will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA (1mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005μF (or larger) capacitor to pin 13 ($+V_S$). This minimizes the possibility that the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package since the SYNC function is not brought out to a package pin and is thus not susceptible to pickup.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD537.

A decoupling capacitor may also be useful from $+V_S$ to SYNC in those applications where very low cycle-to-cycle period variation (jitter) is demanded. By placing a capacitor across $+V_S$ and SYNC this noise is reduced. On the 10kHz FS range, a 6.8μF capacitor reduces the jitter to one in 20,000 which is adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

OPERATION WITH NON-ZERO TC

The good temperature stability of the AD537 can only be realized using stable timing components. However, compensation for timing components which yield a net negative full-scale frequency TC can be easily introduced by adding a resistor between the +1mV/K output and $-V_S$. The value should be selected from the curve given in Figure 6. Over this range of compensation the scale factor is only slightly affected; the error is about +0.03%/ppm/K in frequency (e.g., 150ppm shift would change the scale factor 4.5%).

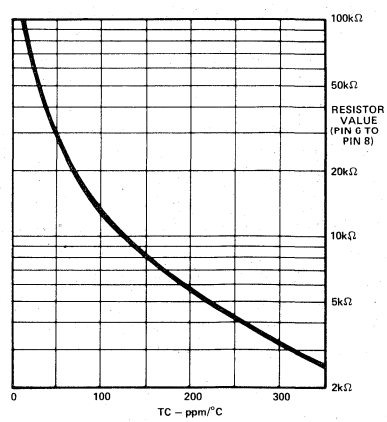


Figure 6. Positive T.C. Induced Versus Correction Resistance

NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full scale frequency and the mode of operation. The AD537 operates best at a 10kHz full scale frequency with a negative voltage input; the linearity is typically within ±0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the specifications. The shape of a typical linearity plot is given in Figure 7.

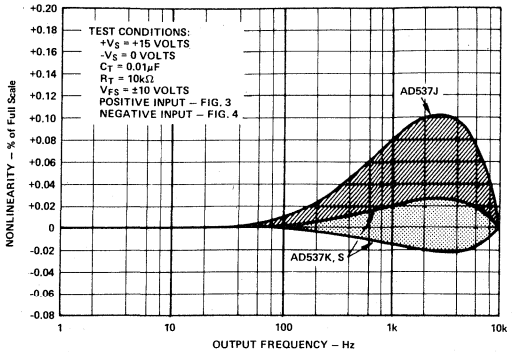


Figure 7a. Typical Nonlinearity Error Envelopes with 10kHz F.S. Output

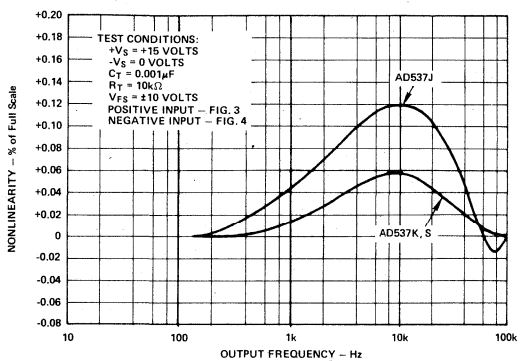
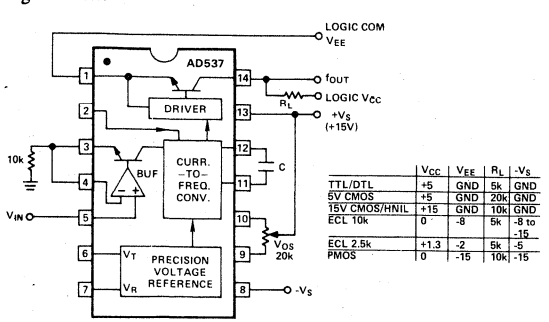


Figure 7b. Typical Nonlinearity Error with 100kHz F.S. Output

OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage allows easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$. The open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can supply up to 20mA (10mA for "H" package) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25mA; it can handle this limit indefinitely without damaging the device.

Figure 8 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The values for the logic common voltage, pull-up resistor, positive logic level, and $-V_S$ supply are given in the accompanying chart for several logic forms.



	VCC	VEE	RL	-VS
TTL/DTL	+5	GND	5k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/HNIL	+15	GND	10k	GND
ECL 10k	0	-8	5k	-8 to -15
ECL 2.5k	+1.3	-2	5k	-5
PMOS	0	-15	10k	-15

Figure 8. Interfacing Standard Logic Families

APPLICATIONS

The diagrams and descriptions of the following applications are provided to stimulate the discerning engineer with alternative circuit design ideas. "Applications of the AD537 IC Voltage-to-Frequency Converter", available from Analog Devices on request, covers a wider range of topics and concepts in data conversion and data transmission using voltage-to-frequency converters.

TRUE TWO-WIRE DATA TRANSMISSION

Figure 9 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

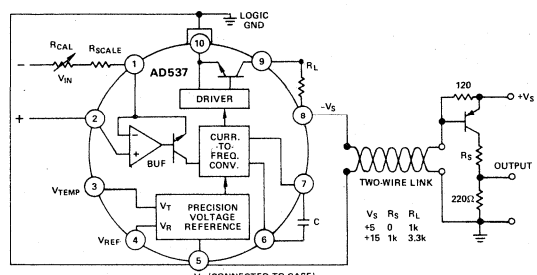


Figure 9. True Two-Wire Operation

F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, responding in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 10 shows a connection using a low-power TTL quad open-collector nand gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40μs. The output voltage is one volt for a 10kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the V_{OS} trimmer to mid-scale. Apply a 10kHz input frequency and trim the 2kΩ potentiometer for 1.00 volts out. Then apply a 10Hz waveform and trim the V_{OS} for 1mV out. Finally, retrim the full scale output at 10kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

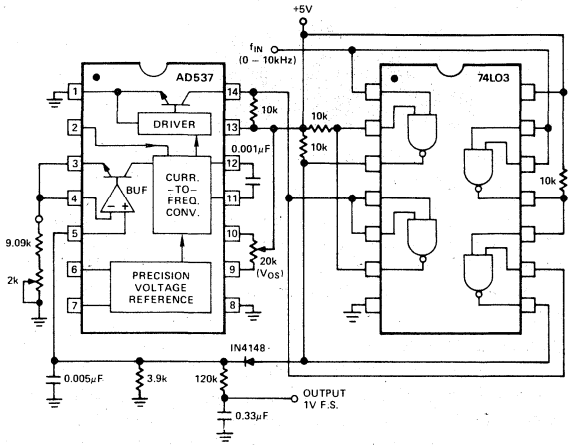


Figure 10. 10kHz F-V Converter

TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

An absolute temperature (° Kelvin) -to-frequency converter is very easily accomplished, as shown in Figure 11. The 1mV per °K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298μA at +25°C (298°K). Use of a 1000pF capacitor results in a corresponding frequency of 2.98kHz. Setting the single 2kΩ trimmer for the correct frequency at a well-defined temperature near +25°C will normally result in an accuracy of ±2°C from -55°C to +125°C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

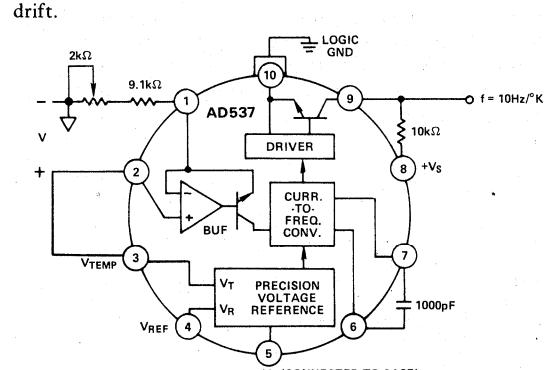


Figure 11. Absolute Temperature to Frequency Converter

OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a scheme is shown by the Celsius-to-frequency converter in Figure 12. Corresponding component values for a Fahrenheit-to-frequency converter which give 10Hz/°F are given in parentheses.

A simple calibration procedure which will provide ±2°C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500Ω trimmer to give 250Hz at +25°C.

High accuracy calibration procedure:

1. Measure room temperature in °K.
2. Measure temperature output at pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$\text{Offset Voltage (mV)} = \frac{V_{TEMP}\ \text{(pin 6) (mV)}}{\text{Room temp (°K)}} \times 273.2$$

4. Temporarily disconnect 49Ω resistor (or 500Ω pot) and trim 2kΩ pot to give the offset voltage at the indicated node. Reconnect 49Ω resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25°C = 250Hz).
   Adjustment for °F or any other scale is analogous.

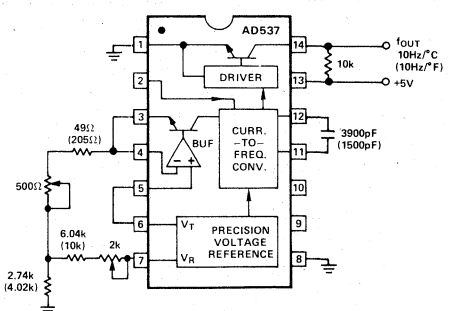


Figure 12. Offset Temperature Scale Converters-Centigrade and (Fahrenheit) to Frequency

SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 of the DIP package can be used to synchronize a free running AD537 to a master oscillator, either at a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 13. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to +V_S will stop the oscillator, and the output will go high (output NPN off).

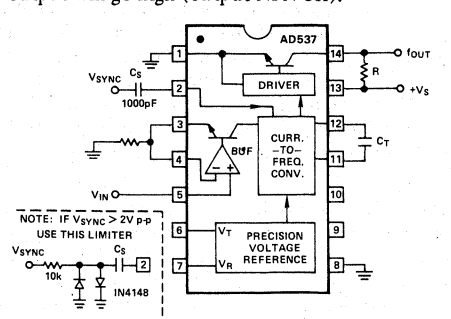


Figure 13. Connection for Synchronous Operation

Figure 14 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square wave; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1-2%.

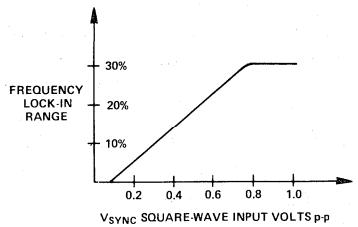


Figure 14. Maximum Frequency Lock-In Range Versus Sync. Signal

LINEAR PHASE LOCKED LOOP

The phase-locked-loop F/V circuit described earlier operates from an essentially noise-free binary input. PLL's are also used to extract frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 15, the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It can be shown that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

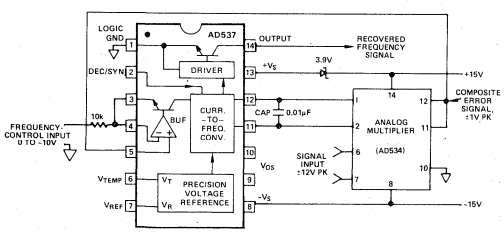


Figure 15. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 16 which shows the response to an input of 1V rms 1kHz sinusoid plus 1V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4V in order to keep the voltages at pins 11 and 12 within the common-mode range of the AD534.

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

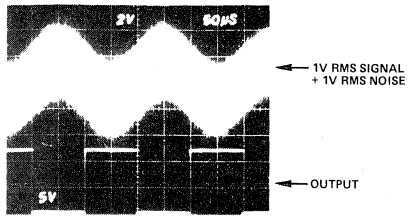


Figure 16. Performance of AD537 Linear Phase-Locked Loop

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to pin 5, a high-resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6V.

TRANSDUCER INTERFACE

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly (unlike many V-F converters which require signal pre-conditioning). The 1.00V stable reference output is also useful in interfacing situations, and the high input resistance allows non-loading interfacing from a source of varying resistance, such as the slider of a potentiometer.

THERMOCOUPLE INPUT

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 to 53.14mV over the temperature range 0 to +700°C with a slope of 80.678μV/degree over most of its range and some nonlinearity over the range 0 to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100ms gate width. Thus, the V-F converter must deliver an output of 7kHz for an input of 53.14mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, Analog Devices' Nonlinear Circuits Handbook, pp92-97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 17 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature-voltage curve back to 0°C shows that an offset of -3.34mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00V output of the AD537. To adjust the scale, the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400°C to 700°C.

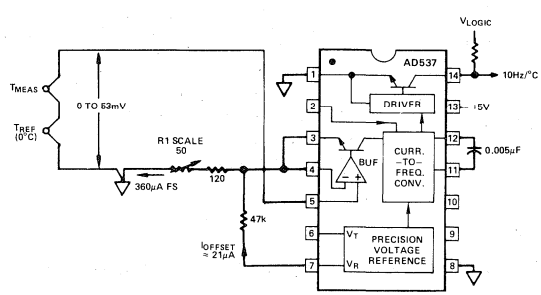


Figure 17. Thermocouple Interface with First-Order Linearization

ANALOG DEVICES

Low-Cost, High Performance, 10/20kHz Voltage to Frequency Converters

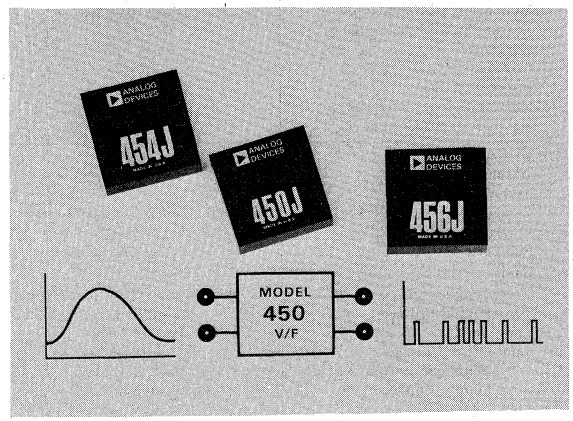
MODELS 450, 454, 456

FEATURES

- Low Cost
- Low Nonlinearity: ±50ppm max; Model 450K
- High Stability: ±25ppm/°C max; Model 450K
- Versatility: Voltage or Current Inputs; Model 454J/K
  - 10V or 20V Full Scale Inputs
  - Bipolar Inputs; Model 454J/K
- Wide Dynamic Range: >86dB; Model 454J/K
- Meet MIL-STD-202E Environmental Testing
- TTL/DTL or CMOS/HNIL Compatible Output

APPLICATIONS

- Long Term Precision Integrator
- Ratiometric Measurements
- High CMV Analog Isolator
- A/D Converter with 13-Bit Accuracy
- 2 Wire High Noise Immunity Digital Transmission



GENERAL DESCRIPTION

Models 450, 454 and 456 comprise a new family of modular voltage to frequency converters that provide exceptional linearity and temperature stability over a wide input signal dynamic range. Available in two convenient full scale frequency ranges of 10kHz or 20kHz, these new low cost models can be easily applied to perform ±0.01% analog measurements while directly interfacing with digital circuits.

WHERE TO USE MODELS 450, 454 AND 456

Pin compatible with existing popular models, these new designs offer economical solutions to a range of demanding applications; in Chemical Analysis and Gas Chomatography – as long-term precision integrators; in Process Control and Remote Data Acquisition Systems – two wire data transmission over long distances; in 3½ digit DVM's – as low-cost A/D converters featuring monotonic 13-bit performance and no missing codes; in Blood Analysis – accurate ratiometric measurements over wide dynamic range; in Medical Instruments – isolation using single low cost optical isolator; in Test Instrumentation – as low cost programmable square wave generators.

MODEL SELECTION GUIDE

These compact modules are available in six versions with performance features aimed at meeting key application requirements:

Economy, 10kHz: Model 456 offers the lowest cost for applications requiring 0.1% (10-bit) accuracy. Available in two selection grades, model 456J has 0.03% max nonlinearity with 120ppm/°C max gain drift; model 456K offers 0.02% max nonlinearity and 80ppm/°C gain drift.

High Performance, 10kHz: For all general purpose applications, model 450 should be considered. Nonlinearity is 0.01% max (450J) and 0.005% max (450K) with full scale gain drift guaranteed at 50ppm/°C max (450J) and 25ppm/°C max (450K). Model 450K can achieve 0.01% (13-bit) accuracy over the 1mV to +15V signal range.

Versatility: Model 454 accepts 0 to +20V or 0 to 0.67mA inputs and can be operated with bipolar signals up to ±10V. Nonlinearity is 0.01% max (454J) and 0.005% max (454K); gain drift is 50ppm/°C max (454J) and 25ppm/°C max (454K).

DESIGN APPROACH – PRECISION CHARGE BALANCE

All models incorporate a superior charge balance technique that results in high linearity and temperature stability. Linearity is maintained for inputs below 1mV and operation is free of latch-up.

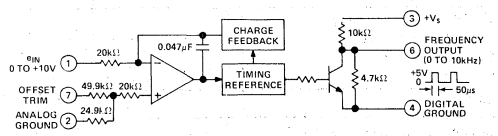


Figure 1. Block Diagram – Models 450 and 456

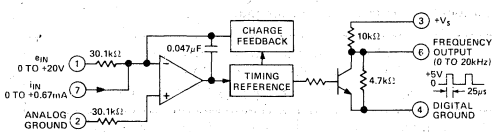


Figure 2. Block Diagram – Model 454

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	ECONOMY 10kHz 456 J	ECONOMY 10kHz 456 K	HIGH PERFORMANCE 10kHz 450 J	HIGH PERFORMANCE 10kHz 450 K	VERSATILE 20kHz 454 J	VERSATILE 20kHz 454 K
TRANSFER FUNCTION						
Voltage Input	$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$		$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$		$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$	
Current Input	–		–		$f_{OUT} = (3 \times 10^4 \frac{Hz}{mA}) i_{IN}$	
ANALOG INPUT						
Voltage Signal Range (e_{IN})	0 to +10V max		0 to +10V max		0 to +20V max	
Current Signal Range (i_{IN})	–		–		0 to 0.67mA min	
Overrange	50% min		50% min		10% min	
Impedance (e_{IN})	20kΩ		20kΩ		30kΩ	
Impedance (i_{IN})	–		–		0Ω	
Max Safe Input Voltage (e_{IN})	+25V, $-V_S$		+25V, $-V_S$		+25V, $-V_S$	
Max Safe Input Current (i_{IN})	–		–		+1mA	
ACCURACY						
Warm-Up Time	1 minute		1 minute		1 minute	
Nonlinearity						
e_{IN} = +1mV to +15V	±0.03% max	±0.02% max	±0.01% max	±0.005% max	–	
e_{IN} = +1mV to +22V	–		–		±0.01% max	±0.005% max
Full Scale Error[1]	(+½, +1½)% max		(+½, +1½)% max		(+½, +1½)% max	
Gain						
vs. Temperature (0 to +70°C)	±120ppm/°C max	±80ppm/°C max	±50ppm/°C max	±25ppm/°C max	±50ppm/°C max	±25ppm/°C max
vs. Supply Voltage	±400ppm/%		±200ppm/% max		±200ppm/% max	
vs. Time	±150ppm/day		±100ppm/day		±100ppm/day	
Input Offset Voltage[1]	±10mV		±5mV max		±5mV max	
vs. Temperature (0 to +70°C)	±100µV/°C max		±50µV/°C	±20µV/°C max	±50µV/°C	±20µV/°C max
vs. Supply Voltage	±10ppm/%		±10ppm/% max		±10ppm/% max	
vs. Time	±20µV/day		±10µV/day		±10µV/day	
RESPONSE						
Settling Time for +10V Step Input	120µs		120µs		120µs	
Overload Recovery Time	15ms		15ms		22ms	
OUTPUT[2]						
Waveform	train of TTL/DTL compatible pulses		train of TTL/DTL compatible pulses		train of TTL/DTL compatible pulses	
Pulse Width	50µs		50µs		25µs	
Rise/Fall Time	200ns/100ns		200ns/100ns		200ns/100ns	
Pulse Polarity	positive		positive		positive	
Logic "1" (High) Level	+2.4V min		+2.4V min		+2.4V min	
Logic "0" (Low) Level	+0.4V max		+0.4V max		+0.4V max	
Capacitive Loading	1000pF max		1000pF max		1000pF max	
Fan Out Loading	10 TTL loads min		10 TTL loads min		10 TTL loads min	
Impedance	3.3kΩ		3.3kΩ		3.3kΩ	
POWER SUPPLY[3]						
Voltage, Rated Performance	±15V dc		±15V dc		±15V dc	
Voltage, Operating	±(12 to 18)V dc		±(12 to 18)V dc		±(12 to 18)V dc	
Current, Quiescent	(+15, -9)mA		(+15, -9)mA		(+15, -9)mA	
TEMPERATURE RANGE						
Rated Performance	0 to +70°C		0 to +70°C		0 to +70°C	
Operating	-25°C to +80°C		-25°C to +80°C		-25°C to +80°C	
Storage	-55°C to +85°C		-55°C to +85°C		-55°C to +85°C	
CASE SIZE	1.5" x 1.5" x 0.4"		1.5" x 1.5" x 0.4"		1.5" x 1.5" x 0.4"	

[1] Adjustable to zero; refer to Adjustment Procedure.
[2] Protected for continuous short-circuit to ground. CAUTION: DO NOT SHORT OUTPUT TO -15V SUPPLY.
[3] Recommended ADI power supply: model 904, ±15V @ 50mA.
Specifications subject to change without notice.

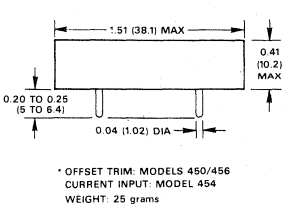
All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

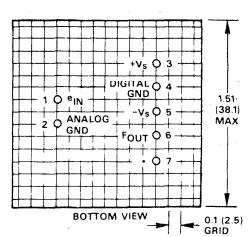
TABLE 1. Environmental Specifications

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



* OFFSET TRIM: MODELS 450/456
CURRENT INPUT: MODEL 454
WEIGHT: 25 grams



MATING SOCKET AC1047

VOLTAGE TO FREQUENCY OPERATION

Models 450, 454 and 456 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracts the input signal responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to low cost digital processing circuits.

Dynamic Range: Models 450 and 456 accept unipolar, single ended input signals from 0V to +10V with 50% minimum overrange. The corresponding output frequency is dc to 10kHz as shown in Figure 3. Model 454 is designed for either bipolar or unipolar single ended input signals. It accepts 0V to +20V or 0mA to 0.67mA input signals directly with 10% min overrange; the corresponding output frequency is dc to 20kHz.

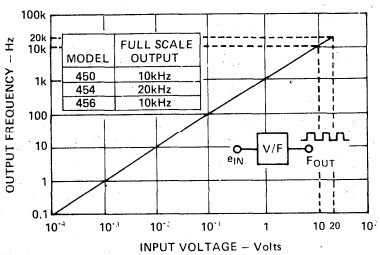


Figure 3. Voltage-to-Frequency Transfer Curve

ADJUSTMENT PROCEDURE

All models may be used directly with no external trim potentiometers required. Overall accuracy and dynamic range may be improved by using two optional trim adjustments as shown in Figures 6 and 7; FULL SCALE and OFFSET adjust. Low temperature coefficient trims must be used to maintain the drift specifications of the V/F model. The T.C. of the trim pot will add to the FULL SCALE DRIFT for each model as follows:

$$\text{FULL SCALE DRIFT CONTRIBUTION} = \left[\frac{R_{ext}}{R_{ext} + 20k\Omega^*}\right] \times \left[\text{T.C. } R_{ext}\right] /^\circ C$$

*30kΩ, model 454

Calibration Procedure: Allow a five minute warm-up after initial power turn on. Using a precision, stable voltage source, set the input voltage, e_{IN}, to +1.00mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 1 second (1Hz). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse interval of 100μs (10kHz). The V/F may now be used without further adjustment.

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity is specified as a % of full scale input: 10V for models 450 and 456; 20V for model 454 – and is guaranteed for each model over the specified input range: 0.005% max, models 450K and 454K; 0.01% max, models 450J and 454J; 0.03% max, model 456J and 0.02% max, model 456K. Typical nonlinearity performance is illustrated for model 450J in Figure 4. Below 1mV input, nonlinearity error remains within the specified limits, but is masked by zero offset stability, input noise and adjustment accuracy.

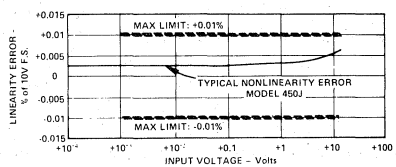


Figure 4. Model 450J: Nonlinearity Error Versus Input Signal

Gain Temperature Stability: Gain drift is specified in ppm of input signal and is guaranteed for each model over the 0 to +70°C temperature range. The curves of Figure 5 illustrate the drift limits for all models; typical performance is half the guaranteed limits.

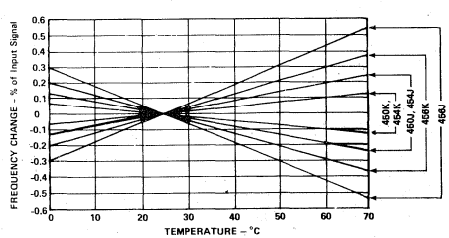


Figure 5. Gain Frequency Drift (Worst Case)

V/F INTERCONNECTION

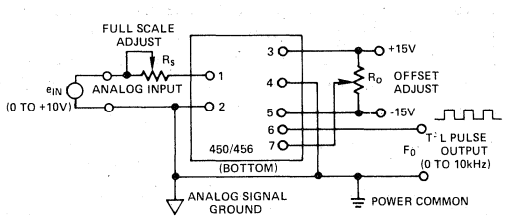


Figure 6. Models 450/456

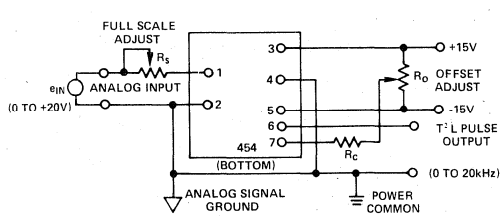


Figure 7. Model 454

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE OUTPUT FREQUENCY ADJUSTMENTS

R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_C = 20MΩ

CAUTION: DO NOT SHORT OUTPUT TO -15V

OUTPUT FREQUENCY SCALING

Lowering Full Scale Frequency: The full scale frequency of a V/F converter can be reduced by three techniques; (1) adding a series trim potentiometer, such as 10kΩ, with the input; (2) adding a voltage divider network at the input; or (3) adding a digital divider at the output. Both input techniques (1) and (2), degrade the full scale gain drift by the added T.C. of the input resistors. By using a frequency divider connected to the V/F output, full scale frequency can be conveniently reduced without degradation of the converter's full scale drift performance. By adding successive frequency dividers, as illustrated in Figure 8, a precision, low-cost, voltage controlled square wave generator can be designed.

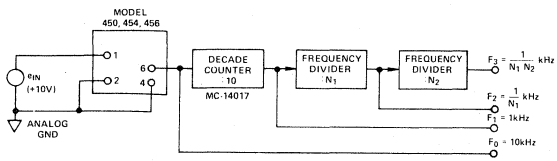
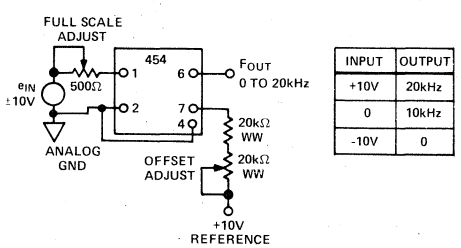


Figure 8. Voltage Controlled Square Wave Generator Using Digital Dividers and V/F Converter

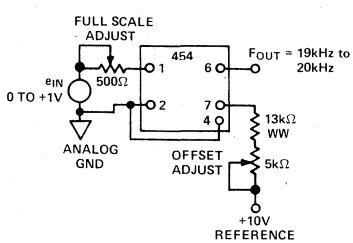
Offsetting Full Scale Frequency; Model 454: The summing input terminal of model 454 (i_{IN} terminal) may be used to conveniently offset the output frequency to permit bipolar input signals up to ±10V, as well as improve the dynamic response to low level input signals. As shown in Figure 9, a current is fed through an external resistor from a voltage reference to the current terminal. A low cost precision +10V voltage reference, such as ADI model AD2700, is recommended to retain the stability and accuracy of model 454.

As illustrated in Figure 10, the output may also be scaled up so that low amplitude signals – (i.e. e_{IN} = 1V – will give full scale output frequency – (e_o = 20kHz). The step response for a 1 volt input change improves to only 50μs, compared to 1ms before offsetting.



INPUT	OUTPUT
+10V	20kHz
0	10kHz
-10V	0

Figure 9. Offsetting Model 454 Output for Bipolar Inputs



INPUT	OUTPUT
+1V	20kHz
0	19kHz

Figure 10. Offsetting Model 454 Output for Improved Dynamic Response

SQUARE WAVE OUTPUT

Using a type D flip-flop connected to the output of the V/F converter offers a simple low cost technique to obtain a voltage controlled, variable frequency, square wave signal; see Figure 11. Using model 454 with current offsetting, a 10kHz full scale square wave output can be achieved with 10V input signal.

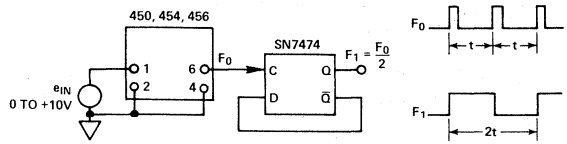


Figure 11. Square Wave Output Using Type D Flip-Flop

DRIVING HIGH NOISE IMMUNITY LOGIC

Adding a 680Ω resistor from the output terminal to the +15V supply provides 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic (see Figure 12).

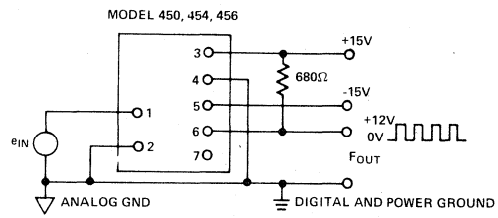


Figure 12. Driving High Noise Immunity Logic and CMOS

DYNAMIC RESPONSE

Overload Recovery: All models can safely withstand input overloads up to +25V, $-V_S$. Overload recovery time will depend on input polarity. Worst case overload recovery occurs following a sustained negative overload. Following removal of the overload, the input must be driven positive to restore normal operation. The recovery time depends upon the input voltage applied after removal of the overload and is given by:

$$\text{Model 450/456: } t_r \text{ (ms)} = \frac{15}{E \text{ (Volts)}}$$

$$\text{Model 454: } t_r \text{ (ms)} = \frac{22}{E \text{ (Volts)}}$$

where E is the voltage applied following overload. Recovery from positive overloads up to the max safe input occurs essentially instantaneously after removal of the overload condition.

Step Response: The output settling time for step input changes is a function of the final output frequency. Settling time is specified as 20μs plus 2 output pulses of the new frequency. For a 10V step input, the settling time will be 120μs. Figure 13 shows typical timing relationships between input and output for input voltages of 2V and 10V.

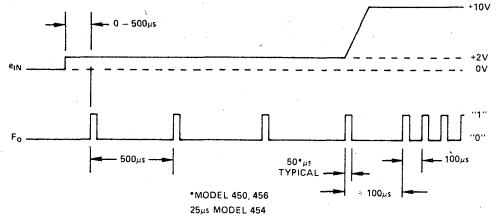


Figure 13. Timing Waveforms; Input/Output

ANALOG DEVICES

High Accuracy, 100kHz and 1MHz Voltage to Frequency Converters

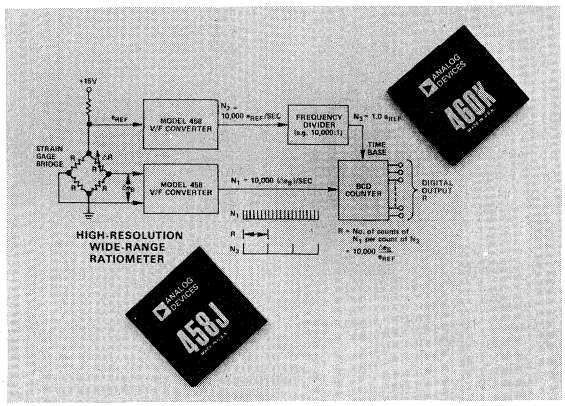
MODELS 458 and 460

FEATURES

High Stability: 5ppm/°C max, Model 458L
15ppm/°C max, Model 460L
Low Nonlinearity: 100ppm max, Model 458
150ppm max, Model 460
Versatility: Differential Input Stage
Voltage and Current Inputs
Floating Inputs: ±10V CMV
Wide Dynamic Range: 6 Decades, Model 460
TTL/DTL or CMOS/HNIL Compatible Output

APPLICATIONS

Fast Analog-to-Digital Converter
High Resolution Optical Data Link
Ratiometric Measurements
2-Wire High Noise Immunity Digital Transmission
Long Term Precision Integrator



GENERAL DESCRIPTION

Models 458 and 460 are high performance, differential input, voltage to frequency modular converters designed for analog to digital applications requiring accuracy and fast data conversion. Model 458 offers a 100kHz full scale frequency, guaranteed nonlinearity of ±0.01% maximum over five decades (1Hz to 100kHz) of operation and guaranteed low maximum gain drift in three model selections; model 458L: 5ppm/°C max; model 458K: 10ppm/°C max; and model 458J: 20ppm/°C max. Model 460 offers a 1MHz full scale frequency, guaranteed maximum nonlinearity of ±0.015% over six decades (1Hz to 1MHz) of operation and guaranteed low maximum gain drift in three selections; model 460L: 15ppm/°C max; model 460K: 25ppm/°C max; and model 460J: 50ppm/°C max. Model 460L is the industry's first 1MHz V/F converter to offer 15ppm/°C maximum gain drift.

The differential input stage of models 458 and 460 provide the versatility of either direct interface to off-ground 0 to +11V input signals with common mode voltages (CMV) to ±10V, as well as ground referenced positive, 0 to +11V or negative, 0 to −11V signals. Both models also accept positive current signals: 0 to +½mA, model 458; 0 to +1mA, model 460 for current to frequency (I/F) applications.

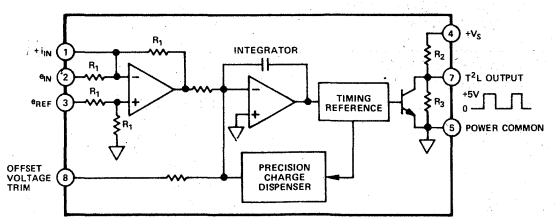
The rated performance of both models 458 and 460 is achieved without the need for external components or adjustments. Optional adjustments are available for trimming full scale frequency and the input offset voltage.

WHERE TO USE MODELS 458 AND 460

The combination of low gain drift, low nonlinearity and the versatility of a differential input with both high speed (100kHz/1MHz) models, offer excellent solutions to a wide variety of demanding applications; in high speed remote data acquisition systems — two wire data transmission over long wires; in 5½ digit DVMs — featuring high resolution A/D conversion, monotonic performance, no missing codes and high noise rejection; in strain gage bridge weighing applications — accurate ratiometric measurements over wide dynamic range.

DESIGN APPROACH - PRECISION CHARGE BALANCE

Models 458 and 460 incorporate a superior charge balance design that result in high linearity and temperature stability - see Figure 1. Both models accept unipolar, single-ended voltage or current input signals directly. By offsetting the input using the current terminal, models 458 and 460 will accept bipolar input voltages up to ±5V.



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram - Models 458, 460

SPECIFICATIONS (typical @ +25°C and V_S = ±15VDC unless otherwise noted)

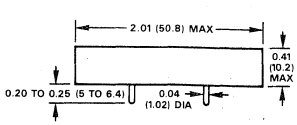
MODEL	100kHz Full Scale 458 J	K	L	1MHz Full Scale 460 J	K	L
TRANSFER FUNCTION						
Voltage Input	$f_{OUT} = (10^4 Hz/V)\ e_{IN}$			$f_{OUT} = (10^5 Hz/V)\ e_{IN}$		
Current Input	$f_{OUT} = (2 \times 10^5 Hz/mA)\ i_{IN}$			$f_{OUT} = (10^6 Hz/mA)\ i_{IN}$		
ANALOG INPUT						
Configuration	Differential			Differential		
Voltage Signal Range						
e_{IN} Terminal (e_{REF} = 0)	0 to +10V dc min			0 to +10V dc min		
e_{REF} Terminal (e_{IN} = 0)	0 to -10V dc min			0 to -10V dc min		
Differential ($e_{IN} - e_{REF}$)	0 to +10V dc min			0 to +10V dc min		
Overrange	+10% min			+10% min		
Current Signal Range (i_{IN})	0 to +0.5mA min			0 to +1mA min		
Common Mode Voltage	±10V			±10V		
Common Mode Rejection	40dB			40dB		
Impedance, e_{IN} Terminal	20kΩ			10kΩ		
e_{REF} Terminal	40kΩ			20kΩ		
i_{IN} Terminal	0Ω			0Ω		
Max Safe Input	$\pm V_S$			$\pm V_S$		
ACCURACY						
Warm Up Time	5 Seconds to 0.01%			2 Minutes to 0.02%		
Nonlinearity, e_{IN} = +0.1mV to +11V	±0.01% of Full Scale, max			±0.015% of Full Scale, max		
e_{IN} = -0.1mV to -11V	±0.01% of Full Scale			±0.015% of Full Scale		
Full Scale Error[1]	+0.1% to +2%, max			+0.1% to +2%, max		
Gain vs. Temperature (0 to +70°C)	±20ppm/°C max	±10ppm/°C max	±5ppm/°C max	±50ppm/°C max	±25ppm/°C max	±15ppm/°C max
vs. Supply Voltage	±15ppm/%			±25ppm/%		
vs. Time	±10ppm/day			±10ppm/day		
Input Offset Voltage[2]	±10mV max			±10mV max		
vs. Temperature (0 to +70°C)	±30μV/°C max			±30μV/°C max		
vs. Supply Voltage	±10μV/%			±10μV/%		
vs. Time	±20ppm/day			±10ppm/day		
RESPONSE						
Settling Time, ±0.01% +10V Step	3 Output Pulses Plus 2μs			2 Output Pulses Plus 2μs		
Overload Recovery Time	10ms			1ms		
FREQUENCY OUTPUT[3]						
Waveform	TTL/DTL Compatible Pulses			TTL/DTL Compatible Pulses		
Pulse Width	5μs			500ns		
Rise and Fall Time	300ns/50ns			60ns/50ns		
Pulse Polarity	Positive			Positive		
Logic "1" (High) Level	+2.4V min			+2.4V min		
Logic "0" (Low) Level	+0.4V max			+0.4V max		
Capacitive Loading	500pF max			200pF max		
Fan Out Loading	10 TTL Loads min			10 TTL Loads min		
Impedance	3kΩ (High State)			670Ω (High State)		
POWER SUPPLY[4]						
Voltage, Rated Performance	±15V dc			±15V dc		
Voltage, Operating	±(13 to 18)V dc			±(13 to 18)V dc		
Current, Quiescent	(+25, -8)mA			(+25, -8)mA		
TEMPERATURE RANGE						
Rated Performance	0 to +70°C			0 to +70°C		
Operating	-25°C to +85°C			-25°C to +85°C		
Storage	-55°C to +125°C			-55°C to +125°C		
MECHANICAL						
Case Size	2" x 2" x 0.4"			2" x 2" x 0.4"		
Weight	45 Grams			45 Grams		
Mating Socket	AC1016			AC1016		

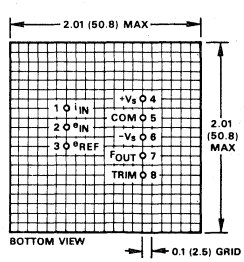
[1] Adjustable to zero using 500Ω potentiometer.
[2] Adjustable to zero using 50kΩ potentiometer.
[3] Protected for continuous short-circuits to ground and momentary (less than 1 sec) shorts to the $+V_S$ supply. Output is not protected for shorts to the $-V_S$ supply.
[4] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





MATING SOCKET: AC1016

VOLTAGE TO FREQUENCY OPERATION

Models 458 and 460 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to digital processing circuits. Adding a resistor from the output terminal, pin 7, to the +15V supply (1.2kΩ model 458; 820Ω model 460), shifts the output swing from 0 to +5V to 0 to +12V, providing a 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic.

BASIC V/F HOOK-UP AND OPTIONAL TRIMS

Models 458 and 460 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figures 2, 3 and 4 below illustrate the basic wiring connections for either V/F converter model. Using the basic hookup without trims, full scale (e_{IN} = 10V) accuracy is +0.1% to +2% and the input offset voltage is ±10mV max. The full scale and input offset voltage errors can be eliminated by using the FINE TRIM PROCEDURE.

FINE TRIM PROCEDURE

Connect the optional trims as shown in Figure 2, 3 or 4 and allow a five minute warm-up after initial power turn-on.

V/F INTERCONNECTIONS

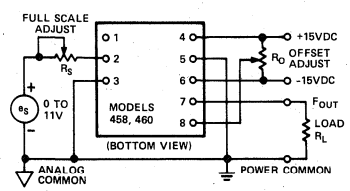


Figure 2. Positive Input Signal

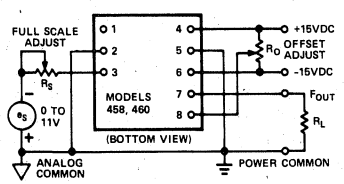


Figure 3. Negative Input Signal

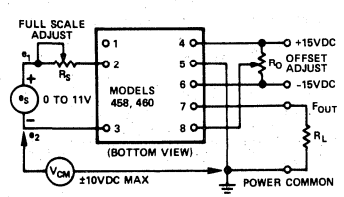


Figure 4. Floating Input Signal

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE FREQUENCY ADJUSTMENTS

R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, < 50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, < 50ppm/°C or equivalent)

CAUTION: DO NOT SHORT OUTPUT TERMINAL TO -15V

Using a precision, stable voltage source, set the input voltage, e_S, to 10mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 0.1 sec (model 458) or 0.01 sec (model 460). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse frequency of 100kHz (model 458), or 1MHz (model 460). The V/F converter may now be used without further adjustment.

DIFFERENTIAL INPUT

The e_{IN} and e_{REF} input terminals represent a true differential input capable of accepting a signal from a strain gage bridge, a balanced line, or a signal source sitting at a common mode voltage. The differential input eliminates the need for a differential amplifier to handle these signals.

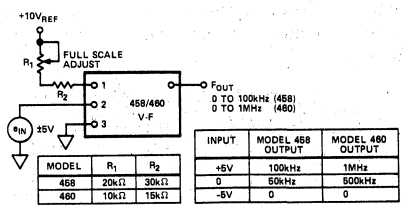
To apply the 458 or 460 voltage inputs differentially, the e_{IN} pin must always be positive with respect to the e_{REF} pin as shown in Figure 4. The differential signal source may be completely floating with common mode voltages up to ±10V max. For differential inputs the output frequency is:

$$F_{OUT} = \left[\underbrace{(e_1 - e_2)}_{\text{INPUT SIGNAL}} + \underbrace{\left(\frac{e_1 + e_2}{2}\right) \times \left(\frac{1}{CMR}\right)}_{\text{CMR ERROR}} \right] K_g$$

$K_g = 10^4$ Hz/V; model 458
10^5 Hz/V; model 460

OFFSETTING INPUT FOR BIPOLAR INPUTS

The input summing terminal, $+i_{IN}$, may be used to improve dynamic response as well as scale the output frequency to directly convert bipolar input voltages. An offset current is fed through an external resistor from a stable voltage reference. As shown in Figure 5, input voltages of ±5V min can be converted directly.

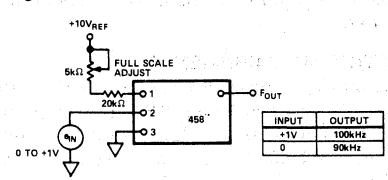


MODEL	R_1	R_2
458	20kΩ	30kΩ
460	10kΩ	15kΩ

INPUT	MODEL 458 OUTPUT	MODEL 460 OUTPUT
+5V	100kHz	1MHz
0	50kHz	500kHz
-5V	0	0

Figure 5. Offsetting Input to Accept ±5V Bipolar Inputs

The output may also be scaled up so that low amplitude signals, such as 1V will give full scale output frequency; 100kHz model 458 or 1MHz model 460. By scaling the output frequency for low level signals, the step response will significantly improve. As shown in Figure 6 for model 458, the step response for a 1 volt input decreases from 200μs before input scaling, to 20μs with scaling.



INPUT	OUTPUT
+1V	100kHz
0	90kHz

Figure 6. Offsetting Input to Achieve Improved Dynamic Response for Small Signal Inputs

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale input and is guaranteed over the 0.1mV to 11V operating signal range; ±0.01% max, models 458J/K/L, ±0.015% max, models 460J/K/L. Typical nonlinearity performance is illustrated in Figure 7.

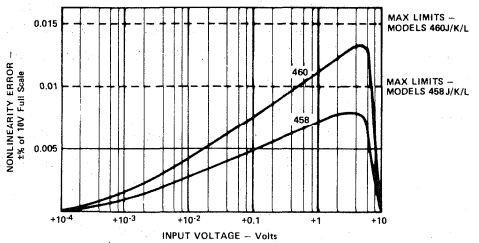


Figure 7. Nonlinearity Error Versus Input Voltage

Gain Temperature Stability: Gain drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range; 5ppm/°C (458L), 10ppm/°C (458K), 20ppm/°C (458J), 15ppm/°C (460L), 25ppm/°C (460K) and 50ppm/°C (460J) max.

LONG TERM PRECISION INTEGRATOR

In critical measurement applications, such as pollution monitoring where it is required to integrate for periods greater than 1 hour with overall accuracy of 0.05%, the V/F converter offers a superior low cost approach when compared to the traditional operational integrator circuit. As shown in Figure 8, the analog signal is applied to a precision input amplifier, model 52K and then to the V/F input. The V/F output is connected to a large capacity counter and display, operating as a totalizer. The total pulse count is equal to the time integral of the analog input signal. Since the output displayed is an accumulated pulse count, there is no integrator drift error. A feature of this approach is the infinite hold capability without errors due to time drift, since the counter may be held at any time without affecting the output reading.

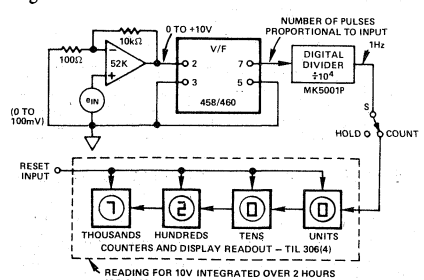


Figure 8. Models 458/460 as Long Term Integrator with Arbitrary Display Calibration. Frequency Division Ratio can Otherwise be Chosen to Provide Direct Readout in any Desired Units.

RATIOMETRIC MEASUREMENTS

The circuit shown in Figure 9 illustrates a simple and inexpensive way of using two 100kHz V/F converters to achieve ratiometric measurements with less than 0.1% error over a dynamic range of 10,000 to 1. One converter is used as the input V/F to a digital counter and display, while a second converter, with a digital divide-by-N circuit is used as the time base for the counter. The counting time is one half the output period of the divide-by-N circuit, resulting in an output count of $2NV_1/V_{REF}$.

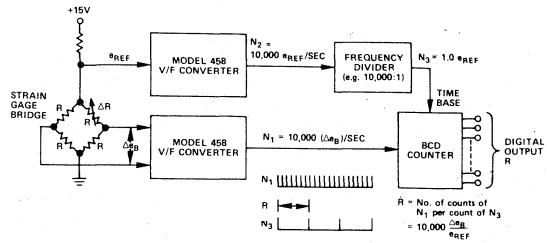


Figure 9. High Resolution, Wide-Range Ratiometer Using Model 458 V/F Converter

PRECISION HIGH CMV ANALOG ISOLATOR

By combining the V/F converter with a floating power supply and optical isolator as shown in Figure 10, accurate low level measurements in the presence of high common mode voltages may be achieved. Only the CMV rating of the optical isolator and the breakdown rating of the power supply limit the CMV rating. Using this approach for isolating transducers, ground loop problems are eliminated. Cost and complexity are minimized since only a single optical isolator is required to couple the serial pulse output from the V/F to the digital readout.

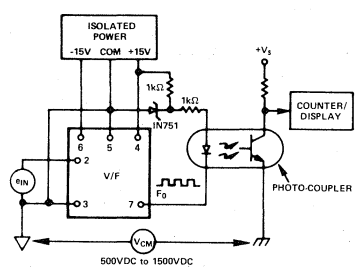


Figure 10. Optical Isolation Using LED Photo Isolator to Provide Up to 1500V dc CMV Isolation

APPLICATION IN DATA ACQUISITION SYSTEMS

High Noise Immunity Data Transmission: A method of accurately transmitting analog data through high noise environments is illustrated in Figure 11. This approach utilizes the self clocking output of models 458 and 460 and eliminates the need for costly additional twisted pair for external synchronization. Model 610 amplifies the low level differential transducer signal up to the 10V full scale V/F input level. A differential line driver is used to drive a twisted pair cable. The differential line driver and receiver offer high noise immunity to common mode noise signals.

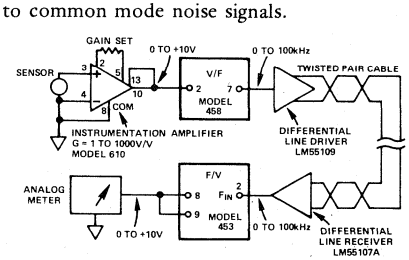


Figure 11. Application of Model 458 V/F Converter in a High Performance, High Noise Rejection Two-Wire Data Transmission System

Low-Cost, Versatile, 10/100kHz Frequency to Voltage Converters

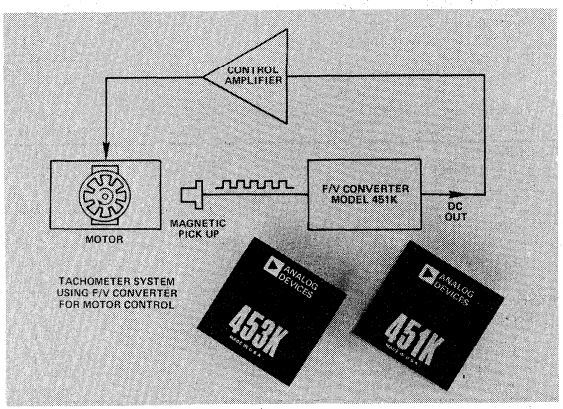
MODELS 451, 453

FEATURES

- Low Cost
- Versatility: Adjustable Threshold, Gain & Output Offset
- Guaranteed Low Nonlinearity: 80ppm Max, 451L and 453L
- Accepts TTL, CMOS, HNIL, Sinewave, Pulse, Squarewave and Triangle Wave Input Signals
- No External Components to Meet Rated Performance
- +20mA Output to Operate Relays and Meters
- Low Profile Package, 0.4" Case Height
- Meet MIL-STD-202E Environmental Testing

APPLICATIONS

- Motor Control and Speed Monitor
- Line Frequency Monitor and Alarm Indicator
- Fluid Flow Measurements and Control
- FM Demodulation and VCO Stabilization
- Frequency vs. Amplitude Response Measurements



GENERAL DESCRIPTION

Models 451 and 453 are low cost 10kHz and 100kHz frequency to voltage converters that feature excellent low nonlinearity to less than 80ppm, output current of +20mA and the capability of interfacing with TTL, HNIL, CMOS, sinewave, squarewave, pulse and triangular input signals. External components are not required to achieve rated performance, however, extreme versatility is maintained by allowing access to all critical points of the design. This versatility allows programmable input threshold, gain, and output offset voltage.

Both models 451 and 453 are available in three selections, each offering guaranteed maximum nonlinearity error as well as maximum gain drift error. Models 451J and 453J offer 0.03% max nonlinearity and 100ppm/°C max gain drift. Models 451K and 453K offer 0.015% max nonlinearity and 50ppm/°C max gain drift. Models 451L and 453L offer 0.008% max nonlinearity and 50ppm/°C max gain drift.

WHERE TO USE FREQUENCY TO VOLTAGE CONVERTERS

Pin compatible with existing popular models, these versatile new designs offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage.

Process Control Systems: For motor speed controllers, power line frequency monitoring and fluid flow measurements where flow transducers, such as variable reluctance magnetic pickups, provide pulse train outputs as a linear function of flow rate.

Audio and Accoustic Systems: For wow and flutter measurements with tape recorders and turntables, FM demodulation and speaker response measurements.

Test Instrumentation: For VCO stabilization, analog readout frequency meter, vibrational analysis and frequency versus amplitude X-Y plots where the vertical axis presents the normal amplitude signal and the horizontal axis presents the output signal from the F/V converter.

Data Acquisition Systems: For converting serially transmitted data back to analog voltages.

DESIGN FEATURES AND USER BENEFITS

The combination of low cost and high performance provided by models 451 and 453 offers exceptional quality and value to the OEM designer. These compact modules have been designed to provide maximum versatility, thereby increasing their utility in a broad scope of applications.

Adjustable Input Threshold: Threshold level is externally resistor programmable from 0 to ±12V, permitting simple, direct interface with low level signals, e.g. 10mV p-p, as well as with high level inputs such as CMOS and HNIL logic levels, e.g. 0 to +12V.

Adjustable Gain: Model 451 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 20kHz. Model 453 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 200kHz. This adjustable gain feature enables the user to easily match the maximum frequency output from a wide class of frequency transducers to the +10V full scale output from models 451 and 453. Increased signal conversion sensitivity with higher resolution results.

Adjustable Output Offset Voltage: The output offset is adjustable from -10V to +10V, enabling bipolar outputs or expanded scale measurements or setting the input frequency where zero output voltage occurs.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	10kHz FULL SCALE J	451 K	L	100kHz FULL SCALE J	453 K	L
TRANSFER FUNCTION	$E_O = (10^{-3}V/Hz)(F_{IN})$			$E_O = (10^{-4}V/Hz)(F_{IN})$		
FREQUENCY INPUT						
Frequency Range	dc to 10kHz min			dc to 100kHz min		
Overrange	10% min			10% min		
Waveforms	Sine, Square, Triangle, Pulse Train			Sine, Square, Triangle, Pulse Train		
Pulse Width (Pulse Train Input)	20µs min			2µs min		
Threshold	+1.4V			+1.4V		
With External Adjustment	0V to ±12V			0V to ±12V		
Hysteresis	±50mV			±100mV		
Levels (TTL Compatible) High	+1.45V to +12V			+1.5V to +12V		
Low	-12V to +1.35V			-12V to +1.3V		
Max Safe Input Voltage[1]	$\pm V_S$			$\pm V_S$		
Impedance	10MΩ‖10pF			10MΩ‖10pF		
ACCURACY						
Warm-Up Time	one minute			one minute		
Nonlinearity[2]						
F_{IN} = 1Hz to 11kHz	±0.03% max	±0.015% max	±0.008% max	–	–	–
F_{IN} = 1Hz to 110kHz	–	–	–	±0.03% max	±0.015% max	±0.008% max
Gain vs. Temperature[3] (0 to +70°C)	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max
vs. Supply Voltage	±300ppm/%			±350ppm/%		
vs. Time	±30ppm/month			±30ppm/month		
RESPONSE						
Step Response to ±0.5% of Final Value						
F_{IN} = dc to Full Scale	4ms			0.8ms		
F_{IN} = Full Scale to dc	30ms			4ms		
Internal Filter Time Constant	200µs			24µs		
External Filter Time Constant	20ms/µF			20ms/µF		
OUTPUT[4]						
Voltage (F_{IN} = Full Scale)[5]	+9.85V min; +9.95V max			+9.85V min; +9.95V max		
Current (E_O = +10V, -10V)	(+20, -2)mA min			(+20, -2)mA min		
Offset Voltage[6] @ +25°C	±7.5mV max			±7.5mV max		
vs. Temperature (0 to +70°C)	±30µV/°C max			±30µV/°C max		
vs. Supply Voltage	±100µV/% max			±50µV/% max		
vs. Time	±100µV/month			±100µV/month		
Ripple						
F_{IN} = 1Hz	3mV p-p			55mV p-p		
F_{IN} = 10kHz	80mV rms			35mV rms		
F_{IN} = 100kHz	–			35mV rms		
Impedance	0.1Ω			0.1Ω		
Offset Scale Factor[7]	-56µA/V			-45µA/V		
POWER SUPPLY[8]						
Voltage, Rated Performance	±15V dc			±15V dc		
Voltage, Operating	±(12 to 18)V dc			±(12 to 18)V dc		
Current, Quiescent	(+10, -8)mA			(+10, -8)mA		
TEMPERATURE RANGE						
Rated Performance	0 to +70°C			0 to +70°C		
Operating	-25°C to +85°C			-25°C to +85°C		
Storage	-55°C to +85°C			-55°C to +125°C		
MECHANICAL						
Case Size	1.5" x 1.5" x 0.4"			1.5" x 1.5" x 0.4"		
Weight	25 grams			25 grams		
Mating Socket	AC1050			AC1050		

[1] F_{IN} and REF terminals can be shorted to $\pm V_S$ indefinitely without damage.
[2] Nonlinearity error is specified as a percentage of 10V full scale output level.
[3] Gain temperature drift is specified in ppm of output signal level.
[4] OUT terminal can be shorted indefinitely to $\pm V_S$ and ground without damage.
[5] Adjustable to +10.000V using FULL SCALE ADJUST trim pot.
[6] Adjustable to zero using 50kΩ OFFSET ADJUST trim pot.
[7] Current into the SUM PT terminal to offset the output voltage positive.
[8] Recommended power supply, ADI model 904, ±15V @ ±50mA output.

Specifications subject to change without notice.

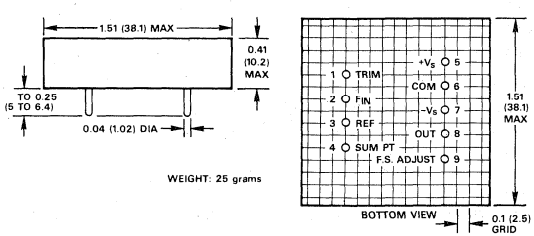
All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

OUTLINE DIMENSIONS

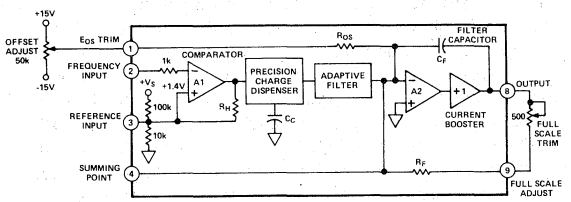
Dimensions shown in inches and (mm)



MATING SOCKET AC1050

FREQUENCY TO VOLTAGE OPERATION

Models 451 and 453 accept virtually any signal waveshape providing accurate conversion into an output voltage proportional to the input signal frequency. The only restriction is that the input signal must remain above the threshold level for 20μs when using model 451, and 2μs when using model 453. Linear, stable conversion over four decades of input range for model 451 and five decades of input range for model 453, is achieved using a precision charge-dispensing design approach. Figure 1 represents a functional block diagram for both models 451 and 453 frequency to voltage converters.



MODEL	C_F	R_{OS}	R_H	R_F
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

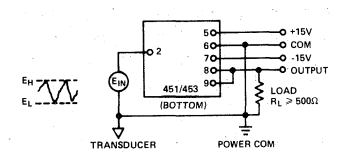
Figure 1. Block Diagram — Models 451 & 453 F/V Converters

THEORY OF OPERATION

Input signals are applied directly to a comparator, A1, which is internally set to provide a +1.4V threshold with ±50mV hysteresis for model 451 and ±100mV hysteresis for model 453. This threshold level offers excellent noise immunity for TTL input levels. Following the input comparator is a precision charge dispensing circuit and output amplifier where the comparator signal is converted to a dc voltage. When the input comparator changes state, C_C is alternately charged from a precision voltage reference and discharged through the summing point of an output amplifier, A2. A fixed amount of charge, Q, is controlled during each charge/discharge cycle. The higher the input frequency, the higher the average current into the summing point of A2. A current to voltage conversion is then accomplished by R_F. The current pulses from the charge dispensing circuit are integrated by C_F to reduce ripple. Added filtering for low frequency input signals is provided by an adaptive filter at the output of the charge dispensing circuit.

BASIC F/V HOOK-UP

Models 451 and 453 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figure 2 illustrates the basic wiring connection for either F/V converter model. Using the basic hookup as shown, full scale output voltage accuracy is ÷10V, -½% to -1½%. The output offset voltage is 0V to ±7.5mV. The Full Scale and Output Offset errors can be eliminated by using the FINE TRIM PROCEDURE.



MODEL	INPUT VOLTAGE RANGE		INPUT FREQUENCY RANGE
	High (E_H)	Low (E_L)	(F_{IN})
451	+1.45V to +12V	-12V to +1.35V	0 to 11kHz
453	+1.5V to +12V	-12V to +1.3V	0 to 110kHz

Figure 2. Basic Wiring Interconnection

FINE TRIM PROCEDURE

Connect the F/V converter as shown in Figure 3 and allow a five minute warm-up after initial power turn-on. Adjust the OFFSET ADJUST pot, R_O, for an output of 0.000V. The input terminal, F_{IN}, can be left open or tied to COM without affecting OFFSET ADJUST. Using a precision, stable frequency source connected to F_{IN} terminal, set the input frequency to 10.000kHz for model 451 or 100.000kHz for model 453. Adjust the FULL SCALE ADJUST trim pot, R_S, for an output of +10.000V.

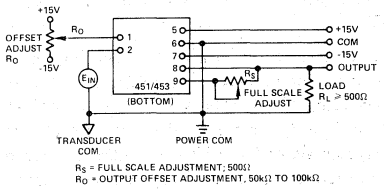


Figure 3. Wiring Interconnection Showing Fine Adjustment Trims for Offset and Full Scale Frequency

ADDITIONAL TRIM CAPABILITY

Adjusting Input Threshold: The input comparator of models 451 and 453 shown in Figure 1, conditions the input signals providing protection against noisy environments as well as preventing double triggering with slow rise-time signals. Input levels up to the supply voltages, $\pm V_S$, will not cause damage to the input comparator.

Threshold voltage level, V_T, is internally set for both models 451 and 453 at +1.4V. Hysteresis, V_H, for model 451 is ±50mV, and ±100mV for model 453. Signals of virtually any waveshape which exceed the combined threshold and hysteresis levels, $V_T \pm V_H$, will trigger the F/V converter. The REF terminal permits the user to conveniently adjust the input threshold over the range from 0 to ±12V to achieve optimum noise rejection or increased triggering sensitivity.

Increasing Threshold for Greater Noise Immunity: Connecting an external resistor from the REF terminal to the positive supply voltage, $+V_S$, increases the input threshold level above +1.4V, offering increased input noise immunity. Optimum noise immunity is generally determined by adjusting the threshold level to a point mid-way between the high and low input signal levels. For example, for a 0 to +12V input swing — representative of CMOS and HNIL logic signals — a 17.6kΩ resistor from +15V to the REF terminal results in a +6V threshold.

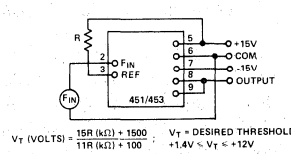


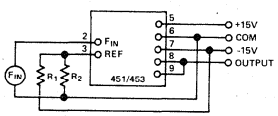
Figure 4. Increasing Threshold Above +1.4V for Greater Noise Immunity

Changes in impedance at the REF terminal result in changes to the hysteresis. Hysteresis levels can be calculated by assuming the comparator output is switching between ±12V. This ±12V signal is attenuated by a resistor-divider network formed by

R_H (see Figure 1) and the parallel combination of all resistors attached at the comparator positive input. For example, with a 17.6kΩ resistor connected to the REF terminal, hysteresis becomes ±35mV for model 451 and ±75mV for model 453. The F/V converter will, therefore, trigger at +6V ±35mV for model 451 and +6V ±75mV for model 453.

Decreasing Threshold for Signals Less Than +1.4V: A resistor connected from the REF terminal to the negative power supply, $-V_S$, will increase the input triggering sensitivity for operation with signals below $+1.4V_{PK}$. As shown in Figure 5, a minimum threshold of zero volts is obtained with a 100kΩ resistor. The triggering level, $V_T \pm V_H$, will be established by the resulting hysteresis levels. With a 100kΩ to -15V, model 451 hysteresis will be ±50mV and model 453 hysteresis will be ±60mV.

To reduce the hysteresis for greater triggering sensitivity, a 1kΩ resistor can be connected from the REF terminal to COM. Signals exceeding ±5mV (10mV p-p) with model 451 and ±15mV (30mV p-p) for model 453, will operate the F/V converter. A 1kΩ resistor from REF to COM is the minimum value recommended to reduce hysteresis and achieve reliable operation.



MODEL	R_1	R_2	THRESHOLD (V_T)	HYSTERESIS (V_H)	TRIGGER LEVELS ($V_T \pm V_H$)
451	∞	∞	+1.4V	±50mV	+1.45V; +1.35V
	100kΩ	∞	0V	±20mV	±20mV (40mV p-p)
	100kΩ	1kΩ	0V	±5mV	±5mV (10mV p-p)
453	∞	∞	+1.4V	±100mV	+1.5V; +1.3V
	100kΩ	∞	0V	±60mV	±60mV (120mV p-p)
	100kΩ	1kΩ	0V	±15mV	±15mV (30mV p-p)

Figure 5. Decreasing Threshold Below +1.4V to Increase Triggering Sensitivity for Low Level Input Signals

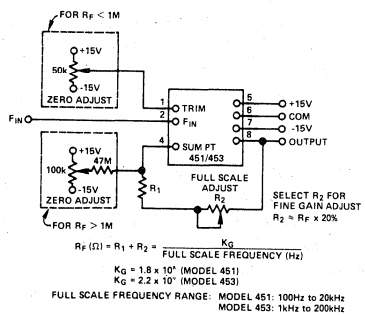


Figure 6. Selecting External Gain Resistor R_F

Adjusting Gain: Connect the FULL SCALE ADJUST terminal to the OUTPUT terminal to set the gain of model 451 at 10^{-3} V/Hz for a 10kHz full scale input frequency and the gain of model 453 at 10^{-4} V/Hz for a 100kHz full scale input frequency. Connecting an external resistor from the SUM PT terminal to the OUTPUT terminal and leaving the FULL SCALE ADJUST terminal open, facilitates gain adjustment. Model 451 can be adjusted over the range from 10^{-1} V/Hz to 5 x 10^{-4} V/Hz resulting in a full scale input frequency from 100Hz to 20kHz respectively. The gain of model 453 can be adjusted over the range from 10^{-2} V/Hz to 5 x 10^{-5} V/Hz resulting in a full scale input frequency from 1kHz to 200kHz respectively. The gain adjustment procedure is capable of increasing full scale frequency beyond the rated ranges for each model, however, nonlinearity will increase above 300ppm.

When using large values of R_F to externally set gain of the F/V converter, the output amplifier gain increases resulting in an increase in sensitivity when using the OFFSET ADJUST trim pot. For improved resolution in high gain applications ($R_F >$ 1MΩ), an alternate method of trimming offset is shown in Figure 6.

Offsetting the Output: The output of models 451 and 453 can be offset over the range from -10V to +10V, enabling scale expansion for increased signal sensitivity as well as bipolar output swings up to 20V p-p.

Current introduced at the SUM PT terminal results in shifts of the output voltage directly proportional to the Offset Scale Factor, K_S. For model 451, K_S = -56μA/V and for model 453, K_S = -45μA/V. The offset current can be generated using an external resistor from a voltage reference to the SUM PT terminal. A stable, well regulated supply voltage, such as ADI's model 904 is recommended. To shift the output positive, 0 to +10V, connect the current resistor to the negative, $-V_S$ supply. To shift the output negative, 0 to -10V, connect the current resistor to the positive, $+V_S$, supply.

The example using model 451 illustrated in Figure 7 provides a 0 to +5V output change in response to a 5kHz to 10kHz input change. With this input, a bipolar output from -2.5V to +2.5V can be obtained by increasing the output voltage shift from -5V, (R_C = 53.6kΩ) to -7.5V, (R_C = 35.7kΩ).

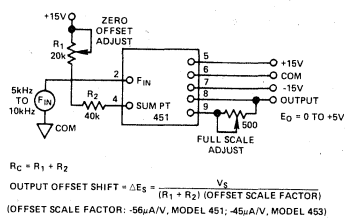


Figure 7. Selecting External Output Offset Resistor, R_C

SCALE EXPANSION

By combining both gain and output offset voltage adjustments, signals which exhibit a center frequency with small frequency changes, can be converted with improved resolution. Representative signals benefiting from the Scale Expansion procedure outlined below, are tachometer and frequency modulated signals. In the case of tachometer outputs, the speed is often set at an idle point and changes in output frequency represent changes in motor loading conditions. In the case of FM signals, the F/V converter can be applied such that the carrier frequency produces zero output. The resulting output voltage from the F/V converter represents the modulating signal.

Procedure for Scale Expansion: The following procedure incorporates both gain and output offset adjustments to achieve scale expansion. An example is illustrated in Figure 8 for an FM signal with a 50kHz carrier frequency and ±5kHz modulating signal.

1) Determine the Gain: $G = \Delta E_O / \Delta F_{IN}$ where ΔE_O is the total output voltage change desired in volts, and ΔF_{IN} is the total input frequency change in Hz.

2) Calculate the external gain resistor, R_F;
$R_F(\Omega) = G(1.8 \times 10^7)$, model 451
$R_F(\Omega) = G(2.2 \times 10^8)$, model 453

3) Calculate the Output Offset Shift, ΔE_S, required to achieve the desired maximum output voltage, E_O (max) with the max input frequency, F_{IN} (max), and the new gain;

$$\Delta E_S \text{ (volts)} = G\ F_{IN} \text{ (max)} - E_O \text{ (max)}$$

4) Calculate the offset current resistor, R_C;

$$R_C\ (\Omega) = \frac{V_S\ G}{(\Delta E_S)\ (k_s)}$$

$k_s = 56 \times 10^{-9}$, model 451
$k_s = 45 \times 10^{-10}$, model 453

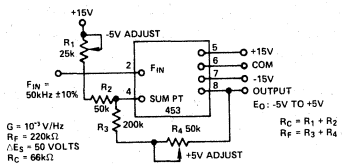


Figure 8. Application of Model 453 in FM Demodulation

INTERFACING SIGNALS WITH DC OFFSETS > 10V

Signals with dc levels up to ±10V can be directly connected to the input terminal of models 451 and 453. Capacitive coupling, as shown in Figures 9 and 10, is used for inputs with dc offsets greater than ±10V. The 1MΩ resistor illustrated in Figure 9 provides a dc return path to power common for the input comparator bias current. Threshold adjustments can be made following the capacitor, to set the F/V input sensitivity to match the ac signal peak-to-peak amplitude. Signals as low as 10mV p-p with model 451 and 30mV p-p model 453 are acceptable. Refer to Figures 4 and 5.

AC signals greater than $\pm V_S$ should be attenuated with a resistive divider network following the capacitor. When large input transients ($>\pm V_S$) are possible due to either a noisy environment or power turn-on surges, protection is provided with the addition of two diodes as shown in Figure 10.

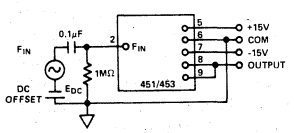


Figure 9. Interfacing Signals With DC Offsets Greater Than ±10V

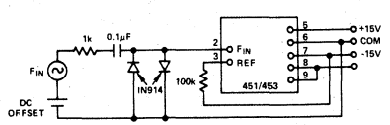


Figure 10. Input Diode Protection for High Voltage Transients

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale output voltage and is guaranteed for each model over the specified input range. Model 451 is rated over 1Hz to 11kHz range and model 453 is rated over 1Hz to 110kHz range. Typical nonlinearity performance is shown for all models in Figure 11.

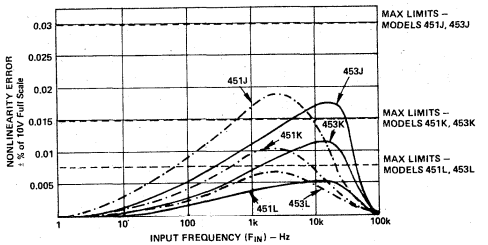


Figure 11. Nonlinearity Error Versus Input Frequency

Gain Temperature Stability: Gain Drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range. Models 451K, 451L, 453K and 453L offer ±50ppm/°C maximum gain drift. Models 451J and 453J offer ±100ppm/°C maximum gain drift. Gain drift is typically half the guaranteed limits.

OUTPUT RIPPLE

The output contains an ac ripple signal which increases in amplitude with input frequency. Adding external capacitance in parallel with the internal filter capacitor will reduce output ripple as shown in Figures 12 and 13.

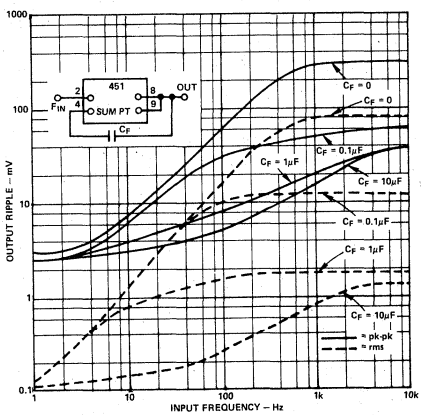


Figure 12. Output Ripple Versus External Filter Capacitor (C_F) – Model 451

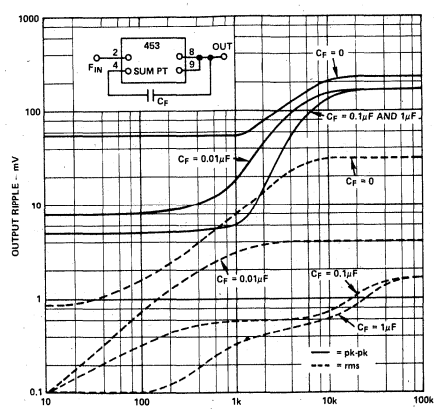


Figure 13. Output Ripple Versus External Filter Capacitor (C_F) – Model 453

SETTLING TIME

Increasing the external filter capacitor to reduce output ripple will increase the settling time to step changes in frequency occurring at the input. Figure 14 shows curves of settling time to ±0.5% of final value for both increasing and decreasing full scale step changes. As C_F increases in value, the total filter time constants for models 451 and 453 approach equal values, resulting in identical settling time.

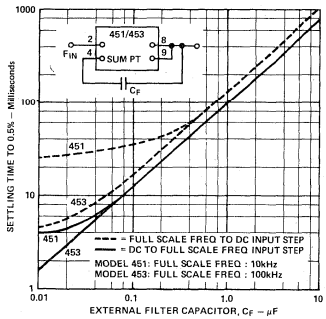


Figure 14. Settling Time Versus External Filter Capacitor

APPLICATIONS IN PROCESS CONTROL SYSTEMS

MOTOR CONTROLLER

In making rpm measurements, transducers are often encountered that have pulse-train outputs from variable-reluctance magnetic pickups (in which the output frequency is a function of rpm). These low level signals are generally in the range of 0 to 200mV peak. The adjustable input threshold feature of models 451 and 453 enables direct connection to low level transducers, offering simple, reliable interfacing.

The motor speed control and monitoring application shown in Figure 15 illustrates the F/V converter applied in a closed loop control system. R1 sets the threshold to +60mV with ±50mV hysteresis for model 451.

The +20mA output current capability of both models 451 and 453, enables direct interface to low impedance loads, up to 500Ω, such as analog meters or relays.

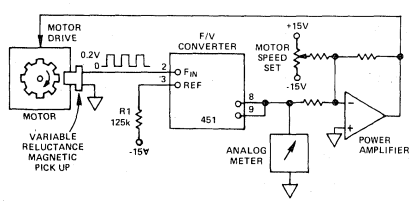


Figure 15. Application of F/V Converter to Control and Monitor Motor Speed in Closed Loop System

SPEED SWITCH

With the addition of a low cost comparator and relay, the F/V converter provides a reliable approach to controlling heavy generator loads after the generator has reached a specified speed. As shown in Figure 16, the relay will remain open until the output from the F/V converter reaches a preset POWER ON trip level. The F/V output signal is linearly related to the speed of the motor, permitting precise control of the POWER ON set point.

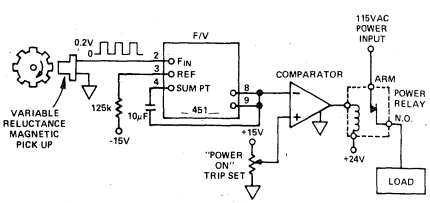


Figure 16. Application of F/V Converter to Control Load Power

APPLICATION IN INSTRUMENTATION SYSTEMS

FREQUENCY MONITORING

Small input frequency changes can be monitored more readily by using the programmable gain feature of models 451 and 453 to achieve greater signal sensitivity. In the application of model 451 illustrated in Figure 17, gain has been set to 0.1V/Hz, resulting in a 100Hz full scale frequency range. The output resolution for small changes occurring in the 60Hz line frequency has been improved. An additional advantage of this approach is the reduced accuracy and stability requirements placed on the relay trip levels, set by the voltage levels at the comparators. A precision voltage reference supply is not required.

Since both models 451 and 453 tolerate input signals up to the supply levels, $\pm V_S$, costly input protection is eliminated in most applications.

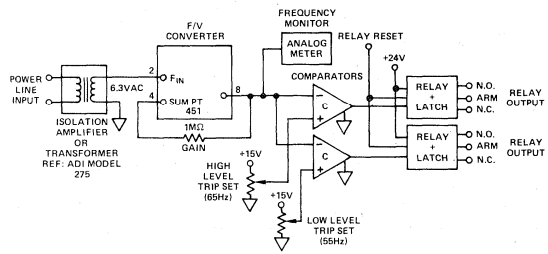


Figure 17. Application of F/V Converter to Monitor 60Hz Line Frequency

APPLICATION IN DATA ACQUISITION SYSTEMS

HIGH NOISE IMMUNITY TRANSMISSION

F/V converters are excellent companion products to V/F converters for use in low cost, two wire data transmission systems. As shown in Figure 18, this V/F/V approach utilizes the continuous self-clocking feature of the V/F converter thereby eliminating the need for costly additional twisted pair cable for external synchronization. Model 610 instrumentation amplifier amplifies the low level differential transducer signal to the 10V full scale of models 450 and 456 10kHz V/F converters. A differential line driver is used to drive a twisted pair cable through a noisy environment. A differential line receiver is used to drive model 451 10kHz F/V converter. The low cost of the V/F and F/V converters in addition to the simple twisted pair cabling approach make it economical to use a V/F/V converter pair for each channel in a data acquisition system.

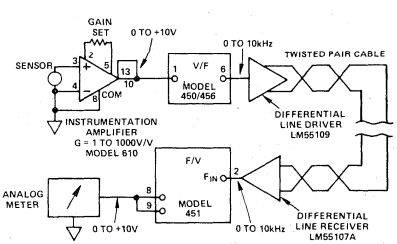


Figure 18. Application of F/V Converter in a Low Cost, High Noise Rejection Two-Wire Data Transmission System

Synchro-Digital Converters

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●New product since 1979 *Data Acquisition Products Catalog Supplement*

Selection Guide
Synchro-Digital Converters

The products catalogued here are divided into four categories:

1. Synchro/Resolver/Inductosyn-to-Digital Converters
2. Digital-to-Synchro/Resolver Converters
3. Digital Processors
4. Miscellaneous

Devices are listed in order of decreasing resolution. Complete descriptions, specifications, and applications information can be found in the data sheets. General information can be found in the following pages. Specifications are typical at rated supply voltage and frequency, and $T_A = 25°C$, except where noted.

Extensive information on synchros, resolvers, inductosyns, and conversion to and from digital can be found in the new book, *Synchro and Resolver Conversion*, edited by Geoffrey Boyes, 1980, available from Analog Devices, at $11.50.

1. SYNCHRO/RESOLVER/INDUCTOSYN-TO-DIGITAL CONVERTERS

Models	Resolution†	Characteristics	Page
SDC1604	16	Module, overall accuracy to ±1 arc-min (max error), tracking rate 360°/s (60 or 400Hz), type 2 servo, requires STM transformer module, described on data sheet	12-25
SDC1704	14	Low-profile module, overall accuracy to ±2 arc-min ±1 LSB and tracking rate 12rev/s @ 400Hz, internal transformer	12-27
SBCD1753/1757	14(BCD)	Module, angular range 0° to 359.9°, overall accuracy to within ±0.2° max error, tracking rate 36 rev/s (400Hz), internal transformer, supply requirement, +5V and ±15V/+15V	12-21
SBCD1752/1756	13(BCD)+Sign	Module, angular range −180° to −0.10 and +0.0° to +179.9°, same accuracy, tracking rate, and supply requirements as SBCD1753/1757	12-21
SDC1700	12	Low-profile modules, overall accuracy to ±8.5 arc-min (max error) and 5.3 arc-min resolution, internal transformer, 36rps tracking rate (400Hz)	12-27
SDC1725	12	0.35″H modules, overall accuracy to ±3.2 arc-min ±1LSB (max error), resolution 5.3 arc-min, internal transformer, 36rps tracking rate (400Hz)	12-33
SDC1741/1742●	12	Hybrid IC's, accuracy to 10/3.2 arc-min ±1LSB (max error), tracking rate 18rps min (400Hz or 2.6kHz), internal transformers	12-37
SDC1702	10	Low-profile module, overall accuracy to ±22 arc-min (max error), resolution 21 arc-min, tracking rate 36rps (400Hz), internal transformer	12-27
SDC1726	10	0.35″H modules, overall accuracy to ±22 arc-min (max error), resolution 21 arc-min, tracking rate 36 rps (400Hz), internal transformers	12-33
TSDC1608-1611	10	Module, coarse synchro-to-digital converter and two-speed processor for binary coarse-fine systems, gear ratios 8:1/16:1/32:1/64:1	*
IDC1703		Module, Inductosyn-to-Digital Converter for measuring displacement and angle with Inductosyns, outputs serial up-down pulse for each 1/N of pitch, plus up-down pulse for each complete pitch. Resolution 1:3600, 1:4000, 1:4096, tracking rate 150 pitches/s	12-25

2. DIGITAL TO SYNCHRO/RESOLVER/ANGLE CONVERTERS

Models	Resolution†	Characteristics	Page
DSC1705	14	Module, overall accuracy to ±4 arc-min max error, 1.3VA output, low radius-vector variation (transformation ratio), 0.1%	12-7
DTM1716	14	Module, Digital Vector Generator, multiplies analog input by sin and cos of digital angle to obtain R sin θ and R cos θ analog outputs, radius accuracy to within 0.1%, angular error less than 3 arc-min, resolution 1.3 arc-min	12-11
DSC1706	12	Module, overall accuracy to ±8 arc-min max error, 1.3VA output, low radius-vector variation (transformation ratio), 0.1%	12-7
DTM1717	12	Digital Vector Generator, same function as DTM1716, resolution 5.3 arc-min	12-11

3. DIGITAL PROCESSORS

Models	Resolution†	Characteristics	Page
TSL1612	19	Module, Digital Processor for Two-Speed synchros and angle displays. Accepts digital angle inputs from coarse and fine synchros and combines them to form a single 19-bit word to represent high-resolution angular information. Handles 36:1, 18:1, 9:1 ratios.	12–43
BDM1617	16	Module, accepts 16-bit parallel binary input, gives out parallel BCD data in degrees (modulo 360°) and decimal fractions, <0.005° rounding error	12–5
BDM1615	14	Module, accepts 14-bit parallel binary input, gives out parallel BCD data in degrees (modulo 360°) and decimal fractions, <0.02° rounding error	12–5
BDM1616	14	Module, accepts 14-bit parallel binary input, gives out parallel BCD data in degrees (modulo 360°) and minutes, <1 arc-min rounding error	12–5

4. MISCELLANEOUS

Model	Resolution†	Characteristics	Page
SAC1763	12 (linear resolution)	Synchro to Linear DC Converter: Converts angle information in synchro and resolver form to dc output voltage proportional to input angle; Internal microtransformers (50Hz or 400Hz), 12-bit resolution ±11 arc-min accuracy, ±10V output at 5mA, <5mV p-p output ripple, tracking conversion loop—13,000°/s, $d\theta/dt$ output.	12–17
SPA1695		Synchro/Resolver Power Amplifier, 5VA output, indefinite short-circuit protection, metal case as heatsink, no derating in operation to 105°C, 50 to 400Hz operation. Can be used with digital vector generators (DTM1716/1717) to drive control transformers.	12–41

†Word length in bits (angular binary, unless noted otherwise)
•New product since 1979 *Data Acquisition Products Catalog Supplement*
*Data sheet available upon request.

Orientation
Synchro-Digital Converters

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, and Inductosyns. In addition to modules that perform the appropriate conversions, the line also includes modules that perform purely algebraic or logical functions; in some cases, solid-state circuitry emulates the functions of electromechanical devices.

The range of synchro processing modules now available covers a wide area of application. They are widely used in military and radar applications, but there are additional fields in which they could be used to advantage because of the proven ruggedness and high precision of the electromechanical hardware, their standardized specifications, and their low cost. They have a number of advantages over potentiometers and optical systems.

In this introductory section, there will be provided a brief set of device definitions. Detailed data and applications information is given in the data sheets. For a complete introduction to synchro/digital conversion, Analog Devices has available a 208-page book, *Synchro and Resolver Conversion*, edited by G. Boyes (1980), $11.50.

In this section, and in much of the text, the word "Synchro" appears frequently. In many cases, the word "Resolver" could be used in its place. The modules make use of angular data in resolver form; if the input data is in three-wire synchro form, transformers in "Scott T" configuration convert it to resolver form; analog outputs are available in both forms. There are a number of voltage and frequency options.

REPRESENTATION OF ANGLES IN DIGITAL FORM

Binary

The most commonly used method of representing angles in digital form is simple natural binary weighting, where the most-significant bit (MSB) represents 180°, the next represents 90°, etc. The table shows the bit weights in degrees, degrees-and-minutes, and radians for this coding method.

Bit No.	Degrees	Degrees, minutes		Radians
1	180	180	0	3.141593
2	90	90	0	1.570796
3	45	45	0	0.785398
4	22.5	22	30	0.392699
5	11.25	11	15	0.196349
6	5.625	5	37.5	0.098175
7	2.8125	2	48.75	0.049087
8	1.40625	1	24.38	0.024544
9	0.70312	0	42.19	0.012272
10	0.35156	0	21.09	0.006136
11	0.17578	0	10.55	0.003068
12	0.08789	0	5.27	0.001534
13	0.04395	0	2.64	0.000767
14	0.02197	0	1.32	0.000383
15	0.01099	0	0.66	0.000192
16	0.00549	0	0.33	0.000096

BCD

When angular measures have to be displayed in visual form, BCD coding is used, through the use of binary-to-BCD converters, such as the BDM1615, which provides the necessary scaling and conversion, e.g., from 10100000000000 (180° + 45°) to 10 0010 0101.0000 000 (or 225.00°).

TYPICAL S/D/S DEVICES

Binary-to-Binary-Coded-Digital Converter (BDM1615/16/17)

A device that accepts angular data in binary form and converts it to BCD form, with fractional degrees in decimal fractions of 1° (1615, 1617) or minutes and seconds (1616). The BCD output is modulo 360°.

Digital-to-Synchro Converters (DSC1705/06)

Devices that accept parallel binary digital inputs (14 or 12 bits) and an ac reference signal, and provide outputs in 3-wire synchro form.

Inductosyn-to-Digital Converter (IDC1703)

A device that produces a digital output capable of resolving (to 12 bits) intermediate distances within a single track-pitch of a Farrand linear-Inductosyn stator in displacement- and angle-measuring Inductosyn systems. The moving element is used as though it were a resolver input.

Synchro-to-Digital Converter

A device that accepts either 3-wire synchro- or 4-wire resolver inputs, together with a 2-wire ac reference, and outputs angular binary data in a continuously tracking mode, employing a Type 2 servo loop. The inputs may be from either remote synchros or from electrically simulated synchros (e.g., DSC's).

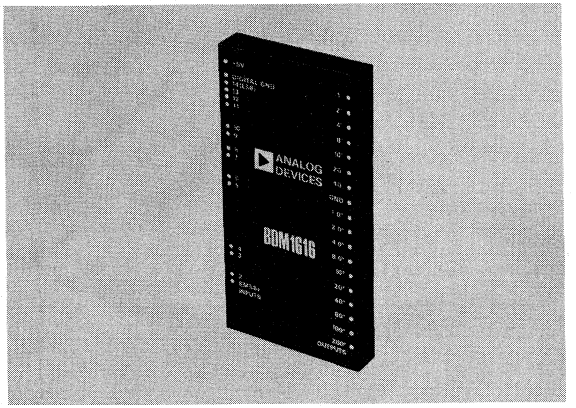
Digital Converters and Processors for Two-Speed Synchros (TSL1612 and TSDC1608/09/10/11)

A two-speed processor takes as inputs two sets of digital information, representing the angles from coarse and fine synchros, and combines them to produce a single 19-bit word representing the actual angle of the "coarse" shaft. The TSL consists of the processing logic alone—it can be used with a pair of SDC's, which provide the two sets of digital information. The TSDC contains the coarse 10-bit SDC, along with the two-speed processing logic.

Binary to BCD Modulo 360° Converter

BDM 1615/6/7

FEATURES
Binary Angle to Modulo 360° BCD Output
Rounding Errors <0.005°
All TTL Levels
Fast Parallel Operation



DESCRIPTION

The BDM 1615/1616/1617 converters are solid state converters which take as inputs angular data in binary form and give out angular data in Binary Coded Decimal form—modulo 360°. The code converters are available in two versions. The first is scaled in degrees and decimal fractions of degrees and the second version is scaled in degrees and minutes.

The BDM 1615 and 1616 accept 14-bit binary inputs and give data in degrees and decimal fractions of a degree, and degrees and minutes respectively.

The BDM 1617 accepts a 16-bit binary input and gives out data in degrees and decimal fractions of a degree.

Rounding errors are <0.02° for the BDM 1615 and <0.005° for the BDM 1617.

All the converters take in parallel data and give out parallel data; the time of operation is <0.5μs.

With most synchro/resolver to digital converters the output digital angle is given in natural binary form with the bit weighting being 180°, 90°, 45° etc. While this natural binary form of angular information is suited for digital computer interfacing and direct angular transmission in serial form, it is not suited for direct conversion to visual digital displays or for use in computers using BCD coding. The BDMs (Binary Decimal Modules) 1615/1616/1617 have been designed to meet this interface requirement.

Two of the main applications for the BDMs are depicted in Figures 1 and 2. Figure 1 shows the BDM being used to convert the binary angular information from a synchro to digital converter into a suitable form for driving the visual display decoder and Figure 2 shows the BDM connected to the binary output from a computer to give a digital display.

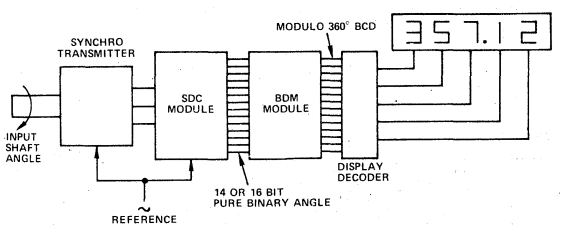


Figure 1.

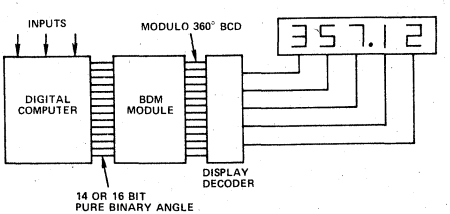


Figure 2.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	BDM 1615	BDM 1616	BDM 1617
Input	14-Bits Natural Binary at TTL Levels	*	16-Bits Natural Binary at TTL Levels
Fan In	5TTL Loads	*	*
Output	Modulo 360° and BCD Fraction—0.01, 0.02, 0.04, 0.08, 0.1, 0.2, 0.4, 0.8°.	Modulo 360° and Minutes Coded—40′, 20′, 10′, 8′, 4′, 2′, 1′.	*
Fan Out	2TTL Loads	*	*
Mode of Operation	Parallel In, Parallel Out	*	*
Speed of Operation	$< 0.5\mu s$	*	*
Rounding Errors	0.02°	1 arc minute	0.005°
Supply Voltage	5.0V ±5%	*	*
Supply Current	350mA	*	700mA
Power	1.75 watts	*	3.5 watts
Operating Temperature	0 to +70°C −50°C to +105°C	*	*
Storage Temperature	−55°C to +125°C	*	*
Size	4″ x 2″ x 0.4″ 102mm x 51mm x 10mm	*	3.125″ x 2.625″ x 0.8″ 79mm x 67mm x 20mm
Enable	–	–	@ "0" = Normal Operation @ "1" = LED Check

*Same specification as BDM 1615 Specifications subject to change without notice.

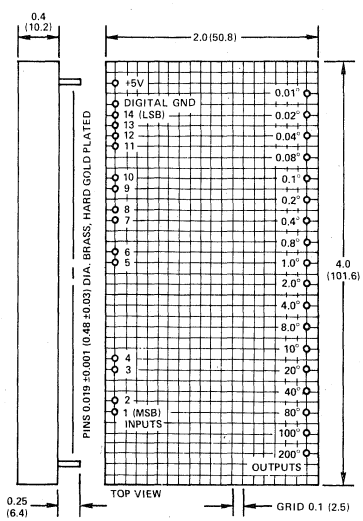
ORDERING INFORMATION

Each of the BDMs is available in either of two versions according to the required operating temperature range. The type number must be followed by a code defining the required temperature range; the code is 500 for 0 to +70°C and 600 for −55°C to +105°C.

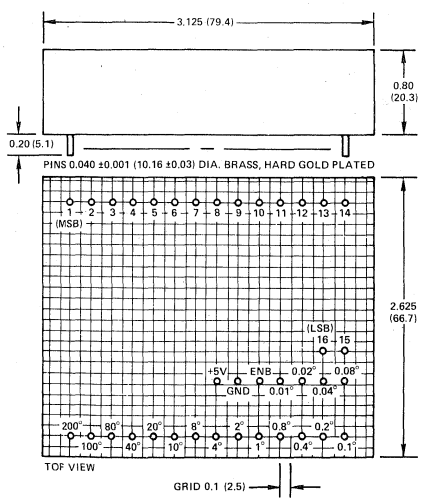
e.g., BDM 1616600 is for a temperature range of −55°C to +105°C.

PIN CONNECTIONS AND OUTLINE DIMENSIONS

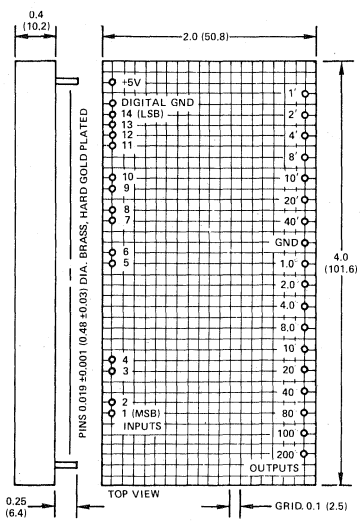
Dimensions shown in inches and (mm).



BDM1615



BDM1617



BDM1616

MATING SOCKET: CAMBION 450-3388-01-03

ANALOG DEVICES

Digital to Synchro Converters

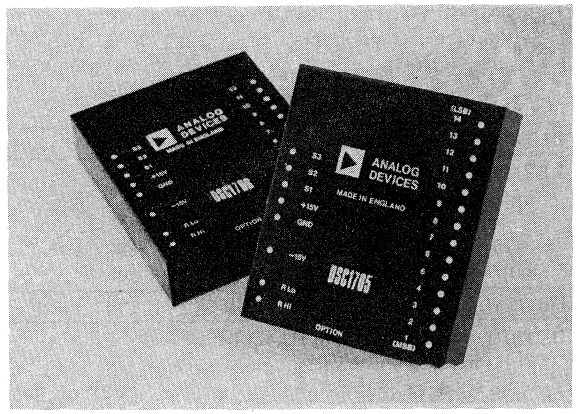
DSC1705/1706

FEATURES

- Very Low Radius Vector Variation (Transformation Ratio) (±0.1%)
- High Accuracy (±2 arc-mins at +25°C)
- 12- or 14-Bit Resolution
- No 5 Volt Power Supply Required
- MIL Spec/Hi Rel Versions Available
- Internal 1.3VA Amplifiers
- Internal Transformers (400Hz Option)
- No Trims or Adjustments Necessary

APPLICATIONS

- Driving Control Transformers
- Driving Torque Receivers (with External Amplifiers)
- Servo Mechanisms
- Retransmission Systems
- Positional Control



GENERAL DESCRIPTION

The DSC1705 and DSC1706 are Digital to Synchro and Digital to Resolver converters capable of driving electromechanical loads of up to 1.3VA.

They accept a 14- or 12-bit digital input representing angle and a reference voltage of either 60Hz or 400Hz, and produce a 3 wire or 4 wire output suitable for driving Synchros or Resolvers.

The 400Hz converters contain internal 1.3VA amplifiers as well as output and reference transformers.

The 60Hz versions contain internal 1.3VA amplifiers but require external output and reference transformers.

If it is necessary to drive a load requiring more than 1.3VA, options for both the 400Hz and 60Hz converters are available allowing the use of external amplifiers and transformers.

RADIUS VECTOR

One of the outstanding features of these converters is the almost negligible Radius Vector variation (Transformation Ratio).

On many Digital to Synchro Converters presently available, the individual sine and cosine outputs produced do not follow the exact sine and cosine laws, and depending upon angle can vary up to ±7%. This is not always important as the ratio of the sine to the cosine, i.e., the tangent, is always correct to the specified accuracy of the converter. There are cases however, when driving torque receivers and certain servo control loops when this variation is unacceptable.

The design of the DSC1705 and DSC1706 has reduced this variation to less than ±0.1%. This means that when the converters are used in closed loop servo systems, the gain of the closed loop is independent of the digital input angle, thus making reference correction unnecessary.

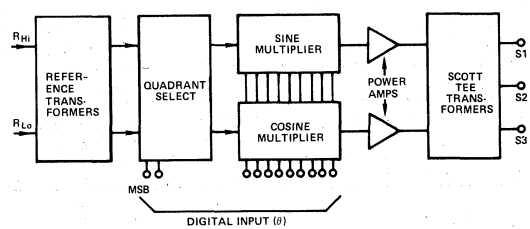
MODELS AVAILABLE

The two Digital to Synchro/Resolver converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:-

Model DSC1705XYZ is a 14-bit converter with an overall accuracy of ±4 arc-minutes.

Model DSC1706XYZ is a 12-bit converter with an overall accuracy of ±8 arc-minutes.

The XYZ option code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the output and the reference voltages, whether the output is in Synchro or Resolver format and whether external transformers are required.



Principle of Operation

FUNCTIONAL DIAGRAM, DSC1705 and DSC1706

The principle of operation of the converters described in this data sheet is shown in the diagram above.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	DSC1705	DSC1706
ACCURACY[1]	±4 arc-minutes	±8 arc-minutes
RESOLUTION	14 Bits (1LSB = 1.3 arc-minutes)	12 Bits (1LSB = 5.3 arc-minutes)
INPUT CODE	14-Bits Natural Parallel Binary with MSB = 180°	12-Bits Natural Parallel Binary with MSB = 180°
REFERENCE VOLTAGE INPUT		
With Internal Transformers		
Low Level	26V rms	*
High Level	115V rms	*
External Transformer Options[2]	4V rms	*
REFERENCE FREQUENCY	60Hz or 400Hz	*
REFERENCE INPUT IMPEDANCE		
With Internal Transformers		
Low Level	20kΩ	*
High Level	200kΩ	*
External Transformer Options[2]	10kΩ	*
DIGITAL INPUT (TTL COMPATIBLE)	1TTL Load	*
OUTPUT VOLTAGE AND FORMAT		
With Internal Transformers		
Low Level	11.8V rms Line-to-Line Synchro or Resolver	*
High Level	90V rms Line-to-Line Synchro or Resolver	*
External Transformer Options[3]	7V rms Sine and Cosine	*
LOAD CAPABILITY	1.3VA	*
SHORT CIRCUIT PROTECTION	Continuous for 5 minutes	*
OUTPUT SETTLING TIME[4]	50μs for 180° Step	*
RADIUS VECTOR VARIATION (Transformation Ratio)	±0.1% max Sine and Cosine	*
INTERNAL TRANSFORMER ISOLATION	500V dc	*
POWER SUPPLIES		
Voltage	±15V dc ±5%	*
Current		
(a) No Load	95mA per Line	*
(b) Full Load Mean	225mA per Line	*
WARM-UP TIME	1sec to Full Accuracy	*
OPERATING TEMPERATURE RANGE	0 to +70°C Standard	*
	-55°C to +105°C Extended	*
STORAGE TEMPERATURE RANGE	-55°C to +125°C	*
SIZE	3.125" x 2.625" x 0.8"	*
	(79.4mm x 66.7mm x 20.3mm)	*
WEIGHT	8 ounces (224 grams) max	*
MEAN TIME BETWEEN FAILURES (MTBF) CALCULATED[5]	150,000 Hours	*

NOTES

[1] Accuracy applies over the full operating temperature range of the option and for:
(a) ±10% reference frequency and amplitude variation.
(b) 10% harmonic distortion on the reference.
(c) ±5% power supply variation.
(d) Any balanced load from no load to full load.

[2] Refers to input to converter and not to external transformers.

[3] Refers to output from internal converter amplifiers and not from external transformers.

[4] Dependent upon option and load conditions.

[5] With MIL-STD-883B components.

Specifications subject to change without notice.

CONNECTING THE CONVERTER

400Hz options. All these converters contain internal output and reference transformers.

The digital input should be connected to pins "1" through "12" on the DSC1706 and pins "1" through "14" on the DSC1705, noting that pin "1" is the Most Significant Bit (MSB).

"S1", "S2" and "S3" should be connected to the appropriate inputs on the synchro being driven. ("S4" is used also when connection is made to a resolver).

The reference should be connected to "R_{Hi}" and "R_{Lo}" ensuring that the phase is correct.

"GND" is the common for both power supplies and digital inputs.

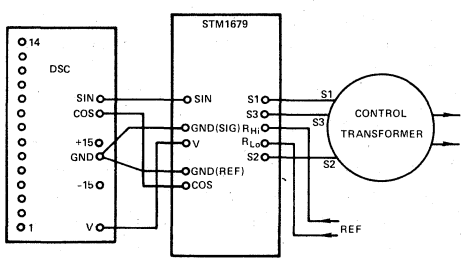
60Hz Options. For 60Hz operation, an external transformer, STM1679 is required.

The power supplies and digital input should be connected as for the 400Hz version.

The STM1679 transformer should have its pins "SIN", "COS" and "V" connected to the equivalent pins on the converter. The "GND(SIG)" and "GND(REF)" should both be connected to "GND" on the converter.

The outputs to the load should be taken from "S1", "S2" and "S3" on the STM1679 transformer ("S4" also in the case of a resolver).

The reference input should be made to "R_{Hi}" and "R_{Lo}" on the STM1679.



60Hz Connection to a Control Transformer (Diagram Shows Bottom View of Modules)

OPERATION WITH EXTERNAL AMPLIFIERS OR TRANSFORMER OTHER THAN STM1679

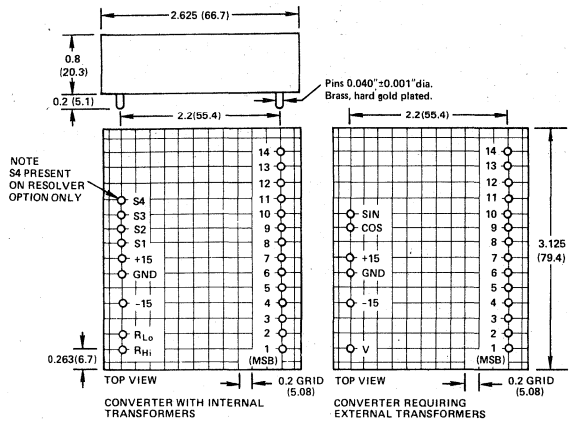
For certain applications, the power output required by the load will be greater than the 1.3VA supplied by the internal amplifiers. Thus external amplifiers and transformers will be needed. Products offered to fulfull this requirement are:

SPA1695 – Dual 5VA Amplifier
STM1696 – 5VA output and reference transformers (400Hz)
STM1697 – 5VA output and reference transformers (60Hz)

If you have a requirement for such products please request the data sheet.

CONVERTER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

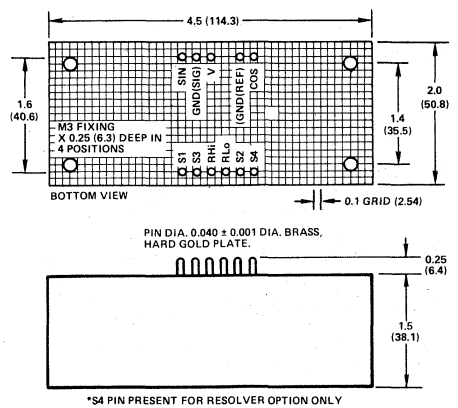


NOTE
DIAGRAMS ABOVE SHOW DSC1705.
DSC1706 DOES NOT HAVE PINS "13" AND "14".

MATING SOCKET: CAMBION 450-3388-01-03

TRANSFORMER (STM1679) OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



*S4 PIN PRESENT FOR RESOLVER OPTION ONLY

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB for DSC1706)	0.0879
13	0.0439
14 (LSB for DSC1705)	0.0220

LOADING THE DSC's WITH CONTROL TRANSFORMERS (CT's)

The most common device to be driven by Digital to Synchro converters is the control transformer (CT)

The minimum power required to drive a CT can be expressed as:

$$(VA) = \frac{V^2}{|Z_{so}|} \cdot \frac{3}{4}$$

where V is the line to line voltage and Z_{so} is the impedance between one input terminal and the other two shorted together with the rotor open circuit. ($Z_{so} = R_{so} + j\,X_{so}$)

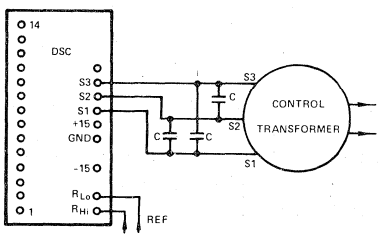
For example, if a CT has a Z_{so} of 700 + j 4900 and a line to line voltage of 90 volts, then:

$$|Z_{so}| = \sqrt{700^2 + 4900^2} = 4950 \text{ Ohms}$$

$$\text{and } (VA) = \frac{90^2}{4950} \cdot \frac{3}{4} = 1.23VA$$

TUNING CT LOADS

The load can be reduced by tuning the output with 3 capacitors as shown below.



Capacitor Connection for Tuning CT's

C should be equal to:

$$\frac{X_{so}}{2\omega\,(R_{so}^2 + X_{so}^2)}$$

The power required after tuning will be:

$$(VA) \text{ untuned} \quad x \frac{R_{so}}{Z_{so}}$$

Therefore in the above example the capacitor value should be:

$$\frac{4900}{2 \times 2\pi \times 400\,(245 \times 10^5)} = 40nF$$

and the power required after tuning will be:

$$1.23 \times \frac{700}{4950} = 0.17VA$$

Note allowance should always be made for tolerances in the CT windings, capacitors and frequency.

PRACTICAL CONSIDERATIONS OF TUNING CT LOADS

1. The capacitors used need not be of high tolerance, 20% is sufficient.
2. Three capacitors must be used, one across S1 and S2, one across S1 and S3 and one across S2 and S3.
3. Voltage working and type of capacitors should be as follows:

   11.8V Line-to-Line options:
   15 Volt ac working or greater, non-polarized tantalum type.

   90V Line-to-Line options:
   100 Volt ac working or greater, for example, low K ceramic types.
4. For tuning Resolver loads, two capacitors only are required, one connected between S1 and S3 and the other connected between S2 and S4.

CONTROL DIFFERENTIAL TRANSMITTERS (CDX's)

The loading on a DSC of these devices can be considered in a similar way to that of CT's. However becasue a CT normally follows a CDX, the effective Z will need to be calculated. This value will normally be between 66% and 80% of the Z_{so} quoted for the CDX.

TORQUE RECEIVERS (TR's)

Torque receivers are more difficult devices to drive than CT's and CDX's, and in general external amplifiers and transformers will be necessary. However, because of the lack of radius vector variation, the DSC1705 and DSC1706 are far more suited to driving TR's than converters with a variation of ±7%.

For a deviation of an angle θ, the drive current required will be:

$$\frac{2 \cdot V \cdot \sin\frac{\theta}{2}}{|Z_{ss}|}$$

Points to be observed are:

(a) The TR should not be allowed to lock up.
(b) A phase lead equal to that specified for the TR should be introduced into the reference input to the DSC.
(c) The reference should always be present on the TR and the converter.
(d) The DSC output voltage should be matched exactly to the voltage requirements of the TR.

CAUTIONS

(a) Do not connect a 115V reference to a 26V converter.
(b) Do not reverse the power supplies.
(c) Do not connect the reference to any other pins except "R_{Hi}" and "R_{Lo}".

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define the item. All standard options and their appropriate option codes are listed below.

Part Number[1]	Resolution	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
DSC1705511	14 Bits	0 to +70°C	11.8V Synchro	26V	400Hz
DSC1705512	14 Bits	0 to +70°C	90.0V Synchro	115V	400Hz
DSC1705611	14 Bits	-55°C to +105°C	11.8V Synchro	26V	400Hz
DSC1705612	14 Bits	-55°C to +105°C	90.0V Synchro	115V	400Hz
DRC1705518	14 Bits	0 to +70°C	11.8V Resolver	26V	400Hz
DRC1705618	14 Bits	-55°C to +105°C	11.8V Resolver	26V	400Hz
DSC1705507 and STM1679522	14 Bits	0 to +70°C	90.0V Synchro	115V	60Hz
DSC1705607 and STM1679622	14 Bits	-55°C to +105°C	90.0V Synchro	115V	60Hz

Note: 1. For 12-bit resolution, substitute DSC1706 in place of DSC1705 in the above.
2. For options not shown above, consult the factory.

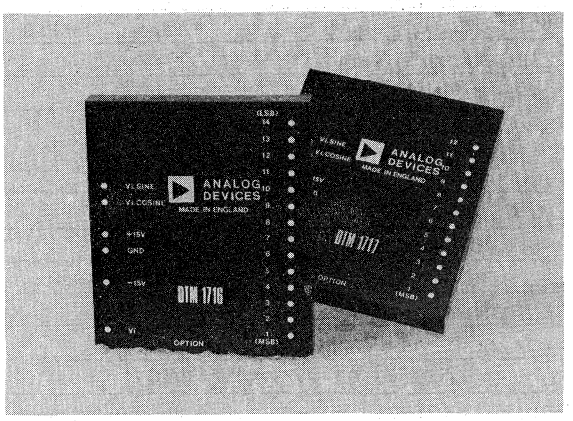
ANALOG DEVICES

Digital Vector Generator

DTM 1716/1717 SERIES

FEATURES
- Accurate Sine, Cosine Multiplication
- 14-Bit Resolution
- 3 Arc-Minutes Accuracy
- 0.1% Radius Accuracy
- Low Profile (0.4")
- Maximum Frequency to Full Accuracy 2.5kHz
- Low Feedthrough

APPLICATIONS
- Digital to Synchro Conversion
- Displays
- Axis Rotation
- Simulators
- Numerical Control
- Prediction
- Vector Resolution
- Spectrum Analysis
- Ultra Low Frequency Oscillators



GENERAL DESCRIPTION

The DTM1716 and DTM1717 are computing converters which have a digital angle input in natural binary form and a bipolar analog input $V_i(t)$. There are two analog outputs $V_{01}(t)$ and $V_{02}(t)$, the outputs are related to the inputs by;

$$V_{01}(t) = V_i(t) \sin \phi(t) \qquad V_{02}(t) = V_i(t) \cos \phi(t)$$

where ϕ is the digital angular input. ϕ ranges from 0 to 360°. The analog input has a range of ±10V; the analog output has a range of ±10V.

The digital input has a resolution of 14 bits for the DTM1716 and 12 bits for the DTM1717. The modules are powered from ±15V supply lines.

If the output voltages are regarded as the components of a vector, the radius accuracy is better than 0.1% and the angular inaccuracy is less than 3 arc minutes for the DTM1716.

A block diagram of the DTM1716 is shown in Figure 1.

Particular attention has been paid in the design to achieve high accuracy in the sine and cosine generation so that they may be used separately as accurate functions.

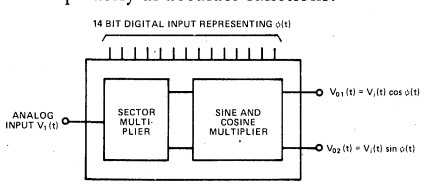


Figure 1. Diagram of DTM1716

Two models are available each with two options as shown below.

DTM1716500 has 14-bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1716600 has 14-bit digital input resolution and a −55°C to +105°C operating temperature range.

DTM1717500 has a 12-bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1717600 has a 12-bit digital input resolution and −55°C to +105°C operating temperature range.

OPERATION

The operation of the DTM1716 is straightforward, being powered from ±15V lines relative to the common pin. No damage is caused by either the +15V or −15V being disconnected but they must not be reversed. The analog input is protected against a short circuit to either power line. The output is short circuit proof and can be connected to either power line without damage. The digital inputs are standard TTL levels. The module dimensions and pin out are shown in Figure 2.

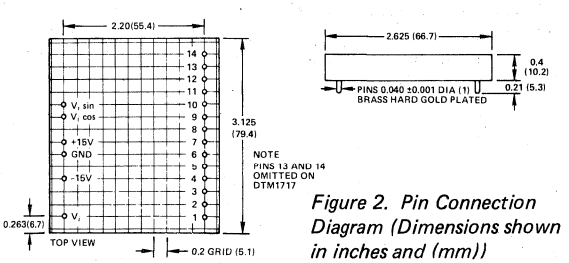


Figure 2. Pin Connection Diagram (Dimensions shown in inches and (mm))

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODELS	DTM1716	DTM1717
DIGITAL ANGULAR RESOLUTION	14 bits (1 LSB = 1.3 arc-mins)	12 bits (1 LSB = 5.3 arc-mins)
FULL SCALE OUTPUT	±10V	*
SCALING ACCURACY	0.1% FSR	*
FULL SCALE INPUT	±10V	*
SCALE TEMPCO	25ppm/°C of FSR	*
ZERO OFFSET	2.5mV	*
OFFSET DRIFT	50μV/°C	*
AC ACCURACY		
Analog Step Response (10V Step)	40μs (to 0.1%)	*
MAX SLEW RATE	0.5V/μs	*
FULL POWER OUTPUT	8kHz	*
FEEDTHROUGH	<1mV at 400Hz	*
ANALOG INPUT IMPEDANCE	10kΩ	*
ANALOG OUTPUT IMPEDANCE	100mΩ	*
OUTPUT LOAD	2kΩ	*
OUTPUT PROTECTION	Short circuit proof	*
DIGITAL INPUT	14-bit natural parallel binary, 1TTL Load	12-bit natural parallel binary, 1TTL Load
RESPONSE TO DIGITAL STEP (90°) (FS Analog Input)	40μs to 0.1% of final value	*
VECTOR ACCURACY[1]		
Radius Error	0.1% FSR	*
Angular Error	±3 arc-mins	*
POWER SUPPLY REJECTION	80dB	*
POWER SUPPLIES	+15V @ 50mA max	*
	-15V @ 40mA max	*
TEMPERATURE RANGE	0 to +70°C Standard	*
Operating	or -55°C to +105°C extended	*
Storage	-55°C to +125°C	*
DIMENSIONS	3.125 x 2.625 x 0.4" 79.4 x 66.7 x 10.2mm	*
WEIGHT	3 oz (85 grams)	*

NOTES

*Specification same as DTM1716.

[1] See Figure 4.

Specifications subject to change without notice.

APPLICATIONS OF THE DTM1716

Figure 3 shows how the DTM1716 can be used in radars and radar simulators for modulating display sawtooth generators using signals derived from a synchro transmitter on the antenna and a Synchro to Digital converter. The synchro signal representing the antenna angle is converted to a 14-bit natural binary representation by the Synchro to Digital converter SDC1704. The digital angle is applied to the digital input of the DTM1716. A dc voltage is applied to the DTM1716 analog input which controls the radius of the displayed raster. The output voltages are used to provide the X and Y time base currents. The switches across the capacitors are opened on the leading edge of the transmission pulse and closed after a time interval determined by the range.

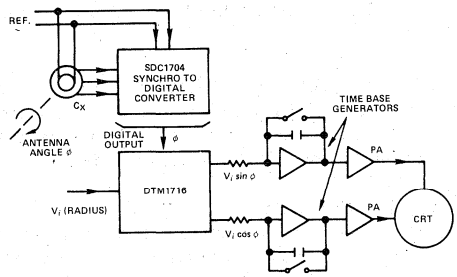


Figure 3. PPI Waveform Generation Using the DTM1716

AXIS ROTATION

Figure 4 shows how two DTM1716's may be used to compute the new two dimensional coordinates of a point relative to a rotated set of axes. The input voltage X_1 and Y_1 are proportional to the coordinates of a point in the XY plane. If a digital angle ϕ is applied to the DTM1716's, the output voltages X_2 and Y_2 correspond to the X and Y coordinates of the point relative to a set of axes rotated through the angle ϕ. The systems can be extended to three dimensions.

The arrangement as shown in Figure 4 may also be used to obtain the new coordinates of a point which is rotated through the angle in the same coordinate set. This scheme provides a low cost, accurate and compact solution to transformation problems.

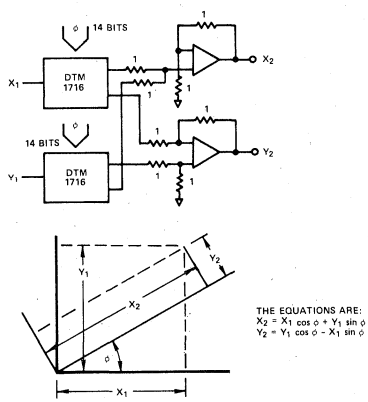


Figure 4. Axis Rotation in Two Dimensions Using the DTM1716

SYNCHRO TO INVARIANT SINE/COSINE

In many engineering applications it is required to obtain voltages proportional to the sine and cosine of an angular movement and to be able to scale the voltages electrically. Figure 5 shows how a Synchro to Digital converter and the DTM1716 may be used for this purpose. The advantage of this scheme is that the coefficients of sine and cosine are electrically scalable by means of the bipolar voltage V_i, saving memory space, multipliers, power and space.

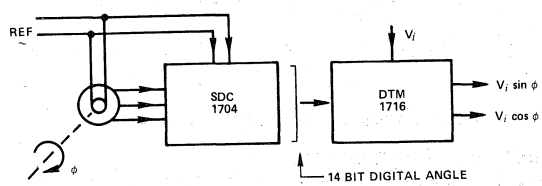


Figure 5. Synchro to Invariant Sine/Cosine Using the SDC1704 and DTM1716

POWER SPECTRUM ANALYSIS

Figure 6 shows a less usual application of the DTM1716 in the spectrum analysis of low frequency signals. This has the advantage of providing almost infinite resolution at extremely low relative cost.

A simple method of obtaining the power in the frequency interval $f \pm \Delta f$ is shown in Figure 6.

The input waveform from which the power spectrum is required is g(t). Multiplication of this waveform by Sin $2\pi ft$ causes the energy in the waveform between $f - \Delta f$ and $f + \Delta f$ to be shifted to lie between $-\Delta f$ and $f + \Delta f$. The low pass filter passes this voltage waveform to the square law devices to produce an output proportional to the power. Two channels, sine and cosine, are used for the case where g(t) may contain a periodic component. If for example there is a line in the power spectrum, without the use of the two channels the output at that frequency would depend upon its phase. The use of both sine and cosine multiplication avoids this problem.

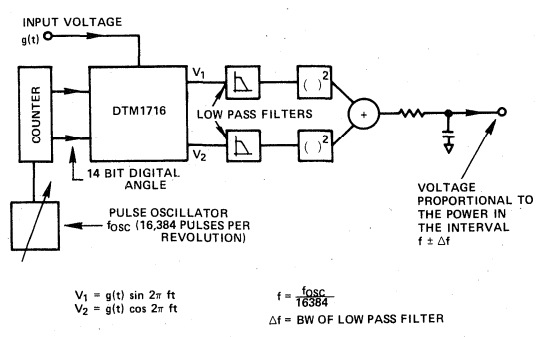


Figure 6. The Use of the DTM1716 to Obtain the Power Frequency Spectrum of g(t)

PHASE MODULATION

The DTM1717 can be used for low frequency phase modulation of subcarriers. Figure 7 shows the method which uses two DTM1717's and an ADC. Frequency modulation can be obtained if the amplitude of the signal is made to be inversely proportional to its frequency. This can be accomplished by inserting an integrator in series with the modulation input. Similar techniques can be used for very low frequency synthesis.

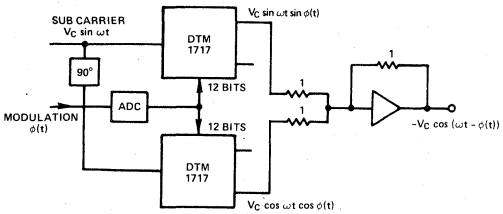


Figure 7. Phase Modulation Using 2 DTM1717's

ORDERING INFORMATION

There are only two options for each of the DTM1716 and DTM1717. They are the commercial or extended temperature ranges. The appropriate designations are as follows:

DTM1716500 (14 bits) 0 to +70°C
DTM1716600 (14 bits) -55°C to +105°C
DTM1717500 (12 bits) 0 to +70°C
DTM1717600 (12 bits) -55°C to +105°C

OTHER PRODUCTS

Many modules concerned with the conversion of synchro data are manufactured by us, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

SYNCHRO TO DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4") converter with a 12-bit natural binary output. Its overall accuracy is ±8.5 arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz.

The SDC1702 is similar to the new SDC1700 but has a 10-bit natural binary output and an overall accuracy of +22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14-bit natural binary output and an overall accuracy of ±2.0 arc-minutes ±1LSB.

The SBCD1752/1753/1756 and 1757 are Synchro to Digital converters based on the SDC1700 which give an output in BCD format.

DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 14 bits are available as well as the DSC1710 which is a one card, 1 channel, two speed DSC system containing its own 20VA power amplifiers.

TWO SPEED PROCESSORS

The TSL1612 combines the digital outputs of the two Synchro to Digital converters in a two speed system in order to produce a single digital word representing the input angle. It is available for any ratio between 2:1 and 36:1.

ANALOG DEVICES

Inductosyn to Digital Converter

IDC 1703

FEATURES
Low Cost
3600, 4000 or 4096 Pulses Per Period
150 Revolutions Per Second Tracking
Low Profile 0.4" (10.2mm)
Velocity Voltage Output
12-Bit Resolution

DESCRIPTION

The inductosyn* converter type IDC 1703 has been specially designed for use with displacement and angle measuring inductosyn systems. It gives out serial up down pulses corresponding to 1/N of the inductosyn pitch together with "up down" pulses for each complete pitch.

The IDC 1703 takes as inputs amplified signals from the inductosyn slider; the input voltages should be 2.5V rms maximum. The inductosyn is used as though it were a resolver transmitter. A diagram showing the method of application is shown opposite, below. It is formed from two basic parts i.e., a fixed scale and a slider. The fixed scale is energized from a current source, typical currents will be from 100 to 500mA at frequencies between 2 and 10kHz. The slider which has two displaced tracks is transformer coupled to the fixed track. The voltage induced in the two slider tracks must be amplified; the gain of the amplifiers should be equal and sufficient to produce voltages of 2.5V maximum for the IDC 1703.

SIGN CONVENTION

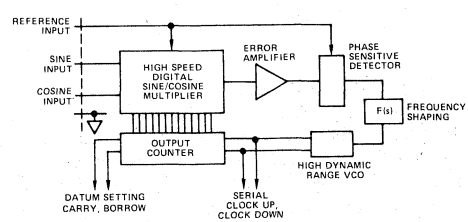
The three inputs to the converter i.e., Sine, Cosine and Reference have a common input terminal, "ground". The connection arrangement is such that if a period of track is regarded as a revolution of 360°, then: – the sine input, cosine input, and reference signal waveforms must all be in time phase in the first 90°.

SYSTEM PHASE SHIFTS

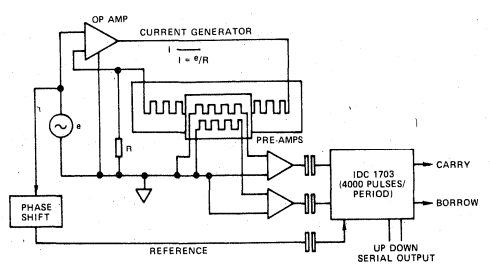
The converter has been designed to work with the reference signal and the data signals either in phase (or out of phase according to angle).

With an inductosyn the L/R ratio is so low that the output voltages on the slider are not in phase with the voltage or current of the scale. For this reason it is necessary for the user to either phase shift the drive to the scale relative to the reference source or to phase shift the reference phase fed to the converter relative to the source. The phase shift required will be nearly 90° when lower carrier frequencies are used, and for higher frequencies will be dependent upon the value of Tan^{-1} X/R of the scale.

The block marked "phase shift" in the figure is probably the most suitable place. A phase lead circuit giving a few degrees less than 90 will be required.



Functional Diagram of the IDC 1703 Tracking Converter



The Inductosyn Used Simulating a Resolver Control TX

*Farrand Inc. Trade Mark

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

FREQUENCY	5kHz (Nominal)
ACCURACY	±9 arc-minutes (Note 1)
RESOLUTION	1 Part in 3600 or 4000 or 4096 (N)
OUTPUTS (Incremental)	Serial 0.2μs to 0.8μs Negative Pulses at TTL Levels for Up Down Counts; Each Count Corresponding to 1/4000 of the Pitch.
OUTPUTS (Complete Pitches)	0.2μs to 0.8μs Negative Pulses at TTL Levels (MSB carry, borrow). These Pulses Occur at Every Complete Pitch of the Inductosyn; They Facilitate Datum Setting.
OUTPUT LOADING	1 Low Level TTL Load
TRACKING RATE	150 Revolutions Per Second (Pitches/Sec).
ACCELERATION	250 Revolutions Per Second Per Second (Pitches/Sec^2) (1LSB Error)
SIGNAL INPUTS	Resolver Form 2.5V rms
INPUT IMPEDANCE (Signal)	3.33kΩ
REFERENCE INPUT	2.5V rms
REFERENCE INPUT IMPEDANCE	10kΩ
SIGNAL AND REFERENCE DATUM	With Respect to Power Supply, Common
VELOCITY VOLTAGE	±10V for ±150 Revolutions Per Second
POWER SUPPLIES	+15V @ 25mA +5V @ 70mA -15V @ 25mA
POWER DISSIPATION (Maximum)	1.1 Watts
TEMPERATURE RANGE	0 to +70°C
WARM UP	<1sec
DIMENSIONS	3.125" x 2.625" x 0.40" (79.3mm x 66.6mm x 10.2mm)

NOTE 1 Accuracy applies for:
±10% reference and signal amplitude variation, 10% reference and signal distortion.
±5% power line variation
Accuracy includes quantization errors.

Specifications subject to change without notice.

PINS AND THEIR FUNCTIONS

Electrical connections to the IDC 1703 is made by means of 0.040 ±0.001" diameter hard gold plated brass pins of length 0.20" (1.02mm ±0.025mm dia. 5mm in length). The module is usually plugged into sockets in the printed circuit board. For environmental conditions of high vibration the pins may be soldered directly into the printed circuit board. The pin designations and their function is as follows:

VEL This pin provides an analog voltage proportional to velocity of ±10V for ±150 revolutions per second.

SIN, COS These are input pins. The sine and cosine inputs must be applied between these pins and common. The input should be ac coupled. The input impedance is 3.3kΩ. The signal levels should be 2.5V rms.

REF This is an input pin. The ac reference voltage of 2.5V rms must be applied to this pin. The input should be ac coupled.

GND This is the common pin for all inputs and outputs and the power supply.

+15V This is a power line pin +15V ±5% must be connected between this pin and GND.

-15V This is a power line pin -15V ±5% must be connected between this pin and GND.

+5V This is the power line pin. A voltage of +5 Volts ±5% from a low impedance source must be connected between this pin and GND.

UP, DOWN These pins are output pins. Pulses 0.2μs to 0.8μs in length at TTL levels appear on one or other of these pins as the input is changed. The pulses appear on the UP pin for increasing distance and on the DOWN pin for decreasing distance. The pulse spacing corresponds to 1/4000th of the inductosyn pitch. The output loading is 1TTL Load.

CARRY, BORROW These pins are output pins. Pulses of 0.2μs to 0.8μs in length at TTL levels appear on these pins at the transition from one period of the inductosyn to the next. The pulse occurs on the CARRY or BORROW pin according to whether the distance is increasing or decreasing. The output loading is 1TTL Load.

RESET This pin resets the internal counter. TTL positive pulse 1μs nominal width.

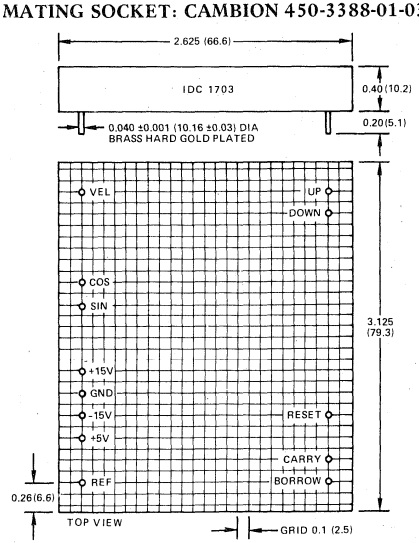
SIGN CONVENTION

The three inputs to the converter i.e., SIN, COS and REF have a common input, GND. The connection arrangement is such that if the pitch is regarded as a revolution of 360°, then SIN, COS and REF waveforms are all in time phase in the first 90°.

IDC 1703
ORDERING INFORMATION

Model	Pulses Per Period
IDC 1703/3600	3600
IDC 1703/4000	4000
IDC 1703/4096	4096

MATING SOCKET: CAMBION 450-3388-01-03



Pin Connections for IDC 1703.
Dimensions shown in inches and (mm).

Synchro/Resolver to Linear DC Converter

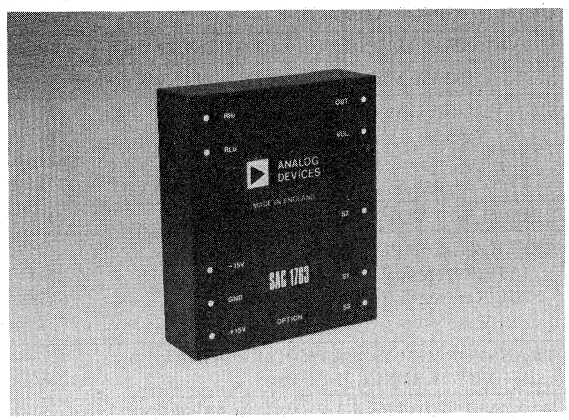
SAC1763

FEATURES

- High Dynamic Performance (27,000°/sec)
- High Accuracy (±11 Arc-Minutes)
- Internal Converter Tracking Loop Provides High Noise Immunity
- Low Output Ripple (Less than 5mV p-p)
- DC Output Proportional to Input Rate
- 50Hz to 2.6kHz Reference Frequency Operation
- Self Contained—No External Transformers or Adjustments Needed

APPLICATIONS

- Measurement and Recording of Synchro or Resolver Information on Chart Recorders, X-Y Plotters, FM Recorders, Etc.
- Servo Control and Positioning



GENERAL DESCRIPTION

The SAC1763 is a Synchro/Resolver to Linear dc Converter. It takes input angular information in synchro or resolver form voltages and gives an output voltage which is linearly proportional to the input angle. The output voltage of ±10V at ±5mA represents an input angular change of ±180 degrees of the synchro or resolver format signals applied to the converter input.

Options are available for all the standard line to line voltages and frequencies for either synchro or resolver inputs. These options together with commercial or extended temperature ranges are determined by a code following the type number (see ordering information).

An important feature of the SAC1763 series converters is that no external transformer modules are required. The transformer isolation is carried out by micro transformers which are inside the converter module *even for the 60Hz versions.*

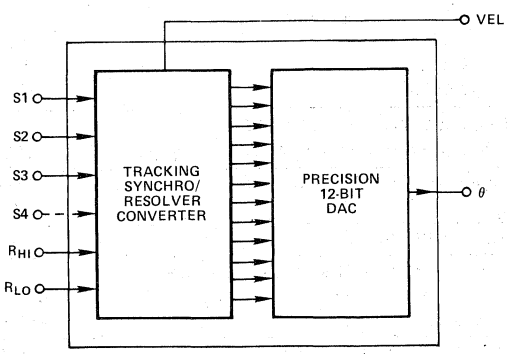
When converters are used in control loops, it is often useful to have a voltage which is proportional to angular velocity. This voltage is available and has been brought out on all SAC1763 converters. The availability of the velocity voltage eliminates the need for a tachometer for stabilization.

MODELS AVAILABLE

Options of the SAC1763 are available to cover all the standard synchro and resolver voltages and frequencies. In addition, options exist for standard operating temperature (0 to +70°C) and extended operating temperature (-55°C to +105°C) (see ordering information).

THEORY OF OPERATION

The SAC1763 is based upon the well proven 12-bit tracking Synchro/Resolver Converter type SDC1700. This is followed by a 12-bit precision DAC (Digital to Analog Converter).



SPECIFICATIONS (max at 25°C unless otherwise stated)[1]

Model	SAC1763
ACCURACY[2]	±11 arc-minutes
RESOLUTION	1 part in 4096
ANALOG OUTPUT	±10V Representing ±180° 5mA is Available
OUTPUT DRIFT	0.175 arc-minutes per °C
OUTPUT RIPPLE AND NOISE	< 5mV p-p
SIGNAL AND REFERENCE FREQUENCY[1]	60Hz, 400Hz and 2.6kHz
SIGNAL INPUT VOLTAGE (LINE TO LINE)	90V, 26V or 11.8V rms
SIGNAL IMPEDANCE	
90V Signal	200kΩ Resistive
26V Signal	58kΩ Resistive
11.8V Signal	27kΩ Resistive
REFERENCE VOLTAGE	115V, 26V or 11.8V rms
REFERENCE IMPEDANCE	
115V Reference	270kΩ
26V Reference	56kΩ
11.8V Reference	27kΩ
TRANSFORMER ISOLATION ON SIGNAL AND REFERENCE INPUTS	500V dc
MAX INPUT RATES FOR FULL ACCURACY	
60Hz Options	5revs/sec
400Hz Options	36revs/sec
2.6kHz Options	75revs/sec
MAX ACCELERATION ON INPUT FOR ADDITIONAL ERROR LESS THAN 6 ARC-MINUTES	
60Hz Options	166°/sec²
400Hz Options	9668°/sec²
2.6kHz Options	45,528°/sec²
STEP RESPONSE (179° Step) (For less than 6 arc-minutes error)	
60Hz	1.5sec
400Hz	125ms
2.6kHz	50ms
VELOCITY VOLTAGE OUTPUT (See also Specifications on the next page)	±10V nominal for ∓max input rate of the option
POWER SUPPLY REQUIREMENTS	+15V at 150mA -15V at 45mA
POWER DISSIPATION	2.93 watts
OPERATING TEMPERATURE RANGE	
Standard	0 to +70°C
Extended	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
DIMENSIONS	3.12" X 2.625" X 0.8" (79.4mm X 66.7mm X 20.3mm)
WEIGHT	7 ozs. (200 grams)

NOTES

[1] The converters can be used over the following reference frequency ranges with no loss of accuracy. They will, however, retain the dynamic characteristics (input rate and acceleration) quoted for the particular option.

60Hz options can be used over 50Hz to 800Hz
400Hz options can be used over 400Hz to 2000Hz
2.6kHz options can be used over 2kHz to 3.5kHz

[2] Accuracy is specfied for the following conditions:

(a) ±10% signal and reference amplitude variation.
(b) ±10% signal and reference harmonic distortion.
(c) ±5% power supply variation.

Specifications subject to change without notice.

CONNECTING THE CONVERTER

The electrical connections to the converter are straighforward. The power lines, which must not be reversed, are ±15V. They must be connected to the "+15V" and "-15V" pins with the common connection to the ground pin "GND".

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND.

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$$

The system reference voltage is connected to pins "R_{HI}" and "R_{LO}" in accordance with the above convention.

The analog output voltage representing the digital angle is between the pin "OUT" and "GND", ±10V corresponding to ±180 degrees. Up to 5mA may be taken from the "OUT" pin. The relationship between the output voltage and the input angle is shown in the diagram below.

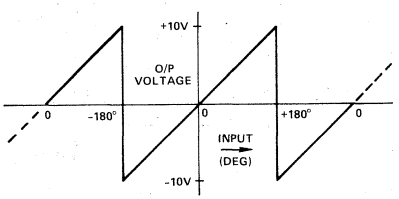


Diagram Showing Relationship Between Input and Output

Sometimes, it is required that the input/output relationship of the converter is the other way round. This can be achieved in the case of synchro options by interchanging connections "S1" and "S3". This is shown in the diagram below.

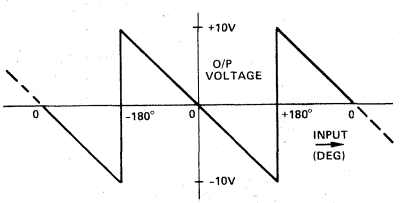


Diagram Showing Relationship Between Input and Output When "S1" and "S3" are Interchanged

VELOCITY PIN

The analog voltage proportional to the rate of change of angle is provided between the pins VEL and GND. The variation is ±10.0V nominal for the maximum velocity of the option.

This pin provides a dc voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the following table.

Scaling of Output Voltage for One Fifth max Velocity	2 Volts (Nominal)
Output Voltage Temp. Coeff.	0.05%/°C of Output
Output Voltage Drift (All Models)	0 to +70°C ±50μV/°C -55°C to +105°C ±100μV/°C
Linearity	0 to 100°/sec 60Hz Options 1.5% 0 to 800°/sec 400Hz Options 2% 0 to 1600°/sec 2.6kHz Options 2%
Noise (0 to 20Hz)	60Hz Options: 0 to 200°/sec 2mV rms 400Hz Options: 0 to 1600°/sec 2mV rms 2.6kHz Options: 0 to 3300°/sec 2mV rms
Impedance (Output)	1Ω
max Current Available	1mA

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

The SAC1763 velocity outputs do not have the disadvantages of being inefficient at low speeds and do not need gearing required by tachometers. In addition, the output is available at no extra cost.

For other velocity output scaling and linearity consult the factory.

RESISTIVE SCALING OF INPUTS

A feature of this converter is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 2.2kΩ per extra volt of reference in series with "R_{HI}".

In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 2.2kΩ per extra volt of reference in series with "R_{HI}".

For example, assume that we have an 11.8V line to line, 26V reference Synchro Converter, and we wish to use it with a 60V line to line signal with a 115V reference.

In each signal input line, the extra voltage capability required is:

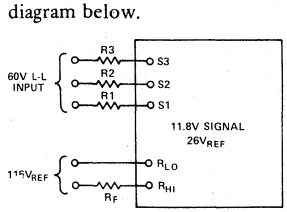
$$60 - 11.8 = 48.2V$$

Therefore each one of the three resistors needs to have a value of:

$$48.2 \times 1.11 = 53.5k\Omega$$

Similarly the single resistor needed in series with "R_{HI}" can be calculated as being 195.8kΩ.

The inputs of the converter can therefore be scaled as in the diagram below.



R1, R2, R3 = 53.5kΩ
R_F = 195.8kΩ

NOTE
IN THE CASE OF THE SIGNAL RESISTORS THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF R_F IS NOT CRITICAL.

USING THE CONVERTERS WITH OTHER THAN THE SPECIFIED REFERENCE FREQUENCY

The converters can be used with different reference frequencies, other than those for which they are basically specified, with no resulting loss of accuracy (see below). However, they will retain the dynamic characteristics given in the specification.

Basic Option	Frequency Range for no Loss in Accuracy
60Hz	50Hz → 800Hz
400Hz	400Hz → 2000Hz
2.6kHz	2kHz → 3.5kHz

TRANSFER FUNCTION

The transfer functions for the three reference frequency options of the converters are shown below.

60Hz Options

$$\frac{\theta_0}{\theta_1} = \frac{1.9 \times 10^5 \, (1 + 5.6 \times 10^{-2} s)}{s^3 + 1.03 \times 10^2 s^2 + 1.08 \times 10^4 s + 1.9 \times 10^5}$$

400Hz Options

$$\frac{\theta_0}{\theta_1} = \frac{8.8 \times 10^7 \, (1 + 6.8 \times 10^{-3} s)}{s^3 + 8.04 \times 10^2 s^2 + 6.1 \times 10^5 s + 8.8 \times 10^7}$$

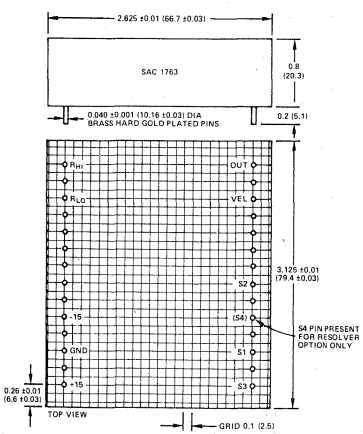
2.6kHz Options

$$\frac{\theta_0}{\theta_1} = \frac{10^9 \, (1 + 3.3 \times 10^{-3} s)}{s^3 + 1.7 \times 10^3 s^2 + 3.303 \times 10^6 s + 10^9}$$

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



APPLICATIONS OF THE SAC1763

The SAC1763 may be used to record synchro or resolver information, from for example gyrocompasses or other navigational aids, on to equipment such as X-Y recorders, chart recorders or FM tape recorders, see below.

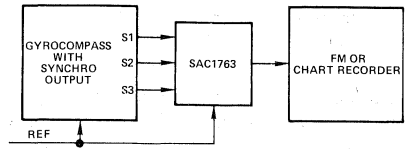


Diagram Showing Gyrocompass Information Being Recorded Using SAC1763

DIAGRAM SHOWING GYROCOMPASS INFORMATION BEING RECORDED USING SAC1763

The applications of the SAC1763 are not only in measurement of synchro or resolver information but also in controlling angular movement. The diagram below shows the SAC1763 being used inside an angular control loop where the input is a dc voltage. The availability of the velocity voltage eliminates the need for an electromechanical tachometer for stabilization purposes.

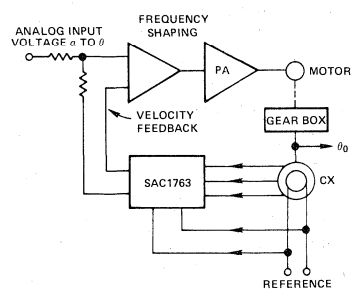


Diagram Showing the SAC1763 Used in a Servo System Where the Input is a dc Voltage

ORDERING INFORMATION

The full part number for all the standard converter options defining reference and signal voltage and frequency, operating temperature range and whether Synchro or Resolver format is given below. It should also be remembered that the signal and reference inputs can be resistively scaled (see section "Resistive Scaling of Inputs") and that in certain cases reference frequencies other than those specified can be used. (See section "Using the Converters with other than the Specified Reference Frequency".)

Part Number	Operating Temp. Range	L to L Voltage/Format	Ref. Voltage	Ref. Freq.
SAC1763511	0 to +70°C	11.8V Synchro	26 Volts	400Hz
SAC1763611	-55°C to +105°C	11.8V Synchro	26 Volts	400Hz
SAC1763512	0 to +70°C	90.0V Synchro	115 Volts	400Hz
SAC1763612	-55°C to +105°C	90.0V Synchro	115 Volts	400Hz
SAC1763522	0 to +70°C	90.0V Synchro	115 Volts	60Hz
SAC1763622	-55°C to +105°C	90.0V Synchro	115 Volts	60Hz
SAC1763513	0 to +70°C	11.8V Resolver	11.8 Volts	400Hz
SAC1763613	-55°C to +105°C	11.8V Resolver	11.8 Volts	400Hz
SAC1763514	0 to +70°C	26.0V Resolver	26 Volts	400Hz
SAC1763614	-55°C to +105°C	26.0V Resolver	26 Volts	400Hz
SAC1763518	0 to +70°C	11.8V Resolver	26 Volts	400Hz
SAC1763618	-55°C to +105°C	11.8V Resolver	26 Volts	400Hz
SAC1763543	0 to +70°C	11.8V Resolver	11.8 Volts	2.6kHz
SAC1763643	-55°C to +105°C	11.8V Resolver	11.8 Volts	2.6kHz
SAC1763544	0 to +70°C	26.0V Resolver	26 Volts	2.6kHz
SAC1763644	-55°C to +105°C	26.0V Resolver	26 Volts	2.6kHz
SAC1763548	0 to +70°C	11.8V Resolver	26 Volts	2.6kHz
SAC1763648	-55°C to +105°C	11.8V Resolver	26 Volts	2.6kHz

ANALOG DEVICES

BCD Output Synchro to Digital Converters

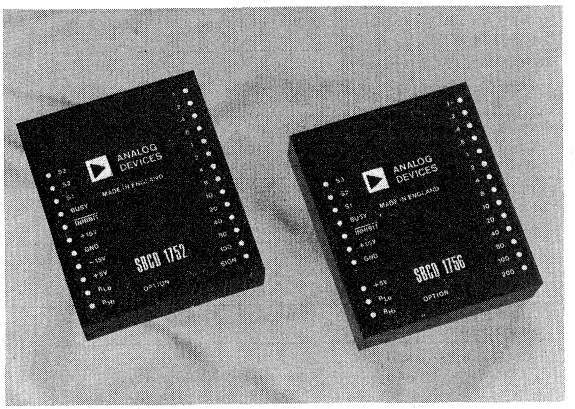
SBCD 1752/1753/1756/1757

FEATURES

- **BCD (Binary Coded Decimal) Output Representing 0 to 359.9° or 0 to ±179.9°**
- **-15V Power Supply Requirement Optional**
- **High Tracking Rate (75 revs/sec)**
- **Internal Microtransformers for 60Hz, 400Hz and 2.6kHz Options**
- **Voltage Scaling with External Resistors (Unique Feature)**
- **Transformer Isolated Outputs**
- **Low Cost**
- **MIL Spec/Hi Rel Options Available**

APPLICATIONS

- **Visual Display of Angular Information**
- **Valve Position Indication**
- **Antenna Monitoring**
- **Industrial Controls**



GENERAL DESCRIPTION

The SBCD1752, SBCD1753, SBCD1756 and the SBCD1757 are modular, continuous tracking Synchro/Resolver to Digital converters which employ a type 2 servo loop.

They are intended for use in both Industrial and Military applications either for displaying angular data directly, or for inputting BCD information directly into a data processing system.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in parallel Binary Coded Decimal (BCD).

Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

One of the outstanding features of these converters is the use made of precision Scott T and reference microtransformers. *This has made it possible to include the transformers within the module, even for the 60Hz version as well as providing facilities for external voltage scaling.*

MODELS AVAILABLE

The four Synchro to Digital converters described in this data sheet, differ primarily in the areas of output format and power supply requirements.

Model SBCD1752XYZ is a 13-bit plus sign, BCD output converter, giving -180.0° to -0.1° and +0.0 to +179.9° requiring ±15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

Model SBCD1753XYZ is a 14-bit, BCD output converter, giving 0 to 359.9°, requiring ±15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

Model SBCD1756XYZ is a 13-bit plus sign, BCD output converter, giving -180.0° to -0.1° and +0.0 to +179.9° requiring +15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

Model SBCD1757XYZ is a 14-bit, BCD output converter, giving 0 to 359.9°, requiring +15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

The XYZ code defines the option thus:

X signifies the operating temperature range.
Y signifies the reference frequency.
Z signifies the input voltage and range and whether it will accept Synchro or Resolver information.

More information about the option code is given under the heading "Ordering Information".

DATA TRANSFER (ALL MODELS)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin. The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the option (see Specifications table). The converter is busy when the BUSY pin is at TTL "High" level. The pulses occur for increasing and decreasing counts.

The most suitable time for transferring data is 400ns after the trailing edge of the BUSY pulse, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.

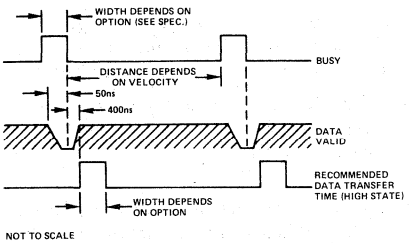
SPECIFICATIONS (typical at 25°C unless otherwise stated)

MODELS	SBCD1752	SBCD1753	SBCD1756	SBCD1757
ACCURACY[1] (max Error)				
All Frequency Options	±0.2 Degrees	*	*	*
OUTPUT	Parallel BCD, 8TTL Loads	*	*	*
RESOLUTION	13-Bit + Sign Representing −180.0° to −0.1° and +0.0° to +179.9°	14 Bit Representing 0 to 359.9°	*	**
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz and 2.6kHz	*	*	*
SIGNAL VOLTAGE (Line to Line)				
Low Level	11.8V rms	*	*	*
High Level	90.0V rms	*	*	*
SIGNAL IMPEDANCES				
Low Level	26kΩ (Resistive)	*	*	*
High Level	200kΩ (Resistive)	*	*	*
REFERENCE VOLTAGE				
Low Level	26V (11.8V Signal)	*	*	*
High Level	115V (90V Signal)	*	*	*
REFERENCE IMPEDANCE				
Low Level	56kΩ (Resistive)	*	*	*
High Level	270kΩ (Resistive)	*	*	*
TRANSFORMER ISOLATION	500V dc	*	*	*
TRACKING RATE (min)				
60Hz	5 Revolutions Per Second	*	*	*
400Hz	36 Revolutions Per Second	*	*	*
2.6kHz	75 Revolutions Per Second	*	*	*
Accel.[1] Constant K_a				
60Hz	2000/sec^2	*	*	*
400Hz	120,000/sec^2	*	*	*
2.6kHz	600,000/sec^2	*	*	*
STEP RESPONSE (179° Step) (For 0.1° Error)				
60Hz	1.5sec	*	*	*
400Hz	125ms	*	*	*
2.6kHz	50ms	*	*	*
POWER LINES	+15V @ 25mA	*	+15V @ 80mA	***
	−15V @ 25mA	*	+5V @ 500mA	***
	+5V @ 500mA	*		
POWER DISSIPATION	3.25 Watts	*	3.7 Watts	***
BUSY LOGIC OUTPUT, POSITIVE PULSE (1 TTL Load)				
60Hz	3.5 to 4.5μs	*	*	*
400Hz	0.5 to 1.25μs	*	*	*
2.6kHz	0.5 to 1.25μs	*	*	*
MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity)				
60Hz	40μs	*	*	*
400Hz	5.0μs	*	*	*
2.6kHz	1.8μs	*	*	*
INHIBIT INPUT (To Inhibit)	Logic "0" 1TTL Load	*	*	*
TEMPERATURE RANGE				
Operating	0 to +70°C Standard	*	*	*
	−55°C to +105°C Extended	*	*	*
Storage	−55°C to +125°C	*	*	*
DIMENSIONS	3.125" x 2.625" x 0.8"	*	*	*
	(79.4 x 66.7 x 20.4mm)	*	*	*
WEIGHT	6.4 ozs. (180 grams)	*	6.5 ozs. (185 grams)	***

[1] Specified over the appropriate operating temperature range and for
(a) ±10% signal and reference amplitude variation
(b) 10% signal and reference harmonic distortion
(c) ±5% power supply variation
(d) ±10% variation in reference frequency.

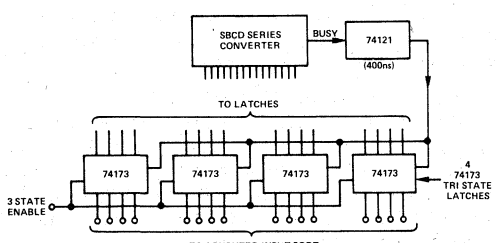
*Specifications same as SBCD1752
**Specifications same as SBCD1753
***Specifications same as SBCD1756

Specifications subject to change without notice.



Data Transfer Diagram

The function of the $\overline{\text{INHIBIT}}$ pin is to enable the user to inhibit the update of the converter's output counter. This is achieved by taking the $\overline{\text{INHIBIT}}$ pin to a TTL Logic zero. If used, the $\overline{\text{INHIBIT}}$ should be applied 400ns after the trailing edge of the BUSY pulse. This will ensure that the data on the output pins is valid. The data should then be transferred and the $\overline{\text{INHIBIT}}$ released before the next BUSY pulse occurs. The worst case times allowable for data transfer in this case are shown in the Specifications under the heading of "MAX DATA TRANSFER TIME (from 400ns After Trailing Edge of BUSY at Max Velocity)". It should be noted that the application of the $\overline{\text{INHIBIT}}$ will not prevent the BUSY pulses appearing on the BUSY pin, and thus if the $\overline{\text{INHIBIT}}$ is not released by the time that the next BUSY pulse occurs, the BUSY pulse will still appear, although the internal converter loop will have been opened. Under this condition, a worst case recovery time, equivalent to that of a step of 179 degrees may be encountered (see Spec.). To avoid this and to ensure valid data transfer, the system shown in the diagram is recommended.



Suggested External Interface Circuitry

In cases where the converter is connected to a data bus or used as a peripheral, the method outlined in the above diagram is recommended. The $\overline{\text{INHIBIT}}$ is not necessary in this case, and the external "Enable" has control of the converter output.

The AC1755 mounting card described later in this data sheet contains the external components shown in the diagram.

CONNECTING THE CONVERTER

The power lines, which should not be reversed, should be connected to "+15V", "-15V" and "+5V" in the case of the SBCD1752 and SBCD1753, and to "+15V" and "+5V" in the case of the SBCD1756 and SBCD1757, with the common connection to "GND" in all cases.

It is suggested that 0.1μF and 6.8μF capacitors by placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output connections in the case of the SBCD1753 and SBCD1757 should be taken from the pins marked "0.1" through to "200"; these values being represented in degrees.

In the case of the SBCD1752 and SBCD1756, the data should be taken from the pins marked "0.1" through to "100", these values also being represented in degrees. In the case of these latter units the "SIGN" pin will indicate the polarity of the output, Logic "0" representing positive angles and Logic "1" representing negative angles.

In the case of a synchro, the signals are connected to S_1, S_2 and S_3 according to the following convention:

Synchro connection

$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$
$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$
$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

Resolver Connection

$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$
$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$

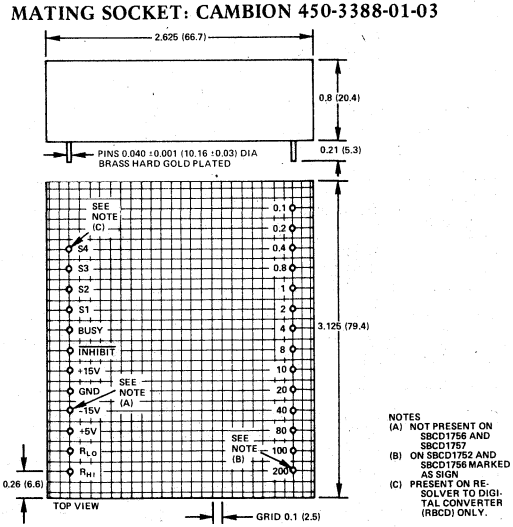
The BUSY and $\overline{\text{INHIBIT}}$ pin (is used), should be connected as described under the heading "DATA TRANSFER".

The reference connections are made to pins R_{HI} and R_{LO}.

PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03

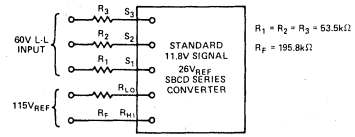


RESISTIVE SCALING OF INPUTS

A unique feature of the SBCD1752/1753/1756/1757 converters is that the inputs can be resistively scaled to accommodate any value of input signal and reference voltage.

In order to calculate the values of the external scaling resistors necessary, add 1.11kΩ in series with the input per extra volt in the case of the signal, and 2.2kΩ per extra volt in the case of the reference.

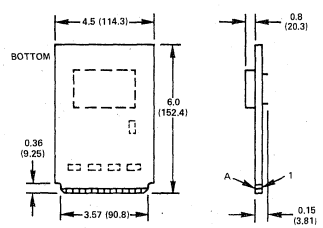
For example, assume that it is required to use a standard 11.8V line to line signal, 26V reference converter with 60V line to line signal and a 115V reference. The resistors should be arranged as in the diagram.



Note: In the case of R_1, R_2, and R_3, the ratio error between the resistances is more critical than the absolute value. In general a 1% ratio error will give rise to an extra inaccuracy of 0.28 Degrees, while a ratio accuracy of 0.1% will give rise to an extra inaccuracy of 0.028 Degrees. The absolute value of R_F is not critical.

CARD MOUNTING

All the converters can be mounted on an AC1755 mounting card. This card contains the latches and monostable, described under the "DATA TRANSFER" heading, which are necessary to transfer the data on to a computer bus system, as well as sockets for the converter. The latches have a tri-state output to facilitate ease of use. The AC1755 also contains facilities for the inclusion of input signal scaling and reference resistors as described under the heading "RESISTIVE SCALING OF INPUTS". The card uses a 22/22 0.156" pitch edge connector. The pin-out is shown below. If it is not required to use the external latches, they can be jumpered on the board.



AC1755 Mounting Card (First Angle Projection). Dimensions Shown in Inches and (mm).

Edge Pin Number	Function	Edge-Pin Letter	Function
1	R (Lo)	A	Tri-State Enable
2	R (Hi)	F	+15 Volts
3	S_3	H	+15 Volts
4	S_2	J	-15 Volts (3)
5	S_1	K	-15 Volts (3)
6	S_4	L	GND
		M	GND
13	BUSY	N	+5 Volts
15	INHIBIT	P	+5 Volts
16	0.1	T	8
17	0.2	U	10
18	0.4	V	20
19	0.8	W	40
20	1	X	80
21	2	Y	100
22	4	Z	200 (1) SIGN (2)

NOTES
(1) SBCD1753 and SBCD1757 only
(2) SBCD1752 and SBCD1756 only
(3) SBCD1752 and SBCD1753 only

AC1755 Mounting Card Edge Connections

ORDERING INFORMATION

Converters should be ordered by the appropriate part number (i.e., SBCD1752, SBCD1753, SBCD1756 or SBCD1757) followed by the appropriate option code.

The XYZ options are as follows:

X signifies the operating temperature range thus;
- X = 5 0 to +70°C (Commercial Temp.)
- X = 6 -55°C to +105°C (Extended Temp.)

Y signifies the reference frequency thus;
- Y = 1 signifies 400Hz
- Y = 2 signifies 60Hz*
- Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is a Synchro to Digital or a Resolver to Digital converter. The options for Z are:
- Z = 1 signifies Synchro, signal 11.8 Volts, reference 26 Volts
- Z = 2 signifies Synchro, signal 90 Volts, reference 115 Volts
- Z = 8 signifies Resolver, signal 11.8 Volts, reference 26 Volts

Thus an SBCD1753 with a commercial (0 to +70°C) operating range, using a 400Hz, 26 volt reference with an 11.8 volt signal would be ordered as an SBCD1753511.

*For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

In addition a 400Hz unit will work with a 2.6kHz reference and a 60Hz unit will work with a 400Hz reference; however they will have the velocity and acceleration characteristics of the lower frequency rated unit.

OTHER PRODUCTS

The SBCD series of Synchro to Digital converters are just a few of the modules and instruments concerned with Synchro conversion manufactured by us. Some of our other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

SYNCHRO TO DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4") converter with a 12-bit natural binary output. Its overall accuracy is ±8.5 arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz. The SDC1702 is similar to the SDC1700 but has a 10-bit natural binary output and an overall accuracy of ±22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14-bit natural binary output and an overall accuracy of ±2.0 arc-minutes ±1LSB.

TWO SPEED PROCESSORS

The TSL1612 and the TSL1729 both produce one digital output word up to 20 bits in length from the outputs of 2 Synchro to Digital converters in a coarse/fine system. The TSL1612 is used for ratios of 9:1, 18:1 and 36:1, while the TSL1729 is programmable for all ratios from 1:1 to 63:1.

DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 16 bits are available as well as the DSC1710, a one card, 2 channel, 40VA, DSC system including power amps for use with 2 speed coarse/fine ratios of 9:1, 18:1, 36:1.

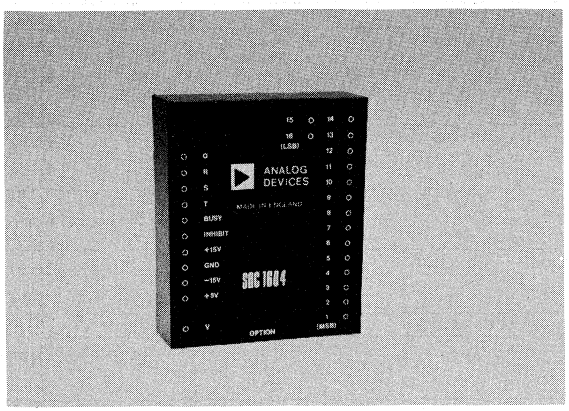
ANALOG DEVICES

Synchro to Digital Converters

SDC1604 SERIES

FEATURES
Tracking Rates Up to 360 Degrees/sec
Accuracies Up to ±1 minute of arc
Resolution of 16 bits for 360°
TTL/DTL Compatible
MIL Spec/Hi Rel Versions

APPLICATIONS
Airframe Data Processing
Position Monitoring
Navigational Computation



GENERAL DESCRIPTION

The "SDC" series converters are continuous tracking, type 2 servo loop, synchro or resolver to digital converters intended for military and industrial control applications.

The Synchro to Digital Converters (SDC's) work from either 3 wire synchro plus reference input signals or resolver plus reference input signals giving binary angular output data. The inputs are usually derived from remote synchros or resolvers but may be derived from electrically simulated resolvers or synchros i.e., Digital to Synchro converters (see our other product literature which describes these units).

Key to the small size and high reliability of the units is extensive use of monolithic analog switches, linear integrated circuits, MSI logic functions and thin film resistor networks.

Units have been qualified to extreme climatic, shock and vibration conditions taken from U.S. Military and Civil Aviation Specifications. Specials are available, built with hi-rel components.

MODELS AVAILABLE

The models described herein are 16-bit resolution converters which primarily differ in the area of reference frequency.

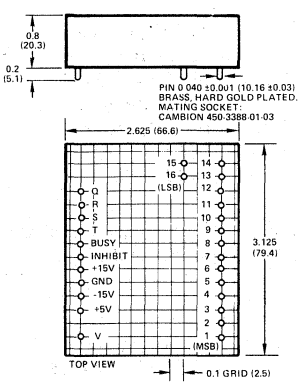
Model SDC1604XYZ is a 16-bit converter which has an over all accuracy of ±1 arc-minute.

XYZ define operating temperature range (X), reference frequency (Y) and input type/voltage (Z). The Ordering Guide gives explicit number substitutions for XYZ.

External signal and reference isolation transformers are required for use with SDC1604. They are designated as

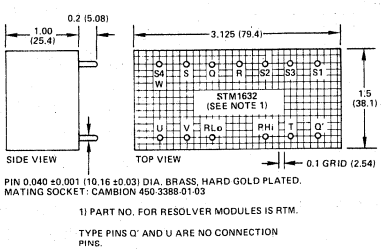
STM1632X1Z	400Hz Models
STM1672X2Z	60Hz Models

SDC1604



NOTE: ABOVE DRAWING ILLUSTRATES PIN CONNECTIONS FOR SDC1604

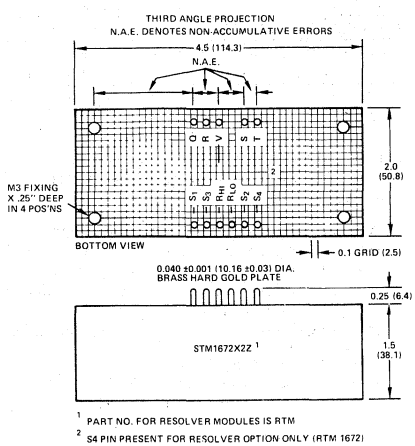
STM1632



1) PART NO. FOR RESOLVER MODULES IS RTM.

TYPE PINS Ω' AND U ARE NO CONNECTION PINS.

STM1672



[1] PART NO. FOR RESOLVER MODULES IS RTM

[2] S4 PIN PRESENT FOR RESOLVER OPTION ONLY (RTM 1672)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

SPECIFICATIONS

(typical @ +25°C and ±15V dc unless otherwise noted)

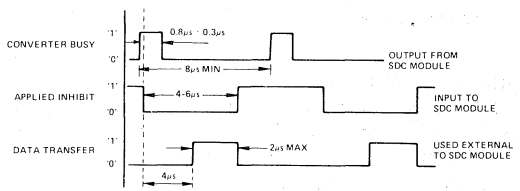
MODELS[1]	SDC1604507 plus STM163251Z SDC1604707 plus STM163271Z SDC1604507 plus STM167252Z SDC1604707 plus STM167272Z
ACCURACY[2] (max)	±1 arc-minute[3]
RESOLUTION	16 bits (1 LSB = 20 arc-seconds)
OUTPUT (in parallel)	16 bits natural binary angle
SIGNAL VOLTAGES (Line-to-Line)	
Low Level	Synchro 11.8V rms L-L Resolver 11.8V rms L-L Resolver 26.0V rms L-L
High Level	Synchro 90.0V rms L-L
SIGNAL IMPEDANCE	
Low Level	20k ohms L-L Balanced
High Level	200k ohms L-L Balanced
REFERENCE VOLTAGE	
Low Level	26V rms 400Hz or 60Hz as appropriate
High Level	115V rms 400Hz or 60Hz as appropriate
REFERENCE IMPEDANCE	
Low Level	20k ohms
High Level	200k ohms
TRANSFORMER ISOLATION	500V dc
TRACKING RATE	
400Hz	360°/sec
60Hz	360°/sec
ACCELERATION (For 1 LSB Error)	
400Hz	60°/sec²
60Hz	6°/sec²
STEP RESPONSE (179° step) (For 1 LSB Error)	
400Hz	400 milliseconds
POWER SUPPLIES	+15V at 60 milliamps -15V at 60 milliamps +5V at 300 milliamps
POWER DISSIPATION (max)	3.3 Watts
LOGIC OUTPUTS	DTL/TTL Compatible Fan Out: Four TTL Input Loads
CONVERTER BUSY, POSITIVE PULSE (±30% tolerance)	1μs
INHIBIT	DTL/TTL Compatible Fan In One TTL Input Load
TEMP. RANGE OPERATING	0 to +70°C or -55°C to +85°C
TEMP. RANGE STORAGE (All)	-55°C to +125°C
WARM UP	1 Second to Rated Accuracy
CONVERTER MODULE SIZE	3.125" x 2.625" x 0.8"
TRANSFORMER MODULE SIZE	1.5" x 3.125" x 1.0" 400Hz 2.0" x 4.5" x 1.5" 60Hz
WEIGHT	7 oz. (200gm)

NOTES:

1. Nominal 60Hz units operate over range of 50 to 400Hz. Nominal 400Hz units operate up to 1500Hz with additional 1LSB error.
2. Accuracy applies over the operating temperature range and for
   (a) ±10% signal & reference amplitude variation
   (b) ±10% reference frequency variation
   (c) 10% signal and reference harmonic distortion
   (d) ±5% power supply variation
   (e) ±20° phase shift between reference and signals
3. 16 bit accuracy is at +25°C
   ±1.3 arc-minutes from 0 to +70°C
   ±2 arc-minutes from -55°C to +85°C

DATA TRANSFER (ALL MODULES)

Whenever the input angle changes, the SDC updates its output in 1LSB steps. Data can be transferred *without error* whenever the "converter busy" signal is at a Logic "0". To transfer data the "inhibit" should be set to a Logic "0" for a time of 4-6 microseconds. The converter will ignore the inhibit command during the converter busy pulse, but after this no further update will take place until the inhibit 0 is removed. The data transfer pulse should not be more than 2 microseconds long and should be applied about 4 microseconds after the leading edge of the inhibit pulse after which the inhibit 0 should be removed to permit further updating. The "converter busy" pulses correspond to the pulses from the V.C.O. which feed the up-down counter. The pulses have a maximum length of 1.1 microseconds. It follows that if the above rules are used for data transfer, no pulses will be kept in abeyance and the control loop will not be affected. See the timing waveform.



Data Transfer Waveforms

ORDERING GUIDE

1. Specify the basic model number per the following table. 400Hz or 60Hz versions of the 16-bit units require separate transformer modules.

# of Bits	Temp. Range (X)	Freq. (Y)	Converter	Transformers
16	0 to +70°C	400Hz	SDC1604507	STM163251Z
16	-55°C to +85°C	400Hz	SDC1604707	STM163271Z
16	0 to +70°C	60Hz	SDC1604507	STM167252Z
16	-55°C to +85°C	60Hz	SDC1604707	STM167272Z

2. Z = 1 signifies synchro 11.8V L-L with 26V reference
   Z = 2 signifies synchro 90V L-L with 115V reference
   Z = 3 signifies resolver 11.8V L-L with 11.8V reference
   Z = 4 signifies resolver 26V L-L with 26V reference
   Z = 8 signifies resolver 11.8V L-L with 26V reference
   Z = 2 is available with either 400Hz or 60Hz unit
   Z = 1, 3, 4, 8 are available only with 400Hz units

3. Resolver input devices, with Z = 3, 4 or 8 are identified as RTM1632718 and the like. An R replaces the S as the first letter in the part number.

MOUNTING CARDS

Two types of PC boards are available to mount the various converters and transformer modules. Both use 22/22 0.156" pitch edge connectors.

AC1637 is used when mounting the SDC1604 alone. AC1656 is used when mounting the SDC1604 and STM1632.

ANALOG DEVICES

Low Profile Synchro/Resolver to Digital Converter

SDC1700/1702/1704 Series

FEATURES

- Internal Microtransformers for 60Hz, 400Hz and 2.6kHz References
- Low Profile (0.4")
- 10-, 12- or 14-Bit Resolution for 360°
- High Tracking Rates (75 revs/sec)
- Voltage Scaling with External Resistors (Unique Feature)
- DC Voltage Output Proportional to Angular Velocity
- Low Cost
- Lightweight 3oz. (85 grams)
- MIL Spec/Hi Rel Options Available

APPLICATIONS

- Servo Mechanisms
- Retransmission Systems
- Coordinate Conversion
- Antenna Monitoring
- Simulation
- Industrial Controls
- Fire Control Systems
- Machine Tool Control Systems

GENERAL DESCRIPTION

The SDC1700, SDC1702 and SDC1704 are modular, continuous tracking Synchro/Resolver to Digital Converters which employ a type 2 servo loop.

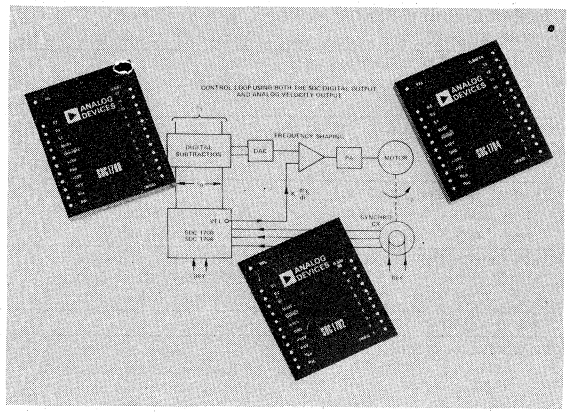
They are intended for use in both Industrial and Military applications.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in TTL compatible, parallel natural binary.

One of the outstanding features of the converters is the use of precision Scott T and reference microtransformers. *This has made it possible to include the transformers within the module, even on the 60Hz option, and yet still maintain the profile height of 0.4".*

Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

When SDC's are used in control loops, it is often useful to have a voltage which is proportional to angular velocity. This voltage is available and has been brought out on all the SDC1700 converters.



Extended temperature range versions of all the converters are available.

MODELS AVAILABLE

The three Synchro to Digital Converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1702XYZ is a 10-bit converter which has an overall accuracy of ±22 arc-minutes and a resolution of 21 arc-minutes.

Model SDC1700XYZ is a 12-bit converter with an overall accuracy of ±8.5 arc-minutes and a resolution of 5.3 arc-minutes.

Model SDC1704XYZ is a 14-bit converter with an overall accuracy of ±2.2 arc-minutes ±1LSB and a resolution of 1.3 arc-minutes.

The XYZ code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the input voltage and range, and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

NOTE
For all the standard options, no external transformers are needed with these converters.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODELS	SDC1702	SDC1700	SDC1704
ACCURACY[1] (max error)			
60Hz	±22 arc-minutes	±8.5 arc-minutes	±2.9 arc-minutes ±1LSB
400Hz	±22 arc-minutes	±8.5 arc-minutes	±2.2 arc-minutes ±1LSB
2.6kHz	±22 arc-minutes	±8.5 arc-minutes	±2.9 arc-minutes ±1LSB
RESOLUTION	10 Bits (1LSB = 21 arc-mins)	12 Bits (1LSB = 5.3 arc-mins)	14 Bits (1LSB = 1.3 arc-mins)
OUTPUT (In Parallel)	10 Bits (Natural Binary)	12 Bits (Natural Binary)	14 Bits (Natural Binary)
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz, 2.6kHz	*	*
SIGNAL VOLTAGE (Line-to-Line)			
Low Level	11.8V rms	*	*
High Level	90V rms	*	*
SIGNAL IMPEDANCES			
Low Level	26kΩ (Resistive)	*	*
High Level	200kΩ (Resistive)	*	*
REFERENCE VOLTAGE			
Low Level	26V (11.8V Signal)	*	*
High Level	115V (90V Signal)	*	*
REFERENCE IMPEDANCE	270kΩ (115V Signal)	*	*
	56kΩ (26V Reference)	*	*
	(Impedance is Resistive)	*	*
TRANSFORMER ISOLATION	500V dc	*	*
TRACKING RATE (min)			
60Hz	5 Revolutions Per Second	*	500°/sec
400Hz	36 Revolutions Per Second	*	12 Revolutions Per Second
2.6kHz	75 Revolutions Per Second	*	25 Revolutions Per Second
Accel.[1] Constant K_a			
60Hz	1880/sec²	*	520/sec²
400Hz	110,000/sec²	*	36,000/sec²
2.6kHz	518,000/sec²	*	170,000/sec²
STEP RESPONSE (179° Step) (For 1LSB Error)			
60Hz	1.5sec	*	*
400Hz	125ms	*	*
2.6kHz	50ms	*	*
POWER LINES	±15V @ 25mA, +5V @ 70mA } ±5%	*	±15V @ 30mA, +5V @ 85mA } ±5%
POWER DISSIPATION	1.1 Watts	*	1.3 Watts
DATA LOGIC OUTPUT[2] (TTL Compatible)	2TTL Loads SDC17026YZ 4TTL Loads SDC17025YZ	2TTL Loads SDC17006YZ 4TTL Loads SDC17005YZ	2TTL Loads on All Options
BUSY LOGIC OUTPUT, POSITIVE PULSE (1 TTL Load)			
60Hz	9.0μs } ±30%	*	9.0μs } ±30%
400Hz	2.0μs } ±30%	*	2.0μs } ±30%
2.6kHz	2.0μs } ±30%	*	1.3μs } ±30%
MAX DATA TRANSFER TIME			
60Hz	40μs	*	35μs
400Hz	5.0μs	*	3.0μs
2.6kHz	1.8μs	*	0.8μs
INHIBIT INPUT (To Inhibit)	Logic "0" 1 TTL Load	*	Logic "0" 2 TTL Loads
WARM UP TIME	1 sec to Rated Accuracy	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C Standard	*	*
	-55°C to +105°C Extended	*	*
Storage	-55°C to +125°C	*	*
DIMENSIONS	3.125" x 2.625" x 0.4" (79.4 x 66.7 x 10.2mm)	*	*
WEIGHT	3 ozs. (85 grams)	*	*

*Specification same as SDC1702

[1] Specified over the appropriate operating temperature range of the option and for: (a) ± 10% signal and reference amplitude variation (b) 10% signal and reference Harmonic Distortion (c) ±5% power supply variation (d) ±10% variation in reference frequency.

[2] It is recommended that buffers should be used if the above converters are required to drive over a distance greater than 6".

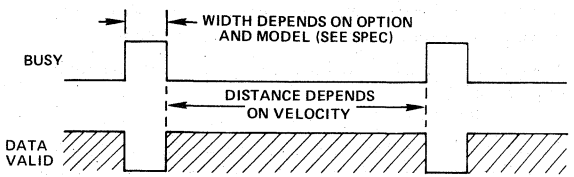
Specifications subject to change without notice.

DATA TRANSFER (All Models)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin.

The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the model and option (see specification table). The converter is busy when the BUSY pin is at a TTL "High" level. These pulses correspond to those delivered by the VCO to increment or decrement the up-down counter (see schematic diagram). Thus the pulses will occur for increasing and decreasing counts.

The most suitable time for transferring data is when the BUSY is at a logic "Lo" state, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.



Data Transfer Diagram

DATA TRANSFER DIAGRAM

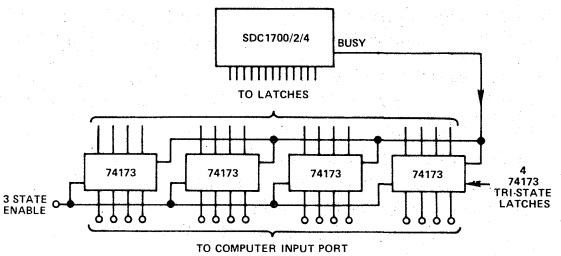
Taking the INHIBIT to a logic "Lo" state prevents the VCO (BUSY) pulses from updating the up-down counter. However, if applied during a BUSY pulse, the INHIBIT will not become effective until the end of the BUSY pulse.

The best method of transferring the data is by applying the INHIBIT (taking it to a logic "Lo" state), waiting for at least the width of a BUSY pulse, transferring the data and releasing the INHIBIT.

Note that sustained application of the INHIBIT opens the internal control loop and the converter may take on appreciable time to recover to full accuracy when the loop is restored.

INTERFACING WITH A COMPUTER

It is recommended that external latches are used to enable data to be transferred onto a computer data bus. One method is shown in the diagram. Using this method will mean that the latches are constantly updated by the BUSY signal, while at the same time enabling inputs to be made to the computer by means of normal data transfer procedures. The AC1755 mounting card contains these external components.



Suggested External Computer Interface Circuitry

THEORY OF OPERATION

If the unit is a Synchro to Digital Converter, then the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$

$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the Synchro Shaft.

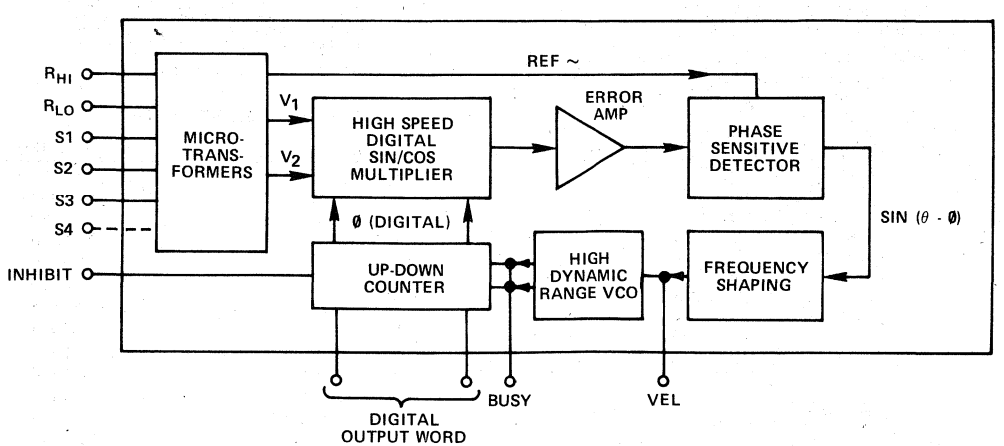
If the unit is a Resolver to Digital Converter, then the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformer will act purely as an isolator.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

The V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give

$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$

and $K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$



Functional Diagram of the SDC1700/2/4 Converters

These signals are subtracted by the error amplifier to give:

$$K E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$$

or $$K E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals within the rated accuracy of the converter, the synchro shaft angle θ.

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are ±15V and 5V. They must be connected to the "±15V" and "5V" pins with the common connection to the ground pin GND.

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output is taken from pins:

1 through to 10 for the SDC1702
1 through to 12 for the SDC1700
1 through to 14 for the SDC1704

Pin 1 represents the MSB in each case. The reference connections are made to pins "R_{HI}" and "R_{LO}".

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \text{ Sin } \omega t \text{ Cos } \theta$$

The analog voltage representing velocity is available between "VEL" and "GND".

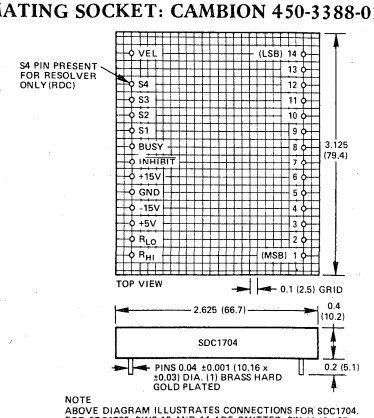
The "BUSY" and "INHIBIT" pin (if used), should be connected as described under the heading "Data Transfer".

NOTE: If the INHIBIT pin is used (i.e., driven to 0 volts), the control loop will be opened and a finite time will be required (see spec) for the converter to recover.

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



NOTE
ABOVE DIAGRAM ILLUSTRATES CONNECTIONS FOR SDC1704. FOR SDC1700, PINS 13 AND 14 ARE OMITTED. PIN 12 IS LSB. FOR SDC1702, PINS 11, 12, 13, 14 ARE OMITTED. PIN 10 IS LSB.

RESISTIVE SCALING OF INPUTS

A unique feature of the SDC1700 series of converters is that the inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered. In addition it should be noted that a 400Hz unit will operate from a 2.6kHz reference. It will however have the velocity and acceleration characteristics as specified for the 400Hz converter. A 60Hz converter will operate from a 400Hz reference and will have the velocity and acceleration characteristics as specified for the 60Hz converter.

To calculate the values of the external scaling resistors for a synchro converter, add 1.11kΩ in series with S1, S2 and S3 per extra volt in the case of the signal, and 2.2kΩ in the case of the reference. In the case of a resolver converter add 2.22kΩ per extra volt in series with S1 and S2 for the signal and 2.2kΩ per extra volt in series with R_{HI} for the reference.

For example, assume that we have an 11.8 volt line to line signal/26.0 volt reference converter, and we wish to use a 60 volt line to line signal with a 115 volt reference.

Thus in each signal input line, the extra voltage capability required is:

$$60 - 11.8 = 48.2 \text{ volts}$$

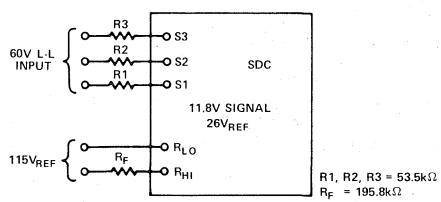
Therefore each resistors needs to have a value of $48.2 \times 1.11 = 53.5k\Omega$. In the case of the reference, the extra voltage capability required is:

$$115 - 26.0 = 89 \text{ volts}$$

Therefore the resistor needs to have a value of:

$$89.0 \times 2.2 = 195.8k\Omega$$

Thus the inputs can be scaled as in the diagram below.



NOTE
IN THE CASE OF R1, R2 AND R3, THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF R_F IS NOT CRITICAL.

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10 (LSB for SDC1702)	0.3516
11	0.1758
12 (LSB for SDC1700)	0.0879
13	0.0439
14 (LSB for SDC1704)	0.0220

VELOCITY PIN

This pin provides a voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the table below.

Scaling of Output Voltage for One Fifth max Velocity	2Volts (Nominal)
Output Voltage Temp. Coeff.	0.05%/°C of Output
Output Voltage Drift (All Models)	0 to +70°C ±50μV/°C -55°C to +105°C ±100μV/°C
Linearity:	0/sec to 800°/sec SDC1704 400Hz 1% 0/sec to 100°/sec SDC1704 60Hz 1% 0/sec to 800°/sec SDC1700/2 400Hz 2% 0/sec to 100°/sec SDC1700/2 60Hz 1.5%
Noise: (0 to 20Hz)	@1600°/sec SDC1700/2/4 400Hz 2mV rms @200°/sec SDC1700/2/4 60Hz 2mV rms
Impedance (Output)	1Ω
max Current Available	1mA

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

The SDC1700/2/4 velocity outputs do not have the disadvantages of being inefficient at low speeds and do not need gearing required by tachometers. In addition, the output is available at no extra cost.

For other velocity output scaling and linearity consult the factory.

Two examples of the use of the velocity pin are shown in the diagram below.

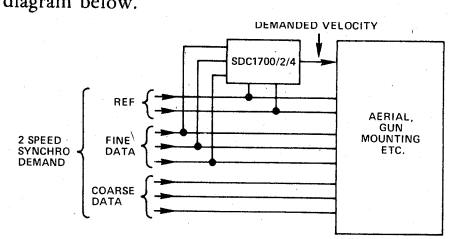


Diagram showing a velocity feed forward application. The SDC is used to produce the demanded velocity from Synchro form inputs.

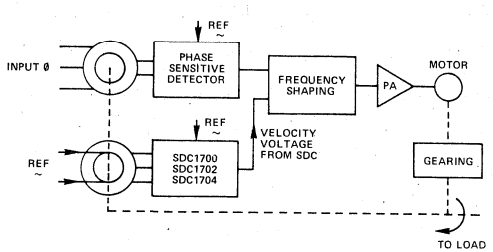
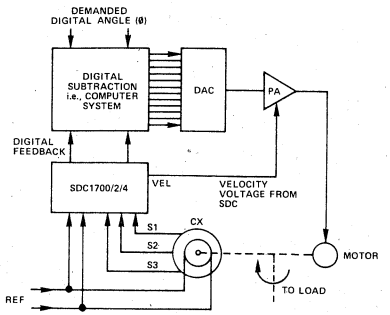


Diagram showing the velocity voltage being used to stabilize an electro-mechanical control loop

APPLICATIONS OF SYNCHRO TO DIGITAL CONVERTERS

SDCs can be used in a variety of ways in control loops as well as for the conversion of angular data into a form which is readily acceptable to digital displays or computers.

The diagram below shows an SDC being used in a digitally controlled feedback loop.



An SDC Being Used in a Digitally Controlled Feedback Loop

Such loops as shown in the diagram above require the high dynamic performance of the SDC1700 series converters. It should be noted that in this application, the SDC1700 series will replace conventional tachometers and phase sensitive detectors while at the same time provide digital position feedback.

Many synchro systems employ a two speed, geared arrangement utilizing one synchro for the fine shaft and one for the coarse. An example of this type is shown below.

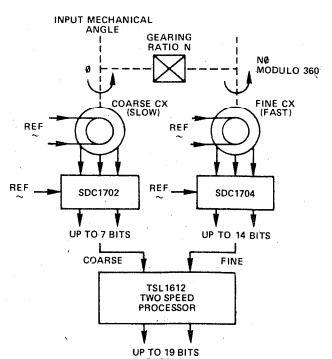


Diagram Showing Coarse/Fine Synchro Processor System

In the above example, two tracking SDC's are being used to provide data for coarse/fine (two speed) data transmission systems.

The TSL1612 is a processor which combines the outputs of two SDC's to provide one output word of up to 19 bits in length.

The TSL1612 is available for any ratio between 2:1 and 36:1 and provides automatic compensation for misalignment of the coarse synchro relative to its shaft. It also corrects for any overlap between the digits of the coarse and fine shafts.

MEAN TIME BETWEEN FAILURES (M.T.B.F.)

The estimated mean time between failures is given as follows:

SDC1700/2	174,000 Hours
SDC1704	167,000 Hours

Further information relating to M.T.B.F. and to the quality control and test procedures employed by us can be obtained from the factory on request.

TRANSFER FUNCTION

The transfer function of the SDC1700/2 and SDC1704, 400Hz versions, is given below.

For the transfer functions of the other models or for a detailed analysis of those given here, please contact us.

SDC1700/2 400Hz

$$\frac{\theta_O}{\theta_1} = \frac{8.8 \times 10^7 \,(1 + 6.8 \times 10^{-3} s)}{s^3 + 8.04 \times 10^2 s^2 + 6.1 \times 10^5 s + 8.8 \times 10^7}$$

SDC1704 400Hz

$$\frac{\theta_O}{\theta_1} = \frac{2.95 \times 10^7 \,(1 + 8.2 \times 10^{-3} s)}{s^3 + 8.05 \times 10^2 s^2 + 1.95 \times 10^5 s + 2.95 \times 10^7}$$

CARD MOUNTING

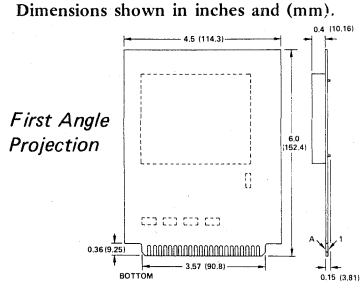
All the converters can be mounted on an AC1755 mounting card. This card contains the latches described under the "Data Transfer" heading, which are necessary to transfer the data on to a computer bus system, and sockets for the converter.

The latches have a tri-state output to facilitate ease of use.

The AC1755 also contains facilities for the inclusion of input signal and reference scaling resistors as described under the heading "Resistive Scaling of Inputs".

The card uses a 22/22 0.156″ pitch edge connector. The pin out is shown below. If it is not required to use the external latches, they can be jumpered on the board.

AC1755 MOUNTING CARD
Dimensions shown in inches and (mm).



EDGE CONNECTIONS AC1755

Edge Pin Number	Function	Edge Pin Letter	Function
1	R (Lo)	A	Tri-State Enable
2	R (Hi)	F	+15V
3	S3	H	+15V
4	S2	J	-15V
5	S1	K	-15V
6	S4	L	GND
8	VEL	M	GND
13	BUSY	N	+5V
15	INHIBIT	P	+5V
16	BIT 14	T	BIT 7
17	BIT 13	U	BIT 6
18	BIT 12	V	BIT 5
19	BIT 11	W	BIT 4
20	BIT 10	X	BIT 3
21	BIT 9	Y	BIT 2
22	BIT 8	Z	BIT 1

NOTE: SDC1702 does not use pins 16, 17, 18 or 19. SDC1700 does not use pins 16 and 17.

ORDERING INFORMATION

Parts should be ordered by the appropriate part number (i.e., SDC1700, SDC1702, SDC1704) followed by the appropriate XYZ option code.

If the unit is to be a Resolver to Digital Converter, the SDC should be replaced by RDC in the part number.

The XYZ options are as follows:
X signifies the operating temperature range and the options are:

X = 5 signifies 0 to +70°C (commercial) temperature.
X = 6 signifies −55°C to +105°C (extended) temperature.

Y signifies the reference frequency and the options are:

Y = 1 signifies 400Hz
Y = 2 signifies 60Hz *
Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is an SDC or an RDC. The options are:

Z = 1 signifies synchro, signal 11.8V rms, reference 26V rms
Z = 2 signifies synchro, signal 90V rms, reference 115V rms
Z = 3 signifies resolver, signal 11.8V rms, reference 11.8V rms
Z = 4 signifies resolver, signal 26V rms, reference 26V rms
Z = 8 signifies resolver, signal 11.8V rms, reference 26V rms

Thus, for example, an SDC1704 with a commercial (0 to +70°C) operating range, using a 400Hz, 26V reference with an 11.8V signal would be ordered as an SDC1704511.

For other than these options, consult the factory.

CAUTIONS

Do not reverse the power supplies.
Do not connect signal and/or reference inputs to other than S1, S2, S3, S4, R_{HI} or R_{LO}.

Do not connect signals and/or references to a lower voltage rated converter. (Such as a 115V Synchro into a 26V Converter).

Misconnections as per the above will damage the units and void the warranty.

OTHER PRODUCTS

The SDC1700/2/4 converters are just a few of the modules and instruments concerned with Synchro and Resolver conversion manufactured by us.

Other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

TWO SPEED PROCESSORS

Which utilize the digital outputs of two SDCs in a 2 speed coarse/fine system to produce one combined digital word of up to 19 bits in length. The TSL1612 in particular is available for any ratio between 2:1 and 36:1.

DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 14 bits are available.

BCD OUTPUT SYNCHRO TO DIGITAL CONVERTERS

The SBCD1752 and SBCD1753 are converters with a BCD instead of a binary output based upon the SDC1700. They have outputs of ±180.0 degrees and 0 to 360.0 degrees respectively.

*50Hz Operation

For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

Ultra-Low Profile (0.35") Three-State Latched Output Synchro to Digital Converters

SDC1725/1726

FEATURES

- Three-State Latched Output
- Continuous Tracking Even During Data Transfer
- Simple Data Transfer Facility
- Low Profile 0.35" (8.9mm)
- Internal Transformers for 60Hz, 400Hz and 2.6kHz References
- Signal and Reference Voltage Scaling with External Resistors
- High Tracking Rates (50 revs/sec)
- Lightweight 3.3 oz. (93 gms)
- MIL Spec/Hi Rel Options Available

APPLICATIONS

- Servo Mechanisms
- Retransmission Systems
- Coordinate Conversion
- Antenna Monitoring
- Simulators
- Industrial Controls
- Artillery Fire Control Systems
- Machine Tool Control Systems

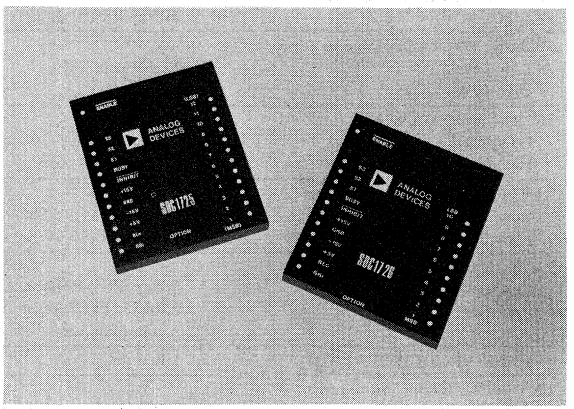
GENERAL DESCRIPTION

The SDC1725 and SDC1726 are modular, continuous tracking Synchro/Resolver to Digital Converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference depending on the option. The outputs will be presented in TTL compatible parallel natural binary, buffered by three-state latches.

The three-state output facility not only simplifies multiplexing of more than one device onto a single data bus but also enables the "$\overline{\text{INHIBIT}}$" to be used without opening the internal converter loop.

Another outstanding feature of these converters is the use of precision Scott T and reference microtransformers. This has made it possible to include internal transformers, even on the 60Hz options, and yet obtain a profile height lower than any other modular Synchro/Resolver to Digital Converter currently available.



MODELS AVAILABLE

The two Synchro/Resolver to Digital Converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:

Model SDC1725XYZ is a 12-bit converter with an overall accuracy of ±3.2 arc-minutes ±1LSB and a resolution of 5.3 arc-minutes.

Model SDC1726XYZ is a 10-bit converter with an overall accuracy of ±22 arc-minutes and a resolution of 21 arc-minutes.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

NOTE
No external transformers are required with these converters.

SPECIFICATIONS (typical at +25°C unless otherwise stated)

Models	SDC1725	SDC1726
ACCURACY[1] (max Error all Options)	±3.2 arc-minutes ±1LSB	±22 arc-minutes
RESOLUTION	12 Bits	10 Bits
OUTPUT	12-Bits Parallel Natural Binary	10-Bits Parallel Natural Binary
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz, 2.6kHz	*
SIGNAL VOLTAGE (Line to Line)		
Low Level	11.8V rms	*
High Level	90.0V rms	*
SIGNAL IMPEDANCES		
Low Level	26kΩ Resistive	*
High Level	200kΩ Resistive	*
REFERENCE VOLTAGE		
Low Level	26V rms (11.8V Signal)	*
High Level	115V rms (90.0V Signal)	*
REFERENCE IMPEDANCE		
Low Level	56kΩ (26V Reference)	*
High Level	270kΩ (115V Reference)	*
	(Impedance is Resistive)	*
TRANSFORMER ISOLATION	500V dc	*
TRACKING RATE (Minimum)		
60Hz Options	5 Revolutions Per Second	*
400Hz Options	36 Revolutions Per Second	*
2.6kHz Options	50 Revolutions Per Second	*
ACCELERATION		
Constant K_a		
60Hz Options	2000/sec^2	*
400Hz Options	120,000/sec^2	*
2.6kHz Options	600,000/sec^2	*
STEP RESPONSE (179° Step) (For 1LSB Error)		
60Hz Options	1.5sec	*
400Hz Options	125ms	*
2.6kHz Options	50ms	*
POWER LINES	+15V @ 25mA	*
	-15V @ 25mA	*
	+5V @ 120mA	*
POWER DISSIPATION	1.35 Watts	*
DATA LOGIC OUTPUTS[2] (TTL Compatible)	6TTL Loads All Options	*
BUSY LOGIC OUTPUT LOADING[2]	2TTL Loads	*
BUSY LOGIC OUTPUT WIDTH[2]	330ns max, 200ns min	*
INHIBIT INPUT (TO INHIBIT)	Logic "0" 1 TTL Load	*
ENABLE INPUT (TO ENABLE)	Logic "0" 1 TTL Load	*
WARM UP TIME	1sec to Rated Accuracy	*
TEMPERATURE RANGE		
Operating	0 to +70°C Standard	*
	-55°C to +105°C Extended	*
Storage	-55°C to +125°C	*
DIMENSIONS	3.125" X 2.625" X 0.35"	*
	(79.4 X 66.7 X 8.9mm)	*
WEIGHT	3.3 ozs (93 gms)	*

*Specifications the same as for SDC1725.

NOTES
[1] Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency.
[2] Schottky logic loading rules apply.

Specifications subject to change without notice.

THEORY OF OPERATION

If the unit is a Synchro to Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$

$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the synchro shaft.

If the unit is a Resolver to Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ.

Then V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$

and

$K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$

These signals are subtracted by the error amplifier to give:

$K E_O \text{ Sin } \omega t (\text{Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$

or

$K E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ) equals, within the rated accuracy of the converter, the synchro shaft angle θ.

Assuming that the "INHIBIT" is at a logic high state, then the digital word ϕ will be strobed into the latches 150ns after the up-down counter has been updated. If the three state "ENABLE" is at a logic low, then the digital output word will be presented to the output pins of the module.

DATA TRANSFER

Data transfer from the SDC1725 and SDC1726 is very straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

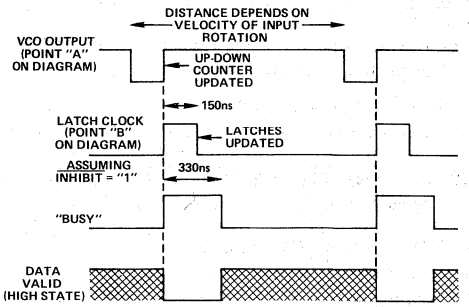
From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for 330ns while the up-down counters and latches are settling, and transfer data when it is in a low state.

However, a much more satisfactory method is to use the "INHIBIT" input. As can be seen from the functional diagram application of the "INHIBIT" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid from 330ns after the INHIBIT has been taken to a logic low state. It can also be seen that this method of data transfer is valid regardless of when the INHIBIT is applied.

The three-state ENABLE can be used at any time in order to present the data in the latches to the output pins. A logic low on this pin will cause the data to be presented to the outputs.

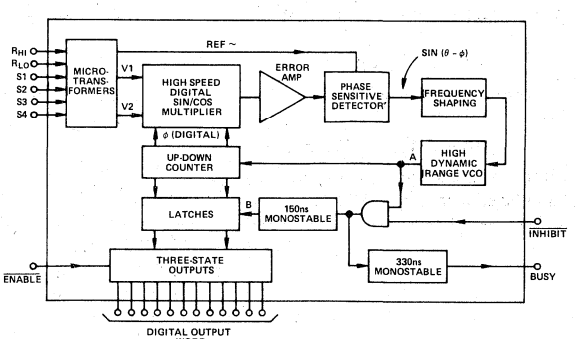
Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the INHIBIT and ENABLE pins.



Timing Diagram

Bit Number	Weight in Degrees
1	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10 (LSB - SDC1726)	0.3516
11	0.1758
12 (LSB - SDC1725)	0.0879

Bit Weight Table



Functional Diagram SDC1725

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1μF and a 6.8μF capacitor is placed in each of the three positions from "+15V" to "GND", from "-15V" to "GND" and from "+5V" to "GND".

The digital output is taken from pins:

"1" through to "10" for the SDC1726

"1" through to "12" for the SDC1725

Pin "1" represents the MSB in each case.

The reference connections are made to "R_{HI}" and "R_{LO}".

In the case of a Synchro the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$$

The "BUSY", "$\overline{\text{INHIBIT}}$" and "$\overline{\text{ENABLE}}$" pins should be connected as described under the heading "Data Transfer".

RESISTIVE SCALING OF INPUTS

A feature of this range of converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 2.2kΩ per extra volt of reference in series with "R_{HI}".

In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 2.2kΩ per extra volt of reference in series with "R_{HI}".

For example, assume that we have an 11.8V line to line, 26V reference Synchro Converter, and we wish to use it with a 60V line to line signal with a 115V reference.

In each signal input line, the extra voltage capability required is:

$$60 - 11.8 = 48.2V$$

Therefore each one of the three resistors needs to have a value of:

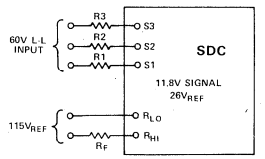
$$48.2 \times 1.11 = 53.5k\Omega$$

Similarly the single resistor needed in series with "R_{HI}" can be calculated as being 195.8kΩ.

The inputs of the converter can therefore be scaled as in the diagram below.

USING THE CONVERTERS WITH OTHER THAN THE SPECIFIED REFERENCE FREQUENCY

A 60Hz converter can be used from 50Hz to 400Hz, and a 400Hz converter can be used from 400Hz up to 2.6kHz, but they will have the dynamic characteristics specified for the unit concerned.



R1, R2, R3 = 53.5kΩ
R_F = 195.8kΩ

NOTE
IN THE CASE OF THE SIGNAL RESISTORS THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

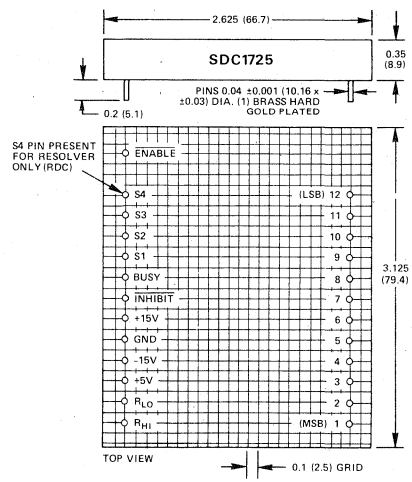
IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF R_F IS NOT CRITICAL.

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



NOTE
THE ABOVE DIAGRAM SHOWS THE CONNECTIONS FOR THE SDC1725. ON THE SDC1726, PINS 11 AND 12 ARE OMITTED AND PIN 10 IS THE LSB.

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

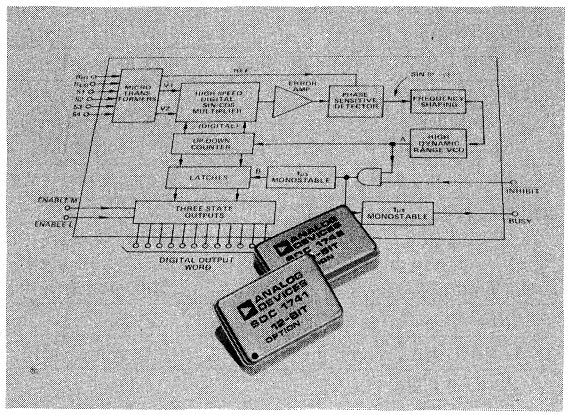
Part Number	Resolution	Operating Temp. Range	L to L Voltage/Format	Ref. Voltage	Ref. Freq.
SDC1725511	12 Bits	0 to +70°C	11.8V Synchro	26 Volts	400Hz
SDC1725611	12 Bits	-55°C to +105°C	11.8V Synchro	26 Volts	400Hz
SDC1725512	12 Bits	0 to +70°C	90.0V Synchro	115 Volts	400Hz
SDC1725612	12 Bits	-55°C to +105°C	90.0V Synchro	115 Volts	400Hz
SDC1725522	12 Bits	0 to +70°C	90.0V Synchro	115 Volts	60Hz
SDC1725622	12 Bits	-55°C to +105°C	90.0V Synchro	115 Volts	60Hz
SDC1726511	10 Bits	0 to +70°C	11.8V Synchro	26 Volts	400Hz
SDC1726611	10 Bits	-55°C to +105°C	11.8V Synchro	26 Volts	400Hz
SDC1726512	10 Bits	0 to +70°C	90.0V Synchro	115 Volts	400Hz
SDC1726612	10 Bits	-55°C to +105°C	90.0V Synchro	115 Volts	400Hz
SDC1726522	10 Bits	0 to +70°C	90.0V Synchro	115 Volts	60Hz
SDC1726622	10 Bits	-55°C to +105°C	90.0V Synchro	115 Volts	60Hz

12-Bit Hybrid Synchro and Resolver to Digital Converters

SDC1741/1742

FEATURES
- Internal Isolating Transformers
- Two Accuracy Options
- Three-State Latched Output
- Continuous Tracking—Even During Data Transfer
- Simple Data Transfer
- Laser Trimmed—No External Adjustments
- MIL Spec/Hi Rel Options Available
- Hermetically Sealed

APPLICATIONS
- Avionic Systems
- Servo Mechanisms
- Coordinate Conversion
- Axis Transformation
- Antenna Monitoring
- Artillery Fire Control Systems
- Engine Controllers



GENERAL DESCRIPTION

The SDC1741 and SDC1742 are hybrid 12-bit output, continuous tracking synchro or resolver to digital converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can either be 3 wire synchro plus reference or 4 wire resolver format plus reference depending on the option and the outputs are presented in TTL compatible parallel natural binary buffered by three-state latches.

The three state output facility, which has separate $\overline{\text{ENABLE}}$ inputs for the most significant 8 bits and the least significant 4 bits, not only simplifies multiplexing of more than one device onto a single data bus, but also enables the $\overline{\text{INHIBIT}}$ to be used without opening the internal converter loop.

An outstanding feature of these converters is that although the profile height is only 0.26 inches (6.6mm) they contain internal transformers which provide for true isolation on the signal and reference inputs.

The SDC1741 and SDC1742 converters are hermetically sealed in a metal 32 pin dual in line package.

To ensure a level of reliability consistent with the performance, each converter receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, fine and gross leak testing, acceleration testing and operating burn-in.

The converters are also available processed in accordance with MIL-STD-883, Method 5008, Class B.

MODELS AVAILABLE

The two converters described in this data sheet both have 12-bit resolution and differ only in terms of accuracy as follows:

SDC1742XYZ has an accuracy of ±3.2 arc-minutes ±1LSB.

SDC1741XYZ has an accuracy of ±10 arc-minutes ±1LSB.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

THEORY OF OPERATION

If the unit is a Synchro to Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$

$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the synchro shaft.

If the unit is a Resolver to Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ.

SPECIFICATIONS (typical at 25°C unless otherwise specified)

Models	SDC1742	SDC1741
ACCURACY[1]		
(Max Error on all Options)	±3.2 arc-minutes ±1LSB	±10 arc-minutes ±1LSB
RESOLUTION	12 Bits	*
OUTPUT	12-Bits Parallel Natural Binary	*
SIGNAL AND REFERENCE FREQUENCY	400Hz or 2.6kHz	*
SIGNAL VOLTAGE (Line to Line)	90V or 11.8V rms	*
SIGNAL IMPEDANCE		
90 Volt Signal	200kΩ (Resistive)	*
11.8 Volt Signal	26kΩ (Resistive)	*
REFERENCE VOLTAGE	115V, 26V or 11.8V rms	*
REFERENCE IMPEDANCE		
115 Volt Reference	270kΩ (Resistive)	*
26 Volt Reference	56kΩ (Resistive)	*
11.8 Volt Reference	27kΩ (Resistive)	*
TRANSFORMER ISOLATION	350V dc	*
TRACKING RATE (Minimum)	18 Revolutions Per Second	*
ACCELERATION		
Constant K_a	85,000/sec^2	*
STEP RESPONSE (179° Step for Settling to 1LSB of Error)	150ms	*
POWER LINES	+15V @ 25mA (Max)	*
	-15V @ 25mA (Max)	*
	+5V @ 150mA (Max)	*
POWER DISSIPATION	1.5 Watts (Max)	*
DATA LOGIC OUTPUTS[2]	6TTL Loads	*
BUSY LOGIC OUTPUT LOADING[2]	2TTL Loads	*
BUSY LOGIC OUTPUT WIDTH	3μs (Max)	*
$\overline{\text{INHIBIT}}$ INPUT (TO INHIBIT)	Logic "0" 1TTL Load	*
$\overline{\text{ENABLE}}$ INPUTS[3] (TO ENABLE)	Logic "0" 1TTL Load	*
TEMPERATURE RANGE		
Operating	-55°C to +125°C	*
Storage	-65°C to +150°C	*
DIMENSIONS	1.74" X 1.14" X 0.26"	*
	(44.2 X 28.9 X 6.6mm)	*
WEIGHT	0.7025 ozs (20 gms)	*

*Specifications the same as for SDC1742.

NOTES

[1] Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency (see also note 2).

[2] Schottky logic loading rules apply.

[3] $\overline{\text{ENABLE}}$ M enable most significant 8 bits.
$\overline{\text{ENABLE}}$ L enable least significant 4 bits.

Specifications subject to change without notice.

Then V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K\ E_O\ \text{Sin}\ \omega t\ \text{Sin}\ \theta\ \text{Cos}\ \phi$$

and

$$K\ E_O\ \text{Sin}\ \omega t\ \text{Cos}\ \theta\ \text{Sin}\ \phi$$

These signals are subtracted by the error amplifier to give:

$$K\ E_O\ \text{Sin}\ \omega t\ (\text{Sin}\ \theta\ \text{Cos}\ \phi - \text{Cos}\ \theta\ \text{Sin}\ \phi)$$

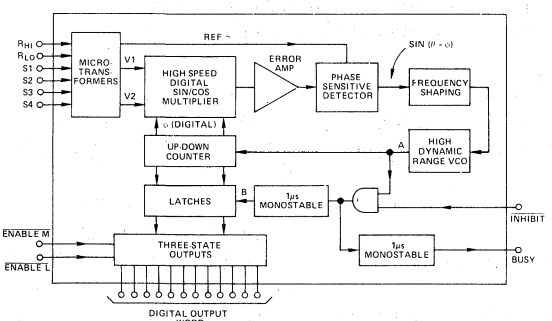
or

$$K\ E_O\ \text{Sin}\ \omega t\ \text{Sin}\ (\theta - \phi)$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ) equals, within the rated accuracy of the converter, the synchro shaft angle θ.

Assuming that the "$\overline{\text{INHIBIT}}$" is at a logic high state, then the digital word ϕ will be strobed into the latches 1μs after the up-down counter has been updated. If the three state "ENABLE" is at a logic low, then the digital output word will be presented to the output pins of the module.



Functional Diagram SDC1741 and SDC1742

DATE TRANSFER

Data transfer from the converters is straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

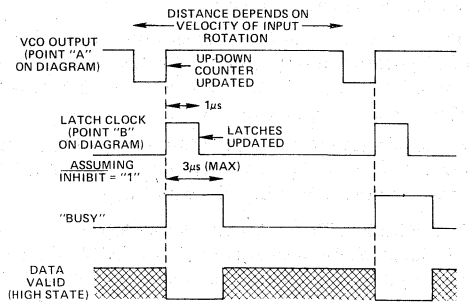
From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for up to 2.0 microseconds (typical) while the up-down counters and latches are settling, and transfer data when it is in a low state.

However, a much more satisfactory method is to use the "$\overline{\text{INHIBIT}}$" input. As can be seen from the functional diagram application of the "$\overline{\text{INHIBIT}}$" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid after 3μs has elapsed from the application of the $\overline{\text{INHIBIT}}$ (i.e. taken to logic low). It can also be seen that this method of data transfer is valid regardless of when the $\overline{\text{INHIBIT}}$ is applied.

The three-state $\overline{\text{ENABLE}}$ can be used at any time in order to present the data in the latches to the output pins. $\overline{\text{ENABLE M}}$ enables the most significant 8 bits while $\overline{\text{ENABLE L}}$ enables the least significant 4 bits.

Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the INHIBIT and ENABLE pins.



Timing Diagram

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB)	0.0879

Bit Weight Table

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1μF and a 6.8μF capacitor is placed in each of the three positions from "+15V" to "GND", from "-15V" to "GND" and from "+5V" to "GND".

The pin marked "case" is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from Pin "1" through to "12" where Pin "1" is the MSB.

The reference connections are made to "R_{HI}" and "R_{LO}".

In the case of a Synchro the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI}\ \text{Sin}\ \omega t\ \text{Sin}\ \theta$$
$$E_{S3-S2} = E_{RLO-RHI}\ \text{Sin}\ \omega t\ \text{Sin}\ (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI}\ \text{Sin}\ \omega t\ \text{Sin}\ (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI}\ \text{Sin}\ \omega t\ \text{Sin}\ \theta$$
$$E_{S2-S4} = E_{RHI-RLO}\ \text{Sin}\ \omega t\ \text{Cos}\ \theta$$

The "BUSY", "$\overline{\text{INHIBIT}}$" and "$\overline{\text{ENABLE}}$" pins should be connected as described under the heading "Data Transfer"

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 2.2kΩ per extra volt of reference in series with "R_{HI}".

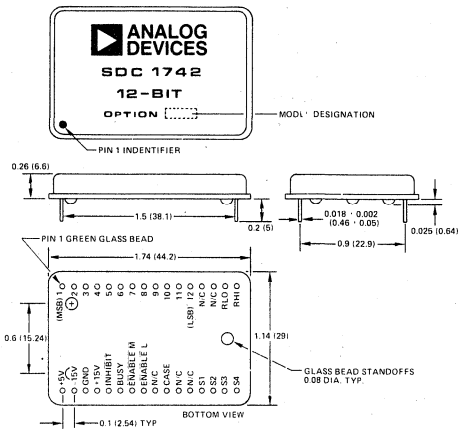
In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 2.2kΩ per extra volt of reference in series with "R_{HI}".

MEAN TIME BETWEEN FAILURES (MTBF)

The calculated MTBF in an airborne inhabited environment at +25°C is in excess of 200,000 hours.

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Stabilization Bake	24 hours @ +150°C
3. Temperature Cycling	10 cycles, -65°C to +150°C
4. Constant Acceleration	5000G
5. Seal, Test, Fine and Gross	In-House Criteria
6. Operating Burn-In	24 hours @ +125°C

PROCESSING TO MIL-STD-883

All models ordered to the requirements of MIL-STD-883, Method 5008, Class B are identified with a /883B suffix, and receive the following processing:

1. Pre-Cap Visual Inspection	2017
2. Stabilization Bake	1008, 24 hours @ +150°C
3. Temperature Cycling	1010, Test Condition C, 10 cycles, -65°C to +150°C
4. Constant Acceleration	2001, Y_1 plane, 5000G
5. Seal, Test, Fine and Gross	1014, Test Condition A and C
6. Operating Burn-In	1015, Test Condition B, 160 hours @ +125°C
7. Final Electrical Testing	Performed at max and min operating temperatures
8. External Visual Inspection	2009

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

Part Number	Accuracy	Ref. Freq.	Signal Line to Line Voltage	I/P Format	Ref. Voltage
SDC1742411	±3.2 arc-minutes ±1LSB	400Hz	11.8 Volts rms	Synchro	26 Volts rms
SDC1742412	±3.2 arc-minutes ±1LSB	400Hz	90 Volts rms	Synchro	115 Volts rms
RDC1742413	±3.2 arc-minutes ±1LSB	400Hz	11.8 Volts rms	Resolver	11.8 Volts rms
RDC1742418	±3.2 arc-minutes ±1LSB	400Hz	11.8 Volts rms	Resolver	26 Volts rms
SDC1741411	±10 arc-minutes ±1LSB	400Hz	11.8 Volts rms	Synchro	26 Volts rms
SDC1741412	±10 arc-minutes ±1LSB	400Hz	90 Volts rms	Synchro	115 Volts rms
RDC1741413	±10 arc-minutes ±1LSB	400Hz	11.8 Volts rms	Resolver	11.8 Volts rms
RDC1741418	±10 arc-minutes ±1LSB	400Hz	11.8 Volts rms	Resolver	26 Volts rms
SDC1742441	±3.2 arc-minutes ±1LSB	2.6kHz	11.8 Volts rms	Synchro	26 Volts rms
SDC1742442	±3.2 arc-minutes ±1LSB	2.6kHz	90 Volts rms	Synchro	115 Volts rms
RDC1742443	±3.2 arc-minutes ±1LSB	2.6kHz	11.8 Volts rms	Resolver	11.8 Volts rms
RDC1742448	±3.2 arc-minutes ±1LSB	2.6kHz	11.8 Volts rms	Resolver	26 Volts rms
SDC1741441	±10 arc-minutes ±1LSB	2.6kHz	11.8 Volts rms	Synchro	26 Volts rms
SDC1741442	±10 arc-minutes ±1LSB	2.6kHz	90 Volts rms	Synchro	115 Volts rms
RDC1741443	±10 arc-minutes ±1LSB	2.6kHz	11.8 Volts rms	Resolver	11.8 Volts rms
RDC1741448	±10 arc-minutes ±1LSB	2.6kHz	11.8 Volts rms	Resolver	26 Volts rms

Note
If processing to MIL-STD-883B is required, and suffix /883B to the part number.

ANALOG DEVICES

Synchro/Resolver Power Amplifier

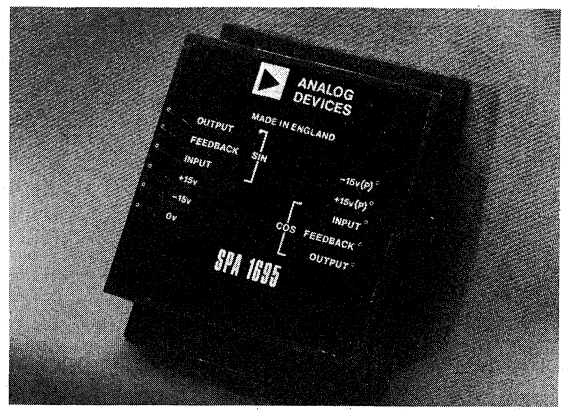
SPA1695

FEATURES

5VA Output – Capable of Driving 4 Size 11 CT's
Indefinite Short Circuit Protection
Metal Case Acts as Heatsink
Easily Mounted
Voltage Sensing Facility
Operation with No Derating Up to +105°C
Suitable for 50 to 400Hz Operation

APPLICATIONS

Can Be Used With the Digital Vector Generators (DTM1716 and DTM1717) to Drive Control Transformers (CT's)



GENERAL DESCRIPTION

The SPA1695 is a two channel amplifier intended for use in conjunction with the DTM1716 and DTM1717 Digital Vector Generators for driving Control Transformers (CT's).

The unit is capable of supplying 5VA to the load and therefore can be used in cases where the internal amplifiers of a Digital to Synchro Converter are not sufficient (i.e., in general when the load exceeds 1.3VA).

The SPA1695 is contained in an aluminium case which has predrilled flanges for mounting purposes and excellent heatsinking properties.

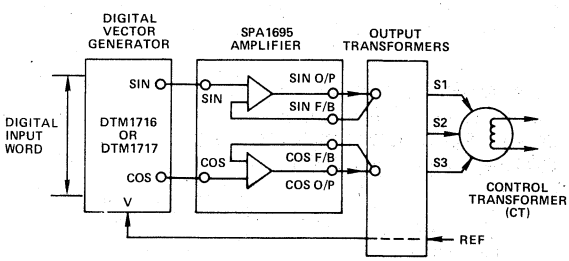
The amplifier has no derating up to +105°C and is indefinitely short circuit protected at 25°C ambient.

The unit accepts resolver format inputs (Sine and Cosine) at 7 volts rms max. The output of the amplifier is in resolver format at 7 volts rms max and should be fed into suitable transformers (see ordering information).

Voltage sensing pins are provided to compensate for any voltage drop which may occur between the output of the amplifier and the output transformer.

MODELS AVAILABLE

The SPA1695 does not require any option numbers in order to fully specify it. The standard unit operates over the frequency range 50 to 400Hz and over the temperature range of -55°C to +105°C.



Implementation of the SPA1695 Amplifier

SCHEMATIC DIAGRAM OF AN SPA1695 AMPLIFIER BEING USED TO DRIVE A CONTROL TRANSFORMER (CT)

The above diagram shows a Digital Vector Generator being used in conjunction with the SPA1695 amplifier and external transformers to drive a Control Transformer.

The diagram illustrates the use of the Sine and Cosine feedback pins ("Sin F/B" and "Cos F/B").

SPECIFICATIONS (typical at 25°C unless otherwise noted)

POWER OUTPUT[1]	5VA
ACCURACY[2] (between channels)	2 arc-minutes
GAIN ACCURACY[2] (matching)	0.1%
INPUT VOLTAGE (per channel)	7V rms
OPERATING FREQUENCY	50 to 400Hz
INPUT IMPEDANCE	Greater than 50kΩ
INPUT BIAS CURRENT	Less than 1μA
GAIN (per channel)	Unity
INPUT DRIFT	50μV/°C
INITIAL OUTPUT OFFSET	3mV max at 25°C
CROSS OVER DISTORTION	0.01% max
DERATING OF AMPLIFIER	None up to +105°C
POWER SUPPLY REQUIREMENTS:	
±15V(P) No Load	115mA Unregulated
±15V(P) Average Full Load	630mA Unregulated
±15V	15mA Regulated
WEIGHT	275 Grams (9.7 ozs)
SIZE	3.46" x 2.68" x 0.98" (88mm x 68mm x 25mm)
OPERATING TEMERATURE RANGE	-55°C to +105°C
STORAGE TEMPERATURE RANGE	-55°C to +125°C

NOTES:
1. Power output is sufficient to drive four 400Hz 90 volts line to line control transformers.
2. Valid over full temperature range of -55°C to +105°C.

Specifications subject to change without notice.

CONNECTING THE SPA1695

The diagram shows the connection of the SPA1695 to the DTM1716 or DTM1717 Digital Vector Generator, and STM1686 output and reference transformers.

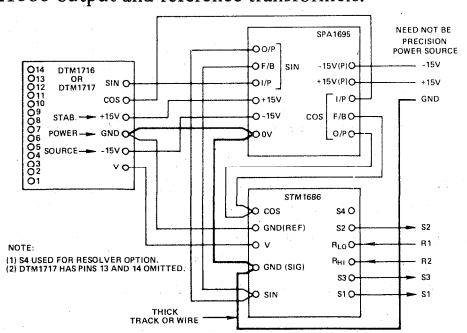


Diagram Showing Connection of the SPA1695 to a DTM1716 or DTM1717 and STM1686

NOTES:

1. The "Sin F/B" and the "Cos F/B" pins of the SPA1695 should be connected directly the the "Sin" and "Cos" terminals on the output transformer at the transformer. This is to compensate for any drop in voltage along the connections between the "Sin O/P" and "Cos O/P" pins of the amplifier and the transformer.
2. The "+15V" and "-15V" pins of the SPA1695 should be connected to a regulated power supply in order to drive the internal operational amplifiers. The "+15V(P)" and "-15V(P)" are used for the output stage and these supplies need not be a precision source. The minimum voltage when considering all tolerances including ripple, should be between 14.75 and 20 volts.
3. The part of the 0 volt system local to the amplifier and converter should be tapped from the "GND(SIG)" pin on the transformer and should not interconnect with any other part of the 0 volt system by any other method (see above diagram).
4. In the above diagram, connection is also shown between the reference transformers, contained in the STM1686 and the Digital Vector Generator.

USING TWO SPA1695 AMPLIFIERS IN PUSH-PULL CONFIGURATION

Twice the output power may be achieved by connecting the outputs from two SPA1695 amplifiers in push-pull configuration, the two devices being fed with out of phase signals.

For more information consult the factory.

ADDITIONAL HEATSINKING

Although the SPA1695 case will provide the necessary heatsink properties to allow the amplifier to provide the 5VA power output over the full temperature range, it is recommended that additional heatsinking be provided where possible.

ORDERING INFORMATION AND TRANSFORMER TYPE

Part number SPA1695 is sufficient to specify the amplifier – no option codes are needed.

The transformers should be ordered according to the following:

STM1686611	400Hz, Synchro output, 11.8 volt signal, 26 volt reference.
STM1686612	400Hz, Synchro output, 90 volt signal, 115 volt reference.
RTM1686618	400Hz, Resolver output, 11.8 volt signal, 26 volt reference.
STM1687622	50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

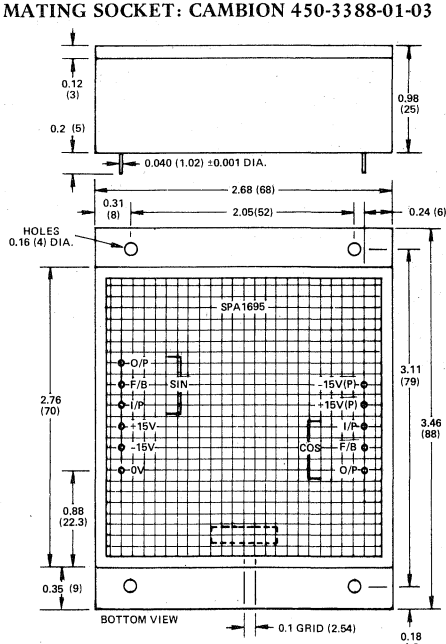
NOTES:

1. Above transformers are suitable for use over the temperature range -55°C to +105°C.
2. If it is required to use the SPA1695 with Digital to Resolver converters, then use:
   a. STM1736 for 400HZ and STM1737 for 50/60Hz systems in the case of the DRC1605 and DRC1606 converters.
   b. STM1696 for 400Hz and STM1697 for 50/60Hz systems in the case of the DRC1705 and DRC1706 converters.

AMPLIFIER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



Two Speed Processor (for Coarse/Fine Synchro/Resolver Systems)

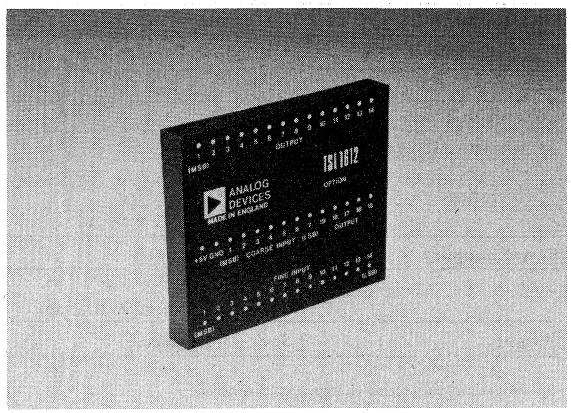
TSL1612

FEATURES

- 36:1, 18:1 or 9:1 Ratios with Same Module
- No False Output Readings
- Fast (500ns) Parallel Operation
- Easy to Use
- Up to 19-Bits Resolution
- Automatic Correction for Misalignment Between Synchros or Resolvers
- Low Profile – 0.4" (10.2mm)

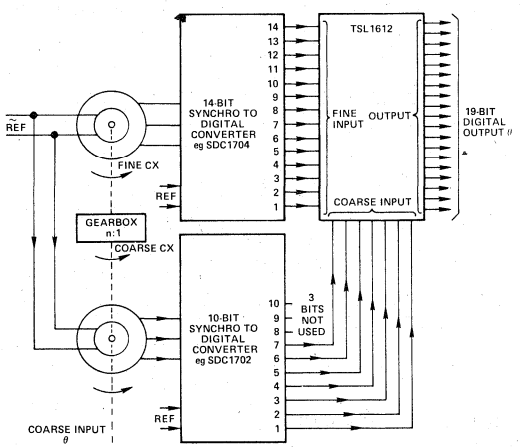
APPLICATIONS

- Combining the Digital Outputs of Synchro or Resolver to Digital Converters in Coarse/Fine Systems



GENERAL DESCRIPTION

The TSL1612 is used for combining the digital outputs of two Synchro or Resolver to Digital Converters in a mechanically or electrically geared coarse/fine system in order to produce a single unambiguous digital word representing the coarse shaft angle (see diagram).



DIGITIZING THE OUTPUT OF THE COARSE AND FINE SYNCHRO TRANSMITTERS (CX'S) IN A TWO SPEED SYSTEM

The unit described in this data sheet provides for ratios of 9:1, 18:1 and 36:1 in a single module. However, other ratios are sometimes encountered in coarse/fine Synchro or Resolver Systems, and details of special versions of the TSL1612 for use with ratios of 2:1 thru 35:1 are available on request.

The digital inputs to the TSL1612 are up to 14 bits from the fine converter and up to 7 bits from the coarse converter according to the gear ratio required. The output is up to 19-bits parallel binary angle data. The module may be used with any Synchro or Resolver Converters which produce parallel binary output.

MODELS AVAILABLE

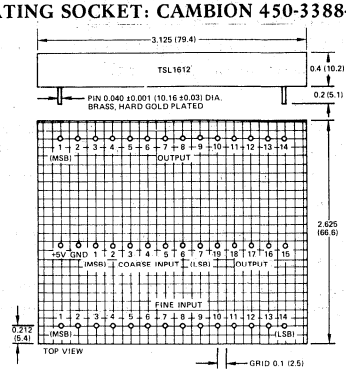
The standard TSL1612 which provides for ratios of 36:1, 18:1 and 9:1 has two options. They are as follows:

TSL1612500	0 to +70°C Operating Temperature
TSL1612600	-55°C to +105°C Operating Temperature

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Ratios:	36:1, 18:1, 9:1
Fine Synchro Input	Up to 14-Bits Parallel Binary Angle
Coarse Synchro Input	Up to 7-Bits Parallel Binary Angle
Logic Levels	DTL/TTL Compatible
Input Loading	2TTL Loads
Output Fan Out	5TTL Loads
Digital Output	Up to 19-Bits Parallel Binary Angle
Accuracy	±1LSB
Conversion Time	500ns
Temperature Range	
Storage	-55°C to +125°C
Operating	0 to +70°C Standard
	-55°C to +105°C Extended
Power Supplies	+5V ±5% @ 600mA
Size	3.125" X 2.625" X 0.4"
	79.4mm X 66.6mm X 10.2mm
Weight	3.5ozs. 100 grams

Specifications subject to change without notice.

CONNECTING THE TSL1612

For all ratios the fine SDC outputs connect directly to the fine TSL1612 inputs i.e. bit (1) out to bit (1) in through to bit 14 out to bit 14 in. If a Synchro or Resolver to Digital Converter with a resolution of less than 14 bits is used to provide the fine input, then the unused inputs to the TSL1612 should be grounded and the output accuracy will be reduced accordingly by the same number of bits.

The connections of the coarse inputs and the TSL1612 outputs change according to the ratio to be obtained ie:-

36:1 RATIOS

Bits 1 to 7 from the coarse Synchro or Resolver to Digital Converter should be connected to bits 1 to 7 on the coarse input of the TSL1612. The output is taken from bits 1 to 19.

18:1 RATIOS

Bits 1 to 6 from the coarse Synchro or Resolver to Digital Converter should be connected to bits 2 to 7 on the coarse input of the TSL1612. The output is taken from bits 2 to 19 (bit 2 is the MSB of the output word).

9:1 RATIOS

Bits 1 to 5 from the coarse Synchro or Resolver to Digital Converter should be connected to bits 3 to 7 on the coarse input of the TSL1612. The output is taken from bits 3 to 19 (bit 3 is the MSB of the output word).

CORRECTION FOR MISALIGNMENT OF THE COARSE AND FINE SYNCHROS OR RESOLVERS

In the two speed digital converters which receive inputs from both the coarse and fine synchros, circumstances will occur when the coarse angle determined by the most significant digits of fine synchro will conflict with the overlapping least significant digits of the coarse synchro. (This is due to the backlash in the gearing or misalignment in the synchros causing different readings at the major transition points.) Digital logic circuits for resolving this conflict are included in the TSL1612. The digital reading from the fine synchro is made to dominate in the overlapping region, and a correction is made bringing the coarse reading into line to provide an unambiguous digital representation of the angle of the coarse shaft. The TSL1612 will correct for a misalignment of (90 divided by the ratio) degrees.

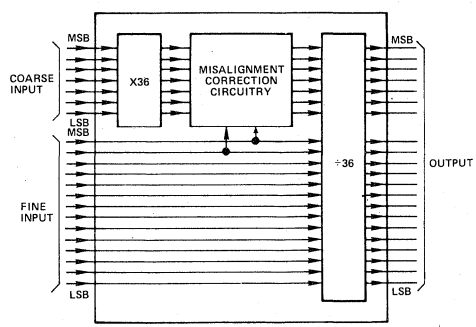
DATA TRANSFER FROM THE TSL1612

Data transfer can be made in a number of ways in which two are listed below.

1. The BUSY outputs of the fine and coarse Synchro/Resolver to Digital Converter can be "OR"ed together to give an indication of when neither converter is being updated (see appropriate converter data sheet). The data can then be taken from the TSL1612. (The conversion time of the TSL1612 is usually insignificant.)
2. The INHIBIT can be applied to both the Synchro/Resolver to Digital Converters simultaneously in order to freeze their outputs (see appropriate data sheet). When the inputs to the TSL1612 are frozen the output data can be taken. In cases where 12 bits is sufficient for the fine input, the three-state input SDC1725 Synchro/Resolver to Digital Converter should be used in conjunction with the SDC1726 on the coarse input. These converters allow the INHIBIT to be used without any risk of opening the internal converter tracking loop (see data sheet).

THEORY OF OPERATION

The theory of operation of the TSL1612 is shown in the diagram below.



FUNCTIONAL DIAGRAM OF TSL1612

ORDERING INFORMATION

Order:-

TSL1612500 for 0 to +70°C Operating Temperature Range.

TSL1612600 for -55°C to +105°C Operating Temperature Range.

Sample/Track-Hold Amplifiers

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AD583K Monolithic IC Sample-Hold Amplifier, High Speed	13-11
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THS/THC Modules, Ultra-High-Speed Track-Hold Amplifier Series	13-31

Selection Guide
Sample/Track-Hold Amplifiers

In this Selection Guide, Sample/Track-Hold Amplifiers are grouped into three categories:

1. General Purpose
2. High Speed
3. High Resolution

Complete descriptions, specifications, and applications can be found in the data sheets. General information regarding Sample/Track-Hold Amplifiers can be found in the following pages. Additional devices with sample-hold functions can be found in Sections 9 (D/A Converters-Deglitchers), 10 (A/D Converters), 15 (Data-Acquisition Subsystems), and 16 (Microcomputer Interfaces). Specifications are typical at rated supply voltage, and $T_A = 25°C$, except where noted otherwise.

1. GENERAL PURPOSE

Model	Acquisition Time	Characteristics	Page
AD583K	4μs to ±0.1% (C = 50pF)	Monolithic IC, aperture time 50ns, 10pC charge transfer	13-11
AD582K/S#	6μs to ±0.1% (C = 100pF)	Monolithic IC, aperture time 150ns, nonlinearity ±0.01%, low cost	13-7

2. HIGH SPEED

Model	Acquisition Time	Characteristics	Page
HTS-0025	20ns to 1%	Hybrid (metal or glass), aperture jitter 20ps, 0.01% nonlinearity	13-15
THS-0025	25ns to 0.1%	Module, TTL or ECL, aperture jitter 20ps, 0.01% nonlinearity	13-31
THS-0060	75ns to 0.1%	Module, TTL or ECL, aperture jitter 20ps, 0.01% nonlinearity	13-31
HTC-0300	100ns to 0.1%	Hybrid (metal or glass), aperture jitter 100ps max, 0.01% nonlinearity	13-15
THC-0300	100ns to 0.1%	Module, aperture jitter 100ps max, 0.01% nonlinearity	13-31
THS-0225	300ns to 0.1%	Module, TTL or ECL, aperture jitter 20ps, 0.01% nonlinearity	13-31
THC-0750	300ns to 0.1%	Module, aperture jitter 100ps max, 0.01% nonlinearity	13-31
SHA-2A	500ns max to 0.01%	Module, aperture jitter 250ps, gain nonlinearity 0.01% max	13-21
THC-1500	1μs to 0.1%	Module, aperture jitter 100ps max, 0.01% nonlinearity	13-31

3. HIGH RESOLUTION

Model	Acquisition Time	Characteristics	Page
SHA1144	8μs max to 0.003%	Module, aperture jitter 0.5ns, max gain nonlinearity 0.001%, use with 14-bit ADC1130/1131	13-25

#Monolithic chips available with guaranteed performance for precision hybrids.
Chip catalog available upon request.

Orientation
Sample/Track-Hold Amplifiers

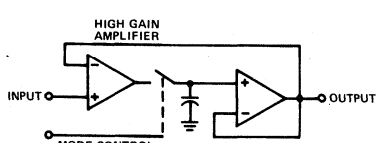
The principal application for sample/track-hold amplifiers is to maintain an analog-to-digital converter's input constant during conversion, at a value representing the analog input as of a certain precisely known time. The characteristics of the SHA are crucial to system accuracy and the reliability of the digital data, especially in 12-bit and/or high-throughput-rate applications.

A sample/track-hold amplifier (s/h or SHA), as its name indicates, has two modes of operation, programmed by a digital control-input. In the *track*– or *sample*–mode, the output follows the input, usually with a gain of +1. When the mode-input switches to *hold*, the output of the SHA ideally retains the last value it had when the command to hold was given, and it retains that value until the logic input dictates *track (sample)*, at which time the output ideally jumps to the input value and follows the input until the next *hold* command is given.

Analog Devices *track-holds* and *sample-holds* are functionally identical; they are designed to acquire input signals for either immediate hold or for a possibly extended period of tracking. They should not be confused with ac devices termed "sample-hold" that can *only* obtain quick samples and cannot track the input continuously.

SHA CIRCUITRY AND HARDWARE

A sample-hold amplifier usually consists of a storage capacitor, input- and output buffer-amplifiers, and a switch and its drive-circuitry. During *sample*, the circuit is connected to promote rapid charging of the capacitor. During *hold*, the capacitor is disconnected from its charging source and–ideally– retains its charge. The figure below shows a typical feedback configuration (AD583): the input buffer is a high-gain differential amplifier with a current output that charges the capacitor through the logic-controlled switch. The capacitor is unloaded by a unity-gain buffer-follower. The output is fed back to the negative input (as in an op-amp follower configuration), and thus, in *sample*, the charge on the capacitor is compelled to follow the input. In *hold*, the input amplifier no longer drives the capacitor; it retains its charge, unloaded by the output follower. In another popular configuration, the capacitor is used as the feedback element of an inside-the-loop integrator (AD582, SHA1144, HTC-0300). The highest-speed devices (HTS-0025) usually run open-loop.

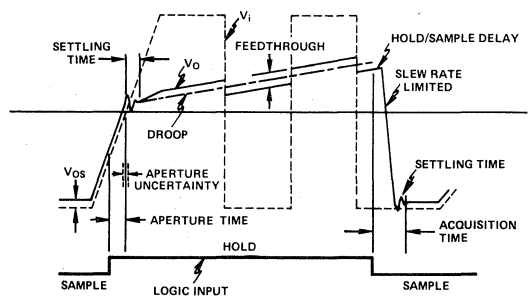


Since drive current is finite, and leakage current in *hold* is not zero, the capacitance–if large–limits the slewing rate in *sample* and–if small–converts leakage current to "droop" in *hold*. In s/h *modules*, the capacitance is usually fixed, and the properties of the complete device are optimized for one condition– and so specified. In s/h *monolithic ICs*, the capacitor is omitted, and furnished by the user (both for flexibility and because good capacitors for this purpose are hard to integrate). The optimum capacitance can be selected for the specific application. Design curves of performance vs. capacitance, given on the IC data sheets (AD582 and AD583) facilitate this process. In some types, the gain connections are external, like those of an op amp (AD582, AD583, SHA1144), permitting gains other than +1.

PERFORMANCE

In the *sample* mode, it is useful to consider that a SHA's performance can be characterized by specifications similar to those of a closed-loop operational amplifier (offset, drift, nonlinearity, gain error, bias current, etc.), but with somewhat slower response (gain-bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However, during the *sample-to-hold, hold,* and *hold-to-sample* states, the dynamic nature of the mode-switching introduces a number of specifications that are peculiar to SHAs. The most-important of these are defined below and illustrated in the adjoining figure. They include the *aperture time* and its *uncertainty*, the *sample-to-hold step, feedthrough* and *droop* (in hold), and *acquisition time.*



DEFINITIONS

Acquisition Time is the time required by the output of the device to reach its final value, within a specified error band, after the *sample* command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

Aperture (Delay) Time is the time required after the *hold* command for the switch to open fully. The sample is, in effect, delayed by this interval, and the *hold* command would have to be advanced by this amount for precise timing.

Aperture Uncertainty—or *Aperture (Delay) Jitter*—is the range of variation in the *aperture time*. If the *aperture time* is "tuned out" by advancing the *hold* command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution. For example, the SHA-2A's specs are 10ns and 0.25ns; the corresponding specs of the AD583 are 150ns and 15ns.

Charge Transfer (or *offset step*), the principal component of *sample-to-hold* offset (or *pedestal*), is the charge transferred to the storage capacitor via stray capacitance when switching to the *hold* mode. It can sometimes be reduced by lightly coupling an appropriate-polarity version of the *hold* signal to the capacitor for cancellation. The associated voltage error ($\Delta Q/C$) can be reduced by using greater capacitance for storage; but this increases response time.

Droop is the change of the output voltage during *hold* as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a *(droop* or *drift)* current, in modules, a dV/dt. (Note: $I = CdV/dt$.)

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in *hold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Sample-to-Hold Offset, a shift in level between the last value in *sample* and the value settled-to in *hold*, is the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as *offset nonlinearity.*

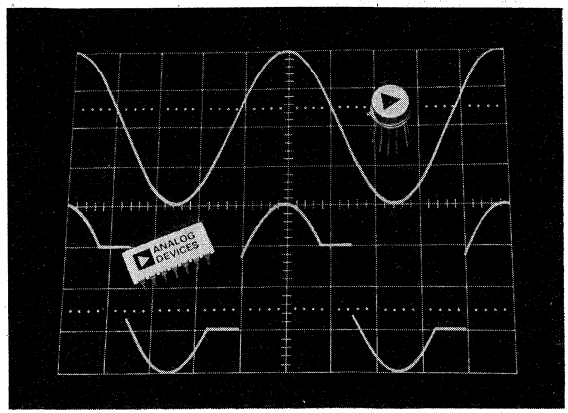
ANALOG DEVICES

Low Cost Sample/Hold Amplifier

AD582

FEATURES

- Low Cost
- Suitable for 12-Bit Applications
- High Sample/Hold Current Ratio: 10^7
- Low Acquisition Time: 6μs to 0.1%
- Low Charge Transfer: <2pC
- High Input Impedance in Sample and Hold Modes
- Connect in Any Op Amp Configuration
- Differential Logic Inputs



PRODUCT DESCRIPTION

The AD582 is a low cost integrated circuit sample and hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample and hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the full military temperature range, −55°C to +125°C. Both versions may be obtained in either the hermetically sealed, TO-100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The monolithic AD582 is the lowest cost sample and hold amplifier available. Until recently, quality sample and hold circuits could only be fabricated with costly discrete or hybrid components.
2. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
3. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
4. The AD582 offers a high, sample-to-hold current ratio: 10^7. The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
5. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
6. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

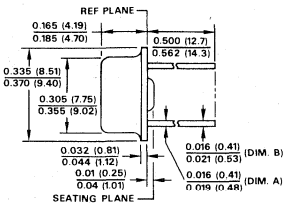
MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Time, 20V p-p Input, Hold 0V	150ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, ±10V_{OUT}	100pA max	*
Droop Current, T_{min} to T_{max}	1nA	50nA max
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	*
Common Mode Rejection V_{CM} = 20V p-p, F = 50Hz	60dB min (70dB typ)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 200pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 200pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 200pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	*
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	±V_S	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	±V_S	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	*
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*
Lead Temperature (Soldering, 15 sec)	+300°C	*

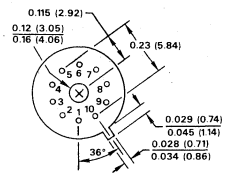
*Specifications same as AD582K.

Specifications subject to change without notice.

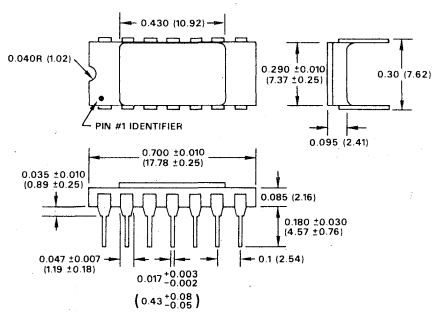
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





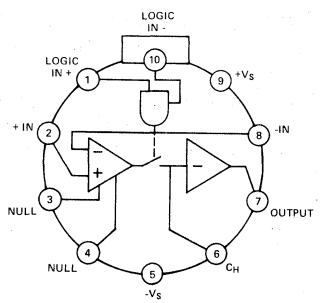
TO-100 "H"



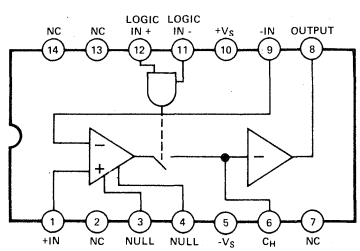
TO-116 "D"

PIN CONFIGURATIONS

TOP VIEW



10 PIN TO-100



14 PIN DIP

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

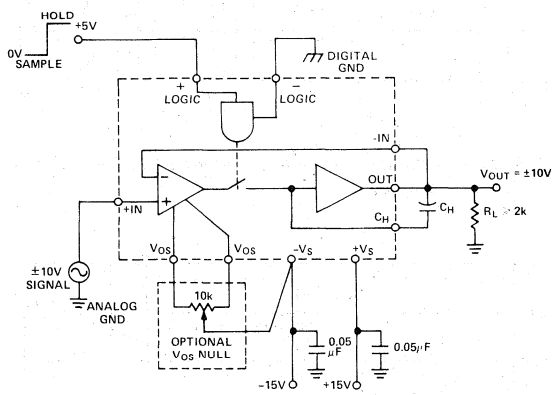


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

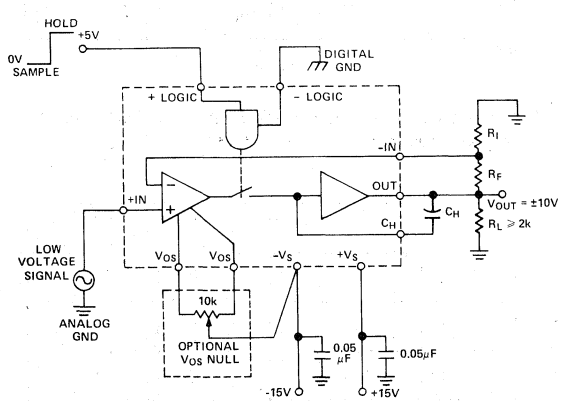


Figure 2. Sample and Hold with A = (1 + R_F/R_I)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

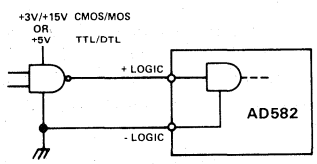


Figure 3A. Standard Logic Connection

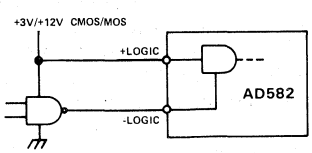


Figure 3B. Inverted Logic Sense Connection

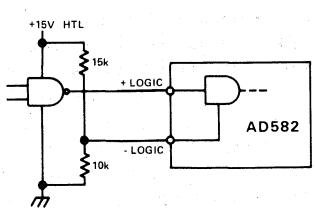


Figure 3C. High Threshold Logic Connection

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

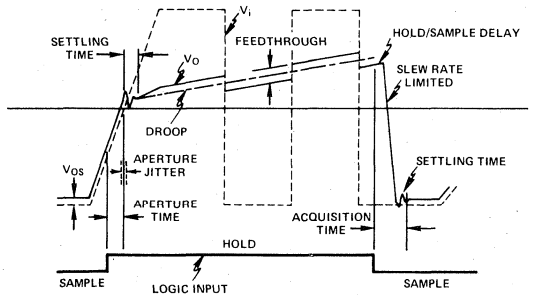


Figure 4. Pictorial Showing Various S/H Characteristics

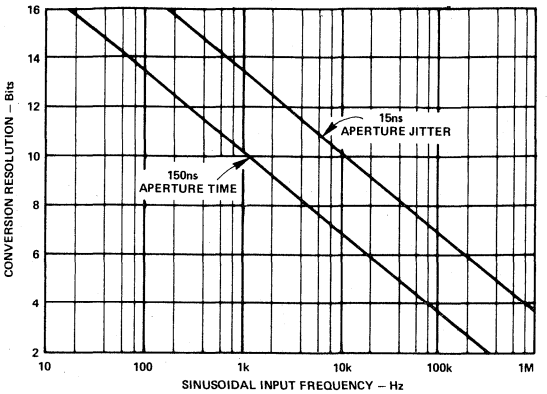


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

Aperture Time is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the sample-to-hold command 150ns with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\ (\text{Volts/sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$

(See also Figure 6.)

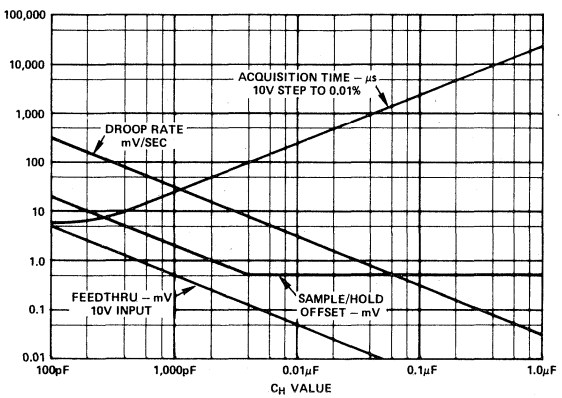


Figure 6. Sample and Hold Performance as a Function of Hold Capacitance

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Charge Transfer is the charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the hold mode. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H(\text{pF})}$$

(See also Figure 6.)

Sample to Hold Offset is that component of D.C. offset independent of C_H (see Figure 6). This offset may be nulled using a null pot, however, the offset will then appear during the sampling mode.

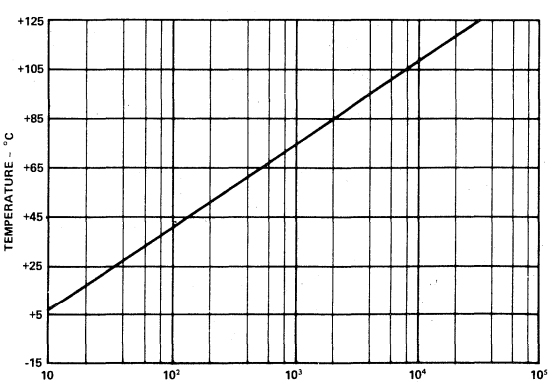


Figure 7. Droop Current vs. Temperature

IC Sample and Hold Gated Op Amp

AD583

FEATURES

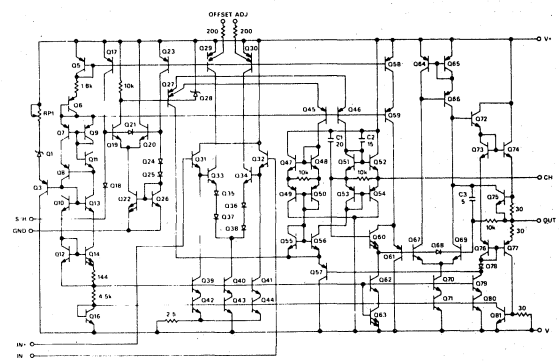
High Sample-to-Hold Current Ratio: 10^6
High Slew Rate: 5V/μs
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

PRODUCT DESCRIPTION

The AD583 is a monolithic sample and hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier. An external holding capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.



Schematic Diagram

PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperture time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise specified)

MODEL	AD583K
OPEN LOOP GAIN R_L = 2kΩ, T_{min} to T_{max}	25k min (50k typ)
OUTPUT VOLTAGE SWING R_L = 2kΩ, T_{min} to T_{max}	±10V min
OUTPUT CURRENT	±10mA min
OUTPUT RESISTANCE	5Ω
OFFSET VOLTAGE T_{min} to T_{max}	6mV max (3mV typ) 8mV max (4mV typ)
BIAS CURRENT T_{min} to T_{max}	200nA max (50nA typ) 400nA max
OFFSET CURRENT T_{min} to T_{max}	50nA max (10nA typ) 100nA max
INPUT RESISTANCE	5MΩ min (10MΩ typ)
COMMON MODE RANGE	±10V min
COMMON MODE REJECTION T_{min} to T_{max}	74dB min (90dB typ)
GAIN BANDWIDTH PRODUCT	2MHz
SLEW RATE Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = ±10V p-p	5V/μs
RISE TIME Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	100ns
OVERSHOOT Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	20%
DIGITAL INPUT CURRENT V_{in} = 0, T_{min} to T_{max} V_{in} = +5.0V, T_{min} to T_{max}	 0.8mA max (Logic "Sample") 20μA max (Logic "Hold")
DIGITAL INPUT VOLTAGE Low T_{min} to T_{max} High T_{min} to T_{max}	 0.8V max 2.0V min
ACQUISITION TIME Av = +1, R_L = 2kΩ, C_L = 50pF to 0.1% of final value: to 0.01% of final value:	 4μs 5μs
APERTURE TIME	50ns
APERTURE JITTER	5ns
DRIFT CURRENT T_{min} to T_{max}	50pA max (5pA typ) 1.0nA max (0.05nA typ)
CHARGE TRANSFER	20pC max (10pC typ)
SUPPLY CURRENT	5.0mA max (2.5mA typ)
POWER SUPPLY REJECTION	74dB min (90dB typ)
OPERATING TEMP	0 to +70°C
STORAGE TEMP	-65°C to +150°C

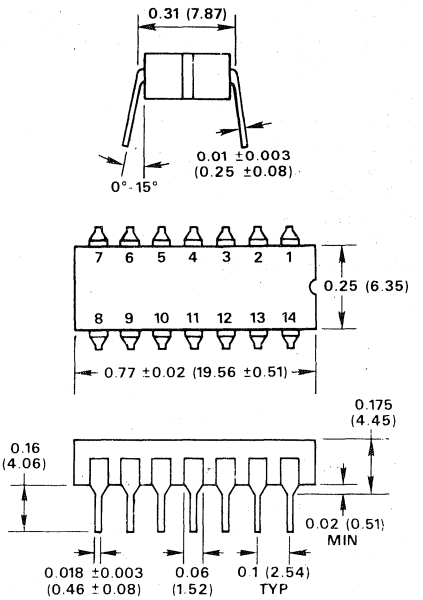
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

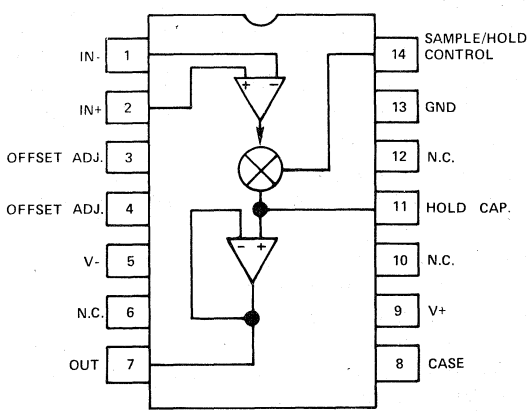
Voltage between V+ and V- Terminals	40V
Differential Input Voltage	±30V
Digital Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



PIN CONFIGURATION



APPLYING THE AD583

Figure 1 shows the AD583 connected in a simple sample and hold configuration with unity gain and offset nulling. Any other standard op amp gain and frequency response configuration may also be used. Note that the holding capacitor, C_H, should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), teflon or Mica types are recommended.

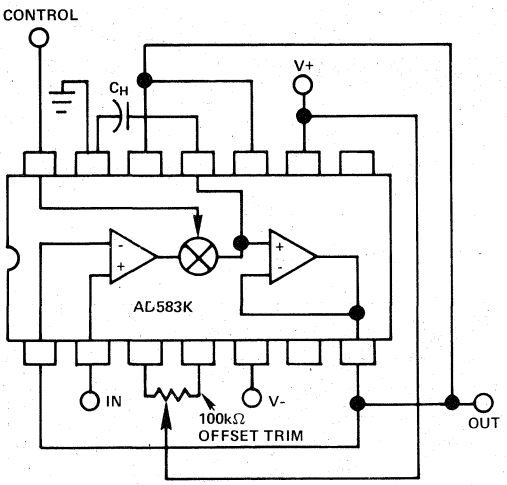


Figure 1. Basic Track-and-Hold/Sample-and-Hold

Figure 2 shows the guard ring used to reduce leakage paths between the pc board and the package. This minimizes drift during the hold command.

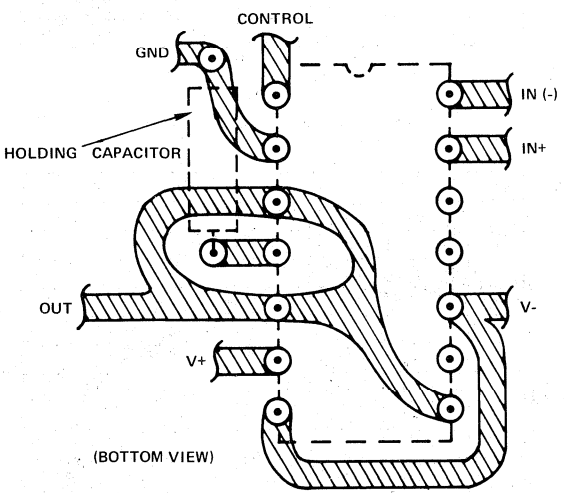


Figure 2. Guard Ring Layout

Also note that the input amplifier of the AD583 may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

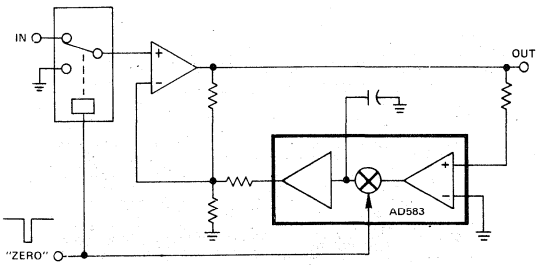


Figure 3. Automatic Offset Zeroing

The circuit of Figure 3 illustrates how the AD583 may be used to automatically zero a high gain amplifier. Basically, the input is periodically grounded and the output offset is then sampled and fed back to cancel the error. This technique is useful in A/D conversion, instrumentation, DVM's to eliminate offset drift errors by periodically rezeroing the system.

Care should be taken to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

DEFINITION OF TERMS

Acquisition Time:

Acquisition Time is the time required by the device to reach its final value within ±0.1% after the sample command has been given. This includes switch delay time, slewing time, and settling time and is the minimum sample time required to obtain a given accuracy.

Charge Transfer:

Charge Transfer is the small charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the sample mode. Sample-to-hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H\text{(pF)}}$$

Aperture Time:

The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

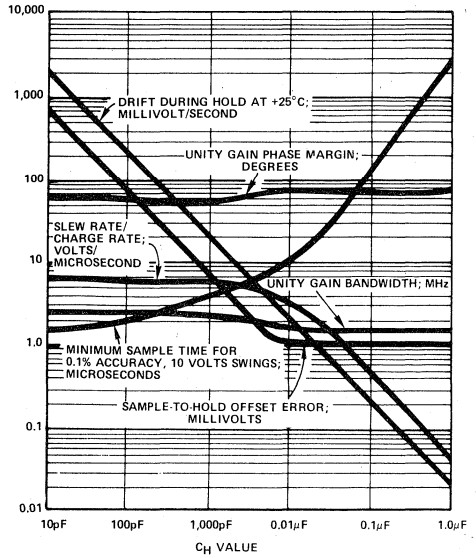
Drift Current:

Leakage currents from the holding capacitor during the sample mode cause the output voltage to drift. Drift rate (or droop rate) is calculated from drift current values using the formula:

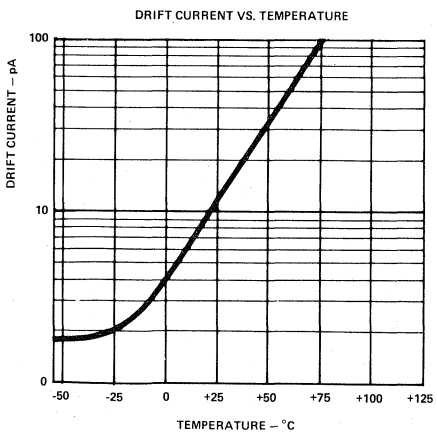
$$\frac{\Delta V}{\Delta T}\ \text{(Volts/sec)} = \frac{I\text{(pA)}}{C_H\text{(pF)}}$$

Performance Curves

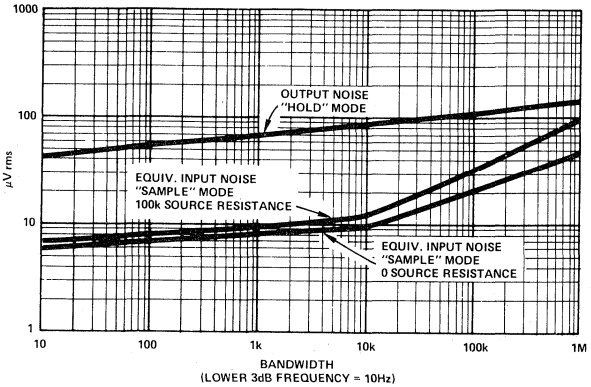
V_{SUPPLY} = ±15V dc, T_A = +25°C, C_H = 1,000pF unless otherwise specified



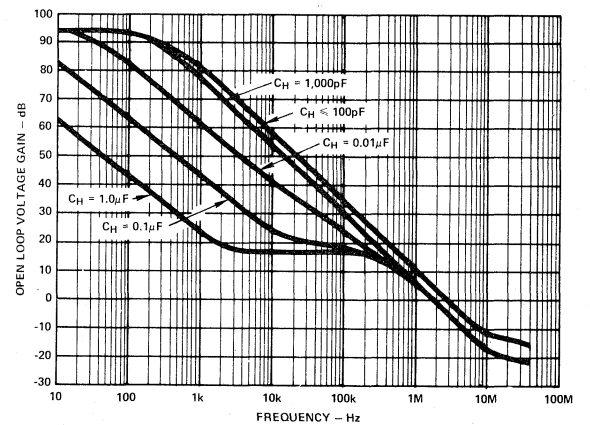
Typical Sample-and-Hold Performance as a Function of Holding Capacitance



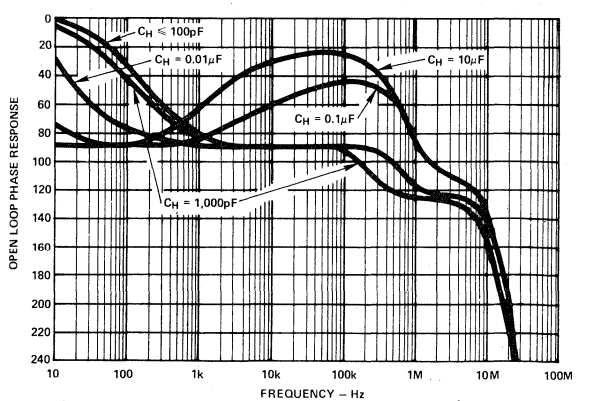
Drift Current vs. Temperature



Broadband Noise Characteristics



Open Loop Frequency Response



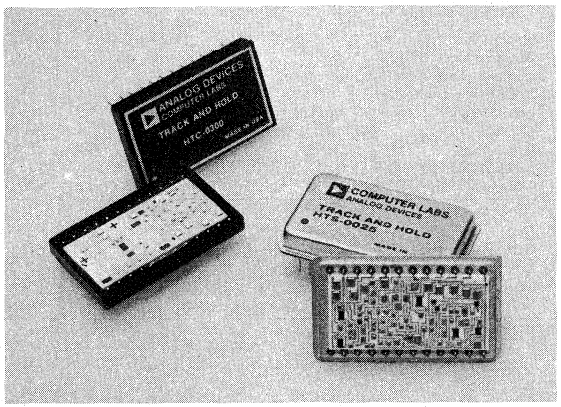
Open Loop Phase Response

Ultra High Speed Hybrid Track-and-Hold Amplifiers

HTS-0025, HTC-0300

FEATURES
- Aperture Times to 20ps
- Acquisition Times to 20ns
- Linearity 0.01%
- $10^{10}\,\Omega$ Input Z (HTS-0025)
- ±50mA Output Current

APPLICATIONS
- Data Acquisition Systems
- Data Distribution Systems
- Peak Measurement Systems
- Simultaneous Sample & Hold
- Analog Delay & Storage



GENERAL DESCRIPTION

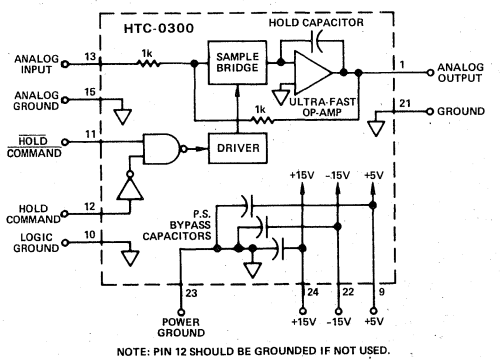
The HTS-0025 and HTC-0300 represent "state of the art" in the ability of an analog device to capture and hold rapidly changing transient or continuous waveforms. The user can choose between them by making engineering trade-offs between maximum speed/bandwidth capability, precision gain, feedthrough rejection, input impedance, hold time, harmonic distortion, output swing, logic type, power requirements and price. With an aperture uncertainty of only 20ps and an acquisition/settling time of 20ns, the HTS-0025 is the fastest hybrid sample/track-and-hold amplifier available.

It achieves this performance with a dc coupled Schottky diode sampling bridge driven by a $10^{10}\,\Omega$ input impedance FET amplifier and followed by a low impedance – 10Ω max – output amplifier.

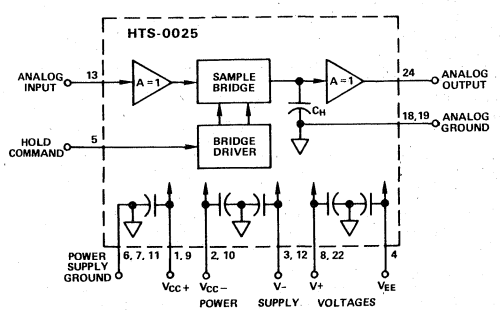
The HTC-0300 provides 100ps aperture uncertainty and 170ns acquisition/settling time to 0.1% for a 10 volt input-output swing (less than 300ns for 12-bit settling). It achieves this speed and precision gain (–1.00 ±0.1%) with high speed op amps and diode switches. These techniques also improve feedthrough rejection, output swing, linearity, harmonic distortion and droop rate.

APPLICATIONS

The most common use for a sample/track-and-hold is to place it ahead of an A/D converter to allow digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the HTS-0025 can allow a reduction of system aperture to 20ps. These sample/track-and-hold amplifiers are also used for peak holding functions, simultaneous sampling A/D's (with appropriate analog multiplexing), and other high-speed analog signal processing applications. These hybrids have been used to construct A/D converters of up to 12 bits of resolution with word rates as high as 20MHz. The HTC-0300 is designed to be used with Analog Devices' HAS Series hybrid A/D converters.



Block Diagram – HTC-0300



Block Diagram – HTS-0025

SPECIFICATIONS (typical at +25°C and nominal power supply voltages unless otherwise noted)

MODEL	UNITS	HTS-0025	HTS-0025M	HTC-0300	HTC-0300M
DYNAMIC CHARACTERISTICS					
Acquisition Time (See Figure 1)					
to 1% for 1V Output Step	ns typ (max)	20 (30)	*	N/A	**
to 0.1% for 10V Output Step	ns typ (max)	N/A	*	170 (200)	170 (200)
Sample Rate[1]	MHz max	30	*	5	**
Aperture Time	ns min (typ) (max)	6 (10) (20)	*	*	*
Settling Time	ns typ (max)	20 (30)	*	100 (120)	**
Bandwidth (3dB 2V p-p Input)	MHz min	30	20	N/A	**
(3dB Small Signal Input)	MHz min	N/A	*	8	**
Slew Rate	V/μs typ (min)	400 (200)	*	250 (120)	250 (100)
Aperture Uncertainty	ps (rms) max	20	*	100	**
Harmonic Distortion (See Figure 6 and Output Loading)	dB typ (max)	65 (60)	*	75 (62)	**
Feedthrough Rejection (2V p-p, 10MHz Input)	dB min	70	*	N/A	**
(dc to 2.5MHz)	dB min	N/A	*	70	**
Droop Rate	mV/μs typ (max)	0.2 (4)[2]	0.2 (30)	0.005 (0.007)	0.005 (0.1)
Pedestal During Hold (See Figure 1)	mV typ (max)	2 (20)	*	5 (50)	**
Transients (See Figure 1)	mV typ (max)	30 (100)	*	N/A	**
ACCURACY/STABILITY DC					
Gain	V/V	+0.92 min	*	−1.00 ±0.1%	**
Gain vs. Temperature	ppm/°C typ (max)	20 (40)	*	10 (50)	**
Zero Offset Voltage	mV typ (max)	2 (20)	*	2 (20)	**
Offset vs. Temperature	typ (max)	50 (150)μV/°C	*	40 (75)ppm/°C	**
Linearity	% max	0.01	*	*	*
INPUT					
Voltage Range	V max	±2	*	±10	**
60dB Feedthrough Rejection	V p-p max	3	*	N/A	**
Impedance	Ω typ (min)	10^{10} (10^{9})	10^{10} (10^{8})	1000	**
Bias Current	nA max	15	100	15μA	**
OUTPUT					
Voltage	V max	±2	*	±10	**
Current (not short circuit protected)	mA max	±50	*	*	*
Impedance	Ω typ (max)	3 (10)	*	0.1 (dc)	**
Loading — Harmonic					
Distortion for 2V p-p 50dB	Ω min	50	*	N/A	**
Signal and Specified R_L 60dB	Ω min	100	*	N/A	**
65dB	Ω min	200	*	N/A	**
Noise[3]	mV rms	0.1 (max)	0.2 (max)	0.1	**
HOLD COMMAND (DIGITAL INPUT)					
Logic Compatible		ECL	*	TTL	**
"0" = Track/"1" = Hold[4]	V	−1.5 to −1.4/−0.7 to −1.05	*	N/A	**
"Hold" Input, "0" = Track/"1" = Hold	V	N/A	*	0 to +0.4/+2.4 to +5	**
"$\overline{\text{Hold}}$" Input, "0" = Hold/"1" = Track	V	N/A	*	0 to +0.4/+2.4 to +5	**
POWER REQUIREMENTS — HTS					
V+ = +15V ±0.5V (Pins 8 and 22)	mA max	40	*	N/A	**
V− = −15V ±0.5V (Pins 3 and 12)	mA max	40	*	N/A	**
V_{CC}+ = +4.4V to +15.5V (Pins 1 and 9)[5]	mA max	15	*	N/A	**
V_{CC}− = −4.95V to −15.5V (Pins 2 and 10)[5]	mA max	15	*	N/A	**
V_{EE} = −5.2V to ±0.25V (Pin 4)	mA max	40	*	N/A	**
POWER REQUIREMENTS — HTC					
±12V to ±18V	mA max	N/A	*	25	**
+5V to ±0.25V	mA max	N/A	*	25	**
Power Supply Rejection Ratio	mV/V	N/A	*	10	**
TEMPERATURE RANGE					
Operating (Case)	°C	0 to +70	−55 to +100	0 to +70	−55 to +100
Storage	°C	−55 to +125	*	*	*

NOTES:

[1] Sample rates shown are a guide only, and are based on system acquisition times — not logic speed. These rates can be exceeded with acquisition time trade-offs.

[2] Droop rate for case temperatures up to 50°C is 1mV/μs max.

[3] Noise level measured in track mode is 5MHz bandwidth. Noise level increases when high duty cycle repetitive hold command is applied. A 50% duty cycle hold command results in approximately 0.3mV (rms) total noise output.

[4] One ECL-10k Gate, no pulldown resistor.

[5] V_{CC}+ may be tied to V^+, V_{CC}− may be tied to V^- or V_{EE}. However, for proper operation, V_{CC}+ and V_{CC}− must have the same numerical value.

*Specifications same as model HTS-0025.

**Specifications same as model HTC-0300.

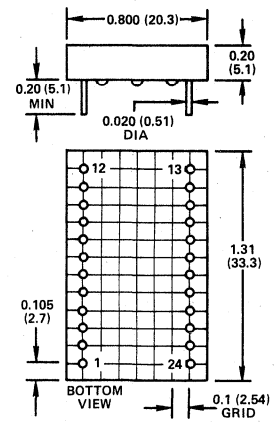
Specifications subject to change without notice.

Specifications in parenthesis ( ) indicate max/min over entire specified operating temperature range.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

HTC-0300 (Only) GLASS PACKAGE



DOT ON TOP INDICATES POSITION OF PIN 1.

PIN DESIGNATIONS

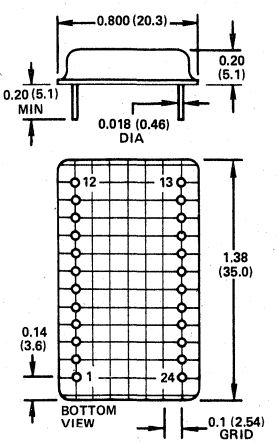
PIN	FUNCTION (HTC-0300)	FUNCTION (HTS-0025)
1	ANALOG OUTPUT	V_{CC}+ [+5V to +15.5V]*
2	N/A	V_{CC}- [-5V to -15.5V]*
3	N/A	V- [-15V]
4	N/A	V_{EE} [-5.2V]
5	N/A	HOLD COMMAND
6	N/A	GROUND
7	N/A	GROUND
8	N/A	V+ [+15V]
9	+5V	V_{CC}+ [+5V to +15.5V]*
10	GROUND	V_{CC}- [-5V to -15.5V]*
11	$\overline{\text{HOLD}}$	GROUND
12	HOLD	V- [-15V]
13	ANALOG INPUT	ANALOG INPUT
15	INPUT GROUND	N/A
18	N/A	ANALOG GROUND
19	N/A	ANALOG GROUND
21	GROUND	N/A
22	-15V	V+ [+15V]
23	GROUND	N/A
24	+15V	ANALOG OUTPUT

*FOR PROPER OPERATION, V_{CC}- SHOULD HAVE THE SAME NUMERICAL VALUE.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

HTS-0025, HTS-0025M, HTC-0300M METAL PACKAGE



DOT ON TOP INDICATES POSITION OF PIN 1.

TRACK-AND-HOLD (T/H) MODE

When operated in the T/H mode, these devices are allowed to "track" the input signal for a period of time prior to initiating a "hold command". During the track period, the output follows the input, and the devices function as operational amplifiers. The HTS-0025 operates as a precision follower with a gain of +1, the HTC-0300, -1.

When a Logic "1" is applied to the "hold command" input of the unit, its output is frozen. This output level is held until the track mode is reestablished by a Logic "0" at the hold command input. This operation is shown graphically in Figure 1. The held output level is the voltage value at the input at the instant (plus the aperture time) the hold command is applied.

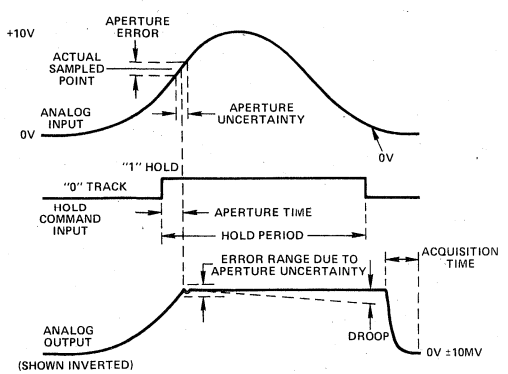


Figure 1a. Track/Hold Waveforms – HTC-0300

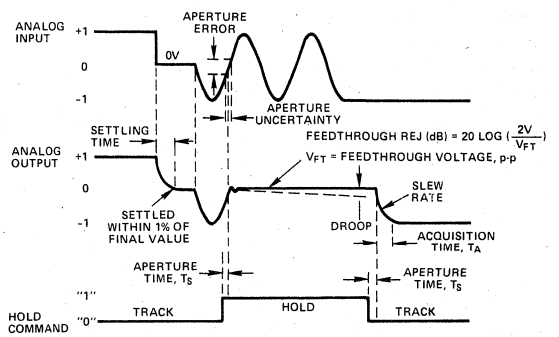


Figure 1b. Track/Hold Waveforms – HTS-0025

The HTC-0300 provides a $\overline{\text{hold}}$ input for use if the hold command is inverted, that is if the user wishes to use a "0" for the hold condition and a "1" for the track mode. Performance of the unit is identical with either type of input.

Variations in the instants of sampling are called aperture uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled. During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track-and-hold have high feedthrough rejection to prevent input-to-output leakage during the hold period. The droop rate is the amount the output changes during the hold period as a result of loading on the internal hold capacitor.

When the hold command input returns to the track condition, the amount of time required for the track-and-hold output to reestablish accurate tracking of the input signal is called the acquisition time.

SAMPLE-AND-HOLD (S/H) MODE

In the S/H mode of operation, the devices are normally left in the hold condition. A very short sample pulse is applied to the hold command input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time. For small sample-to-sample variations, a pulse width as narrow as 20 to 80ns may be used. In general, however, the pulse width should be 100 to 300ns (see Figure 4).

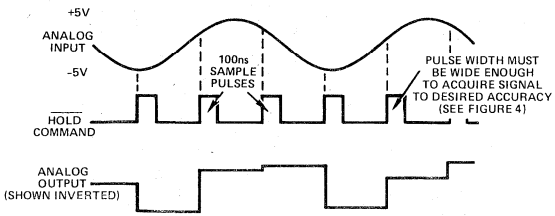


Figure 2. Sample/Hold Operation – HTC-0300

The HTC-0300 hybrid track-and-hold amplifier has been designed to operate without external trimming potentiometers and "compensation" devices required in most modular units. Active laser trimming is used on the HTC-0300 to "null" the pedestal (the offset during "HOLD" times), set the dc offset to zero, and adjust the gain of the device to unity. Internal frequency compensating elements are incorporated to make the HTC-0300 unconditionally stable and to optimize the frequency response of the internal operational amplifier for this application. Unlike other microcircuit T/H amplifiers, the HTC has a high drive capability (±50mA) and a very low output impedance which allows it to drive directly virtually all types of A/D converters (even the "current-bucking" input types which will produce a degraded A/D conversion without sufficient T/H output drive) and those with low input impedance.

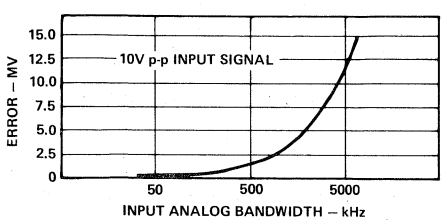


Figure 3. HTC-0300 Error Due to Aperture Uncertainty

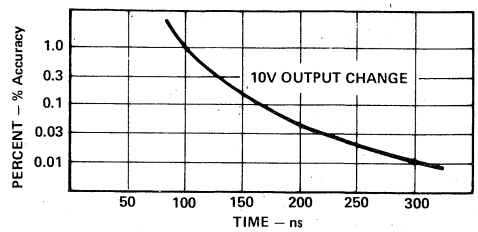


Figure 4a. Settling Accuracy vs. Acquisition Time – HTC-0300

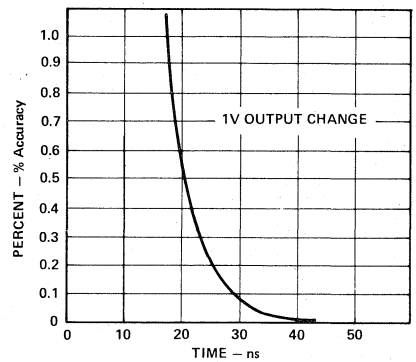


Figure 4b. Settling Accuracy vs. Acquisition Time – HTS-0025

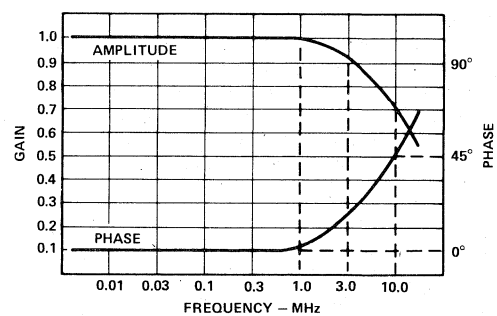


Figure 5. Amplitude and Phase Response – HTC-0300

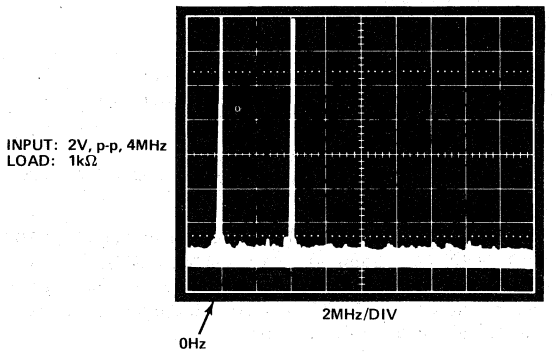


Figure 6a. Harmonic Distortion — Track Mode

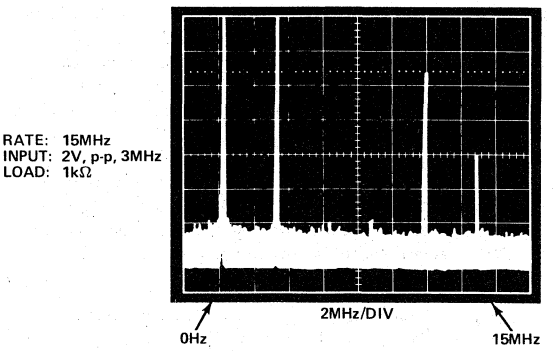


Figure 6b. Frequency Domain Outputs

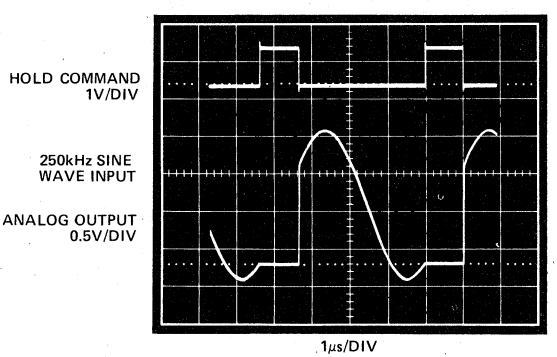


Figure 7a. Track/Hold Operation

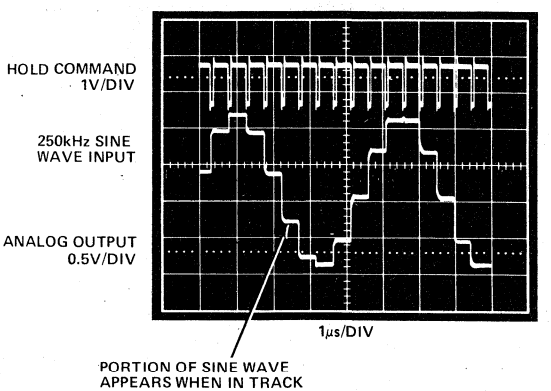


Figure 7b. Sample/Hold Operation

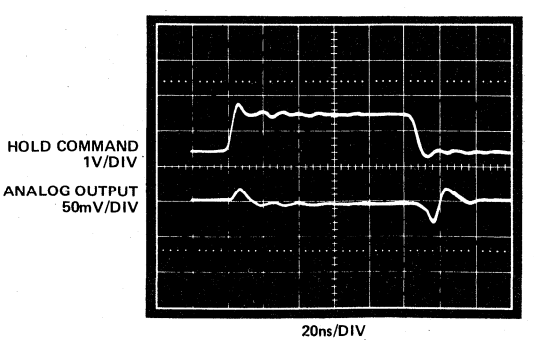


Figure 7c. Expanded View of Output Signal Showing Switching Transients and Pedestal with DC Input

A/D CONVERSION SYSTEM WITH 300kHz CONTINUOUS SAMPLING RATE AND 12-BIT BINARY OUTPUT

The circuit below illustrates a typical application of the HTC-0300 as a sample/hold amplifier preceding a successive-approximation type of A/D converter. During the conversion interval, the input voltage to the A/D must be held constant. To the extent that this input signal is not absolutely constant, an error results in the digitized output of the A/D. However, with the excellent feedthrough-rejection and droop-rate specifications of the HTC-0300, very little error in the A/D conversion process will be due to the T/H circuit. In addition, the very fast acquisition time of this hybrid microcircuit means that the A/D can be operated at very near its maximum sample rate since very little of the conversion cycle time is required for the T/H to acquire each successive signal sample.

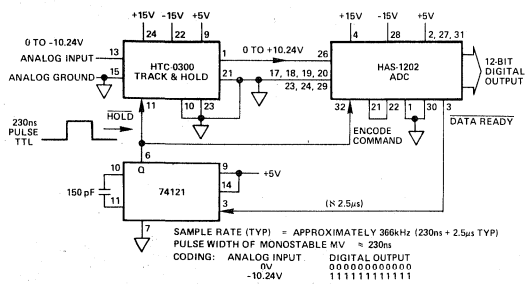


Figure 8. A/D Conversion System

Sample Rate	Approximately 300kHz
Encode Command Rate (f clock)	3.9MHz
Pulse Width of Monostable Multivibrator	230ns
Analog Input	Digital Output
0V	000000000000
+10V	111111111111

Table 1. Performance Parameters For This A/D System

ORDERING INFORMATION

Order Model Number HTS-0025 or Model Number HTC-0300 for 0 to +70°C operation. For operation from -55°C to +100°C order Model HTS-0025M or HTC-0300M in metal cases. For units processed to MIL-STD-883, consult the factory or the nearest Analog Devices' sales office.

Very High Speed 12-Bit Sample-and-Hold Amplifier

SHA-2A

FEATURES
±10V Range
10ns Aperture Delay
¼ns Aperture Jitter
300ns Settling Time
0.01% Linearity Error
Complete with Input Buffer

APPLICATIONS
Track and Hold
Peak Measurement Systems
Data Acquisition Systems
Simultaneous Sample-and-Hold

GENERAL DESCRIPTION

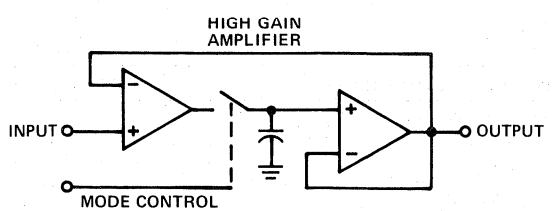
The SHA-2A is a very fast sample-and-hold module with accuracy and dynamic performance appropriate for application with very fast 12-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" mode is appropriate to allow 12-bit accurate conversion by very fast A/D converters, e.g. those having total conversion times of up to several microseconds.

DYNAMIC PERFORMANCE

The SHA-2A was designed for use with very fast A/D converters such as the Analog Devices' ADC1103 series, which convert 12 bits in less than 4μs. Since such converters will often be used to acquire data for fast slewing signal sources, the dynamic parameters were designed with this in mind. Slewing rate is 100V/μs, and settling time to 0.01% is <500ns. The aperture time of <10ns, and aperture jitter of 0.25ns, means that an input signal slewing at 200mV/μs (3kHz) will be acquired to appreciably better than one LSB uncertainty for a 12-bit converter. The maximum droop rate of 100μV/μs means that when the SHA-2A is in "hold," its output is holding constant for the ADC input, changing <0.1LSB per conversion time for a 1μs 12-bit ADC. The fast settling of the sample-hold transient allows the following A/D converter to make an accurate MSB decision only 150ns after the "hold" command is applied.

UNIQUE CIRCUIT ARRANGEMENT

Most sample-and-hold amplifier modules have input terminals connected either to a unity gain buffer, or directly to the hold capacitor through a switch. In the SHA-2A an input buffer is used, but the feedback connection has been omitted in order to allow the user to connect the SHA-2A as a follower, for unity gain, or to provide gain in order to simplify signal conditioning in his system. We call the user's attention to the fact that the input buffer bandwidth will go down as gain is increased, as it does for all op amps. Performance data is given for the unity gain buffer connection.



Typical Block Diagram

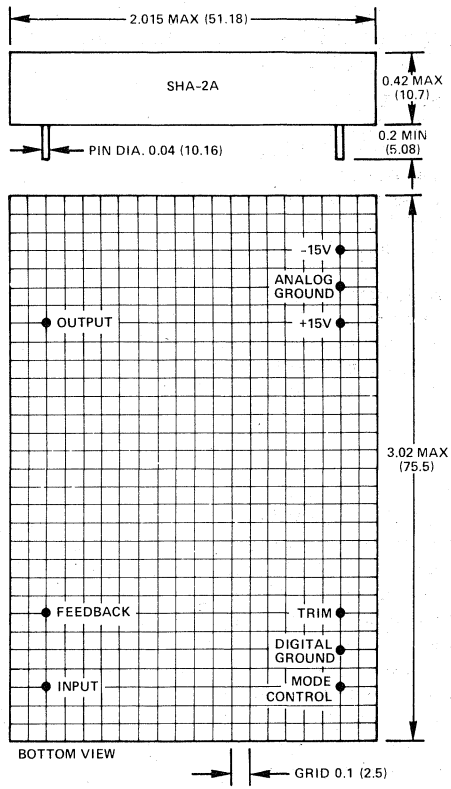
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	SHA-2A
GAIN AND ACCURACY	
Voltage Gain (Follower Connection)	+1
Gain Error (Follower Connection)	+0 -0.01%
Gain Nonlinearity	0.01% max
INPUT CHARACTERISTICS	
Input Impedance	$10^{11}\Omega$ and 7pF
Input Bias Current	100pA max
Input Range	±10V min
Initial Offset Voltage	Adjustable to 0
Offset vs Temp	100μV/°C max
Offset vs Supply	500μV/%
FREQUENCY RESPONSE (SAMPLE MODE)	
Full Power Bandwidth	1.5MHz
Slewing Rate	100V/μs
Settling Time to 0.01%	500ns max
Settling Time to 0.1%	300ns max
Noise (BW 100Hz to 1MHz)	100μV rms
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay Time	10ns
Aperture Delay Jitter	0.25ns
Switching Transient Settling (to 5mV)	150ns max
S-H Offset Nonlinearity	0.025% max
HOLDING CHARACTERISTICS	
Droop Rate	100μV/μs max
Feedthrough (10kHz, 20V p-p Input)	5mV p-p max
OUTPUT CHARACTERISTICS	
Output Voltage	±10V min
Output Current	±20mA min
Short Circuit Current	±70mA
Maximum Capacitive Load	200pF
DIGITAL CONTROL	
Logic Levels[1]	
Sample ("1")	>+2V @ 1μA to 3.7V @ 1mA
Hold ("0")	<0.8V 0 to 0.8V @ -7mA
POWER REQUIREMENTS[2]	±15V ±2% @ 100mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-25°C to +85°C
MATING SOCKET	AC1035

NOTE
[1] To achieve rated specifications, logic driving digital control input should be Schottky TTL.
[2] Recommended power supply, model 920, ±15V @ ±200mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



MATING SOCKET AC1035
The AC1035 is a simple socket assembly, 2" x 3", for mounting the SHA-2A.

MOUNTING BOARD AC1503
The AC1503 is a 2¼" x 4½" PC board with edge connector. It contains a trimmer pot for adjustment of offset, as well as a logic chip, needed to simulate terminal characteristics of the SHA-2. When the SHA-2A is mounted on the AC1503, the assembly is a pin-compatible replacement for the SHA-2.

CIRCUIT DESCRIPTION

The SHA-2A is a typical sample-and-hold module in that it consists of an input isolator, a fast switch, the storage element, and an output buffer. It differs from typical designs in two particular respects:

1. Speed – since it was designed to be compatible with very fast A/D converters of the 1μs total conversion time class, aperture delay time was reduced to 10ns, aperture jitter to 0.25ns, and settling time to 300ns for 10-bit performance.

2. Application versatility – the user completes the feedback circuit for the SHA-2A external to the module. Therefore, the module may be used in various input configurations and can easily be arranged to provide circuit gain of more than unity, to simplify signal conditioning in a subsystem.

FEEDBACK CONNECTIONS

A block diagram of the SHA-2A is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "HOLD" capacitor. The output amplifier isolates the "HOLD" capacitor, and provides low output impedance for driving the load. Since feedback is not hardwired in the module, both inverting and noninverting input terminals are available, and the SHA-2A can be connected as a follower with unity gain or potentiometric gain, as well as an inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data in the specifications is based on this operating mode.

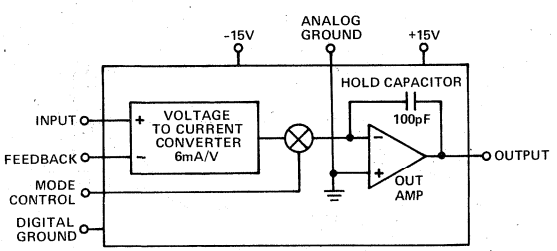


Figure 1. Block Diagram

1. Figure 2 shows feedback connections to the SHA-2A for the unity gain follower mode. Output (pin #3) is connected to feedback (or – input, pin #2). Input signal is applied to pin #1.

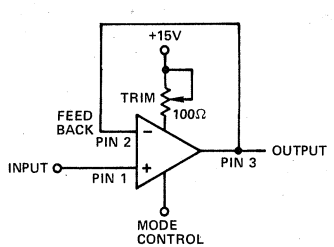


Figure 2.

2. Figure 3 shows feedback connections for noninverting operation with potentiometric gain. When the indicated values are installed, gain will be +5. As in all operational amplifiers, gain-bandwidth product is a constant for a given sample-and-hold. Effective 3dB bandwidth will be inversely proportional to gain.

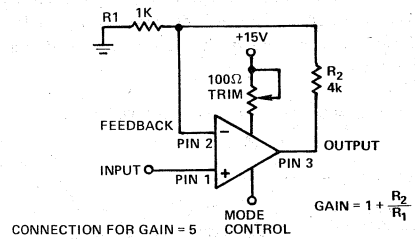


Figure 3.

3. By using conventional operational amplifier feedback connections, the SHA-2A can be connected for use as an inverter, with various gains (as determined by the R_F/R_I ratio), or as a differential amplifier.

CHARACTERISTICS OF REAL SAMPLE-HOLDS

In the ideal Sample-Hold of Figure 4a, tracking is error-free, acquisition and release occur instantaneously, settling times are zero, and hold is infinite. Commercially-available units are specified in terms of the extent to which they depart from the ideal. Here are some of the commonly-occurring deviations.

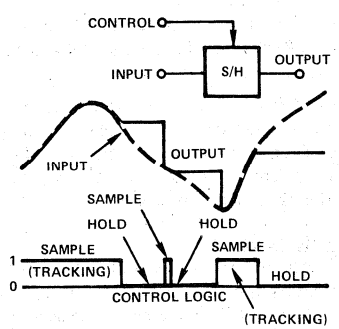


Figure 4a.

<u>During Sample (Figure 4b):</u>

Settling Time: The time required for the output to attain its final value within a specified fraction of full-scale when a full-scale input step is applied (0 to ±FS or -FS to +FS). See also *Acquisition Time* (Figure 4e).

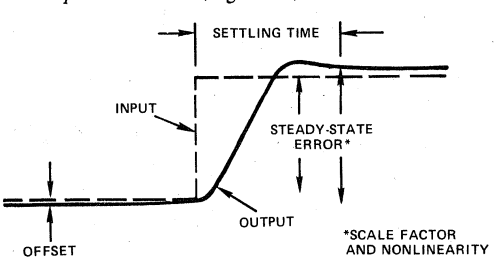


Figure 4b.

Sample to Hold (Figure 4c):

Aperture Time: The time elapsing between the command to *Hold* and the actual opening of the *Hold* switch. It has two components: a nominal time delay, and an uncertainty caused by jitter or variation from time-to-time or unit-to-unit. If a signal changing at a rate of 1V/μs must be resolved to within 0.1% of 10V (FS), the aperture *uncertainty* must be <10ns, provided that it is possible to anticipate the nominal delay and advance the command by an appropriate interval. In some sampled-data system applications, such as spectrum analyzers, auto- and cross-correlation function generators, the delay is unimportant, but the uncertainty directly affects uniformity of the sampling rate.

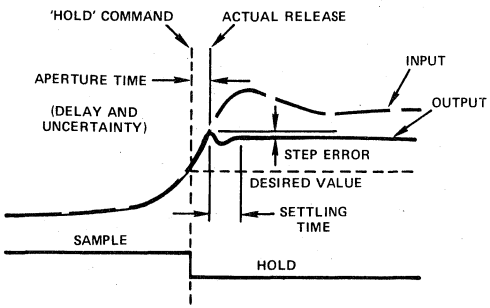


Figure 4c.

Switching Transients: At the time the switch opens, the circuit may not be in equilibrium – especially if the signal is changing rapidly – because of amplifier delay error, etc. This will cause transients at the time the switch opens.

Settling Time: The interval required for the output to attain its final value within a specified fraction of full scale, following the opening of the switch.

Sample-to-Hold Offset: A step error occurring at the initiation of the *Hold* mode caused by "dumping" of charge into the storage capacitor via the capacitance between the control circuit and the capacitor side of the switch (e.g., the gate-to-drain capacitance of a field-effect transistor).

During Hold (Figure 4d):

"DROOP": A drift of the output at an approximately constant rate caused by the flow of current through the storage capacitor (dV/dt = I/C). The current is the sum of the leakage across the switch and the amplifier's bias current.

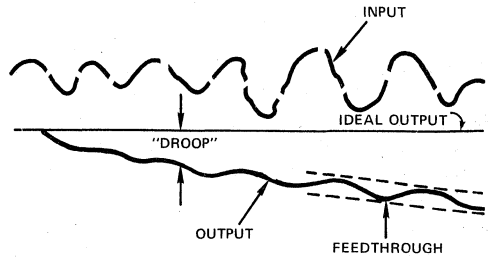


Figure 4d.

Feedthrough: The fraction of input signal that appears at the output in *Hold*, caused primarily by capacitance across the switch. Usually measured by applying a full-scale sinusoidal input at a fixed frequency (e.g., 20V p-p at 10kHz), and observing the output.

Dielectric Absorption: The tendency of charges within a capacitor to redistribute themselves over a period of time, resulting in "creep" to a new level when allowed to rest after large, fast changes. <0.01% for good polystyrene and teflon capacitors, as large as several percent for ceramic and mylar capacitors.

Hold to Sample (Figure 4e):

Acquisition Time: The time duration for which an input must be applied for sampling to the desired accuracy. Essentially the same as *Settling Time* for feedback types.

Hold-to-Sample Transients: Transients (e.g., spikes) occurring between the *Sample* command and final settling.

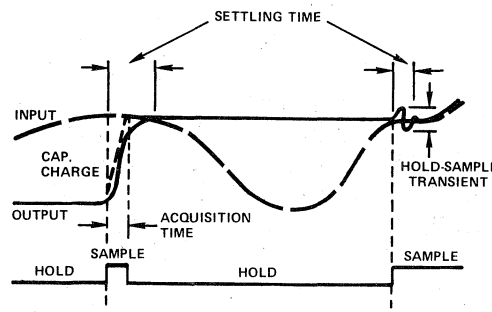


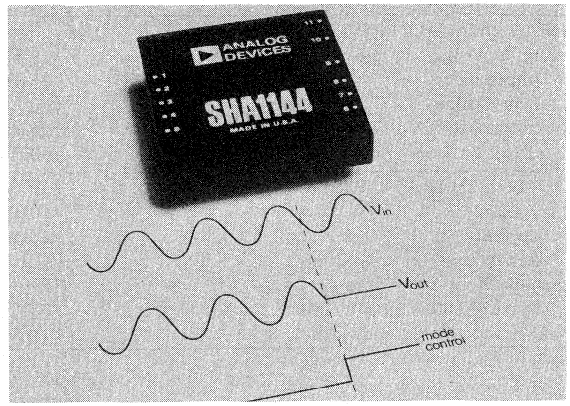
Figure 4e.

High Resolution 14-Bit Sample and Hold Amplifier

SHA1144

FEATURES
- ±10V min Input/Output Range
- 50ns Aperture Delay
- 0.5ns Aperture Jitter
- 6μs Settling Time
- ±0.001% Max Gain Linearity Error
- Complete with Input Buffer

APPLICATIONS
- Track and Hold
- Peak Measurement Systems
- Data Acquisition Systems
- Simultaneous Sample-and-Hold



GENERAL DESCRIPTION

The SHA1144 is a fast sample-hold amplifier module with accuracy and dynamic performance appropriate for applications with fast 14-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" is appropriate to allow accurate conversion by 14-bit A/D converters having conversion times of up to 150μs.

DYNAMIC PERFORMANCE

The SHA1144 was designed to be compatible with fast 14-bit A/D converters such as the Analog Devices' ADC1130 and ADC1131 series, which convert 14 bits in 25μs and 12μs, respectively. Maximum acquisition time of 8μs for the SHA1144 permits high sampling rates for 14-bit conversions. The SHA1144 is guaranteed to have a maximum gain nonlinearity of ±0.001% of full scale to insure 1/2LSB accuracy in 14-bit systems. When in the "hold" mode, the droop rate is 1μV/μs, so the SHA1144 will hold an input signal to ±0.003% of full scale (20V p-p) for over 600μs.

PRINCIPLE OF OPERATION

The SHA1144 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch. It differs from typical sample-and-hold modules in one important respect; application versatility. The user completes the SHA1144 feedback circuit external to the module. Therefore, the module may be used in inverting or noninverting configurations and can easily be arranged to provide circuit gain of more than unity to simplify signal conditioning in a subsystem.

FEEDBACK CONNECTIONS

A block diagram of the SHA1144 is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "hold" capacitor. The output amplifier isolates the "hold" capacitor and provides low output impedance for driving the load. Since feedback is not hardwired in the module, both inverting and noninverting input terminals are available, and the SHA1144 can be connected as a follower with unity gain or potentiometric gain, as well as inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data listed in the specification table is based on this operating mode.

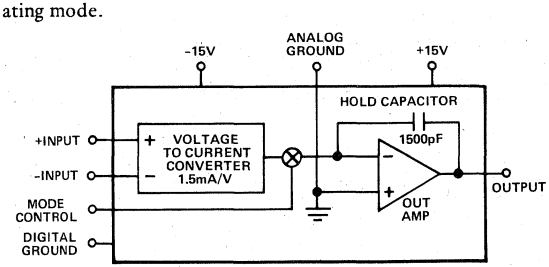


Figure 1. Block Diagram – SHA1144

SPECIFICATIONS (typical @ +25°C, gain = +1V/V and nominal supply voltages unless otherwise noted)

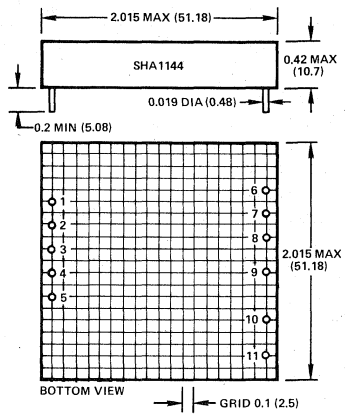
MODEL		SHA1144
ACCURACY		
Gain		+1V/V
Gain Error		±0.005%
Gain Nonlinearity		±0.0005% (±0.001% max)
Gain Temperature Coefficient (0 to +70°C)		±1ppm/°C (±2ppm/°C max)
INPUT CHARACTERISTICS		
Input Voltage Range		±10V
Impedance		$10^{11}\ \Omega \| 10pF$
Bias Current		0.5nA max
Initial Offset Voltage		Adjustable to Zero
Offset vs. Temperature (0 to +70°C)		±30μV/°C max
OUTPUT CHARACTERISTICS		
Voltage		±10V min
Current		±20mA min
Resistance		<1Ω
Capacitive load		350pF
Noise @ 100kHz Bandwidth		70μV p-p
@ 1MHz Bandwidth		175μV p-p
SAMPLE MODE DYNAMICS		
Frequency Response		
Small Signal (-3dB)		1MHz
Full Power		50kHz
Slew Rate		3V/μs
SAMPLE-TO-HOLD SWITCHING		
Aperture Delay Time		50ns
Aperture Uncertainty		0.5ns
Offset Step		1mV
Offset Nonlinearity		160μV
Switching Transient		
Amplitude		50mV
Settling Time to ±0.003%		1μs
HOLD MODE DYNAMICS		
Droop Rate		1μV/μs (2μV/μs max)
Variation with Temperature		double every +10°C
Feedthrough (for 20V p-p Input @ 1kHz)		-80dB
HOLD-TO-SAMPLE SWITCHING		
Acquisition Time to ±0.003%	(20V Step)	6μs (8μs max)
	(10V Step)	5μs
±0.01%	(20V Step)	5μs
	(10V Step)	4μs
DIGITAL INPUT		
Sample Mode (Logic "1")		+2V<Logic "1" <+5.5V @ 15nA max
Hold Mode (Logic "0")		0V<Logic "0" <+0.8V @ 5μA (20μA max)
POWER REQUIRED[1]		+15V ±3% @ 60mA -15V ±3% @ 45mA
TEMPERATURE RANGE		
Operating		0 to +70°C
Storage		-55°C to +85°C

[1] Recommended Power Supply ADI Model 902-2, ±15V @ ±100mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

1. TRIM
2. TRIM
3. +INPUT
4. -INPUT
5. TRIM
6. +15V
7. ANALOG GROUND
8. -15V
9. ANALOG OUTPUT
10. MODE CONTROL
11. DIGITAL GROUND

OFFSET ZERO ADJUST (OPTIONAL)

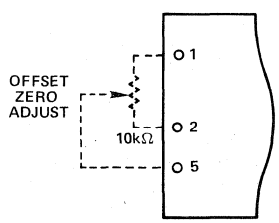


Figure 2 shows feedback connections to the SHA1144 for the unity gain follower mode. Output (pin 9) is connected to input (pin 4). Input signal is applied to pin 3.

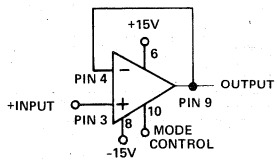


Figure 2. Unity Gain Follower

Figure 3 shows feedback connections for noninverting operation with potentiometric gain. When the indicated values are installed, gain will be +5. As in all operational amplifiers, gain-bandwidth product is a constant for a given sample-and-hold. Effective 3dB bandwidth will be inversely proportional to gain.

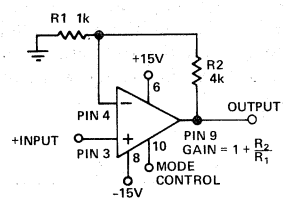


Figure 3. Noninverting Operation

By using conventional operational amplifier feedback connections, the SHA1144 can be connected for use as an inverter, with various gains (as determined by the R_F/R_1 ratio), or as a differential amplifier.

DATA ACQUISITION APPLICATION

Successive-approximation A/D converters can generate substantial linearity errors if the analog input varies during the period of conversion; even the fast 14-bit models available cannot tolerate input signal frequencies of greater than a few Hz. For this reason, sample-and-hold amplifiers like the SHA1144 are connected between the A/D and its signal source to hold the analog input constant during conversion.

When the SHA1144 is connected to an A/D, its aperture time uncertainty, rather than the A/D's conversion time, is the factor which limits the allowable input signal frequency. The SHA1144, with a typical aperture delay time of 50ns and an uncertainty of 0.5ns, will change from the sample mode to the hold mode 50 to 50.5ns after the "1" to "0" transition of the mode control input. If the system timing is so arranged as to initiate the mode control signal 50ns early, then switching will actually occur within 0.5ns of the desired time as shown below.

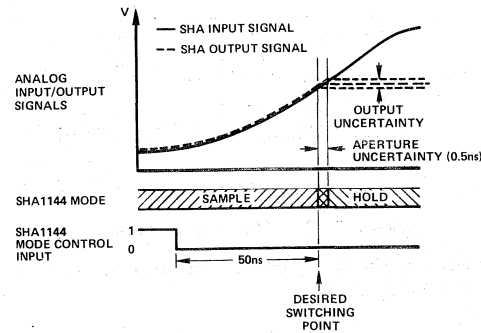


Figure 4. Aperture Uncertainty

The maximum allowable slew rate will thus equal the quotient of the maximum allowable voltage uncertainty and the 0.5ns aperture uncertainty. For sinewave inputs, the corresponding maximum frequency is expressed by:

$$f_{max} = \left(\frac{\Delta E}{E_{FS}}\right)\left(\frac{1}{2\pi\Delta t}\right) \cong 3.18 \times 10^8 \left(\frac{\Delta E}{E_{FS}}\right)$$

where: ΔE = the allowable voltage uncertainty

E_{FS} = the sinewave magnitude

For a system containing a SHA1144 and a 14-bit A/D with ±10V input signals and an allowable input uncertainty of ±1/2LSB (±620μV), the maximum allowable signal frequency will be 19.7kHz.

POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown shown below in Figure 5.

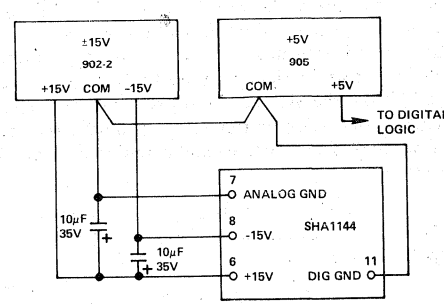


Figure 5. Power Supply and Grounding Connections

The ±15V power supplies must be externally bypassed as shown. The capacitors should be tantalum types and should be installed as close to the module pins as possible. The analog and digital ground lines should be run separately to their respective power supply commons to prevent coupling of digital switching noise to the sensitive analog circuit section.

OPERATION WITH AN A/D CONVERTER

Figure 6 below shows the appropriate connections between the SHA1144 and a successive approximation A/D converter in block diagram form.

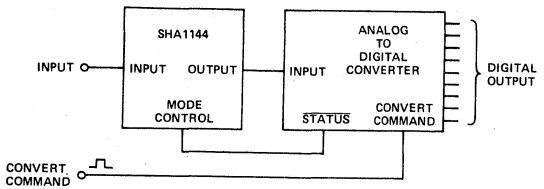


Figure 6. SHA1144 and A/D Connections

The resulting timing sequence at the start of conversion is illustrated in Figure 7.

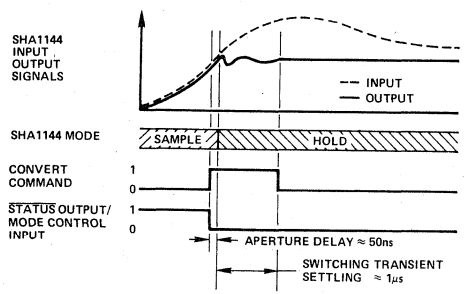


Figure 7. A/D and SHA Timing at Start of Conversion

Note that the leading edge of the convert command pulse causes the converter's STATUS output to go to Logic "0" which in turn switches the SHA1144 from sample to hold. As discussed previously, the typical SHA1144 actually changes modes 50 to 50.5ns after the "1" to "0" transition of the mode control input. This mode switching causes a transient on the output terminal which decays to within 0.003% of the final value in approximately 1μs. Once the transient has settled, the convert command input is returned to Logic "0" and the conversion proceeds. As shown in Figure 8, the STATUS signal returns to Logic "1" and the SHA1144 returns to the sample mode at the end of conversion. Within 6μs, it will have acquired the input signal to 0.003% accuracy and a new conversion cycle may be started.

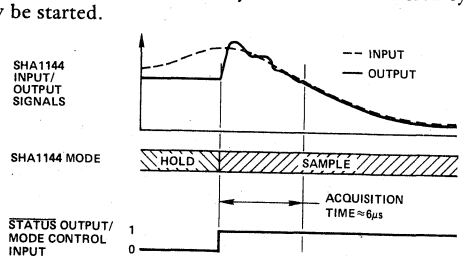


Figure 8. A/D and SHA Timing at End of Conversion

OPERATION WITH AN A/D AND MULTIPLEXER

The subsystem of Figure 9 may also be connected to a multiplexer like the Harris HI508A as shown below.

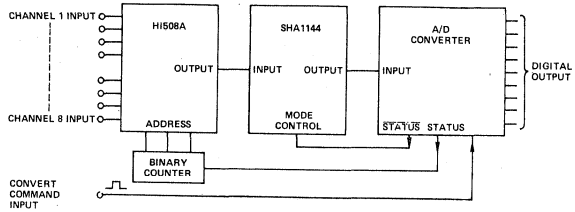


Figure 9. A/D, SHA, and MPX Connections

The leading edge of the convert command pulse sets the STATUS output to Logic "0" thereby switching the SHA1144 to "hold"; the corresponding change to Logic "1" of the STATUS output increments the binary counter and changes the multiplexer address. Since the SHA1144's aperture time is small with respect to the multiplexer switching time, it will have switched to the hold mode before the multiplexer actually changes channels. The multiplexer switching transients will settle out long before the SHA returns to "sample" at the end of conversion. The timing sequence described above is illustrated in Figure 10.

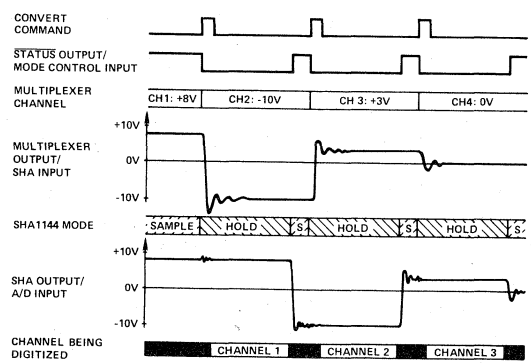


Figure 10. A/D, SHA, and MPX Timing

This method of sequencing the multiplexer may be altered to permit random addressing or addressing in a preset pattern. The timing of the multiplexer address changes may also be altered but consideration should be given to the effects of feedthrough in the SHA1144. Feedthrough is the coupling of analog input signals to the output terminal while the SHA is in "hold". Large multiplexer switching transients occuring during A/D conversion may introduce an error.

GENERAL DESCRIPTION

High resolution, high speed data acquisition demands that considerable thought be given to wiring connections, even when simply evaluating the unit in a temporary laboratory bench set-up. To assist with such evaluations, an AC1580 is available. This 4 1/2″ X 6″ printed circuit card has sockets that allow a SHA1144 and ADC1130 or ADC1131 to be plugged directly onto it. It also has provisions for two optional Harris HI508A multiplexers. This card includes gain and offset adjustment potentiometers and power supply bypass capacitors. It mates with a Cinch 251-22-30-160 (or equivalent) edge connector (P1) and Cinch 251-06-30-160 (or equivalent) edge connector (P2) which are supplied with every card.

To use the AC1580, program as shown in the wiring chart of Table 1, by installing the appropriate jumpers. An outline drawing and schematic are provided for reference.

Calibration Procedure

Set up the SHA1144 for the desired gain per the wiring chart of Table 1. Short W9 which drives the SHA MODE CONTROL with the STATUS of the ADC. Calibrate offset and gain in the manner described below. When calibration is completed W9 may be removed and the SHA MODE CONTROL may be driven in accordance with the option chart.

Offset Calibration

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00. . . . . 0 to 00. . . . . 1.

For the +5V bipolar range, set the input voltage precisely to –4.9997V; for ±10V units set it to –9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . . 0 to 00 . . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . . 0 to 100 . . . . . 1.

Gain Calibration

Set the input voltage precisely to +9.9991V for 0 to +10V units, +4.9991V for ±5V units or +9.9982V for ±10V units. Note that these values are 1 1/2LSB's less than the nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . . 0 to 11 . . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.

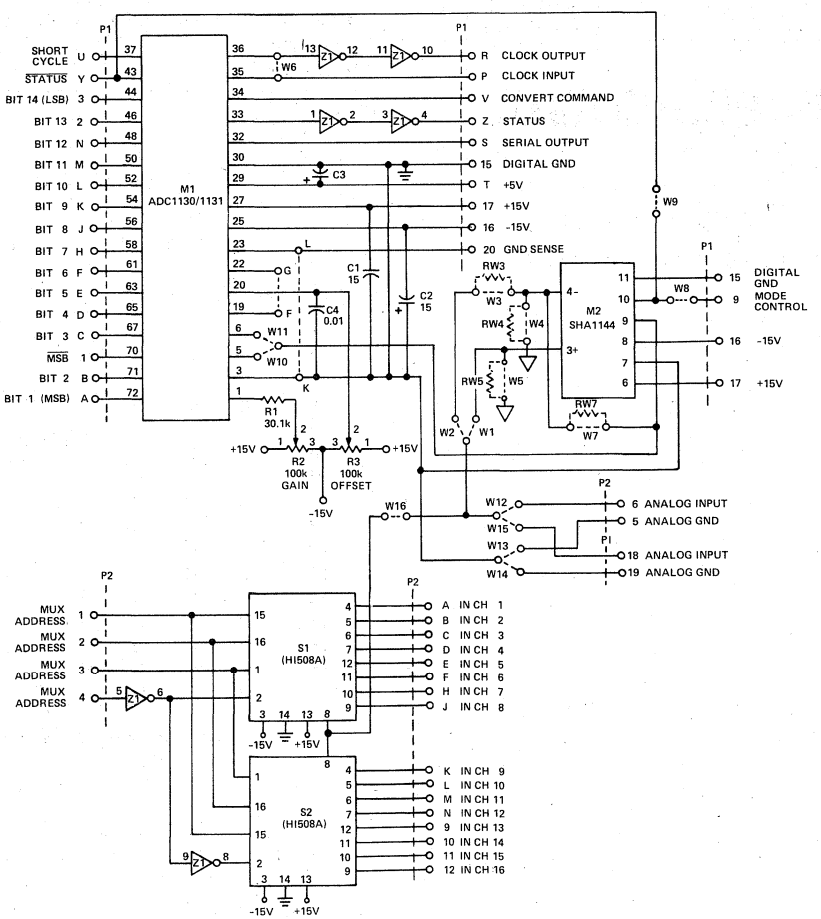


Figure 11. Schematic and Pin Designations

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

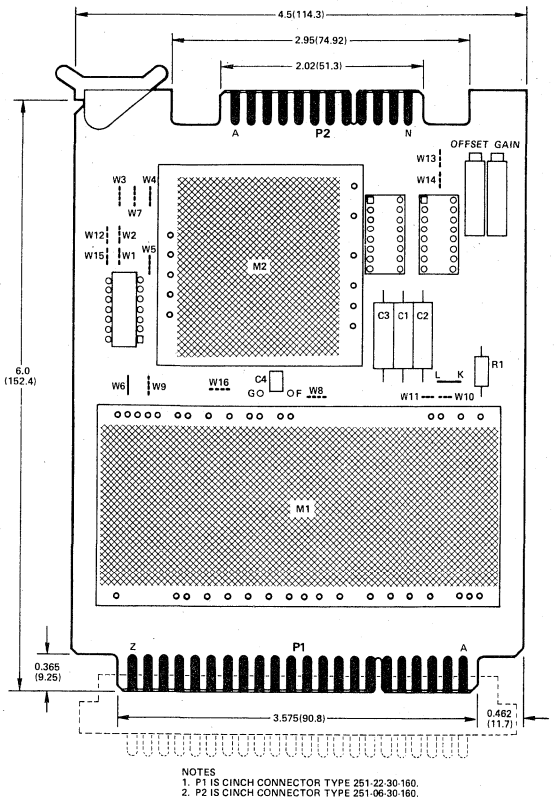


Figure 12. AC1580 Mounting Board

A to D Converter Options

Range	Jumpers
0V to 10V	Jumper W11
±5V	Jumper W11 and Jumper G to F on Board
±10V	Jumper W10 and Jumper G to F on Board

SHA Options

SHA Unity Gain (+1)	Jumper W1 and Jumper W7
SHA with Gain[1,3]	Jumper W1 and Install RW4 and RW7 in W4 and W7 Locations[3]
SHA as an Inverter[2,3]	Jumper W2 and Jumper W5 and Install RW3 and RW7 in W3 and W7 Locations[3]

SHA Mode Control

Internal (Driven from Status of the ADC)	Jumper W9
External (Apply External Signal to Pin 9 of Connector P1)	Jumper W8

Multiplexer Option

When Using Multiplexers — Jumper W16

INPUT OPTIONS

Inputs	From Connector P1	From Connector P2
Analog Input	Jumper W15	Jumper W12
Analog Ground	Jumper W14	Jumper W13

NOTES

[1] $G = 1 + \frac{RW7}{RW4}$ [2] $G = -\frac{RW7}{RW3}$

[3] See Figure 11 for appropriate gain setting resistor locations (RW3, RW4, RW7)

Table 1. Option Chart

"ON" Channel	1	2	3	4
1	L	L	L	L
2	L	L	H	L
3	L	H	L	L
4	L	H	H	L
5	H	L	L	L
6	H	L	H	L
7	H	H	L	L
8	H	H	H	L
9	L	L	L	H
10	L	L	H	H
11	L	H	L	H
12	L	H	H	H
13	H	L	L	H
14	H	L	H	H
15	H	H	L	H
16	H	H	H	H

L = TTL Logic "0" (0V ≤ "0" ≤ +0.8V)

H = TTL Logic "1" (+2V ≤ "1" ≤ +5.5V)

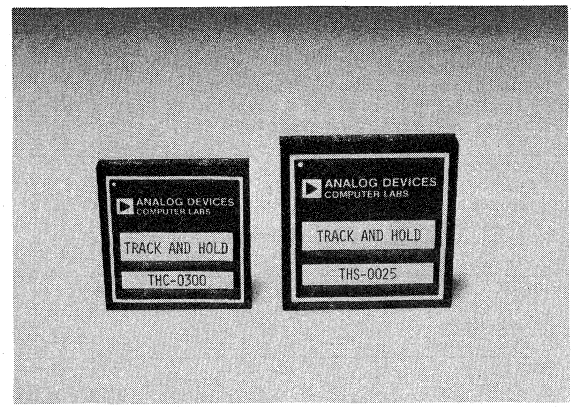
Table 2. Multiplexer Address

Ultra High Speed Sample/Track-and-Hold Amplifiers

THS, THC SERIES

FEATURES
20ps Aperture Uncertainty (THS)
15 to 1000ns Acquisition Times
0.01% Linearity
DC Coupled High Input Z Buffer

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Peak Measurement Systems
Simultaneous Sample & Hold
Analog Delay & Storage



GENERAL DESCRIPTION

The THS/THC series' modules include the fastest sample/track-and-hold amplifier (SHA) available (THS-0025), as well as general purpose high speed low droop rate, low feedthrough devices such as the THC-1500. The six devices in the series allow a wide range of trade-offs between speed, price, droop rate, output noise levels, gain precision and offset drift. All devices feature high input impedance buffer amplifiers and high output current amplifiers (50mA). The THS units achieve their speed through the use of a dc-coupled Schottky diode sampling bridge while the THC series use MOS FET switches. TTL, or ECL logic can be used on any THC device, and either is available as a no cost option on THS units.

APPLICATIONS

The most common use for a track and hold is to place it ahead of an A/D converter to allow the digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the THS series track and holds can allow a reduction of system aperture to 20ps while THC units provide 100ps. These track and holds may also be used for peak holding functions, simultaneous sampling A/D's (with appropriate analog multiplexing), and other high speed analog signal processing applications. These modules have been used to construct 13-bit A/D converters with word rates as high as 10MHz. The THS/THC series is designed to operate in either the track-and-hold or sample-and-hold modes. They perform well with the MAS series' A/D converters.

TRACK-AND-HOLD (T/H) MODE

When a THS/THC unit is operated in the T/H mode, it is allowed to "track" the input signal for a period of time prior to initiating a "hold command". During the track period, the output follows the input, and the device functions like an amplifier. In the THC units a resistor gain programmable op amp provides this function.

When a Logic "1" is input to the "hold command" input of the T/H, its output is frozen. This output level is held until the track mode is reestablished by a Logic "0" at the "hold command" input. This operation is shown graphically in Figure 1. The held output level is the voltage value at the input at the instant the hold command is applied, plus the aperture time.

Variations in the instants of sampling are called aperture uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled.

During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track and hold have high feedthrough rejection to prevent input to output leakage during the hold period. The droop rate is the amount the output changes during the hold period, as a result of loading on the internal hold capacitor.

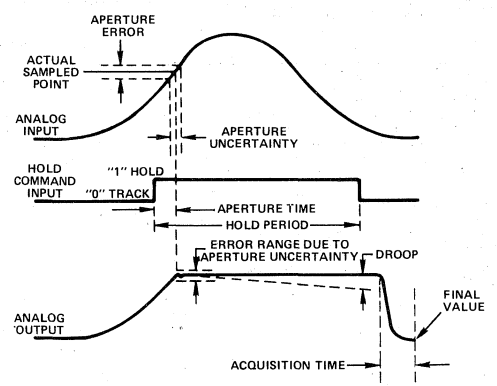


Figure 1. Track-and-Hold Operation

SPECIFICATIONS (typical at 25°C and nominal supply voltages)

MODEL	UNITS	FAST THC SERIES THC-0300	THC-0750	THC-1500	ULTRA FAST THS SERIES THS-0025	THS-0060	THS-0225
DYNAMIC CHARACTERISTICS							
Acquisition Time (to 0.1%)	ns	100	300	1000	25	75	300
Sample Rate (max)[1]	MHz	5	2.5	1	30	15	3.5
Aperture Time TTL	ns	18	*	*	10	**	**
ECL	ns	8	*	*	6	**	**
Settling Time THC to 0.1%, THS to 1% (See Figure 2)	ns	80	250	900	15	50	200
Bandwidth (Small Signal 3dB)	MHz	12	4	1.2	60	20	5
Slew Rate	V/μs	300	100	30	300	100	25
Aperture Uncertainty	ps max	100	*	*	20	**	**
Harmonic Distortion, 500kHz THC, 5MHz THS	dB	68	*	*	*	*	*
Feedthrough Rejection (dc to max Sample Rate/2) (dc to 5MHz THS)	dB	63	70	80	65	75	80
Droop Rate	μV/μs	12	5	2	5000	500	100
ACCURACY/STABILITY DC							
Gain	V/V	−1 ±2% (Pin 6 to Pin 15)			0.975	**	**
Gain vs. Temperature	ppm/°C	10	*	*	5	**	**
Zero Offset Voltage		Adjustable to Zero			Adjustable to Zero		
Offset vs. Temperature	ppm/°C	10	*	*	30	**	**
Linearity	%	±0.01	*	*	*	*	*
INPUT							
Voltage	V max	±10	*	*	±2	**	**
Impedance	Ω	1000	*	*	1M	**	**
Bias Current	nA	0.05	*	*	*	*	*
OUTPUT							
Voltage	V max	±10	*	*	±2 (No Load)	**	**
Current	mA	±50	*	*	*	*	*
Impedance		Less than 0.01Ω @ dc			5Ω (Output 1, Pin 21) 75Ω (Output 2, Pin 22)		
Noise (dc to 15MHz THS) (dc to 2.5MHz THC)	μV rms	100	50	50	200	100	50
HOLD COMMAND (DIGITAL INPUTS)					(TTL or ECL Purchased as no cost Options)		
TTL Single Line Input (2 Std. TTL Loads)							
"0" = Sample/Track		0 to +0.4V	*	*	*	*	*
"1" = Hold		+2.4 to +5V	*	*	*	*	*
ECL		Single Line Input[2]			Two Line Complementary[3]		
"0" = Sample/Track	V	−1.7	*	*	*	*	*
"1" = Hold	V	−0.8	*	*	*	*	*
POWER REQUIREMENTS							
+15V ±5% (THC) +12V to +15V (THS)	mA max	90	*	*	100	**	**
−15V ±5% (THC) −12V to −15V (THS)	mA max	80	*	*	100	**	**
+5V ±5% (THS) TTL Option	mA max	N/A	*	*	20	**	**
−5.2V ±5% (THS) TTL Option	mA max	N/A	*	*	80	**	**
−5.2V ±5% (THS) ECL Option	mA max	N/A	*	*	24	**	**
Power Supply Rejection Ratio ±15V	mV/V max	10	*	*	20	**	**
TEMPERATURE RANGE							
Operating	°C	0 to +70	*	*	*	*	*
Storage	°C	−55 to +125	*	*	*	*	*
PHYSICAL CHARACTERISTICS							
Case		diallyl phthalate per MIL-M-14 type SDG-F			diallyl phthalate per MIL-M-14 type SDG-F		

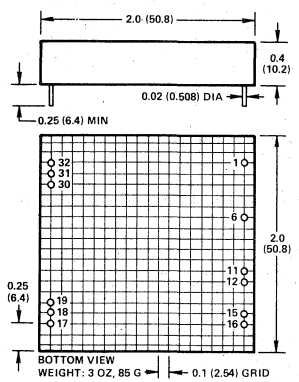
NOTES:
[1] Sample rates shown are a guide only and are based on system acquisition times—not logic speed. These rates can be exceeded with acquisition time trade-offs.
[2] These inputs are unterminated. An external pull down resistor should be used when driven by ECL 10k logic source.
[3] These inputs are each terminated with a 330Ω pull down resistor to −5.2V.

*Specifications same as THC-0300.
**Specifications same as THS-0025.

Specifications subject to change without notice.

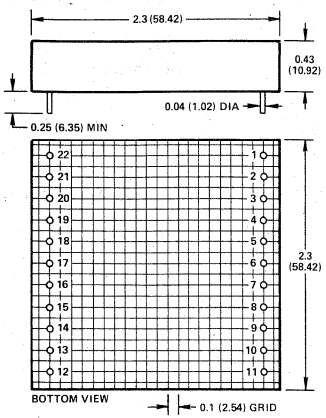
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES: SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.
PINS ARE GOLD PLATED.
DOT ON TOP INDICATES POSITION OF PIN 1.

THC Series



NOTES: SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.
PINS ARE GOLD PLATED.
DOT ON TOP INDICATES POSITION OF PIN 1.

THS Series

PIN DESIGNATIONS

PIN	THC SERIES' FUNCTION	THS SERIES' FUNCTION
1	ANALOG INPUT	GROUND
4	N/A	+15V
5	N/A	GROUND
6	FEEDBACK	-15V
7	N/A	HOLD COMMAND (ECL)
8	N/A	HOLD COMMAND (ECL)
9	N/A	HOLD COMMAND (TTL)
10	N/A	-5.2V
11	OFFSET ADJUST	+5V
12	OFFSET ADJUST	GROUND
13	N/A	OFFSET ADJUST
14	N/A	ANALOG INPUT 1
15	UNITY GAIN	N/A
16	ANALOG OUTPUT	GROUND
17	GROUND	N/A
18	-15V	N/A
19	+15V	N/A
20	N/A	GROUND
21	N/A	ANALOG OUTPUT 1
22	N/A	ANALOG OUTPUT 2
30	HOLD COMMAND (ECL)	N/A
31	HOLD COMMAND (TTL)	N/A
32	GROUND	N/A

When the hold command input returns to the track condition, the amount of time required for the T/H output to reestablish accurate tracking of the input signal is called the acquisition time. Figure 2 shows settling accuracy versus acquisition time for the THS/THC series. Figure 3 shows superimposed photographs of the input and output waveforms of a THS-0025 operated as a track-and-hold amplifier. Note that the output reacquires the input just 12ns after the end of the hold time.

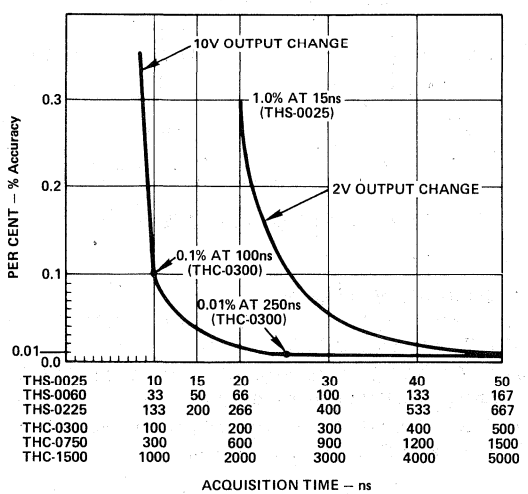


Figure 2. Acquisition Time vs. Settling Accuracy

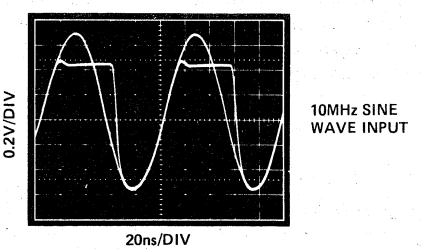


Figure 3. Track-and-Hold Operation (THS-0025)

SAMPLE AND HOLD (S/H) MODE

In the S/H mode of operation, devices are normally left in the hold condition. A very short sample pulse is applied to the hold command input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time. For small sample-to-sample variations, a pulse width as narrow as 12ns may be used for THS units and 80ns for THC units. If possible for greater accuracy, sample pulses should be wider (see Figure 2).

In general, however, the pulse width to the THS-0025 should be 15ns to 50ns, depending on required accuracy. Figure 4 shows the input and output waveforms of a THS-0025 used in the S/H mode.

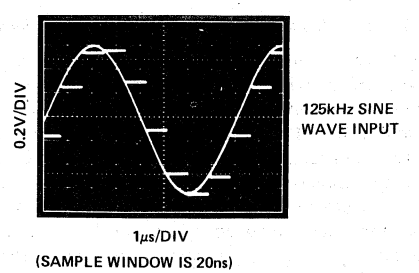


Figure 4. Sample-and-Hold Operation (THS-0025)

APPLICATION NOTES

Figure 5 shows a slope sensitive circuit which is capable of finding the peaks of positive excursions of an input waveform and digitizing the result. The circuit may be implemented without the A/D converter, in which case the output is an analog level held by the T/H module that may be observed or measured in some other manner.

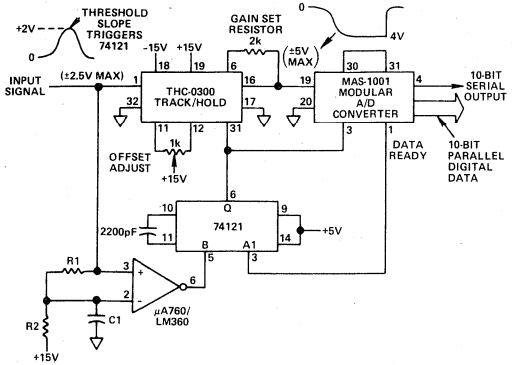


Figure 5. Peak Detector (THC-0300)

The comparator triggers the T/H module when the positive slope of the input signal drops below a threshold slope equal to 15V/R2C1. A minimum positive slope of 15V/R1C1 is required to arm the detector. Resistors R1 and R2 are used to provide a guard band to prevent noise from triggering the circuit. The guardband voltage is equal to 15V X R1/R2 and is generally set to approximately 5 to 20mV.

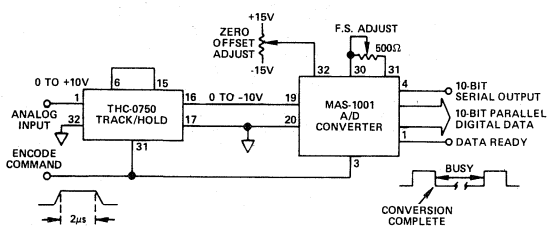


Figure 6. A/D Conversion System (THC)

Throughput Rate	Greater than 400kHz
Overall Accuracy	0.05%
Resolution	One Part in 1024 (10 Bit)
Aperture Uncertainty	100ps

Analog Input	Digital Output
0V	0000000000
+5.000V	1000000000
+9.990V	1111111111

Table 1. Capsule Performance for the A/D System

Analog Devices' THC series track-and-holds are designed to interface directly with the MAS series A/D converters as well as other commercially available modular A/D's. In the above application, the THC module is used to acquire the analog signal to be converted and hold the sampled output over a much longer time period to permit the A/D module to accurately encode the analog data sample. In this way, the system aperture time is reduced to less than 100ps, and analog bandwidths up to the Nyquist limit may be accurately digitized.

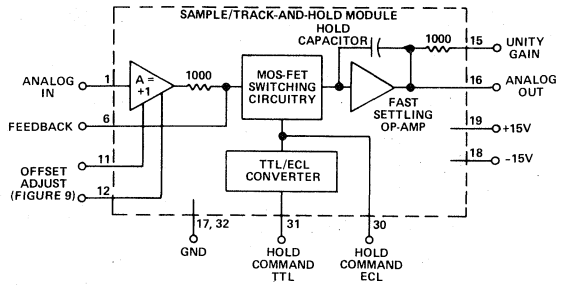


Figure 7. Sample/Track-and-Hold THC Series Block Diagram

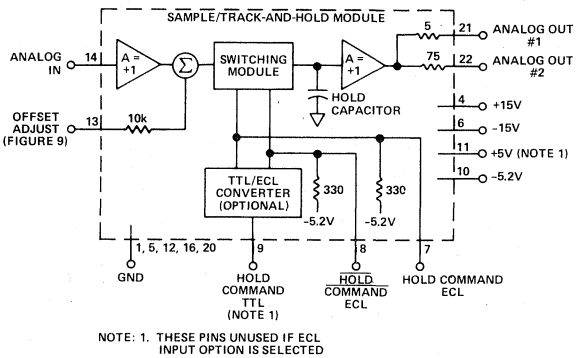


Figure 8. Sample/Track-and-Hold THS Series Block Diagram

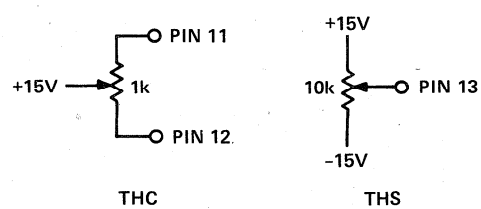


Figure 9. Optional Offset Adjustments

ORDERING INFORMATION

Order THS-0025 TTL, THS-0060 TTL, or THS-0225 TTL for TTL Hold Command Option.

Order THS-0025 ECL, THS-0060 ECL, or THS-0225 ECL for Balanced ECL Hold Command Input.

Order THC-0300, THC-0750, THC-1500 as required. All have available TTL and ECL Logic Inputs.

CMOS Switches & Multiplexers

Contents

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AD7510DI	Dielectrically Isolated Quad SPST; Address High Closes Switch	14–13
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AD7512DI	Dielectrically Isolated Quad SPDT	14–13
ADG200	Dielectrically Isolated Dual SPST, Replaces DG200	14–21
ADG201	Dielectrically Isolated Quad SPST, Replaces DG201	14–25

Selection Guide
CMOS Switches & Multiplexers

The devices catalogued in this section are grouped into two classes: Switches and Multiplexers. Descriptions, specifications, and application information can be found in the data sheets; definitions of the terminology can be found in the following pages.

Devices and subsystems with multiplexing functions can also be found in Sections 8 (Transducers, Signal Conditioners, and Instrumentation), 10 (Analog-to-Digital Converters—AD7583 9-channel CMOS 8-bit ADC), 15 (Data-Acquisition Subsystems), and 16 (Microcomputer Interfaces).

CMOS IC SWITCHES

Type	Characteristics	Page
AD7510DI#	Dielectrically isolated Quad SPST; Address High closes switch	14-13
AD7511DI#	Dielectrically isolated Quad SPST; Address Low closes switch	14-13
ADG201#	Dielectrically isolated Quad SPST, replace DG201	14-25
ADG200#	Dielectrically isolated Dual SPST, replace DG200	14-21
AD7512DI#	Dielectrically isolated Quad SPDT	14-13

CMOS IC MULTIPLEXERS

Type	Characteristics	Page
AD7501	8-channel multiplexer, High enables	14-5
AD7503	8-channel multiplexer, Low enables	14-5
AD7502	4-channel differential multiplexer	14-5
AD7506	16-channel multiplexer	14-9
AD7507	8-channel differential multiplexer	14-9

#Monolithic chips available with guaranteed performance for precision hybrids; information available upon request. All can be found in the 1979 Chip Catalog, available upon request.

Orientation
CMOS Switches & Multiplexers

Analog Devices offers a complete line of monolithic CMOS analog multiplexers and switches, which utilize a high-breakdown CMOS process, in conjunction with a double-layer interconnect for high density. Both 8- and 16-channel multiplexers are available, in one-line and two-line (4- and 8-channel differential) versions. The switches are dielectrically isolated duals and quads, available in a variety of contact forms. Both direct and inverted logic options are available for the most-popular types. The popular AD7510/11/12DI (quad SPST/dual SPDT), which utilize dielectric isolation, are latchup-proof and can withstand overrange to ±25V beyond the supplies.

CMOS switches have extremely low quiescent power dissipation, require little drive or supply current while switching, and are low in cost. Their R_{ON} is low and is, to a first-order, independent of applied voltage; in the off condition, leakage is quite small, both across the gate and to the drive and supply circuits. Most types respond to TTL/DTL, as well as CMOS, logic.

Definitions for terminal nomenclature used in the data sheets are given below, and a summary of device functions appears on the preceding page. General information on the nature of CMOS, its advantages, its applications, and its protection, is to be found in the *Guide to CMOS Switches and Multiplexers*, available from Analog Devices upon request.

MULTIPLEXER TERMINOLOGY

R_{ON}:	Ohmic resistance between the output and an addressed input.
R_{ON} vs. Temperature:	R_{ON} drift over the temperature range.
ΔR_{ON} between Switches:	Difference between the R_{ON}'s of any two switches.
R_{ON} vs. Temperature between Switches:	Difference between the R_{ON} drifts of any two switches.
I_S:	Current at any switch input, S1 through S_N. This is a leakage current when the switch is open.
I_{OUT}:	Current at the output. This is a leakage current when all switches are open.
$I_{OUT} - I_S$:	Difference between the current going into terminal "S" and the current going out of terminal "out" when terminal "S" is addressed.
V_{INL}:	Digital threshold voltage for the low state.
V_{INH}:	Digital threshold voltage for the high state.
C_S:	Capacitance between any open terminal "S" and ground.
C_{OUT}:	Capacitance between the output terminal and ground with all switches open.
C_{S-OUT}:	Capacitance between any open terminal "S" and the output terminal.
C_{SS}:	Capacitance between any two "S" terminals.
$t_{transition}$:	Delay time when switching from one address state to another.
t_{open}:	"OFF" time of both switches when switching from one address state to another.
t_{on} (En):	Delay time between the 50% points of the enable input and the switch "ON" condition.
t_{off} (En):	Delay time between the 50% points of the enable input and the switch "OFF" condition.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

SWITCH TERMINOLOGY

R_{DS}:	Ohmic resistance between terminals D and S.
I_D (I_S):	Current at terminals D or S. This is a leakage current when the switch is OFF.
I_{DS}:	Current flowing through the closed switch.
$I_D - I_S$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (C_D):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any 2 switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

ANALOG DEVICES

CMOS 4/8 Channel Analog Multiplexers

AD7501, AD7502, AD7503

FEATURES
DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Output "Enable" Control
AD7503 Replaces HI-1818

GENERAL DESCRIPTION

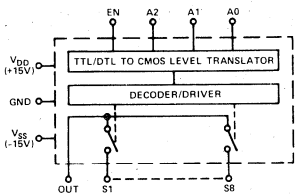
The AD7501 and AD7503 are monolithic CMOS, 8-channel analog multiplexers which switches one of 8 inputs to a common output depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output buses to two of 8 inputs.

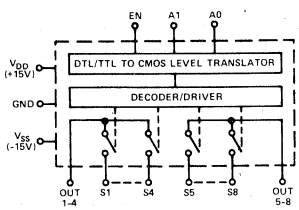
All 3 devices are excellent examples of a high breakdown CMOS process combined with a double layer interconnect for high density. Silicon nitride passivation ensures long term stability and reliability.

FUNCTIONAL DIAGRAMS

AD7501, AD7503

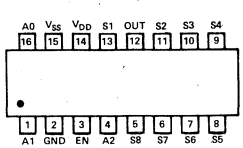


AD7502

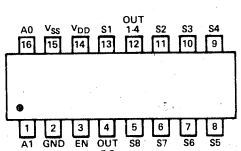


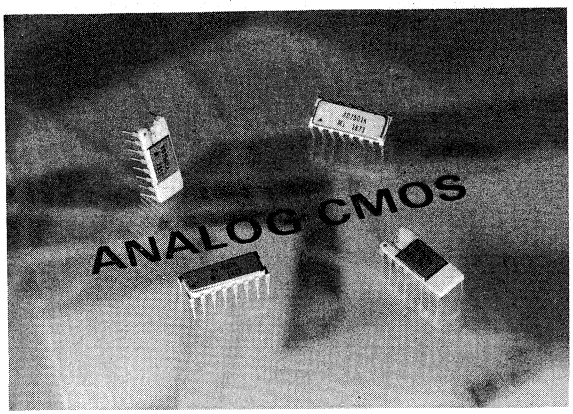
PIN CONFIGURATIONS (Top View)

AD7501, AD7503



AD7502





ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} – GND	+17V
V_{SS} – GND	-17V
V Between Any Switch Terminals	25V
Switch Current (I_S, Continuous)	35mA
Switch Current (I_S, Surge)	
1ms duration, 10% duty cycle	50mA
Digital Input Voltage Range	V_{DD} to GND
Power Dissipation (package)	
16 pin Ceramic DIP	
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
16 pin Plastic DIP	
Up to +70°C	670mW
Derates above +70°C by	8.3mW/°C
Operating Temperature	
Plastic (JN, KN versions)	0 to +70°C
Ceramic (JD, KD versions)	-25°C to +85°C
Ceramic (SD versions)	-55°C to +125°C
Storage Temperature	-65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER	VERSION[1]	SWITCH CONDITION	@25°C AD7501, AD7503	@25°C AD7502	OVER SPECIFIED TEMP. RANGE AD7501, AD7503	OVER SPECIFIED TEMP. RANGE AD7502	TEST CONDITIONS
ANALOG SWITCH							
R_{ON}	All	ON	170Ω typ, 300Ω max	*			-10V ≤ V_S ≤ +10V
R_{ON} vs. V_S	All	ON	20% typ	*			I_S = 1.0mA
R_{ON} vs. Temperature	All	ON	0.5%/°C typ	*			V_S = 0V, I_S = 1.0mA
ΔR_{ON} Between Switches	All	ON	4% typ	*			
R_{ON} vs. Temperature Between Switches	All	ON	±0.01%/°C	*			
I_S	J, K	OFF	0.2nA typ, 2nA max	*	50nA max	*	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V
	S	OFF	0.5nA max	*	50nA max	*	
I_{OUT}	J, K	OFF	1nA typ, 10nA max	0.6nA typ, 5nA max	250nA max	125nA max	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V
	S	OFF	5nA max	3nA max	250nA max	125nA max	AD7501/02: Enable LOW AD7503: Enable HIGH
$\lvert I_{OUT} - I_S \rvert$	J, K	ON	12nA max	7nA max	300nA max	175nA max	V_S = 0
	S	ON	5.5nA max	3.5nA max	300nA max	175nA max	
DIGITAL CONTROL							
V_{INL}	All				0.8V max	*	
V_{INH}	J				3.0V min	*	Note 2
	K, S				2.4V min	*	
I_{INL} or I_{INH}	All		10nA typ	*			
C_{IN}	All		3pF typ	*			
DYNAMIC CHARACTERISTICS							
t_{ON}	All		0.8μs typ	*			V_{IN} = 0 to +5.0V (See Test Circuit 2)
t_{OFF}	All		0.8μs typ	*			
C_S	All	OFF	5pF typ	*			
C_{OUT}	All	OFF	30pF typ	15pF typ			
C_{S-OUT}	All	OFF	0.5pF typ	*			
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ	*			
POWER SUPPLY							
I_{DD}	All		500μA max	*	500μA max	*	All Digital Inputs Low
I_{SS}	All		500μA max	*	500μA max	*	
I_{DD}	All		800μA max	*	800μA max	*	All Digital Inputs High
I_{SS}	All		800μA max	*	800μA max	*	

NOTES
*Same specifications as AD7501 and AD7503.
[1] JN, KN versions specified for 0 to +70°C; JD, KD versions for -25°C to +85°C; and SD versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ is required to make the AD7501J, AD7502J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.

Specifications subject to change without notice.

TRUTH TABLES

AD7501

A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7502

A_1	A_0	E_N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

AD7503

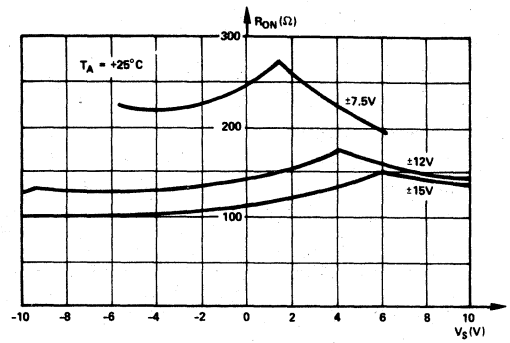
A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

ORDERING INFORMATION

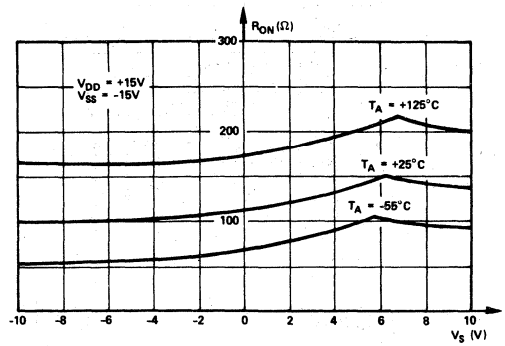
Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7501JN AD7501KN AD7503JN AD7503KN		0 to +70°C
	AD7501JD AD7501KD AD7503JD AD7503KD	-25°C to +85°C
	AD7501SD AD7503SD	-55°C to +125°C
AD7502JN AD7502KN		0 to +70°C
	AD7502JD AD7502KD	-25°C to +85°C
	AD7502SD	-55°C to +125°C

Note: Ceramic versions are available 100% screened to MIL-STD-883, method 5004 for a class B device. To order, add "/883B" to model number.

1. R_{ON} As A Function Of Switch Voltage (V_S)

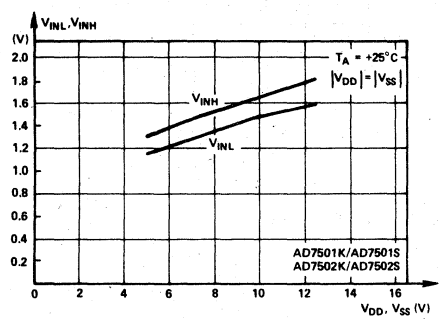


At Different Power Supplies

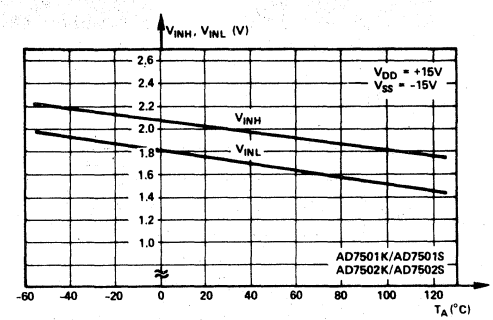


At Different Temperatures

2. Digital Threshold Voltage (V_{INH}, V_{INL})

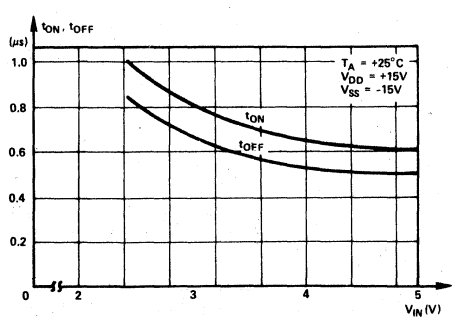


vs. Power Supply



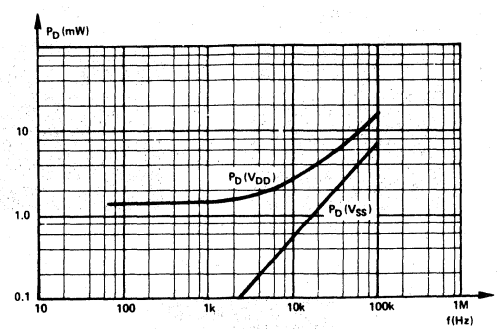
vs. Temperature

3. T_{ON}, T_{OFF}



vs. Digital Input Voltage

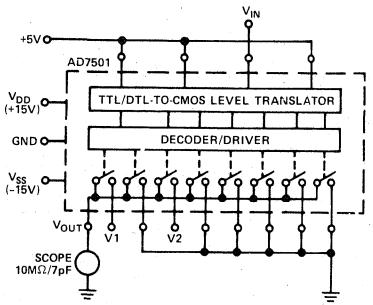
4. Power Dissipation



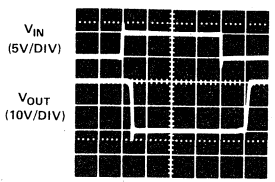
vs. Logic Frequency (50% Duty Cycle)

TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

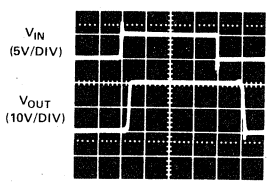


1μs/DIV



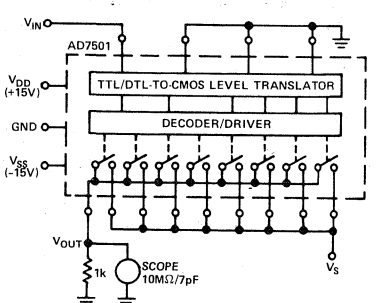
V_1 = -10V, V_2 = +10V

1μs/DIV

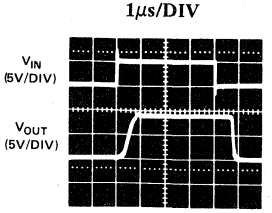


V_1 = +10V, V_2 = -10V

TEST CIRCUIT 2

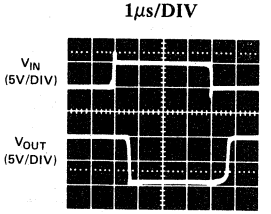


1μs/DIV



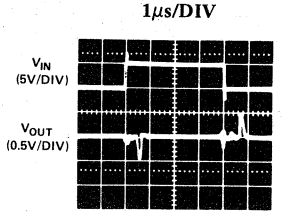
V_S = +10V

1μs/DIV



V_S = -10V

1μs/DIV

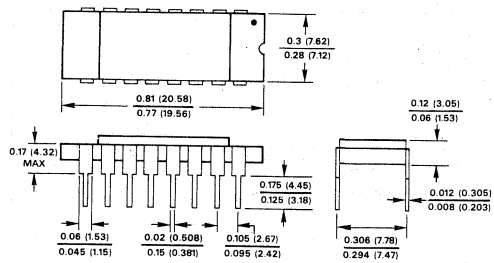


V_S = OPEN

OUTLINE DIMENSIONS

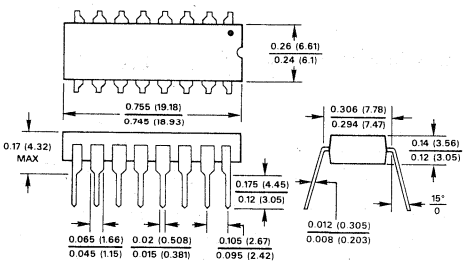
Dimensions shown in inches and (mm).

16-PIN CERAMIC DIP (SUFFIX D)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

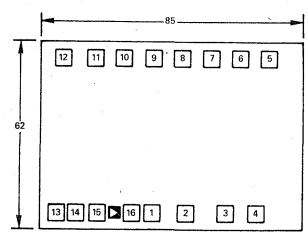
16-PIN PLASTIC DIP (SUFFIX N)



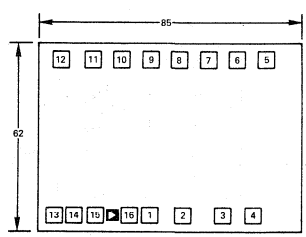
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

BONDING DIAGRAMS

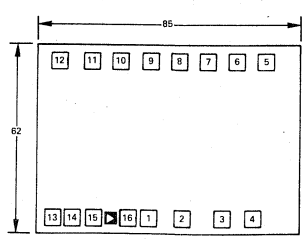
AD7501



AD7502



AD7503



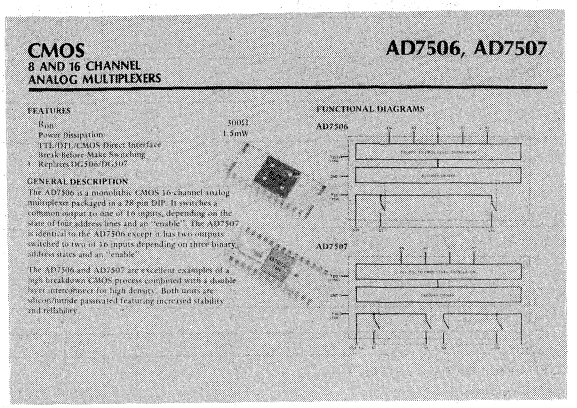
All bonding pads are 4 x 4 MIL.
All pad numbers correspond with DIP package pin configuration.

ANALOG DEVICES

CMOS 8- and 16-Channel Analog Multiplexers

AD7506, AD7507

FEATURES
R_{ON}: 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG506/DG507


CMOS
8 AND 16 CHANNEL
ANALOG MULTIPLEXERS
AD7506, AD7507
FEATURES
R_{ON} 300Ω
Power Dissipation 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG506/DG507
GENERAL DESCRIPTION
FUNCTIONAL DIAGRAMS
AD7506
AD7507

GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

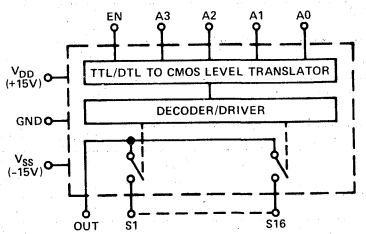
V_{DD} – GND . . . . . +17V
V_{SS} – GND . . . . . -17V
V Between Any Switch Terminals. 25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Switch Current (I_S, Continuous). 20mA
Switch Current (I_S, Surge)
  1ms duration, 10% duty cycle 35mA
Power Dissipation (Package)
28 pin Ceramic DIP
  Up to +50°C. 1000mW
  Derates above +50°C by . . . . . 10mW/°C
28 pin Plastic DIP
  Up to +50°C. 1200mW
  Derates above +50°C by . . . . . 12mW/°C
Operating Temperature
  Plastic (J, K versions). . . . . 0 to +70°C
  Ceramic (J, K versions). . . . . -25°C to +85°C
  Ceramic (S, T versions). . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

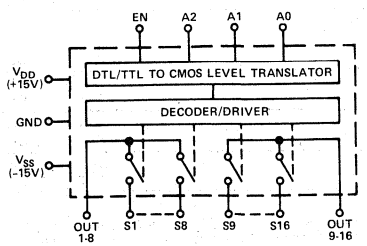
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

FUNCTIONAL DIAGRAMS

AD7506

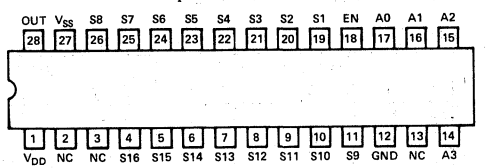


AD7507

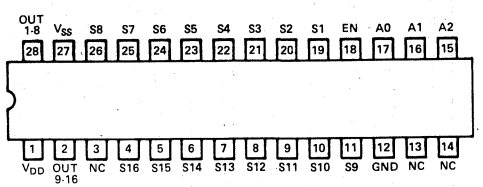


PIN CONFIGURATIONS (Top View)

AD7506



AD7507



SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER		VERSION[1]	SWITCH CONDITION	@ +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ANALOG SWITCH						
R_{ON}		J, K	ON	300Ω typ, 450Ω max	550Ω max	V_S = -10V to +10V, I_S = 1mA
		S, T	ON	400Ω max	500Ω max	
R_{ON} vs. V_S		All	ON	15% typ		
R_{ON} vs. Temperature		All	ON	0.5%/°C typ		V_S = 0V, I_S = 1mA
ΔR_{ON} Between Switches		All	ON	4% typ		
R_{ON} vs. Temperature Between Switches		All	ON	0.05%/°C typ		
I_S		J, K	OFF	0.05nA typ, 5nA max	50nA max	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V "Enable" Low
		S, T	OFF	0.05nA typ, 1nA max	50nA max	
I_{OUT}	AD7506	J, K	OFF	0.3nA typ, 20nA max	500nA max	
		S, T	OFF	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	OFF	0.3nA typ, 10nA max	250nA max	
		S, T	OFF	0.3nA typ, 5nA max	250nA max	
$I_{OUT} - I_S$	AD7506	J, K	ON	0.3nA typ, 20nA max	500nA max	V_S = 0
		S, T	ON	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	ON	0.3nA typ, 10nA max	250nA max	
		S, T	ON	0.3nA typ, 5nA max	250nA max	
DIGITAL CONTROL						
V_{INL}					0.8V max	
		J, S			3.0V min	Note 2
V_{INH}		K, T			2.4V min	
I_{INL} or I_{INH}		All		10μA max	30μA max	
C_{IN}		All		3pF typ		
DYNAMIC CHARACTERISTICS[3]						
$t_{TRANSITION}$		J, S		700ns typ		V_{IN}: 0 to 3.0V
		K, T		700ns typ, 1000ns max		
t_{OPEN}		All		100ns typ		
t_{ON} (En)		J, S		0.8μs typ		V_{EN}: 0 to 3.0V
		K, T		1.5μs max		
t_{OFF} (En)		J, S		0.8μs typ		
		K, T		1μs max		
"OFF" Isolation		All		70dB typ		V_{EN} = 0, R_L = 200Ω, C_L = 3.0pF, V_S = 3.0V rms, f = 50kHz
C_S		All	OFF	5pF typ		
C_{OUT}	AD7506	All	OFF	40pF typ		
	AD7507	All	OFF	20pF typ		
C_{S-OUT}		All	OFF	0.5pF typ		
C_{SS} Between Any Two Switches		All	OFF	0.5pF typ		
POWER SUPPLY						
I_{DD}		J, K	OFF	0.05mA typ, 1mA max		
		S, T	OFF	0.05mA typ, 1mA max	2mA max	All Digital Inputs Low
I_{SS}		J, K	OFF	0.05mA typ, 1mA max		
		S, T	OFF	0.05mA typ, 1mA max	2mA max	
I_{DD}		J, K	ON	0.3mA typ, 1mA max		
		S, T	ON	0.3mA typ, 1mA max	2mA max	All Digital Inputs High
I_{SS}		J, K	ON	0.05mA typ, 1mA max		
		S, T	ON	0.05mA typ, 1mA max	2mA max	

NOTES:
[1] JN, KN versions specified for 0 to +70°C; JD, KD versions for -25°C to +85°C; and SD, TD versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.
[3] AC parameters are sample tested to ensure conformance to specifications.
Specifications subject to change without notice.

TRUTH TABLES

AD7506

A_3	A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

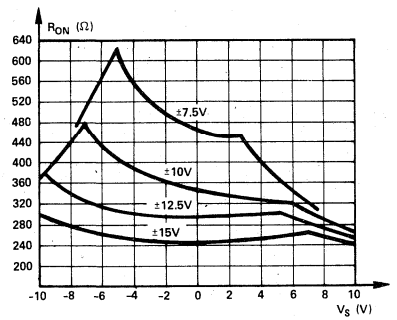
AD7507

A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

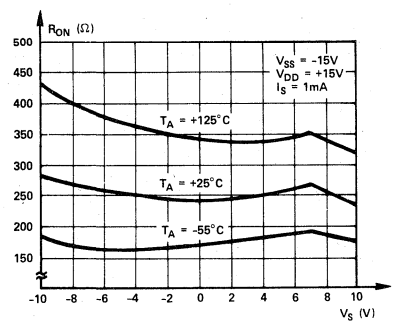
ORDERING INFORMATION

Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7506JN AD7506KN AD7507JN AD7507KN		0 to +70°C
	AD7506JD AD7506KD AD7507JD AD7507KD	-25°C to +85°C
	AD7506SD AD7506TD AD7507SD AD7507TD	-55°C to +125°C

1. R_{ON} vs. V_S

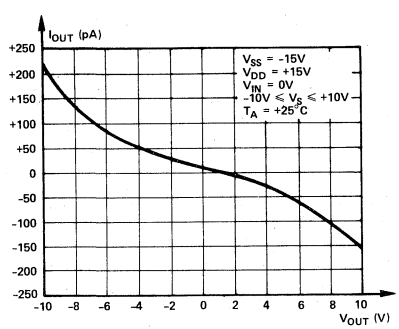


At Different Power Supplies

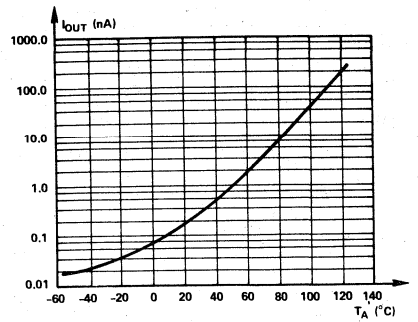


At Different Temperatures

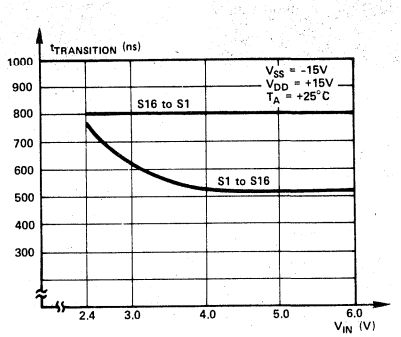
2. I_{OUT} vs. V_{OUT}



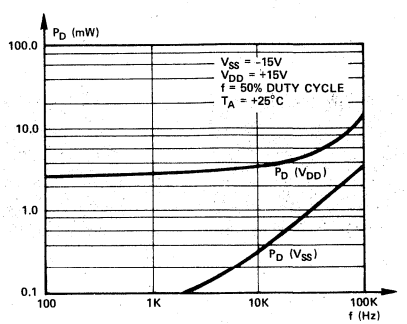
3. I_{OUT} vs. T_A



4. $t_{TRANSITION}$ vs. V_{IN}

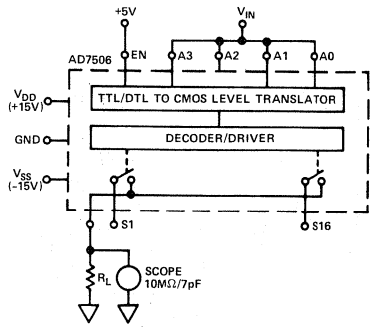


5. P_D vs. Logic Frequency

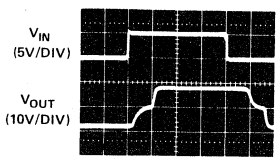


TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

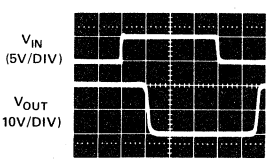


0.5μs/DIV



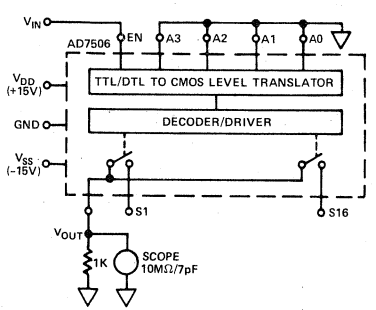
S_1 = -10V, S_{16} = +10V,
S_2 – S_{15} = 0V, R_L = 1K

0.5μs/DIV

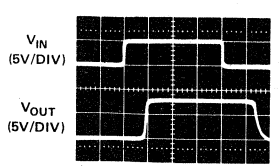


S_1 = +10V, S_2 = -10V,
S_2 – S_{15} = 0V, R_L = ∞

TEST CIRCUIT 2

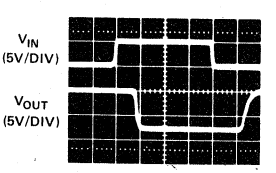


0.5μs/DIV



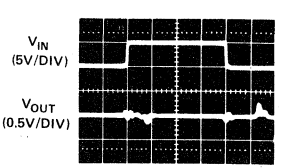
S_1 through S_{16} = +10V

0.5μs/DIV



S_1 through S_{16} = -10V

0.5μs/DIV

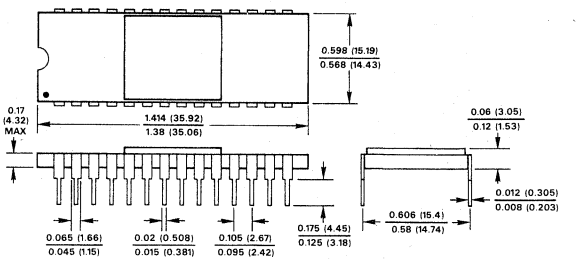


S_1 through S_{16} = 0V

OUTLINE DIMENSIONS

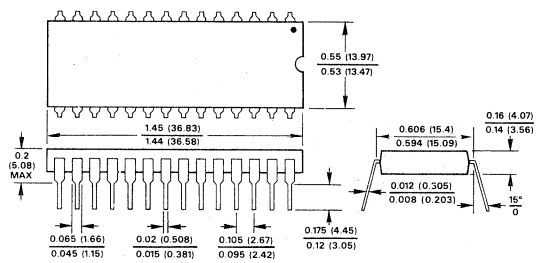
Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (SUFFIX D)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES) KOVAR OR ALLOY 42

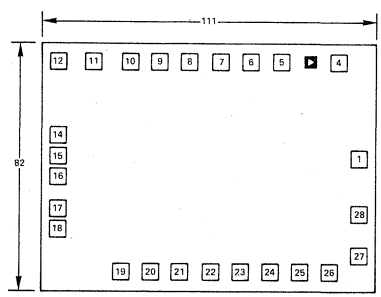
28-PIN PLASTIC DIP (SUFFIX N)



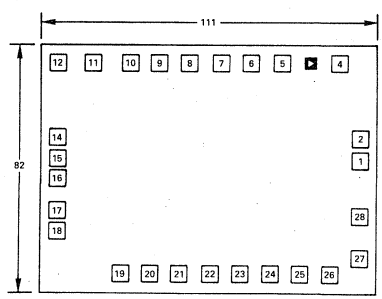
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

BONDING DIAGRAMS

AD7506



AD7507



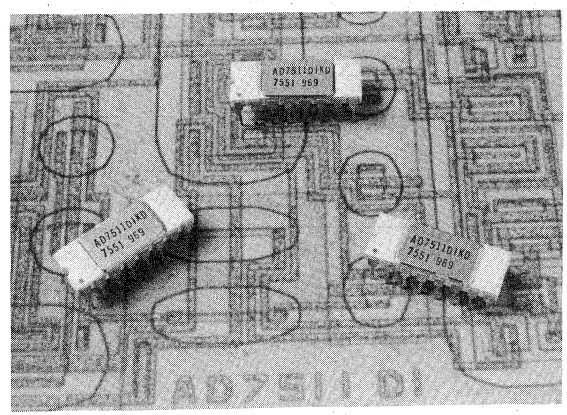
All bonding pads are 4 x 4 MIL.
All pad numbers correspond with DIP package pin configuration.

ANALOG DEVICES

DI CMOS Protected Analog Switches

AD7510DI, AD7511DI, AD7512DI

FEATURES
Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Monolithic Dielectrically-Isolated CMOS



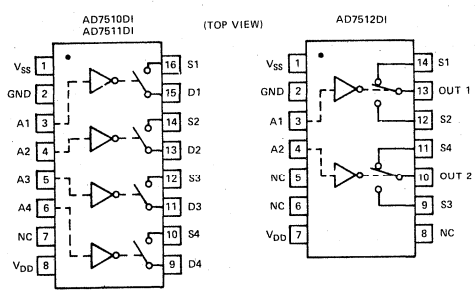
GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (400pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged in a 14-pin DIP.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

PIN CONFIGURATIONS



ORDERING INFORMATION

Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7510DIJN AD7510DIKN AD7511DIJN AD7511DIKN AD7512DIJN AD7512DIKN		0 to +70°C
	AD7510DIJD AD7510DIKD AD7511DIJD AD7511DIKD AD7512DIJD AD7512DIKD	−25°C to +85°C
	AD7510DISD AD7511DISD AD7511DITD AD7512DISD AD7512DITD	−55°C to +125°C

All ceramic versions are available screened to MIL-STD-883, method 5004 for a class B device. To order, add "/883B" to model number.

CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

COMMERCIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C	0 to +70°C (N) −25°C to +85°C (D)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	J, K	75Ω typ, 100Ω max	175Ω max	$-10V \leq V_D \leq +10V$
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		
R_{ON} Match	All	J, K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S) OFF[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = −10V, V_S = +10V and V_D = +10V, V_S = −10V
I_D $(I_S)_{ON}$[2]	All	J, K	10nA max		$V_S = V_D$ = +10V $V_S = V_D$ = −10V
I_{OUT}[1]	AD7512DI	J, K	15nA max	1500nA max	$V_{S1} = V_{OUT} = \pm 10V$, $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$, $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}[1]	All	J, K		0.8V max	
V_{INH}[1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	3pF typ		
I_{INH}[1]	All	J, K	10nA max		$V_{IN} = V_{DD}$
I_{INL}[1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		
	AD7511DI	J, K	350ns typ		V_{IN} = 0 to +3.0V
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)OFF	All	J, K	8pF typ		
C_S (C_D)ON	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to −10V
POWER SUPPLY					
I_{DD}[1]	All	J, K	800μA max	800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	J, K	800μA max	800μA max	
I_{DD}[1]	All	J, K	500μA max	500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	J, K	500μA max	500μA max	

NOTES:
[1] 100% tested.
[2] Guaranteed, not production tested.
[3] A pullup resistor, typically 1-2kΩ is required to make "J" versions TTL compatible.

Specifications subject to change without notice.

MILITARY VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	S, T	100Ω max	175Ω max	$-10V \leqslant V_D \leqslant +10V$ I_{DS} = 1mA
I_D $(I_S)_{OFF}$ [1]	All	S, T	3nA max	200nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D $(I_S)_{ON}$ [2]	All	S, T	10		$V_S = V_D$ = +10V and $V_S = V_D$ = -10V
I_{OUT} [1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL} [1]	All	S, T		0.8V max	
V_{INH} [1,3]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH} [1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL} [1]	All	S, T	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON} [2]	AD7510DI	S, T	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF} [2]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$ [2]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD} [1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS}	All	S, T		800μA max	
I_{DD} [1]	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS}	All	S, T		500μA max	

NOTES:
[1] 100% tested.
[2] Guaranteed, not production tested.
[3] A pullup resistor, typically 1-2kΩ is required to make AD7511DISD and AD7512DISD TTL compatible.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . -17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . . V_{DD} +25V
or V_{SS} -25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} -20V
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . 0V to V_{DD}
Power Dissipation (Package)
14 & 16 pin Ceramic Dip
Up to +75°C. 450mW
Derates above +75°C by . . . . . 6mW/°C
14 & 16 pin Plastic Dip
Up to +70°C. 670mW
Derates above +75°C by . . . . . 8.3mW/°C
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature
Plastic (J, K Versions) . . . . . 0 to +70°C
Ceramic (J, K Versions) . . . . . -25°C to +85°C
Ceramic (S, T Versions) . . . . . -55°C to +125°C

CAUTION: The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.

CIRCUIT DESCRIPTION

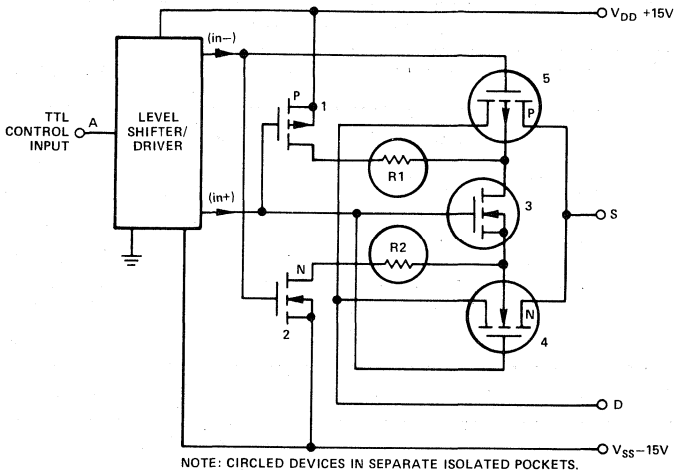


Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenum necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in−) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON." Hence, the back-gates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. (The circled devices are located in separate dielectrically isolated pockets.) Floating the output switch back-gates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the back-gates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-back-gate diode is forward biased; however, R1 and R2 provide current limiting action.

Consequently, without external current limiting resistance (or increased R_{ON}), the AD7510DI series switches provide:

1. Latch-proof operation
2. Overvoltage protection 25V beyond the V_{SS} and V_{DD} supply voltage

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices—*not* in series with the signal path between the S and D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor, causing device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or current limiting devices (output of op amps) will prevent damage to the device.

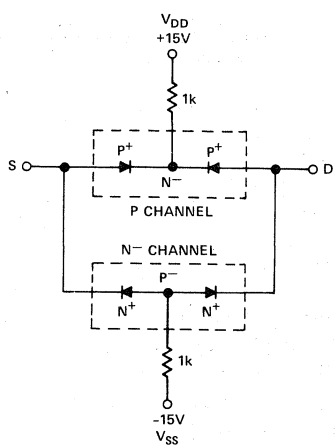
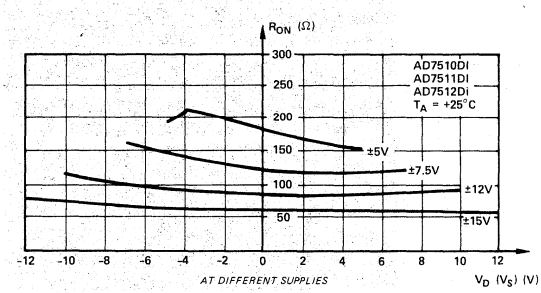
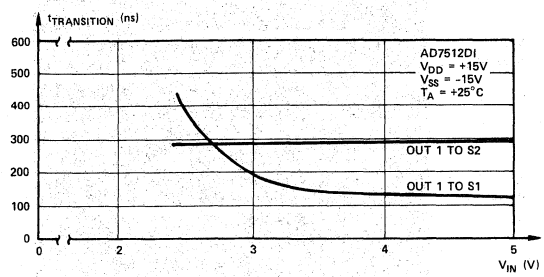


Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit

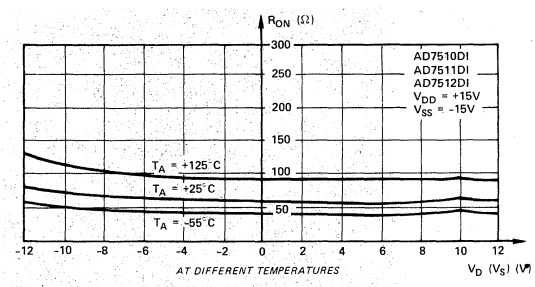
TYPICAL PERFORMANCE CHARACTERISTICS



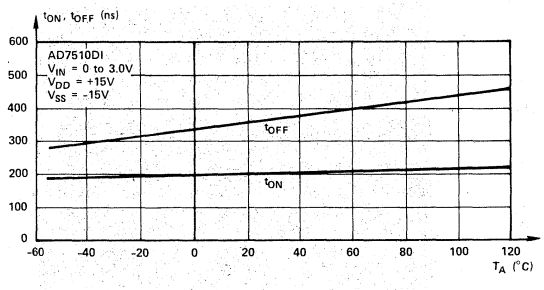
R_{ON} as a Function of V_D (V_S)



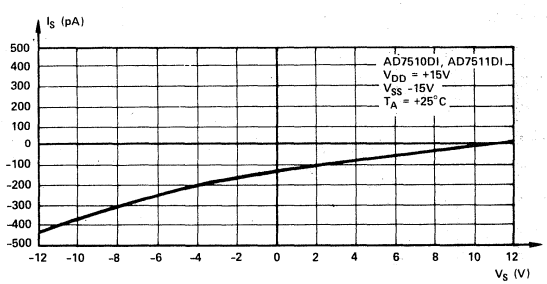
$t_{TRANSITION}$ as a Function of Digital Input Voltage



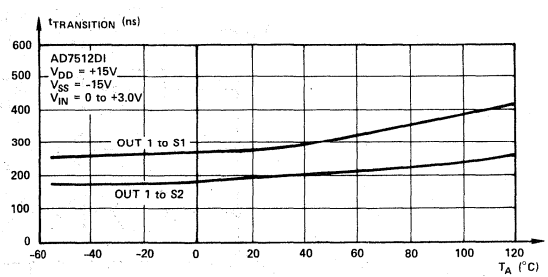
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature

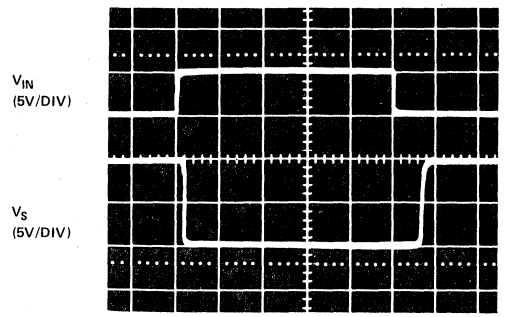


I_S, $(I_D)_{OFF}$ vs V_S



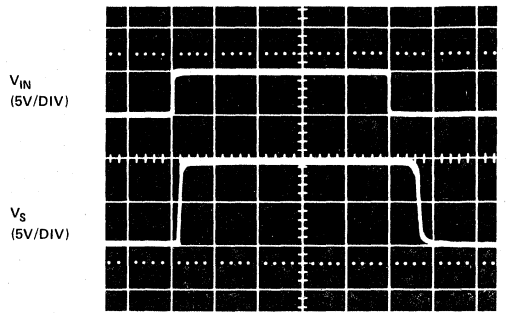
$t_{TRANSITION}$ as a Function of Temperature

0.5μs/DIV



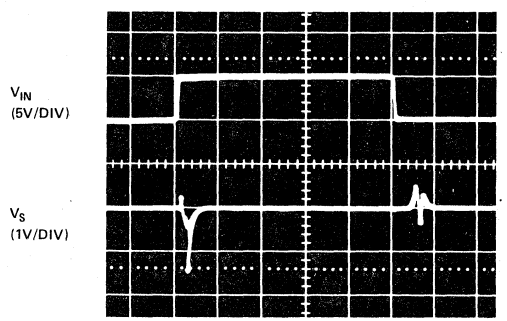
Switching Waveforms for V_D = -10V

0.5μs/DIV



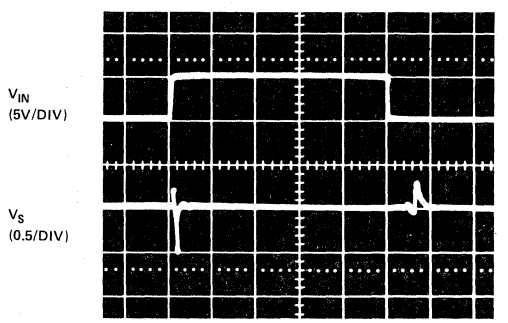
Switching Waveforms for V_D = +10V

0.5μs/DIV



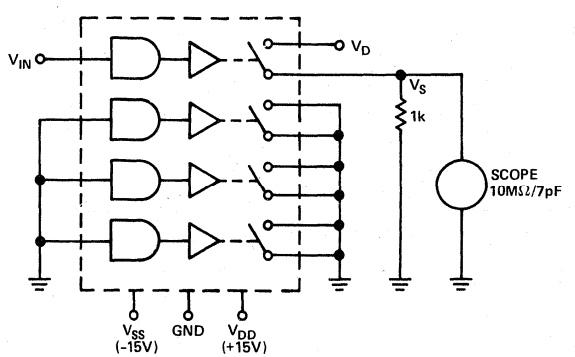
Switching Waveforms for V_D = Open

0.5μs/DIV



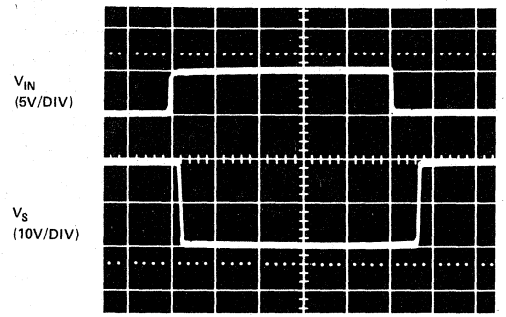
Switching Waveforms for V_D = 0V

AD7510DI, AD7511DI TEST CIRCUIT



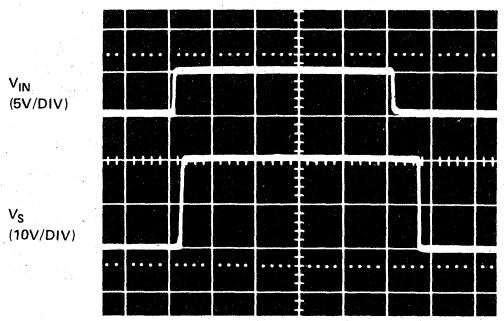
TYPICAL SWITCHING CHARACTERISTICS AD7512DI

0.5μs/DIV



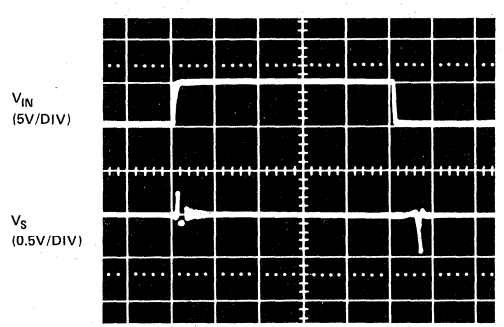
Switching Waveforms for
V_{S1} = -10V, V_{S2} = +10V, R_L = 1k

0.5μs/DIV



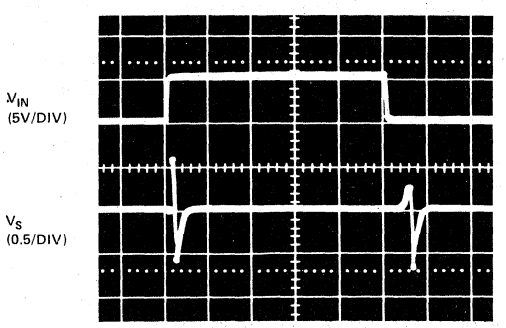
Switching Waveforms for
V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

0.5μs/DIV



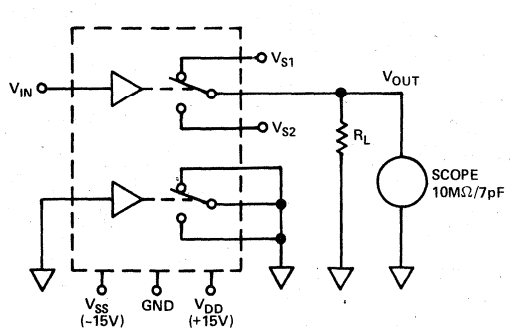
Switching Waveforms for
V_{S1} and V_{S2} = 0V, R_L = ∞

0.5μs/DIV



Switching Waveforms for
V_{S1} and V_{S2} = Open, R_L = 1k

AD7512DI TEST CIRCUIT

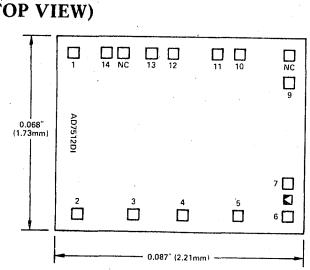


TERMINOLOGY

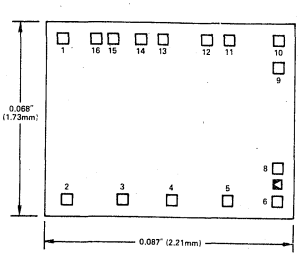
R_{ON}:	Ohmic resistance between terminals D and S.
R_{ON} Drift Match:	Difference between the R_{ON} drift of any two switches.
R_{ON} Match:	Difference between the R_{ON} of any two switches.
I_D $(I_S)_{OFF}$:	Current at terminals D or S. This is a leakage current when the switch is "OFF."
I_D $(I_S)_{ON}$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (CD):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
$t_{transition}$:	Delay time when switching from one address state to another.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

BONDING DIAGRAMS (TOP VIEW)

AD7512DI



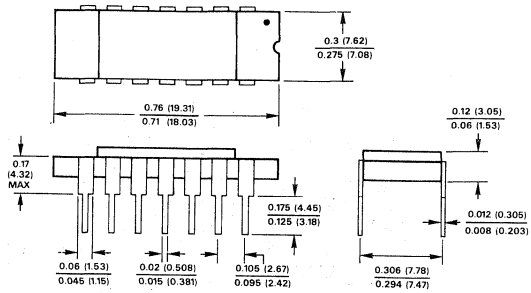
AD7510DI, AD7511DI



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

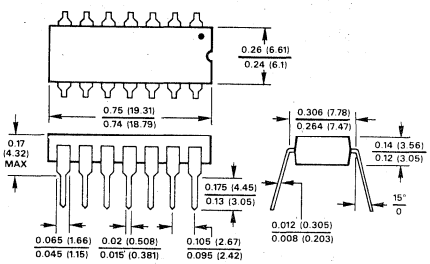
14-PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

AD7512DI

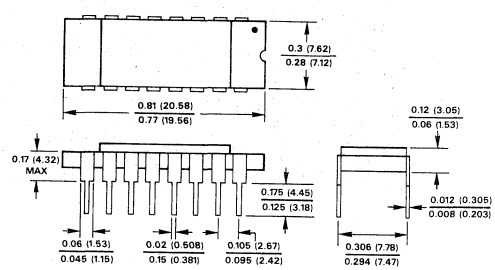
14-PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

AD7512DI

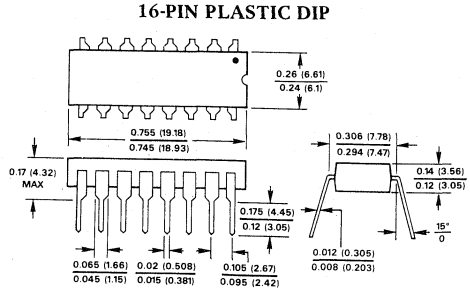
16-PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

AD7510DI, AD7511DI

16-PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

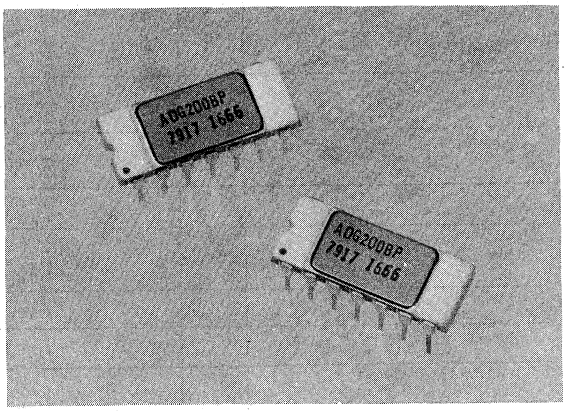
AD7510DI, AD7511DI

ANALOG DEVICES

DI CMOS Protected Dual SPST Analog Switch

ADG200

FEATURES
- Latch-Proof DI CMOS
- Overvoltage-Proof: V_{SUPPLY} ±25V
- Superior DG-200 Replacement
- Break-Before-Make Switching Action
- R_{ON}: 100Ω max over Full Temperature Range
- Direct TTL/CMOS Interface

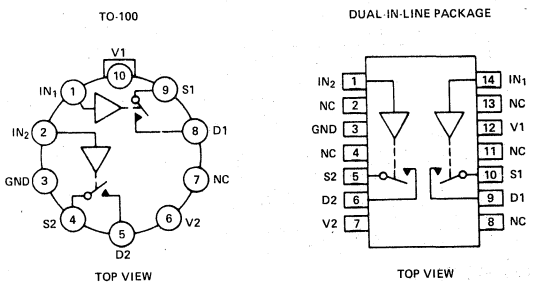


GENERAL DESCRIPTION

The ADG200 is a dual single-pole-single-throw analog switch. In the ON condition, the switch conducts current in either direction, maintaining nearly constant ON resistance over the entire analog signal range. In the OFF condition, the switch blocks voltages of peak values equal to the switch V+ and V– supplies. Switch action is break-before-make. The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated using an advanced monolithic dielectrically-isolated CMOS process, the ADG200 is a superior plug-in replacement for the DG200. The ADG200 provides additional advantages (over the DG200) of: overvoltage protection to ±25V beyond the power supplies, total latch-free operation, much lower power dissipation (30mW max) and faster switching time.

PIN CONFIGURATION



SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ORDERING INFORMATION

Commercial 0 to +70°C	Industrial -25°C to +85°C		Military -55°C to +125°C	
Plastic	Ceramic	TO-100	Ceramic	TO-100
ADG200CJ	ADG200BP	ADG200BA	ADG200AP	ADG200AA ADG200AA/883

Note: "/883" version is 100% screened to MIL-STD-883, class B as per note 3 on specifications table, next page.

SPECIFICATIONS

CHARACTERISTIC[1]		TYP[1] +25°C	MAX LIMITS AA, AP Suffix[3] -55°C[2]	+25°C	+125°C	BA, BP/CJ Suffix -25/0°C[2]	+25°C	+85/70°C[2]	UNITS	TEST CONDITIONS[4] Unless Noted V_1 = +15V, V_2 = -15V, GND = 0V	
SWITCH											
$r_{DS(ON)}$	Drain-Source ON Resistance	60 40	70 70	70 70	100 100	80 80	80 80	100 100	Ω	V_D = 10V V_D = -10V	V_{IN} = 0.8V I_S = 0.1mA
$I_{S(OFF)}$	Source OFF Leakage Current	0.2 -0.2	500 -500	2 -2	500 -500	500 -500	5 -5	500 -500	nA	V_S = 10V, V_D = -10V V_S = -10V, V_D = 10V	V_{IN} = 2.4V
$I_{D(OFF)}$	Drain OFF Leakage Current	0.3 -0.3	500 -500	2 -2	500 -500	500 -500	5 -5	500 -500	nA	V_D = 10V, V_S = -10V V_D = -10V, V_S = 10V	V_{IN} = 2.4V
$I_{D(ON)}$[5]	Channel ON Leakage Current	0.1 -0.1	500 -500	2 -2	500 -500	500 -500	2 -2	500 -500	nA	V_D = V_S = 10V V_D = V_S = -10V	V_{IN} = 0.8V
INPUT											
I_{INH}	Input Current Input Voltage High		-10 10	-1 1	-10 10	-10 10	-1 1	-10 10	μA	V_{IN} = 2.4V V_{IN} = 15V	
$I_{IN(PEAK)}$[6]	Peak Input Current Required for Transition	NOT APPLICABLE[6]									
I_{INL}	Input Current Input Voltage Low		-10	-1	-10	-10	-1	-10	μA	V_{IN} = 0V	
DYNAMIC											
t_{ON}	Turn-ON Time[7]	300		1000[2]			1000[2]		ns	V_{IN} = 3.5V to 0V	R_L = 1kΩ, C_L = 35pF
t_{OFF}	Turn-OFF Time[7]	120		500[2]			500[2]		ns	V_{IN} = 0V to 3.5V	V_S = ±5V
$C_{S(OFF)}$	Source OFF Capacitance	11							pF	V_S = 0V, V_{IN} = 5V	
$C_{D(OFF)}$	Drain OFF Capacitance	11							pF	V_D = 0V, V_{IN} = 5V	f = 140kHz
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance	28							pF	V_D = V_S = 0V V_{IN} = 0V	
OFF Isolation[8]		64							dB	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF V_S = $7V_{rms}$, f = 500kHz	
SUPPLY											
I_1	Positive Supply Current	0.02	2	1	2	2	1	2	mA	Both Channels ON; V_{IN} = 0V	
I_2	Negative Supply Current	-0.02	-2	-1	-2	-2	-1	-2	mA		
I_1	Positive Supply Current	0.1	2	1	2	2	1	2	mA	Both Channels OFF; V_{IN} = 5V	
I_2	Negative Supply Current	-0.02	-2	-1	-2	-2	-1	-2	mA		

NOTES:
[1] Typical values for information only, not guaranteed or production tested.
[2] Guaranteed, not subject to 100% production test.
[3] ADG200AP is available 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for a class B device. Final electrical tests are: $r_{DS(ON)}$, $I_{S(OFF)}$, $I_{D(OFF)}$, I_{INH}, I_{INL}, I_1 and I_2 at +25°C and +125°C (AA/883 version).
[4] Functional operation is possible for supply voltages less than ±15V, but the input logic switching threshold will shift.
[5] I_D(ON) is leakage from driver gate into ON switch.
[6] Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.
[7] Switch action is guaranteed break-before-make.
[8] OFF isolation (dB) = 20 log V_S/V_D where V_S = input to OFF switch and V_D = output.

Specifications subject to change without notice.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

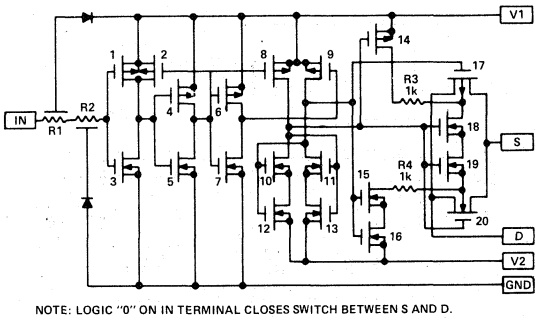
ABSOLUTE MAXIMUM RATINGS

V_{IN}(Digital Input) to Ground . . . . . -0.3V, V_1
V_S or V_D to V_1
(1 second surge) . . . . . +25V, -40V
(continuous) . . . . . +20V, -35V
V_S or V_D to V_2
(1 second surge) . . . . . -25V, +40V
(continuous) . . . . . -20V, +35V
V_1 to Ground . . . . . -0.3V, +17V
V_2 to Ground . . . . . +0.3V, -17V
Current, Any Terminal Except S or D 30mA
Current, S or D 50mA
Current, S or D Pulsed
(1ms, 10% duty cycle max) 150mA

Operating Temperature
AA, AP Suffix . . . . . -55°C to +125°C
BA, BP Suffix . . . . . -25°C to +85°C
CJ Suffix . . . . . 0°C to +70°C
Storage Temperature
CJ Suffix . . . . . -65°C to +125°C
All Others . . . . . -65°C to +150°C
Power Dissipation (Package)*
Metal Can** 450mW
14 Pin Ceramic DIP*** 825mW
14 Pin Plastic DIP**** 470mW

* Devices with all leads welded or soldered to printed circuit board
** Derate 6mW/°C above +75°C
*** Derate 11mW/°C above +75°C
**** Derate 6.5mW/°C above +25°C

CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram (1 of 2 channels)

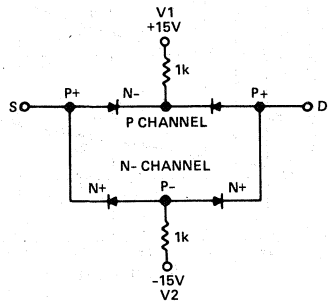


Figure 2. ADG200 Output Switch Diode Equivalent Circuit

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as R_{ON} or leakage, or provide only limited protection in the event of overvoltage.

The ADG200 switch utilizes a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is V_1 and the gate of device 17 is V_2 from the driver circuits. Device numbers 14, 15, and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter R_{ON} versus V_S response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through 1kΩ resistors R_3 and R_4 to the respective supply voltages through the "ON" devices 14, 15, and 16.

If a voltage is applied to the S or D terminals which exceeds V_1 or V_2, the S- or D-to-back-gate diode is forward biased; however, R_3 and R_4 provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased R_{ON}), the ADG200 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the V_1 or V_2 supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices — *not* in series with the signal path between the S & D terminals.

In some applications it is possible to run on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or the output of op amps will prevent damage to the device.

TYPICAL PERFORMANCE CHARACTERISTICS

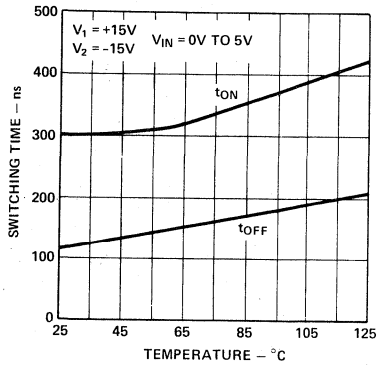


Figure 3. Switching Time vs. Temperature

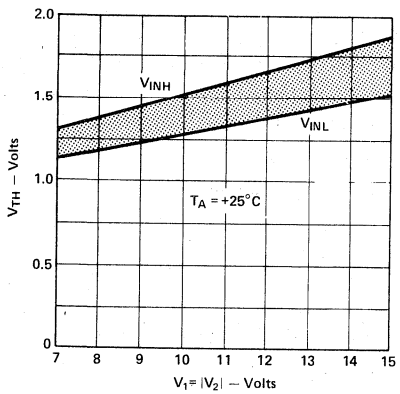
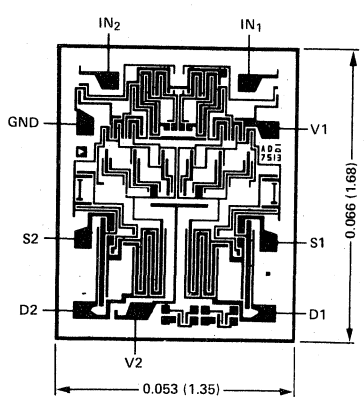


Figure 4. Input Logic Threshold vs. Power Supply Voltage

BONDING DIAGRAM

Dimensions shown in inches and (mm).

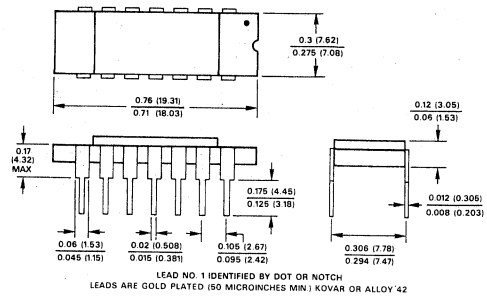


NOTES:
1. BOND GND PIN FIRST TO MINIMIZE ESD HAZARD.
2. BONDING PADS ARE 0.004 X 0.004 INCHES (0.102 X 0.102mm).

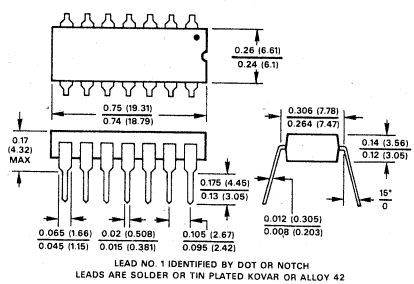
MECHANICAL INFORMATION

Dimensions shown in inches and (mm).

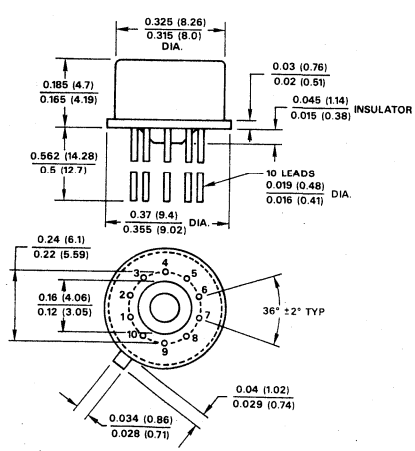
14-PIN CERAMIC DIP



14-PIN PLASTIC DIP



TO-100

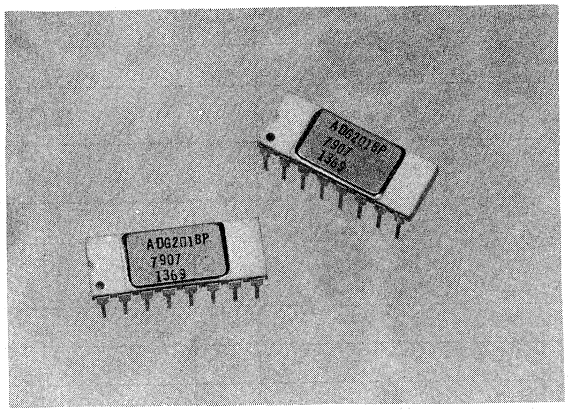


ANALOG DEVICES

DI CMOS Protected Quad SPST Analog Switch

ADG201

FEATURES
- Latch-Proof DI CMOS
- Overvoltage Proof to 25V Beyond Supplies
- Superior DG201 Replacement
- Break-Before-Make Switching Action
- Low R_{ON}: 80Ω
- Low Power Dissipation: 30mW max
- Direct TTL or CMOS Interfacing



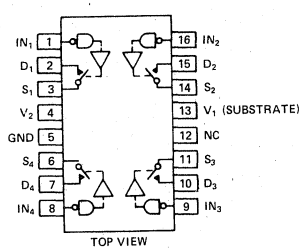
GENERAL DESCRIPTION

The ADG201 is a quad SPST analog switch. In the ON state, the switch conducts current in either direction, maintaining nearly constant ON resistance over its signal handling range. In the OFF state, it blocks voltages equal to the switch V+ and V- supplies. Switch action is break-before-make.

The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated with an advanced monolithic dielectrically-isolated CMOS process, the ADG201 is a superior plug-in replacement for the DG201. ADG201 advantages over other designs include: lower R_{ON}, lower power dissipation, faster switching time, overvoltage protection (25V beyond power supplies), and latch-free operation.

PIN CONFIGURATION



TOP VIEW

SWITCH IS OPEN FOR LOGIC "1" (POSITIVE TRUE) INPUT

ORDERING INFORMATION

Commercial 0 to +70°C	Industrial -25°C to +85°C	Military -55°C to +125°C
Plastic	Ceramic	Ceramic
ADG201CJ	ADG201BP	ADG201AP ADG201AP/883[1]

Note: [1] "/883" version is 100% screened to MIL-STD-883, class B as per note 3 on specifications table, next page.

SPECIFICATIONS

CHARACTERISTIC		TYP[1] +25°C	MAX LIMITS AP SUFFIX[3] −55°C[2]	AP SUFFIX[3] +25°C	AP SUFFIX[3] +125°C	BP, CJ SUFFIX −25/0°C[2]	BP, CJ SUFFIX +25°C	BP, CJ SUFFIX +85/70°C[2]	UNITS	TEST CONDITIONS[4] Unless Noted V_1 = +15V, V_2 = −15V, GND = 0V	
SWITCH											
$r_{DS(ON)}$	Drain-Source ON Resistance	60 40	80 80	80 80	125 125	100 100	100 100	125 125	Ω	V_D = 10V V_D = −10V	V_{IN} = 0.8V I_S = −1mA
$I_{S(OFF)}$	Source OFF Leakage Current	0.2 0.2	500 −500	1 −1	500 −500	250 −250	5 −5	250 −250	nA	V_S = 10V, V_D = −10V V_S = −10V, V_D = 10V	V_{IN} = 2.4V
$I_{D(OFF)}$	Drain OFF Leakage Current	0.3 0.3	500 −500	1 −1	500 −500	250 −250	5 −5	250 −250	nA	V_D = 10V, V_S = −10V V_D = −10V, V_S = 10V	V_{IN} = 2.4V
$I_{D(ON)}$[5]	Drain ON Leakage Current	0.1 0.1	500 −500	1 −1	500 −500	250 −250	5 −5	250 −250		V_D = V_S = 10V V_D = V_S = −10V	V_{IN} = 0.8V
INPUT											
I_{INH}	Input Current Input Voltage High		−10 10	−1 1	−10 10	−10 10	−1 1	−10 10	μA	V_{IN} = 2.4V V_{IN} = 15V	
$I_{IN(PEAK)}$[6]	Peak Input Current Required for Transition	NOT APPLICABLE[6]									
I_{INL}	Input Current Input Voltage Low		−10	−1	−10	−10	−1	−10	μA	V_{IN} = 0V	
DYNAMIC											
t_{ON}	Turn-ON Time[2,7]	260		1000			1000		ns	V_{IN} = 3.5V to 0V	R_L = 1kΩ, C_L = 35pF
t_{OFF}	Turn-OFF Time[2,7]	130		500			500		ns	V_{IN} = 0V to 3.5V	V_S = ±5V
$C_{S(OFF)}$	Source OFF Capacitance	9							pF	V_S = 0V, V_{IN} = 5V	
$C_{D(OFF)}$	Drain OFF Capacitance	9							pF	V_D = 0V, V_{IN} = 5V	
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance	21							pF	V_D = V_S = 0V V_{IN} = 0V	
OFF Isolation[8]		65							dB	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF V_S = $7V_{rms}$, f = 500kHz	
SUPPLY											
I_1	Positive Supply Current	0.015	2	1	2	2	1	2	mA	One Channel ON, V_{IN} = 0V	
I_2	Negative Supply Current	−0.015	−2	−1	−2	−2	−1	−2	mA		
I_1	Positive Supply Current	0.2	2	1	2	2	1	2	mA	All Channels OFF, V_{IN} = 5V	
I_2	Negative Supply Current	−0.015	−2	−1	−2	−2	−1	−2	mA		

NOTES:
[1] Typical values for information only, not guaranteed or production tested.
[2] Guaranteed, not subject to 100% production test.
[3] ADG201AP is available 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for a class B device. Final electrical tests are: $r_{DS(ON)}$, $I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$, I_{INH}, I_{INL}, I_1 and I_2 at +25°C and +125°C (AP/883 version).
[4] Functional operation is possible for supply voltages less than ±15V, but the input switching threshold will shift.
[5] $I_{D(ON)}$ is leakage from driver gate into ON switch.
[6] Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.
[7] Switch action is guaranteed break-before-make.
[8] OFF isolation (dB) = 20 log V_S/V_D where V_S = input to OFF switch and V_D = output.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

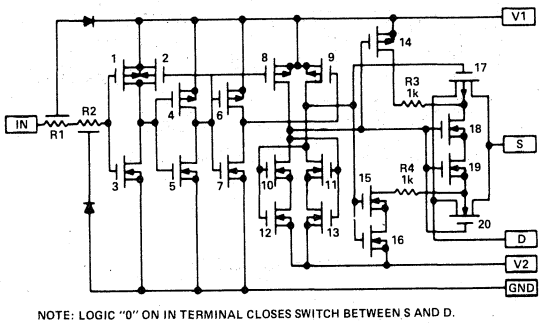
V_{IN} (Digital Input) to Ground . . . . . −0.3V, V_1
V_S or V_D to V_1
(1 second surge) . . . . . +25V, −40V
(continuous) . . . . . +20V, −35V
V_S or V_D to V_2
(1 second surge) . . . . . −25V, +40V
(continuous) . . . . . −20V, +35V
V_1 to Ground . . . . . −0.3V, +17V
V_2 to Ground . . . . . +0.3V, −17V
Current, any terminal except S or D 30mA
Continuous Current, S or D 50mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 150mA

Operating Temperature
(AP Suffix) . . . . . −55°C to +125°C
(BP Suffix) . . . . . −25°C to +85°C
(CJ Suffix) . . . . . 0°C to +70°C
Storage Temperature
(AP, BP Suffix) . . . . . −65°C to +150°C
(CJ Suffix) . . . . . −65°C to +125°C
Power Dissipation (Package)*
16 Pin Ceramic DIP** 900mW
16 Pin Plastic DIP*** 470mW

* Device mounted with all leads soldered or welded to PC board
** Derate 12mW/°C above +75°C
*** Derate 6.5mW/°C above +25°C

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed for insertion.

CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram, 1 of 4 Channels

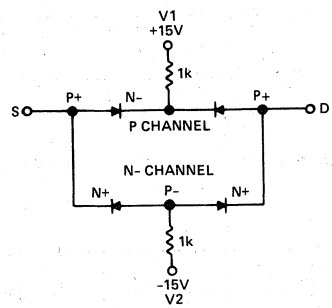


Figure 2. ADG201 Output Switch Diode Equivalent Circuit

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as R_{ON} or leakage, or provide only limited protection in the event of overvoltage.

The ADG201 switch utilises a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. the output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is V_1 and the gate of device 17 is V_2 from the driver circuits. Device numbers 14, 15 and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter R_{ON} versus V_S response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through 1kΩ resistors R_3 and R_4 to the respective supply voltages through the "ON" devices 14,15 and 16.

If a voltage is applied to the S or D terminals which exceeds V_1 or V_2, the S- or D-to-back-gate diode is forward biased; however, R_3 and R_4 provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased R_{ON}), the ADG201 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the V_1 or V_2 supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices-*not* in series with the signal path between the S & D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or the output of op amps will prevent damage to the device.

TYPICAL PERFORMANCE CHARACTERISTICS

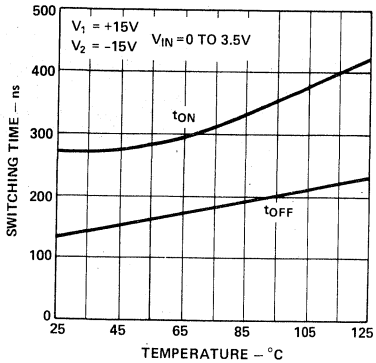


Figure 3. Switching Time vs. Temperature

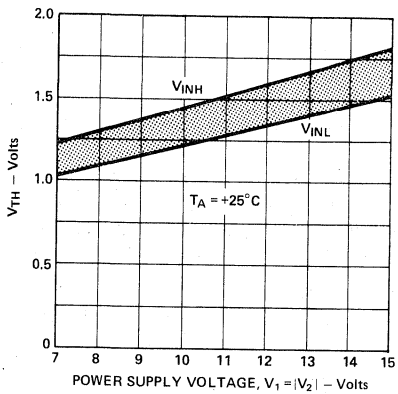
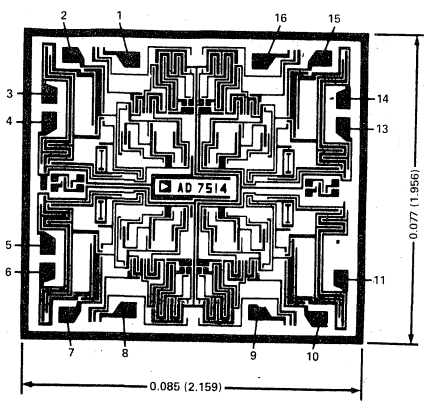


Figure 4. Input Logic Threshold vs. Power Supply Voltage

BONDING DIAGRAM

Dimensions shown in inches and (mm).

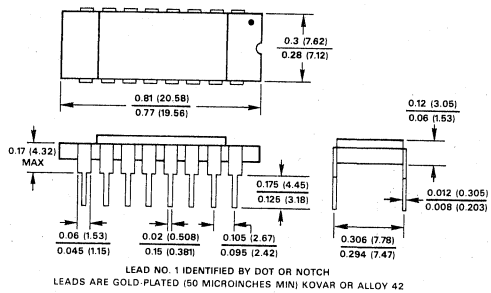


NOTES:
1. PADS ARE 0.004 × 0.004 INCHES (0.102 × 0.102mm.) MIN.
2. TO MINIMIZE ESD HAZARD, BOND PIN 5 FIRST.
3. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN ON PIN CONFIGURATION.

MECHANICAL INFORMATION

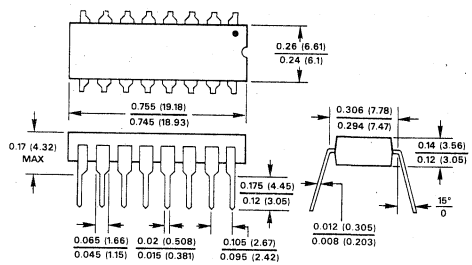
Dimensions shown in inches and (mm).

16 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD-PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

16 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

Data-Acquisition Subsystems

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AD364●	Hybrid-IC 16-to-8-Channel 12-Bit Complete μP-Compatible DAS	15-25
DAS1128	16/8-Channel 12-Bit Data-Acquisition Module	15-29
DAS1150	Low-Level-Input 12-Bit Data-Acquisition Module with Resistor-Programmable Gain	15-37
DAS1151	Low-Level-Input 12-Bit Data-Acquisition Module with Logic-Programmable Gain	15-37

●New product since the 1979 *Data Acquisition Products Catalog Supplement.*

Selection Guide
Data-Acquisition Subsystems

The products catalogued in this section are modules and hybrid circuits that perform at least two of the following functions: multiplexing, sample-hold, a/d conversion. In addition, some types have programmable-gain amplifiers, microprocessor interface logic, and/or switching for applications involving both differential and single-ended inputs. They are classified here in order of number of single-ended/differential channels available within the device.

The data sheets provide complete descriptions, specifications, and application information. Additional general information regarding portions of the subsystems may be found in the appropriate sections of this catalog (e.g., 2: Instrumentation Amplifiers, 10: Analog/Digital Converters, and 13: Sample/Track-Hold Amplifiers). Additional data-acquisition subsystems may be found in Sections 10 (Track-Hold and ADC for Video Applications, e.g., MOD-1205) and 16 (Microcomputer Interface Boards). Data for the AD7583, listed in this Selection Guide, will be found in Section 10: A/D Converters.

Specifications are typical at +25°C and rated supply voltages, unless noted otherwise.

DATA-ACQUISITION SUBSYSTEMS*

Model	Channels	Resolution (Bits)	Characteristics	Page
DAS1128	16/8	12	General-purpose complete 12-bit data-acquisition module. Performs multiplexing, sample-hold, a/d conversion, with maximum throughput rate of 35kHz. Can be readily interfaced with microcomputer systems via 8255 or PIA.	15-29
AD364●	16 to 8	12	Hybrid-IC general-purpose 12-bit data-acquisition subsystem, with 30kHz throughput rate, complete in two hermetically sealed dual in-line packages, furnished with high quality external *hold* capacitor. The analog input package accepts up to 16 single-ended or 8 differential channels, in combinations selectable by a logic-switchable mode control, and provides multiplexing, differential amplification, and sample-hold. The second package is a two-chip 12-bit successive-approximation a/d converter with on-board three-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus.	15-25
AD363	16 to 8	12	Hybrid-IC general-purpose 12-bit data-acquisition subsystem, with 30kHz throughput rate, in two 32-pin metal DIP packages, furnished with high quality external *hold* capacitor. The analog input package accepts up to 16 single-ended or differential channels, in combinations selected by a logic-switchable mode control, and provides multiplexing, differential amplification, and sample-hold. The second package is a high-accuracy 12-bit successive-approximation a/d converter with parallel and serial output and an uncommitted unity-gain analog buffer amplifier. The packages are connected externally by an analog signal line and a digital control line.	15-13
AD362●	16 to 8	12+	Hybrid IC analog front end (used in AD364 and AD363), made available separately for applications with user's choice of a/d converter. Accepts up to 16 single-ended or 8 differential channels, in combinations selected by a logic-switchable mode control, and provides multiplexing, differential amplification, and sample-hold (capacitor furnished). Nonlinearity $\leq \pm 0.005\%$, 10μs acquisition time to 0.01%, high differential input impedance ($10^{10}\ \Omega$) and common-mode rejection (80dB) fully protected multiplexer inputs, aperture uncertainty 0.5ns max, simple interface to popular a/d converters.	15-5
AD7583●	9	8	CMOS IC monolithic single-supply 9-channel (expandable) 8-bit ratiometric a/d converter. On-board are multiplexer, quad-slope switch array and counters, three-state output buffer and bidirectional data bus, and all required control logic. Most applications require the addition of a few passive components and two general-purpose op amps.	10-89

Model	Channels	Resolution (Bits)	Characteristics	Page
DAS1150/51	1	12	General-purpose single-channel 12-bit data-acquisition modules with 25kHz throughput rate. Contain differential-input amplifier, sample-hold and 12-bit successive-approximation a/d converter. DAS1150's amplifier has resistor-programmable gain from 1 to 1000; DAS1151's amplifier is software programmable for gains of 1, 2, 4, 8. Multiplexing for desired number of channels (if >1) provided externally by user.	15-37

*See also SHA1144 data sheet in Section 13 (Sample/Track-Hold), the AC1580 utility card for assembling 14-bit data-acquisition subsystem using ADC1130/1131 a/d converters. The scanning meters in Section 8 (AD2036, AD2037, and AD2038) also function as data-acquisition subsystems with BCD output.

•New product since 1979 *Data Acquisition Products Catalog Supplement.*

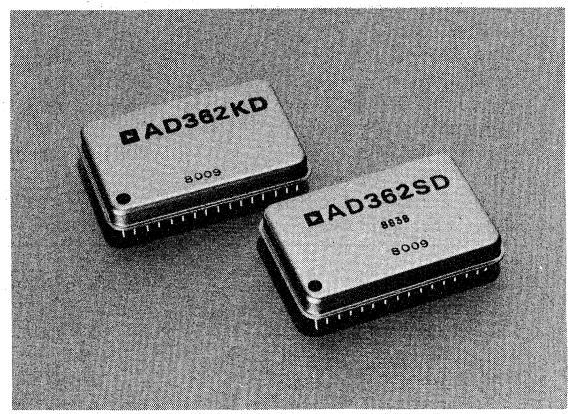
ANALOG DEVICES

Precision Sample-and-Hold with 16-Channel Multiplexer

AD362

FEATURES

- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Precision: Nonlinearity ≤±0.005%
- High Speed: 10μs Acquisition Time to 0.01%
- Complete and Calibrated: No Additional Parts Required
- Small, Reliable: 32 Pin Hermetic Metal DIP
- Versatile: Simple Interface to Popular Analog to Digital Converters
- High Differential Input Impedance ($10^{10}\Omega$) and Common Mode Rejection (80dB)
- Fully Protected Multiplexer Inputs



PRODUCT DESCRIPTION

The AD362 is a complete, precision 16-channel data acquisition system analog input section in hybrid integrated circuit form. Large-scale linear integrated circuitry, thick- and thin-film technology and active laser trimming gives the AD362 extensive applications versatility along with full 12-bit accuracy.

The AD362 contains two 9-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

The sample-and-hold mode control is designed to connect directly to the "Status" output of an analog to digital converter so that a convert command to the ADC will automatically put the sample-and-hold into the "Hold" mode. A precision hold capacitor is included with each AD362. The AD362 output amplifier is capable of driving the unbuffered analog input of most high-speed, 12-bit successive-approximation ADCs. Interface is thereby reduced to two simple connections with no additional components required.

When used with a 12-bit, 25-microsecond ADC such as the AD572, AD574 or AD ADC80, system throughput rate is as high as 30kHz at full rated accuracy. The AD362KD is specified for operation over a 0 to +70°C temperature range while the AD362SD operates to specification from −55°C to +125°C. Processing to MIL-STD-883, Class B is available for the AD362SD. Both grades are packaged in a hermetic, electrostatically shielded 32-pin metal dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD362, when used with a precision analog to digital converter, forms a complete, accurate, high-speed data acquisition system.
2. The 16-input channels may be configured in single-ended, differential or a mixture of both modes. Mode switching is provided by a user-controllable internal analog switch.
3. Multiplexers, differential amplifier, sample-and-hold and high-speed output buffer provide complete analog interfacing capabilities.
4. Internal channel address latches are provided to facilitate interfacing the AD362 to data, address or control buses.
5. All grades of the AD362 are hermetically sealed in rugged metal DIP packages.
6. A precision hold capacitor is provided with each AD362.
7. The AD362SD is specified over the entire military temperature range, −55°C to +125°C. Processing to MIL-STD-883, Class B is available.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD362KD	AD362SD/AD362SD-883B[1]
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Range, Linear T_{min} to T_{max}	±10V min	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
Offset, Channel to Channel	±2.5mV max	*
ACCURACY		
Gain Error, T_{min} to T_{max}	±0.02% FSR, max	*
Offset Error, T_{min} to T_{max}	±4mV	*
Linearity Error	±0.005% max	*
T_{min} to T_{max}	±0.01% max	*
Noise Error	1mV p-p, 0.1 to 1MHz, max	*
T_{min} to T_{max}	2mV p-p, 0.1 to 1MHz, max	*
TEMPERATURE COEFFICIENTS		
Gain, T_{min} to T_{max}	±4ppm/°C max	±2ppm/°C max
Offset, ±10V Range, T_{min} to T_{max}	±2ppm/°C max	±1.5ppm/°C max
SAMPLE AND HOLD DYNAMICS		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time, for 20V Step to ±0.01% of Final Value	18μs max (10μs typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[2]		
Input Channel Select (Pins 28-31)	4-Bit Binary, Channel Address	*
	1LS TTL Load	*
Channel Select Latch (Pin 32)	"1": Latch Transparent	*
	"0": Latched	*
	8LS TTL Loads	*
Single Ended/Differential Mode Select (Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode	*
	3TTL Loads	*
Sample and Hold Command (Pin 13)	"0": Sample Mode	*
	"1": Hold Mode	*
	1TTL Load	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ 30mA max	*
	-15V, ±5% @ 30mA max	*
	+5V, ±5% @ 40mA max	*
Total Power Dissipation	1.1 Watts max	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[3]	-55°C to +150°C

NOTES:

[1] The AD362 is available fully processed and screened to the requirements of MIL-STD-883, Class B. A complete list of tests is given on next page. When ordering, specify "AD362SD/883B".

[2] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V. One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.

[3] AD362KD External Hold Capacitor is limited to +85°C; AD362 device itself may be stored at up to +150°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all models of the AD362 receive the following processing:

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	In-house Criteria
2) Stabilization Bake	24 hours @ +150°C
3) Seal Test, Gross Leak	Method 1014 Test Condition C
4) Operating Burn-In	24 hours @ +125°C

PROCESSING TO MIL-STD-883

All models of AD362 ordered to the requirements of MIL-STD-883. Method 5008 are identified with a /883B suffix and receive the following processing:

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	2017.1
2) Stabilization Bake	1008, 24 hours @ +150°C
3) Temperature Cycle	1010, Test Condition C, 10 cycles, -65°C to +150°C
4) Constant Acceleration	2001, Y1 Plane, 1000G
5) Visual Inspection	Visable Damage
6) Operating Burn-In	1015, Test Condition B 160 hours @ +125°C
7) Seal Test: Fine Leak	1014, Test Condition A, 5 x 10^{-7}std cc/sec
Gross Leak	1014, Condition C
8) Final Electrical Test	Per Data Sheet
9) External Visual Inspection	2009

AD362 PIN FUNCTION DESCRIPTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Status
14	Offset Adjust (See Figure 5)
15	Offset Adjust (See Figure 5)
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch Transparent

AD362 ORDERING GUIDE

Model	Specification Temp Range	Max Gain TC
AD362KD	0 to +70°C	±4ppm/°C
AD362SD	-55°C to +125°C	±2ppm/°C
AD362SD/883B	-55°C to +125°C	±2ppm/°C

NOTE: D Suffix = Dual-In-Line package designator.

AD362 DESIGN

The AD362 consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output buffer, channel address latches and control logic as shown in Figure 1. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD362 to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD362 by dynamically switching the input mode control.

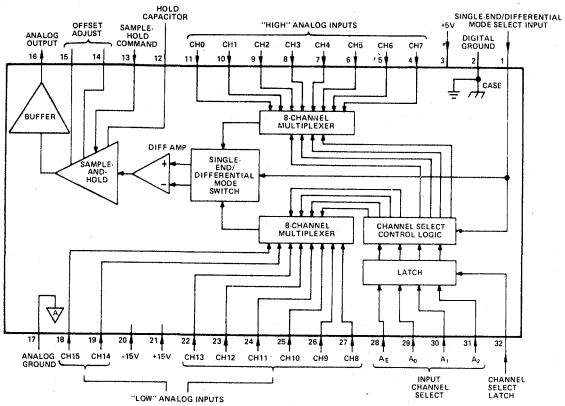


Figure 1. AD362 Analog Input Section Functional Block Diagram and Pinout

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range device (AD362KD) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD362SD). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD362 may drive a fast, unbuffered, precision ADC without loss of accuracy.

The AD362 is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

THEORY OF OPERATION

Concept

The AD362 is intended to be used in conjunction with a high-speed precision analog-to-digital converter to form a complete data acquisition system (DAS) in microcircuit form. Figure 2 shows a general AD362-with-ADC DAS application.

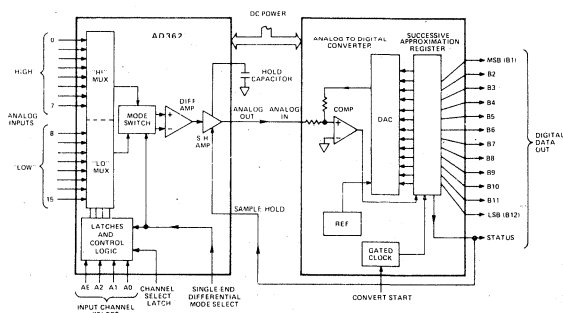


Figure 2. AD362 with ADC as a Complete Data Acquisition System

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

System Timing

Figure 3 is a timing diagram for the AD362 connected as shown in Figure 2 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12 bit type such as the AD572 or AD ADC80.

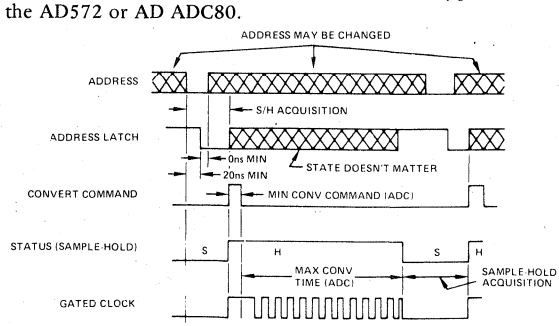


Figure 3. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

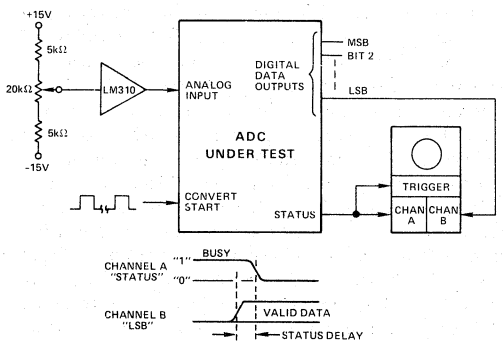


Figure 4. ADC Status Valid Test

NOTE:

Valid Output Data

Not all ADCs have all data bits available when Status indicates that the conversion is complete. Successive approximation ADCs based on the 2502/3/4 type of register must have a Status delay built in or the final data bit will lag Status by approximately 50ns. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external 100ns delay or use of an ADC with a valid Status output is necessary to prevent this problem. The applications shown in this data sheet ensure that all data bits will be valid.

The following test may be made to determine if the ADC Status timing is correct:

1. Connect the ADC under test as shown in Figure 4.
2. Trigger the oscilloscope on Status. Delay the display such that Status is mid-screen.
3. Observe the LSB data output of the ADC.
4. Vary the analog input control to confirm that the LSB transition precedes the Status transition.

Single-Ended/Differential Mode Control

The AD362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 1. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD362 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (pin 13) is normally connected to the Status output (pin 20) from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD362. One side of this capacitor is wired to pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD362KD is Polystyrene while the wider operating temperature range of the AD362SD requires a Teflon capacitor (supplied).

Smaller capacitors will allow slightly faster operation, but only with increased noise and decreased precision. 1000pF will typically allow acquisition to 0.1% in four microseconds.

Larger capacitors may be substituted to reduce noise, and sample-to-hold offset, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD326KD only) or Teflon (AD362KD or SD). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to AD362 voltage offset and gain was to be inserted between the AD362 and the ADC. To adjust the offset of the AD362, the circuit shown in Figure 5 is recommended.

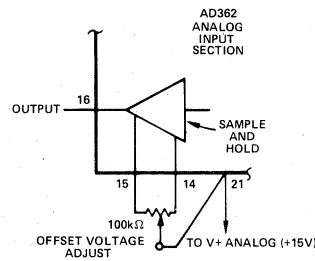


Figure 5. AD362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (pin 17) and Digital Ground (pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 6. This will protect the AD362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

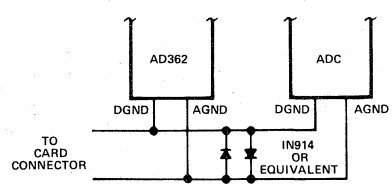


Figure 6. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Interfacing to Popular Analog to Digital Converters

The AD362 has been designed to interface directly to most analog to digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made (see page 15-9).
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

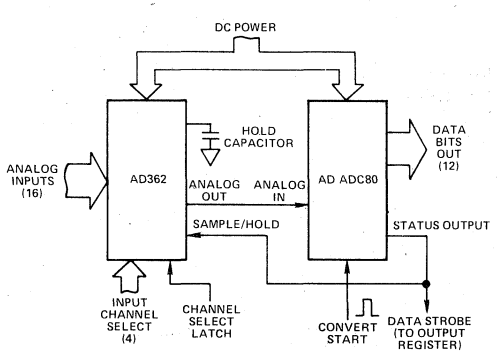
Complete system throughput performance is determined by combining the worst-case specifications of the AD362 and the ADC. If guaranteed system performance is required, the AD363 and AD364 are recommended. The AD363 includes an AD362 and an AD572 12-bit, 25-microsecond precision ADC. The AD364 consists of an AD362 and an AD574 12-bit, microprocessor-compatible, low cost ADC. Each is specified as a complete, two-package system; data sheets are available upon request.

Figure 7a shows the AD362 driving an AD ADC80. The AD ADC80 is a 12-bit, 25-microsecond, low-cost ADC that meets all of the requirements listed above. Throughput rate is typically 30kHz with no missing codes over the operating temperature range.

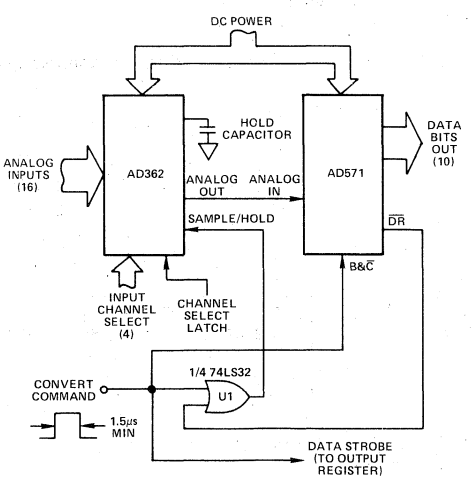
Figure 7b shows a 10-bit application based on the AD362 and the AD571, a complete low cost 10-bit, 25-microsecond ADC. In this case, two of the above requirements are not met:

1. $\overline{DR}$ ($\overline{DATA\ READY}$), as Status, is positive-true but. . .
2. $\overline{DR}$ does not indicate that a conversion is in progress until 1.5μs after conversion starts.
3. $\overline{DR}$ does indicate conversion complete after the LSB decision is made, but. . .
4. $\overline{DR}$ precedes the enabling of the AD571 output 3-state gates by 500ns.

The gating provided by U1 allows the applied convert command (CC) to initiate input hold at the AD362. CC must last for more than 1.5μs so that $\overline{DR}$ may then assume control of Hold. If conversion is continuous (consistent with multi-channel operation), the next convert command can be used to load the previously-converted data into an output register. For single conversion operation, a 1μs delay of the falling edge of $\overline{DR}$ may be used to signify valid data.



a. 12-Bit DAS Using AD362 and AD ADC80



b. 10-Bit DAS Using AD362 and AD571

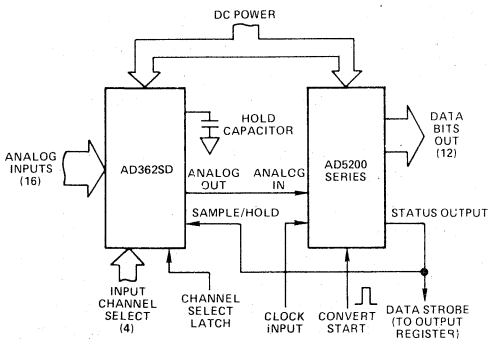
Figure 7. Data Acquisition Systems Based on the AD362 and Popular ADC's

Interfacing to Special Purpose ADCs

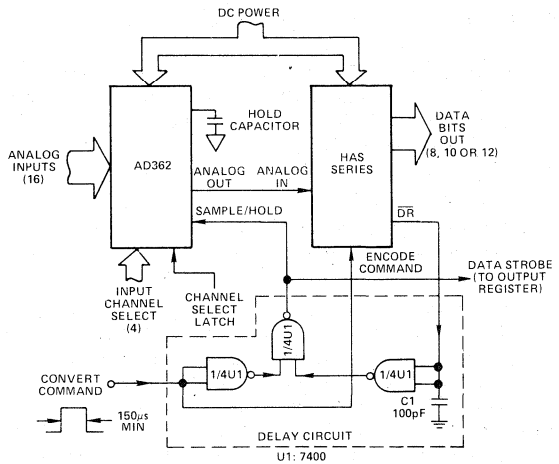
The AD5200 series of ADCs perform a 12-bit conversion in 50 microseconds and feature totally adjustment-free operation, high accuracy, and a small hermetically-sealed 24-pin package.

These ADCs are often used in high-reliability applications and, like the AD362SD (which operates over the -55°C to +125°C temperature range) are available processed to MIL-STD-883, Class B. The AD5200 series meets all of the interfacing requirements for direct connection to the AD362 as shown in Figure 8a. System throughput rate is typically 16kHz.

The HAS series of ultra-fast ADCs are 8-bit (HAS0801), 10-bit (HAS1001) and 12-bit (HAS1202) devices that convert in 1.5, 1.7, and 2.8 microseconds (maximum) respectively. These devices are hybrid IC's, packaged in 32-pin DIPs. Since the Data Ready signal from the HAS precedes the LSB decision, $\overline{DR}$ must be delayed. Figure 8b shows the appropriate circuitry to provide that delay. Throughput rate for the 12-bit system is typically 80kHz.



a. 12-Bit High Accuracy and Reliability DAS Using AD362 and AD5200



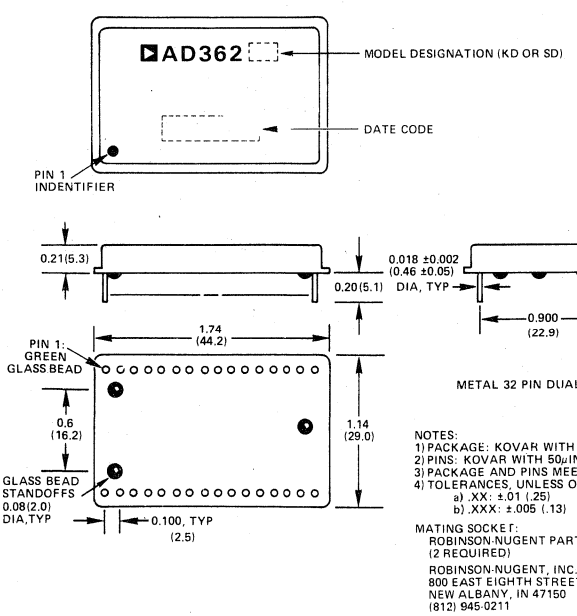
b. High-Speed DAS Using AD362 and HAS

Figure 8. Data Acquisition Systems Based on the AD362 and Purpose ADCs

OUTLINE DIMENSIONS
PACKAGE SPECIFICATIONS

Dimensions shown in inches and (mm).

"D" PACKAGE



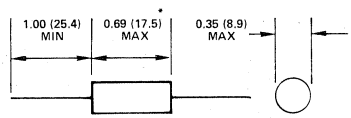
METAL 32 PIN DUAL-IN-LINE PACKAGE

NOTES:
1) PACKAGE: KOVAR WITH 100µIN. MIN., NICKEL PLATE
2) PINS: KOVAR WITH 50µIN. MIN 24K GOLD PLATE
3) PACKAGE AND PINS MEET ALL REQUIREMENTS OF MIL-STD-883
4) TOLERANCES, UNLESS OTHERWISE NOTED:
   a) .XX: ±.01 (.25)
   b) .XXX: ±.005 (.13)

MATING SOCKET:
ROBINSON-NUGENT PART NUMBER SB-16-G
(2 REQUIRED)

ROBINSON-NUGENT, INC.
800 EAST EIGHTH STREET
NEW ALBANY, IN 47150
(812) 945-0211

HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH AD362KD

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH AD362SD IS 1.00".

Complete 16-Channel 12-Bit Integrated Circuit Data Acquisition System

AD363

FEATURES

Versatility
- **Complete System in Reliable IC Form**
- **Small Size: Two 32-Pin Metal DIP's**
- **16 Single-Ended or 8 Differential Channels with Switchable Mode Control**
- **Military/Aerospace Temperature Range: -55°C to +125°C (AD363S) MIL-STD-883B Processing Available**
- **Versatile Input/Output/Control Format**
- **Short-Cycle Capability**

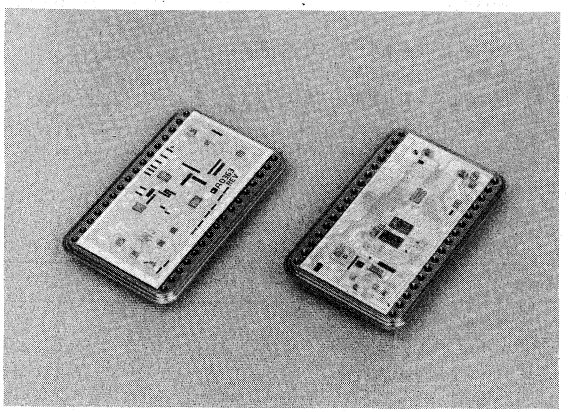
Performance
- **True 12-Bit Operation: Nonlinearity ≤±0.012%**
- **Guaranteed No Missing Codes Over Temperature Range**
- **High Throughput Rate: 30kHz**
- **Low Power: 1.7W**
- **Hermetically-Sealed, Electrostatically-Shielded Metal DIP's**

Value
- **Complete: No Additional Parts Required**
- **Reliable: Hybrid IC Construction, Hermetically Sealed by Welding. All Inputs Fully Protected.**
- **Precision +10.0 ±0.005 Volt Reference for External Application**
- **Fast Precision Buffer Amplifier for External Application**
- **Low Cost**

PRODUCT DESCRIPTION

The AD363 is a complete 16 channel, 12-bit data acquisition system in integrated circuit form. By applying large-scale linear and digital integrated circuitry, thick and thin film hybrid technology and active laser trimming, the AD363 equals or exceeds the performance and versatility of previous modular designs.

The AD363 consists of two separate functional blocks, each hermetically-sealed in an electrostatically-shielded 32-pin metal dual-in-line package. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD363 by dynamically switching the input mode control.



The Analog-to-Digital Converter Section contains a complete 12-bit successive approximation analog-to-digital converter, including internal clock, precision 10 volt reference, comparator, buffer amplifier and a proprietary-design 12-bit D/A converter. Active laser trimming of the reference and D/A converter results in maximum linearity errors of ±0.012% while performing a 12-bit conversion in 25 microseconds.

Analog input voltage ranges of ±2.5, ±5.0, ±10, 0 to +5 and 0 to +10 volts are user-selectable. Adding flexibility and value are the precision 10 volt reference (active-trimmed to a tolerance of ±5mV) and the internal buffer amplifier, both of which may be used for external applications. All digital signals are TTL/DTL compatible and output data is positive-true in parallel and serial form.

System throughput rate is as high as 30kHz at full rated accuracy. The AD363K is specified for operation over a 0 to +70°C temperature range while the AD363S operates to specification from -55°C to +125°C. Processing to MIL-STD-883B is available for the AD363S. Both device grades are guaranteed to have no missing codes over their specified temperature ranges.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD363K	AD363S
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5V, ±5.0V, ±10.0V	*
Unipolar	0 to +5V, 0 to +10V	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
RESOLUTION	12 BITS	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adj. to Zero)	*
Unipolar Offset Error	±10mV (Adj to Zero)	*
Bipolar Offset Error	±20mV (Adj to Zero)	*
Linearity Error	±½LSB max	*
Differential Linearity Error	±1LSB max (±½LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1mV p-p, 0 to 1MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30ppm/°C max (±10ppm/°C typ)	±25ppm/°C max (±15ppm/°C typ)
Offset, ±10V Range	±10ppm/°C max (±5ppm/°C typ)	±8ppm/°C max (±5ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25μs max (22μs typ)	*
Throughput Rate, Full Rated Accuracy	25kHz min (30kHz typ)	*
Sample and Hold		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time		
To ±0.01% of Final Value for Full Scale Step	18μs max (10μs, typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[4]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion.	*
	1TTL Load	*
Input Channel Select (To Analog Input Section, Pins 28-31)	4 Bit Binary, Channel Address.	*
	1LS TTL Load	*
Channel Select Latch (To Analog Input Section, Pin 32)	"1" Latch Transparent	*
	"0" Latched	*
	4LS TTL Loads	*

MODEL	AD363K	AD363S
DIGITAL INPUT SIGNALS, cont.		
Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20)	"0" Sample Mode "1" Hold Mode 2LS TTL Loads	* * *
Short Cycle (To ADC Section Pin 14)	Connect to +5V for 12 Bits Resolution. Connect to Output Bit n + 1 For n Bits Resolution. 1TTL Load	* * *
Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)	"0": Single-Ended Mode "1": Differential Mode 3TTL Loads	* * *
DIGITAL OUTPUT SIGNALS[4]		
(All Codes Positive True)		
Parallel Data		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Two's Complement	*
Output Drive	2TTL Loads	*
Serial Data (NRZ Format)		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2TTL Loads	*
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	*
Output Drive	2TTL Loads	*
Internal Clock		
Output Drive	2TTL Loads	*
Frequency	500kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±5mV	*
Max External Current	±4mA	*
Voltage Temp. Coefficient	±20ppm/°C, max	±10ppm/°C, max
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ +45mA max (+38mA typ) -15V, ±5% @ -45mA max (-38mA typ) +5V, ±5% @ +136mA max (+113mA typ)	* * *
Total Power Dissipation	2 watts max (1.7 watts typ).	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[3]	-55°C to +150°C

NOTES:
[1] With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 7 and 8.
[2] Conversion time of ADC Section.
[3] AD363K External Hold Capacitor is limited to +85°C; Analog Input Section and ADC Section may be stored at up to +150°C.
[4] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V.
One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)	
+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION	
Pin Number	**Function**
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided, See Figure 1)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 20
14	Offset Adjust (See Figure 6)
15	Offset Adjust (See Figure 6)
16	Analog Output Normally Connected to ADC "Analog In" (See Figure 1)
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION	
Pin Number	**Function**
1	Data Bit 12 (Least Significant Bit) Out
2	Data Bit 11 Out
3	Data Bit 10 Out
4	Data Bit 9 Out
5	Data Bit 8 Out
6	Data Bit 7 Out
7	Data Bit 6 Out
8	Data Bit 5 Out
9	Data Bit 4 Out
10	Data Bit 3 Out
11	Data Bit 2 Out
12	Data Bit 1 (Most Significant Bit) Out
13	$\overline{\text{Data Bit 1}}$ ($\overline{\text{MSB}}$) Out
14	Short Cycle Control Connect to +5V for 12 Bits Connect to Bit (n+1) Out for n Bits
15	Digital Ground
16	Positive Digital Power Supply, +5V
17	$\overline{\text{Status}}$ Out "0": Conversion in Progress (Parallel Data Not Valid) "1": Conversion Complete (Parallel Data Valid)
18	+10Volt Reference Out (See Figures 3, 7, 8, 11)
19	Clock Out (Runs During Conversion)
20	Status Out "0": Conversion Complete (Parallel Data Valid) "1": Conversion in Progress (Parallel Data Not Valid)
21	Convert Start In Reset Logic : ⎍‾‾↑‾‾ Start Convert : ‾‾↓⎍
22	Comparator In (See Figures 3, 7, 8)
23	Bipolar Offset Open for Unipolar Inputs Connect to ADC Pin 22 for Bipolar Inputs (See Figure 8)
24	10V Span R In (See Figure 7)
25	20V Span R In (See Figure 8)
26	Analog Ground
27	Gain Adjust (See Figures 7 and 8)
28	Positive Analog Power Supply, +15V
29	Buffer Out (For External Use)
30	Buffer In (For External Use)
31	Negative Analog Power Supply, -15V
32	Serial Data Out Each Bit Valid On Trailing (‾‾↓⎍) Edge Clock Out, ADC Pin 19

AD363 DESIGN

Concept

The AD363 consists of two separate functional blocks as shown in Figure 1; each is packaged in a hermetically-sealed 32-pin metal DIP.

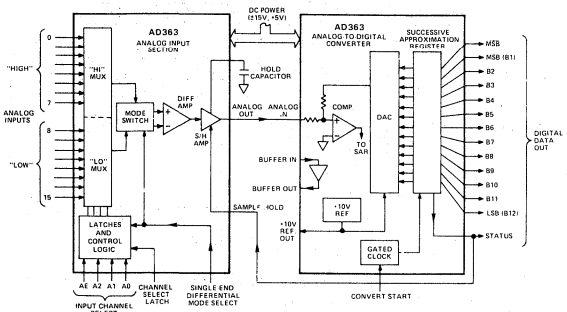


Figure 1. AD363 Functional Block Diagram

The Analog Input Section contains multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. Analog-to-digital conversion is provided by a 12 bit, 25 microsecond "ADC" which is also available separately as the AD572.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration 32 pin packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

Analog Input Section Design

Figure 2 is a block diagram of the AD363 Analog Input Section (AIS).

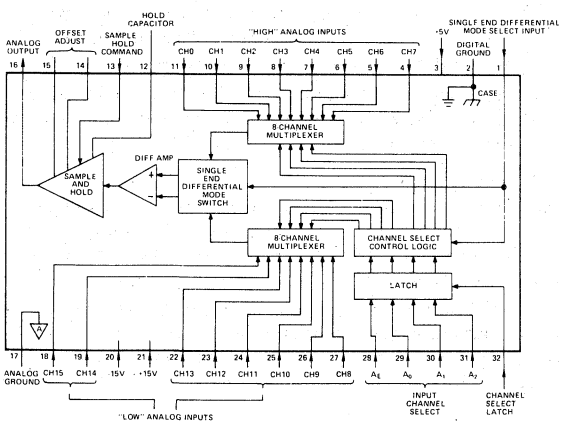


Figure 2. AD363 Analog Input Section Functional Block Diagram and Pinout

The AIS consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold, channel address latches and control logic. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single product to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD363 by dynamically switching the input mode control.

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range system (AD363K) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD363S). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The Analog Input Section is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

Analog-to-Digital Converter Design

Figure 3 is a block diagram of the Analog-to-Digital Converter Section (ADC) of the AD363.

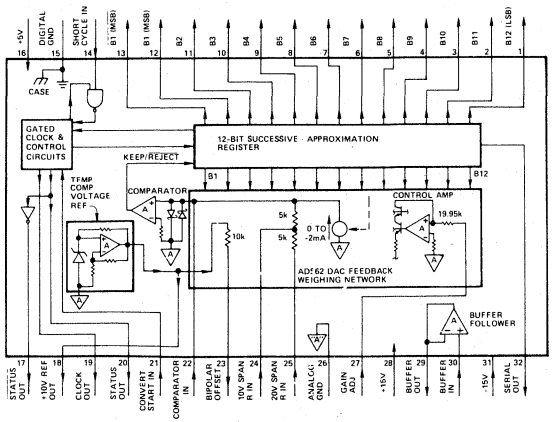


Figure 3. AD363 ADC Section (AD572) Functional Diagram and Pinout

Available separately as the AD572, the ADC is a 12-bit, 25 microsecond device that includes an internal clock, reference, comparator and buffer amplifier.

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, ±5mV by active laser-trimming of the thin-film resistors which determine the closed-loop gain of the op amp. 4mA of current is available for external use. The reference circuit is constructed on its own thin-film substrate which is, in turn, mounted on the thick-film ADC main substrate.

The DAC feedback weighing network is comprised of a proprietary 12-bit analog current switch chip and silicon-chromium thin-film ladder network. (Packaged separately, this DAC is available as the AD562.) This ladder network is active laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.005% of FSR (full-scale range) to guarantee no missing codes over the operating temperature range. The design of the ADC includes scaling resistors that provide user-selectable analog input signal ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts.

Other useful features include true binary output for unipolar inputs, offset binary and two's complement output for bipolar inputs, serial output, short-cycle capability for lower resolution, higher speed measurements, and an available high input impedance buffer amplifier which may be used elsewhere in the system.

As in the Analog Input Section, the ADC main substrate includes thick-film resistors in non-critical areas. Thin-film substrates are separately mounted to assure accurate and stable reference and DAC performance. Packaging considerations are the same as for the AIS.

THEORY OF OPERATION

System Timing

Figure 4 is a timing diagram for the AD363 connected as shown shown in Figure 1 and operating at maximum conversion rate.

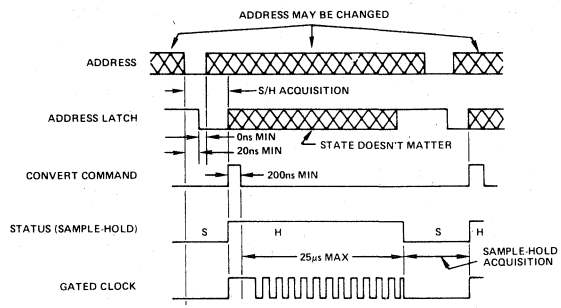


Figure 4. AD363 Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy" the sample-and-hold is in the hold mode.
4. The ADC goes into its 25 microsecond conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not effect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

ADC Operation

On receipt of a Convert Start command, the analog-to-digital converter converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

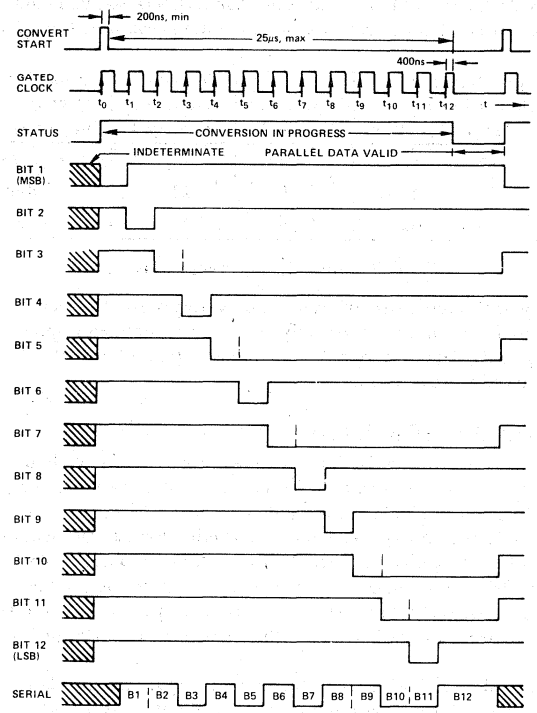


Figure 5. ADC Timing Diagram (Binary Code 110101011001)

The timing diagram is shown in Figure 5. Receipt of a Convert Start signal sets the Status flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and Status flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the Convert Start signal. At time t0, B1 is reset and B2-B12 are set unconditionally. At t1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t12. After 400ns delay period, the Status flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the Status flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges.

Incorporation of this 400ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the Status flag, permitting parallel data transfer to be initiated by the trailing edge of the Status signal.

The versatility and completeness of the AD363 concept results in a large number of user-selectable configurations. This allows optimization of most systems applications.

Single-Ended/Differential Mode Control

The 363 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. Figure 11 illustrates an example of a "mixed" application. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "hold mode"). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Analog Input Section, pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexes singly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 1. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode).

Input Channel Address Latch

The AD363 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32 of the Analog Input Section) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the time of the "1" to "0" transition.

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Analog Input Section, pin 13) is normally connected to the Status output (pin 20) from the ADC section. When a conversion is initiated by applying a Convert Start command to the ADC (pin 21), Status goes to Logic "1", putting the sample-and-hold into the "hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the sample mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD363. One side of this capacitor is wired to the Analog Input Section pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD363K is Polystyrene while the wider operating temperature range of the AD363S demands a Teflon capacitor (supplied).

Larger capacitors may be substituted to minimize noise, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD363K only) or Teflon (AD363K or S). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Short Cycle Control

A Short Cycle Control (ADC Section, pin 14) permits the timing cycle shown in Figure 5 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (ADC Section, pin 10). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the Status flag resets after the Bit 10 decision (t10 + 400ns in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table 2.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at: (Figure 5)
16	12	0.024	25	t_{12} + 400ns
2	10	0.10	21	t_{10} + 400ns
4	8	0.39	17	t_8 + 400ns

Table 2. Short Cycle Connections

One should note that the calibration voltages listed in Table 4 are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolution.

Digital Output Data Format

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or two's complement binary, depending on whether Bit 1 (ADC Section pin 12) or its logical inverse $\overline{\text{Bit 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the Status flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the Status flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 5. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred at the completion of the conversion period.

Analog Input Voltage Range Format

The AD363 may be configured for any of 3 bipolar or 2 unipolar input voltage ranges as shown in Table 3.

Range	Connect Analog Input To ADC Pin:	Connect ADC Span Pin:	Connect Bipolar ADC Pin 23 To:
0 to +5V	24	25 to 22	—
0 to +10V	24	—	
-2.5V to +2.5V	24	25 to 22	22
-5V to +5V	24	—	
-10V to +10V	25	—	

Table 3. Analog Input Voltage Range Pin Connections

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0	
:	:	:	:	:	:	
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0	
:	:	:	:	:	:	
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0	

Table 4. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

The resulting input-output transfer functions are given by Table 4.

Analog Input Section Offset Adjust Circuit

The offset voltage of the AD363 may be adjusted at either the Analog Input Section or the ADC Section. Normally the adjustment is performed at the ADC but in some special applications, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to Analog Input Section voltage offset and gain was inserted between the Analog Input Section and the ADC. To adjust the offset of the Analog Input Section, the circuit shown in Figure 6 is recommended.

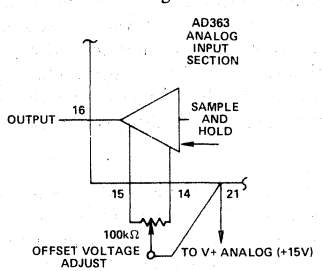


Figure 6. Analog Input Section Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

ADC Offset Adjust Circuit

Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 7 and 8, respectively. The Bipolar Offset, ADC pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator input (ADC pin 22) for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9MΩ resistor to Comparator input (ADC pin 22) for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of 8 x 244 x 10^{-6} x 1200ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor normally contributes no more than 1ppm/°C of FSR offset tempco.

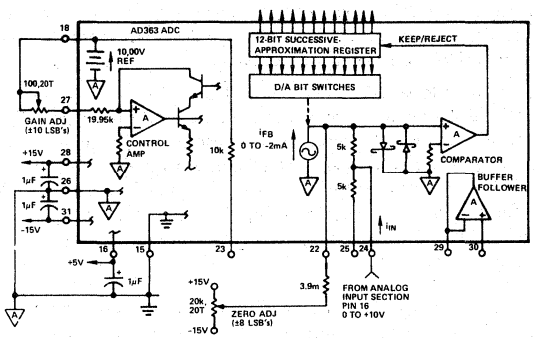


Figure 7. ADC Analog and Power Connections for Unipolar 0 to +10V Input Range

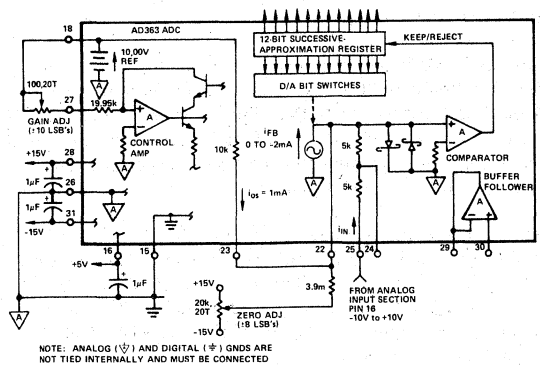


Figure 8. ADC Analog and Power Connections for Bipolar -10V to +10V Input Range

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 9.

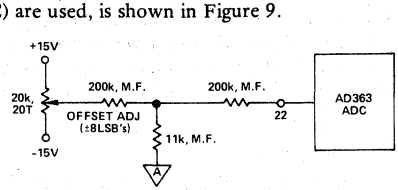


Figure 9. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to ADC pin 22 should be located close to this pin to keep the connection runs short, since the Comparator input (ADC pin 22) is quite sensitive to external noise pick-up.

Gain Adjust

The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input (ADC pin 27) for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco = 100ppm/°C max) types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to ±0.1% of FSR is guaranteed.

Calibration

Calibration of the AD363 consists of adjusting offset and gain. Relative accuracy (linearity) is not affected by these adjustments, so if absolute zero and gain error is not important in a given application, or if system intelligence can correct for such errors, calibration may be unnecessary.

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 7, 8, and 9, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −½FSR for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR −2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

−10V to +10V Range: Set analog input to −9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, −5V to +5V, and −10V to +10V ranges is shown in Table 4. Coding relationships are calibration points for 0 to +5V and −2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and −5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter II-4.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (Analog Input Section pin 17, ADC Section pin 26) and Digital Ground (Analog Input Section pin 2 and ADC Section pin 15) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the system as possible. The cases are connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with both system packages, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 10. This will protect the AD363 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The system will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

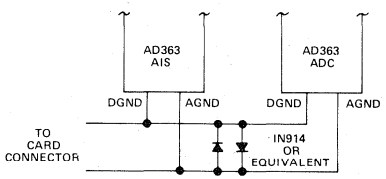


Figure 10. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Applications

The AD363 contains several unique features that contribute to its application versatility. The more significant features include a precision +10V reference, an uncommitted buffer amplifier, the dynamic single-ended/differential mode switch and simple, uncommitted digital interfaces.

Transducer Interfacing

The precision +10V reference, buffer amplifier and mode switch can simplify transducer interfacing. Figure 11 illustrates how these features may be used to advantage.

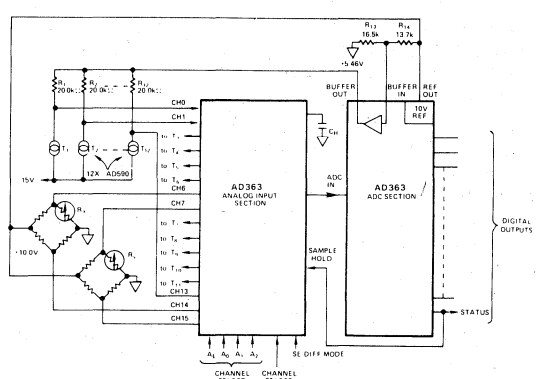


Figure 11. AD363 Transducer Interface Application

The AD590 is a temperature transducer that can be considered an ideal two-terminal current source with an output of one microamp per degree Kelvin (1μA/°K). With an offsetting current of 273μA sourced from the +5.46 volt buffered reference through 20kΩ resistors (R1-R12) each of the 12 AD590 circuits develop -20mV/°C. The outputs are monitored with the AD363 front-end in the single-ended mode (Logic "0" on the Mode Control input). The +5.46 volt reference is derived from the ADC +10 volt precision reference and voltage divider R13, R14. Low output impedance for this +5.46 volt reference is provided by the ADC internal buffer amplifier. (The 10μV/°C offset voltage drift of the buffer amplifier contributes negligible errors.) At 0°C, each temperature transducer circuit delivers a 0 volt output. At 125°C, the output is -2.5V; at -55°C, the output is +1.10V. By using the two's complement ADC output (complemented MSB or sign bit), the negative voltage versus temperature function is inverted and digital reading proportional to temperature in degrees centigrade is provided. Resolution is 0.061°C per least significant bit.

The precision +10 volt reference is also used to power several bridge circuits that require differential read-out. When addressing these bridge transducers, a Logic "1" at the mode control input will switch the AD363 to the differential mode. In many cases, this feature will eliminate the requirement for a differential amplifier for each bridge transducer.

Microprocessor Interfacing

Digital interfacing to the AD363 has been deliberately left uncommitted; every processor system and application has different interface requirements and designing for one specific processor could complicate other applications.

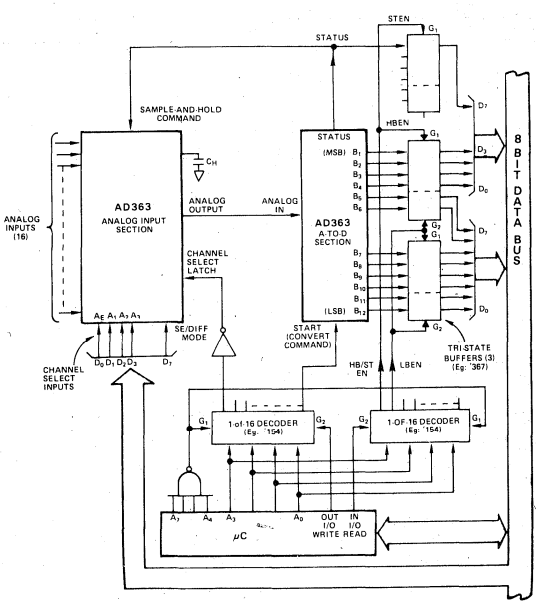


Figure 12. AD363 Microprocessor Interface Application

The addition of a small amount of hardware will satisfy most interface requirements; an example based on 8080-type architecture is shown in Figure 12.

In this system the data bus is used to transmit multiplexer channel selection and convert and read commands to the AD363. It is also possible to address the AD363 as memory using the address bus to perform channel selection, convert and read operations.

The address lines can be decoded to provide channel selection, ADC convert start, status and ADC data (2 bytes) locations. These are accessed with I/O read/write instructions.

The ADC outputs are buffered with tri-state drivers. Figure 12 shows the 4 most significant ADC data bits and status as one byte

FF_H:	STATUS	—	—	—	B1 (MSB)	B2	B3	B4
	D7							D0

and the 8 least significant ADC data bits as the second byte.

FE_H:	B5	B6	B7	B8	B9	B10	B11	B12 (LSB)
	D7							D0

Internal tri-state buffering is not provided because in many applications it would be better to have the first byte contain the 8 most significant bits. To accomodate both left and right justified formats would require more package pins and increase complexity.

The operating sequence for this system is as follows:

1	MVI	80_H	puts the address for channel 0 (including SE/DIFF mode) into accumulator
2	OUT	FF_H	puts 80_H on data bus and FF_H on address bus. Pulses I/O WRITE. OUT FF_H is decoded as a "LOAD ADDRESS" command to the channel select latches.
3	OUT	FO_H	puts FO_H on address bus and pulses I/O WRITE. This is decoded to issue a "CONVERSION START" to the ADC. Accumulator contents are of no significance.
4	IN	FF_H	puts FF_H on address bus and pulses I/O READ. This is decoded to enable the appropriate tri-states, thus putting status and the 4 most significant bits on the data bus.

The status may be examined for "0" (conversion complete). In that case, the 4 MSB's would be read.

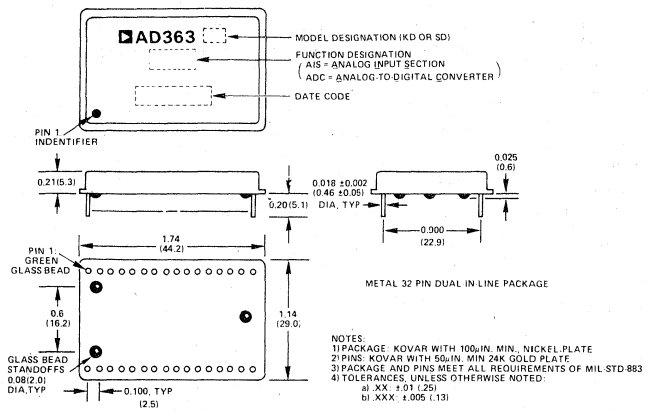
5	IN	FE_H	puts FE_H on address bus and pulses I/O READ. This is decoded to enable the appropriate tri-states, thus putting the 8 least significant bits on the data bus.

At this point, the multiplexer channel selection may be changed and another channel processed with the same instruction set (steps 2 through 5).

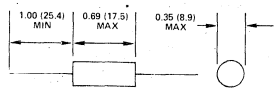
OUTLINE DIMENSIONS
PACKAGE SPECIFICATIONS

Dimensions shown in inches and (mm).

ANALOG INPUT SECTION AND ANALOG-TO-DIGITAL CONVERTER



HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH K GRADE.

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH S GRADE IS 1.00"

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all models of the AD363 receive the following processing:

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	In-house Criteria
2) Stabilization Bake	24 hours @ +150°C
3) Seal Test, Gross Leak	Method 1014 Test Condition C
4) Operating Burn-In	24 hours @ +125°C

PROCESSING TO MIL-STD-883

All models of AD363 ordered to the requirements of MIL-STD-883B, Method 5008 are identified with a /883B suffix and receive the following processing:

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	2017.1
2) Stabilization Bake	1008, 24 hours @ +150°C
3) Temperature Cycle	1010, Test Condition C, 10 cycles, -65°C to +150°C
4) Constant Acceleration	2001, Y1 Plane, 1000G
5) Visual Inspection	Visible Damage
6) Operating Burn-In	1015, Test Condition B 160 hours @ +125°C
7) Seal Test: Fine Leak	1014, Test Condition A, 5 x 10^{-7} std cc/sec
Gross Leak	1014, Condition C
8) Final Electrical Test	Per Data Sheet
9) External Visual Inspection	2009

AD363 ORDERING GUIDE

Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes
AD363KD	0 to +70°C	±30ppm/°C	±20ppm/°C	0 to +70°C
AD363SD	-55°C to +125°C	±25ppm/°C	±10ppm/°C	-55°C to +125°C
AD363SD/883B	Meets all AD363SD specifications after processing to the requirements of MIL-STD-883B, Method 5008.			

NOTE: D Suffix = Dual-In-Line package designator.

Fast, Complete, 16-Channel uP Compatible 12-Bit Data Acquisition System

AD364

ADVANCED TECHNICAL DATA

FEATURES

- Complete Data Acquisition System in 2-Package IC Form
- Full 8- or 16-Bit Microprocessor Bus Interface
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Operation: Nonlinearity ⩽±0.012%
- Guaranteed No Missing Codes Over Specified Temperature Range
- High Throughput Rate: 20kHz
- Fast Successive Approximation Conversion: 25μs
- Buried Zener Reference for Long-Term Stability and Low Gain TC
- Small Size: Requires Only 2.8 Square Inches
- Short-Cycle Capability
- Low Power: 1.4 Watts
- Military/Aerospace Temperature Range: -55°C to +125°C MIL-STD-883 Class B Processing Available

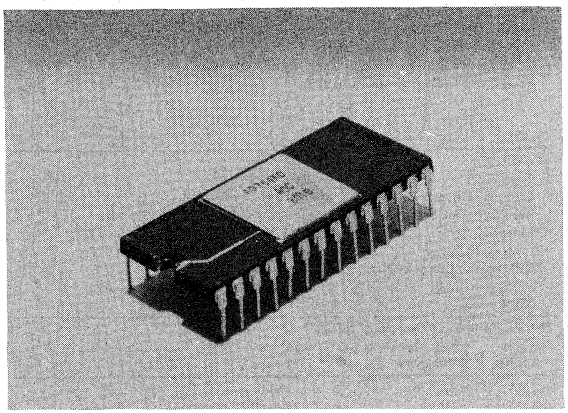
PRODUCT DESCRIPTION

The AD364 is a complete 16 channel, microprocessor compatible, 12-bit data acquisition system in integrated circuit form. The AD364 design is implemented with linear compatible LSI chips, active laser trimming and hybrid technology resulting in maximum performance and flexibility.

The AD364 consists of two separate functional blocks, each in a hermetically sealed dual-in-line package. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD364 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD364 by dynamically switching the input mode control.

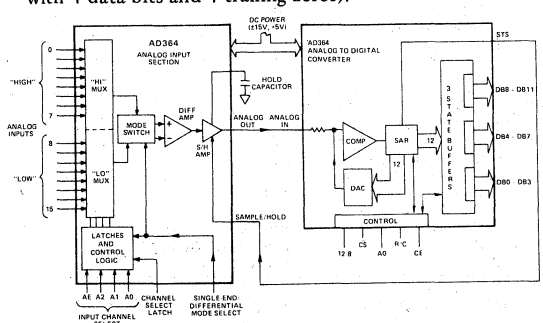
The ADC section contains a complete 12-bit successive approximation ADC, including internal clock, precision 10 volt reference, comparator and bus interface. The ADC uses the newly-developed LCI (Linear-Compatible Integrated Injection Logic) process to provide the low power logic necessary to make a high speed 12-bit ADC and a 3-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus.

The AD364 is available in 4 different grades. The AD364J and K grades are specified for operation over the 0 to +70°C temperature range. The AD364S are not specified for the -55°C to +125°C range.



PRODUCT HIGHLIGHTS

1. The precision laser-trimmed scaling and bipolar offset resistors provide three calibrated ranges; 0 to +10 volts unipolar, or -5 to +5 and -10 to +10 volts bipolar. Typical bipolar offset and full scale calibration errors of ±0.05% can each be trimmed to zero with one external component.
2. The internal buried zener reference is trimmed to 10.00 volts with a ±1% maximum error and 15ppm/°C typical TC. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.
3. The AD364 interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).



AD364 Functional Block Diagram

SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

PARAMETER	AD364J	AD364K	AD364S	AD364T	UNITS
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range					
T_{min} to T_{max}	±10	*	*	*	V
Input (Bias) Current per Channel	±50	*	*	*	nA max
Input Impedance ON Channel	10^{10}/100	*	*	*	Ω/pF
OFF Channel	10^{10}/10	*	*	*	Ω/pF
Input Fault Current	20	*	*	*	mA max
(Power ON or OFF)					(Internally Limited)
Common Mode Rejection					
Differential Mode 1kHz 20Vp-p	70 min (80 typ)	*	*	*	dB
Mux Cross Talk (Any OFF Channel to Any ON Channel) 1kHz					
20V p-p	-80 max (-90 typ)	*	*	*	dB
Offset, Channel to Channel	±5	*	*	*	mV max
ACCURACY					
Gain Error[1]	0.3	0.3	*	**	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error[2]	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024 max	0.012	*	**	% of FSR
T_{min} to T_{max}	0.024 max	0.012	*	*	% of FSR
Noise Error	1mV p-p 0.1Hz to 1MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10V Range)	12	7	*	**	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	25 typ (32 max)	*	*	*	μs
Throughput Rate, Full Accuracy	25 typ (20 min)	*	*	*	kHz
Sample Hold					
Aperture Delay	50 typ (100 max)	*	*	*	ns
Aperture Uncertainty	100 typ (500 max)	*	*	*	ps
Acquisition Time					
To 0.01% of Final Value					
For Full Scale Step	10 typ (18 max)	*	*	*	μs
Feedthrough at 1kHz	-80 typ (-70 max)	*	*	*	dB
Droop Rate	1 typ (2 max)	*	*	*	mV/μs
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single Ended/Differential	"0" Single Ended	*	*	*	
Mode Select	"1" Differential	*	*	*	
	3TTL Loads	*	*	*	
Sample and Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1TTL Load	*	*	*	
ADC SECTION[3] $4.5 \leq V_L \leq 5.5$					
Logic Input Threshold					
T_{min} to T_{max}					
Logic "1"	2.0	*	*	*	V min
Logic "0"	0.8	*	*	*	V max
Logic Input Current					
T_{min} to T_{max}					
Logic "1"	10	*	*	*	μA max
Logic "0"	10	*	*	*	μA max
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current V_{OUT} = 0.4V	1.6	*	*	*	mA min
Source Current V_{OUT} = 2.4V	0.5	*	*	*	mA min
Output Leakage When In					
Three State	±40	*	*	*	μA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset Binary	*	*	*	
POWER REQUIREMENTS					
Supply Voltages/Currents	+15V, ±5% @ 36mA max	*	*	*	
	-15V, ±5% @ 65mA max	*	*	*	
	+5V, ±5% @ 75mA max	*	*	*	

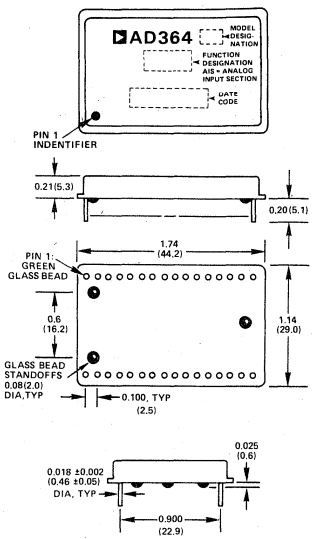
[1] With 50Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2] Adjustable to zero.
[3] See timing diagram for sequence, does not include 12/8 line.
*Specifications same as AD364J.
**Specifications same as AD364K.

Specifications subject to change without notice.

OUTLINE DIMENSIONS
PACKAGE SPECIFICATIONS

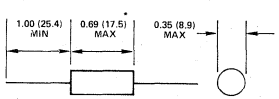
Dimensions shown in inches and (mm).

ANALOG INPUT SECTION



NOTES:
1) PACKAGE: KOVAR WITH 100μIN. MIN., NICKEL PLATE
2) PINS: KOVAR WITH 50μIN. MIN 24K GOLD PLATE
3) PACKAGE AND PINS MEET ALL REQUIREMENTS OF MIL-STD-883
4) TOLERANCES, UNLESS OTHERWISE NOTED:
a) .XX: ±.01 (.25)
b) .XXX: ±.005 (.13)

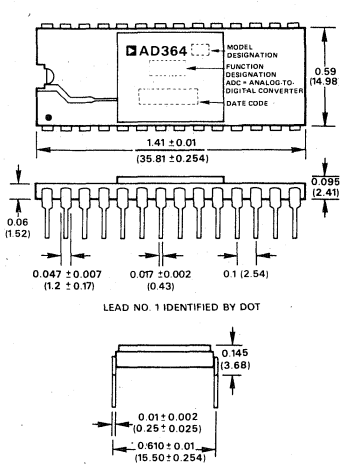
HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH J AND K GRADES.

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH S AND T GRADES IS 1.00".

ANALOG-TO-DIGITAL CONVERTE



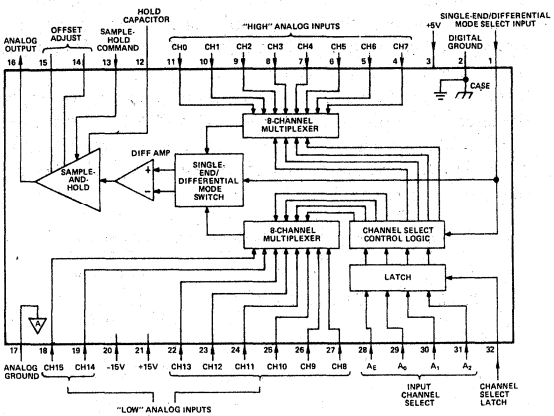


Figure 1. AD364 Analog Input Section Functional Block Diagram and Pinout

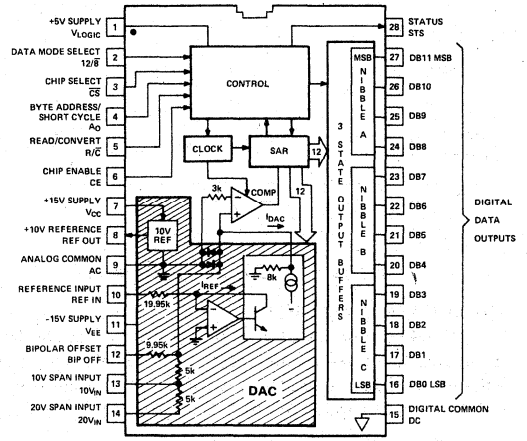


Figure 2. ADC Section Functional Block Diagram and Pinout

SYSTEM TIMING

Figure 3 is a timing diagram for the AD364 connected as shown in the Functional Block Diagram (page 15-25) and operating at maximum conversion rate.

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start Control Sequence is issued to the ADC which in response indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC STS controls the sample-and-hold. When the ADC is "busy" the sample-and-hold is in the hold mode.
4. The ADC goes into its 35 microsecond conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

ADC SECTION FULL CONTROL INTERFACE*

The timing for the standard full control interface is shown in Figure 3. In this operating mode, $\overline{CS}$ is used as the address input which selects the particular device, R/$\overline{C}$ selects between the Read Data and Start Conversion functions, and CE is used to time the actual functions.

The left side of the figure shows the conversion start control. $\overline{CS}$ and R/$\overline{C}$ are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and R/$\overline{C}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold time requirements for $\overline{CS}$ and R/$\overline{C}$ following the rising edge of the start pulse at CE are not observed, the conversion may not be initiated.

The A_0 line determines the conversion cycle length and must be selected prior to conversion initiation. If A_0 is low, a 12-bit cycle results; if A_0 is high, an 8-bit short cycle results. Minimum set-up and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal to the ADC is allowed to vary until the STS goes high. It must then be held steady until STS again goes low at the end of conversion.

The data read function operates in a similar fashion except that R/$\overline{C}$ is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the A_0 line now functions as the byte select address with set-up and hold times as shown. The A_0 line can be switched directly from one byte to the next without recycling the other three control lines. With A_0 low, pins 20 to 27 (DB4 - DB11) come out of three-state and present data. With A_0 high, pins 16–19 (DB0 - DB3) come out of three-state with data and pins 20–23 present active trailing zeros. In the 8-bit mode pins 16–19 will be hard-wired directly to pins 24–27 for direct two-byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low: t_{HD} is the delay until data is no longer valid; t_{HL} is the delay until the outputs are fully into the high impedance state.

TIMING SPECIFICATIONS – FULL CONTROL MODE

t_{DSC}	300ns max	t_{DD}	400ns max
t_{HEC}	300ns min	t_{HD}	100ns min
t_{SSC}	300ns min	t_{SSR}	350ns min
t_{HSC}	200ns min	t_{SRR}	0 min
t_{SRC}	200ns min	t_{SAR}	200ns min
t_{HRC}	200ns min	t_{HSR}	100ns min
t_{SAC}	0 min	t_{HRR}	0 min
t_{HAC}	300ns min	t_{HAR}	100ns min
t_C	15-32μs (12 bit)	t_{HL}	600ns max
	10-20μs (8 bit)	t_{SAL}	20ns min
t_{SHA}	12μs max	t_{SA}	0 min

*For more information on the ADC Section see the AD574.

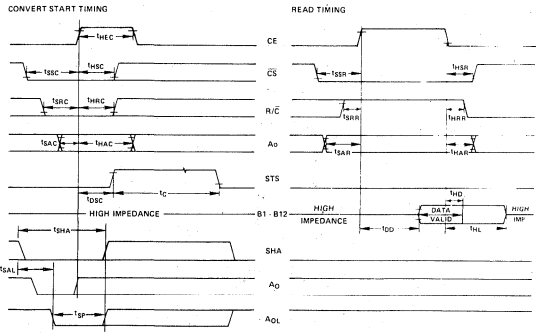


Figure 3. AD364 Timing Diagram

ANALOG INPUT SECTION

The AD364 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "hold mode"). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Analog Input Section, pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexes singly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 1. Input Channel Addressing Truth Table

HOLD CAPACITOR

A Polystyrene hold capacitor is provided with each commercial temperature range system (AD364J, K) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD364S, T). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

AD364 ORDERING GUIDE

Model	Linearity %	Temperature Range
AD364JD	0.024	0 to +70°C
AD364KD	0.012	0 to +70°C
AD364SD	0.024	-55°C to +125°C
AD364TD	0.012	-55°C to +125°C
AD364SD/883B	0.024	-55°C to +125°C
AD364TD/883B	0.012	-55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

(ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	200mV

Low-Cost, High Speed Data Acquisition Module

DAS1128

FEATURES

- **Complete Data Acquisition System**
- **12-Bit Digital Output**
- **16 Single or 8 Differential Analog Inputs**
- **High Throughput Rate**
- **Selectable Analog Input Ranges**
- **Versatile Input/Output/Control Format**
- **Low 3 Watt Power Dissipation**
- **Small 3" x 4.6" x 0.375" Module**

GENERAL DESCRIPTION

The DAS1128 is a complete self-contained miniature high speed data acquisition system. The compact 3" x 4.6" x 0.375" module provides the designer with an easily implemented solution to the data acquisition problem. It contains an analog input signal multiplexer, a sample-and-hold amplifier, a 12-bit A/D converter, and all of the programming, timing and control circuitry needed to perform the complete data acquisition function.

The DAS1128 is a high performance device which can digitize an analog signal to an accuracy of ±½LSB out of 12 bits, relative to full scale. It has ±8ppm/°C gain temperature coefficient, and the maximum throughput rate can be varied from 50,000 conversions/second for a 12 bit conversion from different analog input channels, to 200,000 conversions/second for a successive 4-bit conversion made on a single channel.

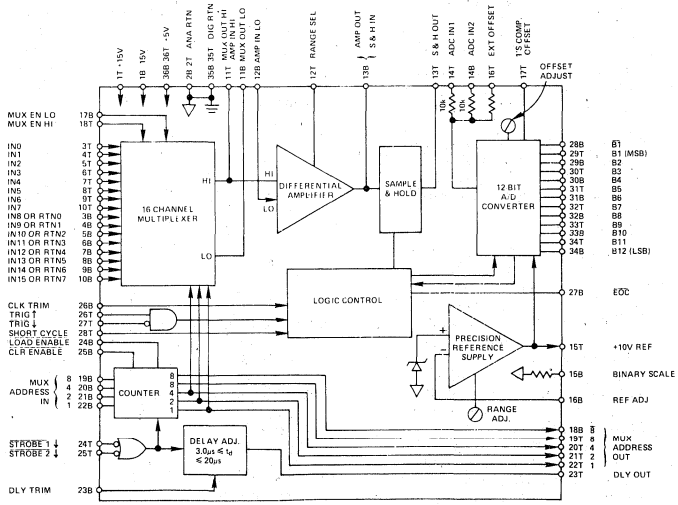


Figure 1. Functional Block Diagram

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

ANALOG INPUTS

Number of Inputs to Multiplexer	16 Single Ended, 8 True-Differential, 16 Pseudo-Differential
Input Voltage (Full Scale Range)	-10V to +10V, 0V to +10V, -5V to +5V, 0V to +5V, -10.24V to +10.24V, 0V to +10.24V, -5.12V to +5.12V, or 0V to +5.12V.
Maximum Input Voltage	±15V
Input Current (per channel)	5nA max
Input Impedance	$>10^{10}$ ohms
Input Capacitance	10pF for "OFF" channel 100pF for "ON" channel
Input Fault Current (power off or MUX failure)	Internally limited to 20mA
Direct ADC Input Impedance	10kΩ for each input line

ACCURACY[1]

Resolution	12 Bits
Error Relative to F.S.	±½LSB
Quantization Error	±½LSB
Differential Nonlinearity Error	
@ 33kHz throughput rate	±½LSB, 1LSB max
@ 50kHz throughput rate	±1LSB
Noise Error	±¼LSB
-FS to +FS Error Between Successive Channel Transitions	±1LSB

TEMP. COEFFICIENTS

Gain	8ppm/°C, 20ppm/°C max
Offset	5ppm/°C, 15ppm/°C max
Differential Nonlinearity	2.5ppm/°C, 6ppm/°C max

SIGNAL DYNAMICS

Throughput Rate (12 Bits)	50kHz (max) (includes 5μs for MUX and SHA settling time plus 15μs for ADC)
MUX Crosstalk ("OFF" channels to "ON" channel)	>80dB down @ 1kHz
Differential Amplifier CMRR	70dB to 1kHz
SHA Acquisition Time to 0.01%	4.5μs max
SHA Aperture Uncertainty	10ns
SHA Feedthrough	70dB down @ 1kHz

DIGITAL INPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels, 1 unit load/line
MUX Address Inputs (8, 4, 2, 1; Pins 19B through 22B)	Positive true natural binary coding selects channel for random addressing mode. Must be stable for 100ns after $\overline{\text{STROBE}}$.
MUX ENABLE HI (Pin 18T)	High (Logic "1") input enables MUX "HI" output (for inputs 0 through 7)
MUX ENABLE LO (Pin 17B)	High (Logic "1") input enables MUX "LO" output (for inputs 8 through 15)
$\overline{\text{STROBE}}$ (Pin 24T or 25T)	Negative going transition (Logic "1" to Logic "0") updates MUX address register. $\overline{\text{STROBE}}$ 1 must be a Logic "1" to enable $\overline{\text{STROBE}}$ 2. $\overline{\text{STROBE}}$ 2 must be at Logic "1" to enable $\overline{\text{STROBE}}$ 1.
$\overline{\text{LOAD ENABLE}}$ (Pin 24B)	High (Logic "1") input allows next $\overline{\text{STROBE}}$ command to sequentially advance MUX address register. Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to update MUX address register according to external address inputs.
$\overline{\text{CLEAR ENABLE}}$ (Pin 25B)	Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to reset MUX address to channel "0" overriding $\overline{\text{LOAD ENABLE}}$.
TRIGGER (Pin 26T)	Positive going transition (Logic "0" to Logic "1") initiates A/D conversion (even during conversion); $\overline{\text{TRIGGER}}$ (Pin 27T) must be at Logic "0" to allow TRIGGER function.
$\overline{\text{TRIGGER}}$ (Pin 27T)	Negative going transition (Logic "1" to Logic "0") initiates A/D conversion; Pin 26T (TRIGGER) must be at Logic "1" to allow $\overline{\text{TRIGGER}}$ function.

DIGITAL OUTPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels; 5 unit loads/line.
Parallel Outputs	$\overline{\text{B1}}$, B1 through B12
Coding	Natural binary, two's complement, offset binary, or one's complement. Pin selectable.
MUX Address Outputs ($\overline{8}$, 8, 4, 2, 1; pins 18B, 19T through 22T)	Positive true natural binary coding indicates channel selected.
DELAY OUT (Pin 23T)	Negative going transition (Logic "1" to Logic "0") occurring normally 5μs (adjustable from 3.0μs to 20μs) after $\overline{\text{STROBE}}$ command initiates A/D conversion automatically when connected to the $\overline{\text{TRIGGER}}$.
$\overline{\text{EOC}}$ (Pin 27B)	High (Logic "1") output during A/D conversion.

ADJUSTMENTS & TRIMS

Offset Adjust	
Internal Adjustment (Externally Accessible)	±10LSB's (min)
Remote External Adjustment (Pin 16T)	±10LSB's (min)
Range Adjust	
Internal Adjustment (Externally Accessible)	±10LSB's (min)
Remote External Adjustment (Pin 16B)	±10LSB's (min)
Clock Trim (Pin 26B)	
Factory Setting (Pin 26B "OPEN")	1.25μs/Bit
External Adjustment Range	1.25μs/Bit to 2.08μs/Bit
Delay Trim (Pin 23B)	
Factory Setting (Pin 23B "OPEN")	3.0μs
External Adjustment Range	3.0μs to 20μs

CONTROLS

SHORT CYCLE (Pin 28T)	Connect to ground for full 12 bit resolution. Connect to B_n output for resolution to B_{n-1} bits.
Channel Selection Mode (MUX Address Loading Mode)	Random, sequential continuous, and sequential triggered. Pin selectable.
A-D Conversion/Channel-Select Sequences	Normal (input channel remains selected during its A/D conversion) and overlap (next channel selected during A/D conversion). Pin selectable.
Range Select (Pin 12T)	Differential Amplifier gain control: connect to ANA RTN (Pin 2T) for X1 gain; connect to AMP OUT (Pin 13B) for X2 gain. This control is used in FSR selection procedure.
BINARY SCALE (Pin 15B)	Connect to REF ADJ (Pin 16B) to set reference to 10.24V. This control is used in FSR selection procedure, see Table II.
OUTPUT CODING (Pin 17T)	Ground for 1's complement output code; connect to -15V dc for other available codes.

POWER REQUIREMENTS

+15V ±3%	40mA, 50mA max
-15V ±3%	70mA, 100mA max
+5V ±5%	250mA, 500mA max
Power Supply Sensitivity[2]:	
Gain	±2.0mV/V
Offset	±4.0mV/V
Ref	±0.5mV/V

ENVIRONMENT & PHYSICAL

Operating Temperature	0 to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	Up to 95% non-condensing
Electrical Shielding	RFI & EMI 6 sides (except connector area)
Packaging	Insulated steel cased module 3.00" x 4.60" x 0.375"

[1] Warmup time to rated accuracy is 5 minutes.
[2] Specification applies only when tracking +15V and -15V supplies are used, and for slowly occuring variations in power supply voltages.

Specifications subject to change without notice.

THEORY OF OPERATION

A block diagram of the DAS1128 is shown in Figure 1. Analog input signals are applied to the various inputs of the 16 channel CMOS multiplexer. This multiplexer in conjunction with the differential amplifier that follows it, can be configured by the user to accept 16 single ended analog inputs, or 8 fully differential analog inputs. It can also be connected as a 16 channel "pseudo-differential" input device, which permits some of the benefits of differential operation while maintaining a 16 channel input capability.

The differential buffer amplifier is gain programmable by the user via jumpers at the module pins. This feature, along with the selectable reference voltages, permits the user to set up the DAS1128 to operate on any of 8 input voltage ranges. The differential amplifier drives a sample-and-hold amplifier, whose function it is to hold the selected analog input signal at a constant level while the A/D converter is making a conversion.

The A/D converter is a high speed 12-bit successive approximation device that has been designed using the Analog Devices' AD562, 12-bit integrated circuit D/A. The reference voltage for the conversion is supplied by an adjustable precision reference circuit that has a temperature coefficient of 5ppm/°C.

In addition to these basic functional blocks, the DAS1128 also contains all of the clock circuitry necessary to perform the complete data acquisition function. The internal clock can be externally adjusted to provide various throughput rates at different accuracies. Input channel addressing logic is provided, as is the capability to short cycle the A/D converter (i.e. perform conversions of less than 12-bits resolution). It is also possible for the user to adjust the time interval between input channel selection and the commencement of a conversion. The user can thus trade off speed vs. accuracy in the settling time of the multiplexer and sample-and-hold amplifier, as well as speed versus accuracy of the A/D converter.

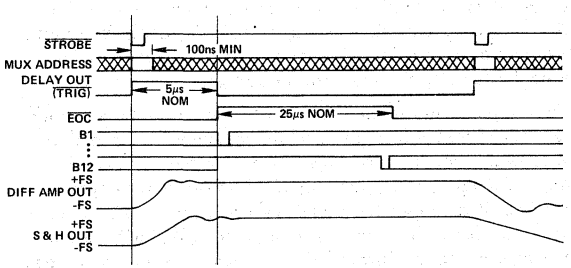


Figure 2. Simplified Timing Diagram, Showing Time-Interval Assignments and Constants

INPUT CONNECTIONS

As shown in Figure 3, three input configurations can be used. 16 single-ended inputs (3a) can be connected to the multiplexer, all referenced to analog gnd. In the second configuration (3b), the inputs are connected individually as 8 true differential pairs. In this case the differential amplifier is connected "Differentially" with the output of the MUX. Finally, a "Quasi-Differential" connection (3c) can be realized under favorable ground path conditions. In this configuration the differential amplifier Lo terminal is used as the ground return for all sensors. In each of these input schemes, it should be noted that the input multiplexer has been designed to protect itself and signal sources from both overvoltage failure and from fault currents due to power-off loading or MUX failure.

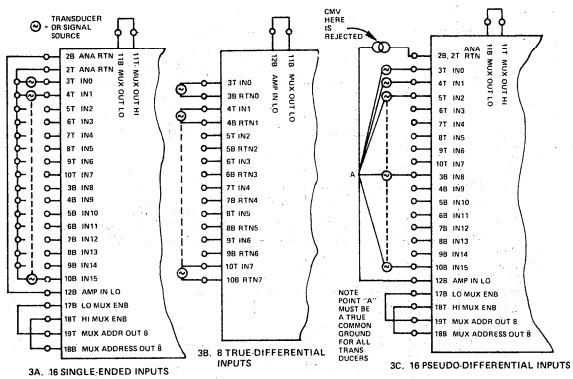


Figure 3. Signal Input Connections for Three Different Configurations

Full scale range of the DAS1128 may be set by appropriate jumper connections for 8 different ranges: 0 to +10V; 0 to +5V; 0 to +10.24V; 0 to +5.12V; -10 to +10V; -5 to +5V; -10.24 to +10.24V; -5.12 to +5.12V.

Note that 10.24 and 5.12 ranges are commonly used since conversion increments become 5mV/bit, 2.5mV/bit, and 1.25mV/bit.

MUX AND S/H DYNAMICS – OVERLAP MODE

The overlap mode is defined as the ability of MUX to accept a new channel address thereby selecting the next channel to be sampled while the previously acquired sample is being held by the S/H for conversion. The dynamic characteristics of the S/H circuit are shown in Figure 4. Maximum throughput rates are obtainable when a single channel is held at a single address and the channel is sampled repeatedly. In a dynamic condition, data-throughput rates obtainable are shown in Figure 5.

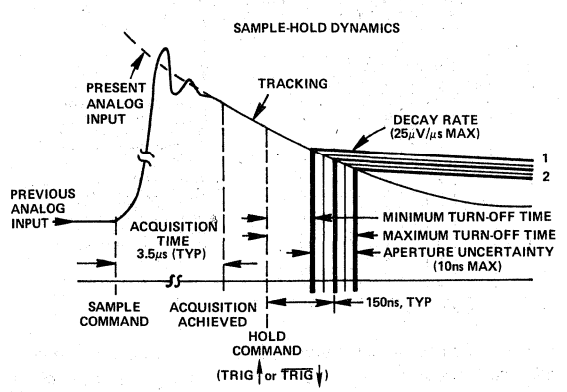


Figure 4. Sample-Hold Parameters Defined and Specified

SHORT CYCLE

It is possible to short cycle the DAC1128, i.e., stop the conversion after less than 12 bits. This can be done by connecting an external jumper between short cycle terminal and one of the output terminals. With shorter cycles the attainable throughput rate increases, see Figure 5. In short cycle operation the $\overline{EOC}$ will decrease proportionately to the number of bits selected. Note the short cycle terminal *must* be grounded for full 12-bit operation.

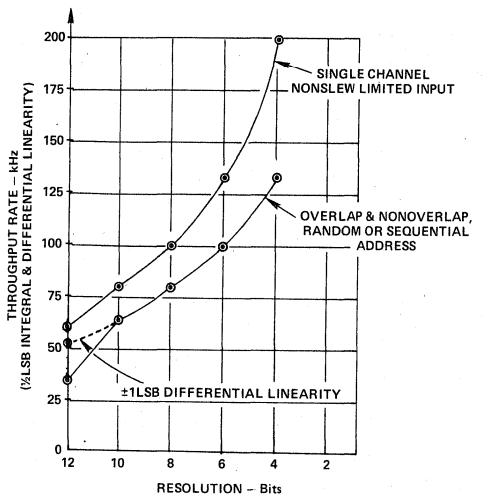
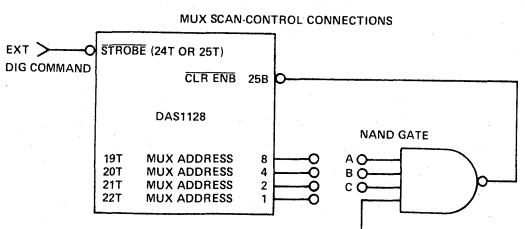


Figure 5. DAS1128 Throughput Rates

MUX ADDRESSING

External terminals have been provided for the address counter. Thus the address counter can be configured to produce the following modes: Continuous sequential scanning (free running), sequential scanning with external step command, abbreviated scan continuously, random channel selection. See Figure 6 and set up procedure for details.



LAST CHANNEL	MUX ADDRESS 8	4	2	1	DIG. GROUND
1	X	X	X	A	X
2	X	X	B	X	X
3	X	X	B	A	X
4	X	C	X	X	X
5	X	C	X	A	X
6	X	C	B	X	X
7	X	C	B	A	X
8	C	X	X	X	X
9	C	X	X	A	X
10	C	X	B	X	X
11	C	X	B	A	X
12	B	C	X	X	X
13	B	C	X	A	X
14	A	C	B	X	X
15	X	X	X	X	A

X = NO CONNECTION

IF $\overline{LOAD\ ENB}$ IS ALSO USED, CONNECT THIS INPUT TO IT (TO 24B). THIS GIVES LOADING PREFERENCE OVER CLEARING.

NOTE: FOR INITIAL CHANNEL = M, CONNECT GATE OUTPUT TO $\overline{LOAD\ ENB}$ (24B) AND CODE CHANNEL IN 8, 4, 2, 1 TO ADDRESS M. HOWEVER, THIS PRECLUDES RANDOM ADDRESSING.

Figure 6. To shorten scanning sequency of multiplexer channels, make the appropriate connections, (as shown in the chart) between an external NAND gate and MUX ADDRESS terminals 19T to 21T

GROUNDING CONSIDERATIONS

Attention should be given to the methods of connection for electrical returns and voltage reference points. Analog return (ANA RTN) and digital return (DIG RTN) are provided. The following rules should be applied when integrating the DAS1128 into the system.

1. If the ±15V power supply is floating (for optimum analog accuracy), connect its return to ANA RTN (Pin 2B or 2T). If the ±15V power supply is *not* floating, connect its return to DIG RTN (Pin 35T or 35B).
2. Connect the +5V supply return to DIG RTN (Pin 35T or 35B). If this supply also powers additional equipment, run separate, parallel returns to the equipment ground and to DIG RTN (Pin 35T or 35B).
3. To minimize signal grounding problems, single-ended input signals should only be returned to ANA RTN (Pin 2B or 2T). If this is not possible, then connect the input signals in either the "true differential" or "pseudo-differential" configurations (see Figure 3).
4. Connect computer ground to DIG RTN (Pin 35T or 35B). Use heavy wire or ground planes.
5. The computer chassis should be connected to the computer and power supply grounds at only one point.
6. Connect the third-wire ground from main ac power input to the computer power supply return.

GAIN AND OFFSET ADJUSTMENTS

The DAS1128 is calibrated with external gain and offset adjustment potentiometers connected as shown in Figure 7 and 8. The offset adjustment potentiometer has an adjustment range of at least ±10LSB's, and the gain range adjustment potentiometer has an adjustment range of at least ±10LSB's.

Offset calibration is not affected by changes in gain calibration, and should therefore be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within ±1/10LSB of the desired value at any point within its range.

These adjustments are not made with zero and full scale input signals, and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the converter to be on the verge of switching between two adjacent digital outputs, the unit can be calibrated so that it does switch at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D converters.

OFFSET CALIBRATION

For unipolar +10V operation set the input voltage precisely to +0.0012V and adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V bipolar operation set the input voltage precisely to -4.9988V; for ±10V units set it to -9.9976V. Adjust the offset

potentiometer, Figure 7, until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching 100000000000 to 100000000001.

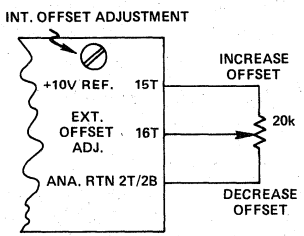


Figure 7. Ext. Offset Adjustment

GAIN CALIBRATION

Set the input voltage precisely to +9.9963V for unipolar operation, +4.9963V for inputs of ±5V or +9.9926V for inputs of ±10V. Note that these values are 1½LSB's less than nominal full scale. Adjust the 20k variable gain resistor, Figure 8, until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.

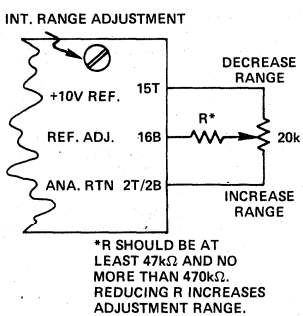


Figure 8. Ext. Ref. Adjustment

CLOCK RATE ADJUSTMENT

The clock rate may be adjusted for best conversion time/accuracy trade-off. The conversion time is varied by means of the external circuitry shown in Figure 9. An open CLK TRIM terminal (Pin 26B) results in 1.25μs/bit nominal conversion time. A grounded CLK TRIM terminal (for highest accuracy) results in 2.08μs/bit conversion.

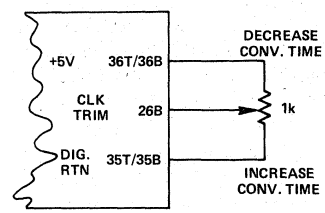


Figure 9. Clock Trim

DELAY TIME ADJUSTMENT

The DLY OUT signal may be adjusted to vary the A/D converter triggering time by means of the external circuitry shown in Figure 10. An open DLY TRIM terminal (Pin 23B) results in a nominal delay time of 3.0μs. A grounded DLY TRIM terminal (for highest-accuracy) results in 20μs delay time nominal.

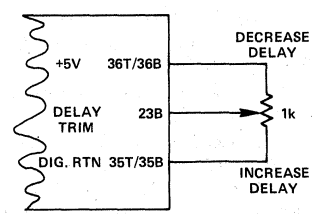


Figure 10. Delay Trim

TABLE I

INPUT CONFIGURATION	ANALOG INPUT CONNECTIONS	ANALOG INPUT RETURN	JUMPER CONNECTIONS
16 Single-Ended Inputs (Figure 3a)	3T thru 10T and 3B thru 10B	All input returns to 2B or 2T	11B to 11T 12B to 2B or 2T 17B to 19T 18T to 18B
8 Differential Inputs (Figure 3b)	3T thru 10T	3B thru 10B	11B to 12B 17B to 18T to "1"
16 Pseudo-Differential Inputs (Figure 3c)	3T thru 10T and 3B thru 10B	Common Input return to 12B	11B to 11T 17B to 19T 18T to 18B

RECOMMENDED SET-UP PROCEDURE

1. Select input configuration, see Table I.
2. Select MUX address mode.
   The method of addressing the multiplexer can be selected by connecting the unit as follows:

   RANDOM. Set Pin 24B ($\overline{\text{LOAD ENB}}$) to Logic "0". The next falling edge of $\overline{\text{STROBE}}$ will load the address presented to Pins 19B through 22B (8, 4, 2, 1). The code on these lines must be stable during the falling edge of $\overline{\text{STROBE}}$ plus 100ns.

   SEQUENTIAL FREE RUNNING. Set to Logic "1", Pin 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 27B ($\overline{\text{EOC}}$) to Pin 24T ($\overline{\text{STROBE 1}}$). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$). Use Pin 26T ($\overline{\text{TRIG}}$) as a run/stop control (i.e., A/D conversion will continue while TRIG is high and will stop while TRIG is low).

   SEQUENTIAL TRIGGERED. Set to Logic "1", Pins 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 24T ($\overline{\text{STROBE}}$) to external triggering source. The multiplexer address register will automatically advance by one channel whenever a $\overline{\text{STROBE}}$ command is received. The initial channel can be selected by setting Pin 24B ($\overline{\text{LOAD ENB}}$) to Logic "0" during only one $\overline{\text{STROBE}}$ command. The multiplexer address will then be determined by the logic levels on Pins 19B through 22B (the external MUX address lines). Channel "0" can be selected as the initial channel by setting Pin 25B ($\overline{\text{CLR ENB}}$) to Logic "0" during only one $\overline{\text{STROBE}}$ command. The final channel can be selected by following the procedure presented in Figure 6.
3. Select A-D conversion/channel select sequence (see Figure 5).
   (1) NORMAL (input channel remains selected during its A/D conversion). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$).
   (2) OVERLAP (next channel is selected during A/D conversion). Connect Pin 27B ($\overline{\text{EOC}}$) to TTL compatible inverter input. Connect inverter output to Pin 24T ($\overline{\text{STROBE}}$). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$). Adjust the delay to at least 4μs greater than $\overline{\text{EOC}}$, 20μs max (see Figure 10). The signal on Pin 26T (TRIG) serves as RUN/STOP control.
   (3) REPETITIVE SINGLE CHANNEL. After selecting the input channel to be repetitively sampled (see MUX ADDRESS MODE, above), set Pin 27T ($\overline{\text{TRIG}}$) to Logic "0". Connect Pin 26T (TRIG) to a triggering source. Conversion process is initiated by positive edge of TRIG command.
4. Select output resolution.
   a. Full 12-bit resolution: connect Pin 28T (SHT CYC) to Pin 35B (DIG RTN).
   b. Bn (Bn < 12) bit resolution: connect Pin 28T to the output pin for Bn + 1.
5. Select optimum throughput rate.
   The system clock frequency and the STROBE to TRIG delay (if used) can be trimmed to optimize the accuracy/throughput rate trade-off. See Figures 9 and 10.
6. Select input voltage full scale range. See Table II.
7. Select output digital coding. See Table III.

TABLE II

FOR FULL SCALE RANGE OF:	MAKE THE FOLLOWING CONNECTIONS
0 to +10V	12T to 2T; 14T to 14B to ADC Source*.
0 to +10.24V	same as 0 to +10V, *plus* 15B to 16B.
0 to +5V	12T to 13B; 14T and 14B to ADC Source*.
0 to +5.12V	same as 0 to +5V, *plus* 15B to 16B
-10V to +10V	12T to 2T; 14T to 15T; and 14B to ADC Source*.
-10.24V to +10.24V	same as -10V to +10V, *plus* 15B to 16B
-5V to +5V	12T to 13B; 14T to 15T and 14B to ADC Source*.
-5.12V to +5.12V	same as -5V to +5V, *plus* 15B to 16B.

*ADC Source is usually Sample and Hold Output (13T), but may be any signal source including Diff. Amp. Output (13B) if Sample and Hold is not desired.

TABLE III

OUTPUT CODE	CONNECTIONS
Unipolar Binary	Connect 17T to -15V Use 29T (B1) for MSB
2's Complement	Connect 17T to -15V Use 28B ($\overline{\text{B1}}$) for MSB
Offset Binary	Connect 17T to -15V Use 29T (B1) for MSB
1's Complement	Connect 17T to 2B Use 28B ($\overline{\text{B1}}$) for MSB

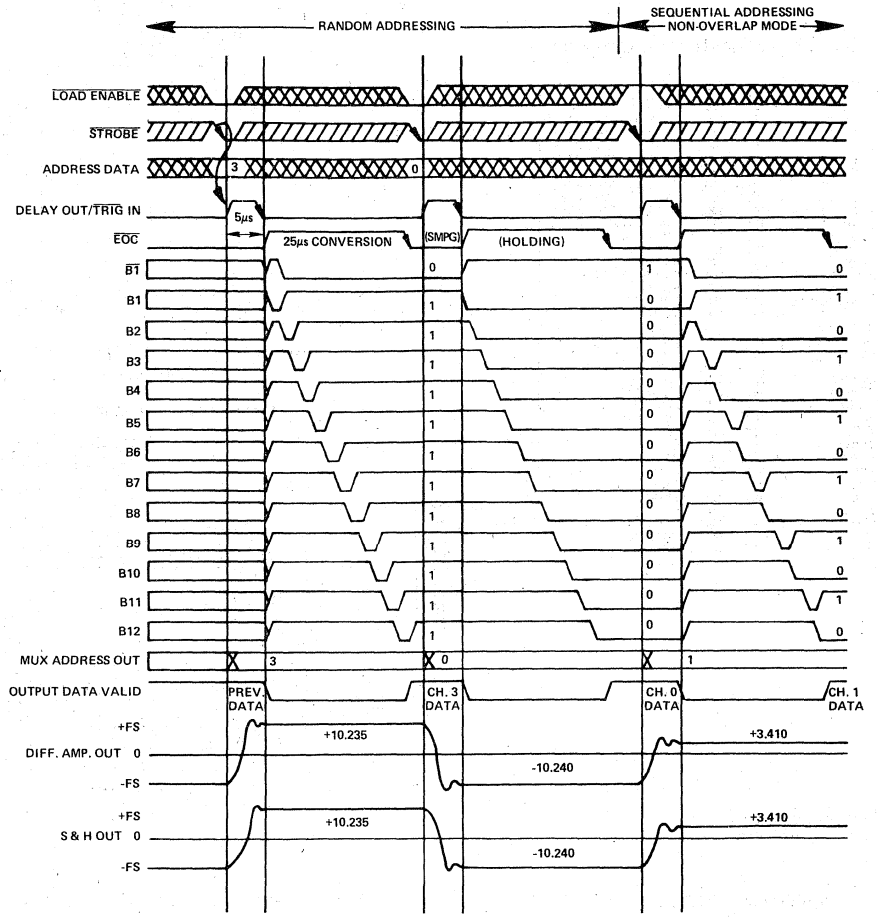


Figure 11. Timing for Non-Overlap Operation in Both Random and Sequential Addressing Modes. For Status Keys and Signal Condition Data, Refer to Box Below.

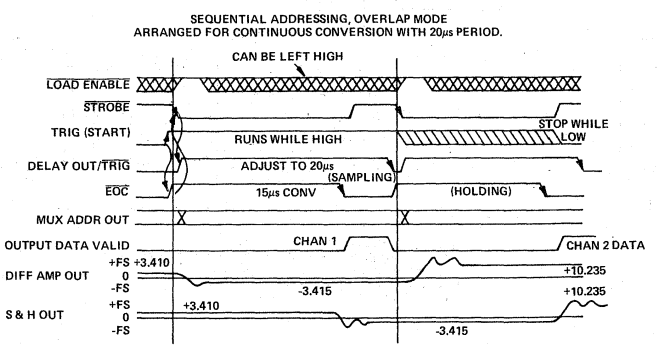


Figure 12. Timing Diagram for Overlap Operation in the Sequential Addressing Mode. For Status Keys and Signal Condition Data, See Box at Right.

SIGNAL CONDITIONS AND STATUS KEYS FOR FIGURES 11 AND 12.

CH. 2 = -3.415V CODE 010 101 010 101
CH. 3 = +10.235V CODE 111 111 111 111
CH. 0 = -10.240V CODE 000 000 000 000
CH. 1 = +3.410V CODE 101 010 101 010

ADC SET UP FOR ±10.24V. INPUT, OFFSET BINARY. (FOR TWO'S COMPLEMENT, USE $\overline{B1}$ FOR M.S.B.)

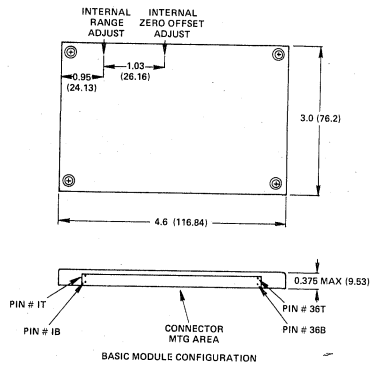
KEY	INPUTS	OUTPUTS
XXX	May change	Don't know
ZZZ	May change 0 to 1	Changes 0 to 1
SSS	May change 1 to 0	Changes 1 to 0
OR	Must be stable	Will be stable

Outline Drawings and Pin Designations

DAS1128 Connector Pin Diagram

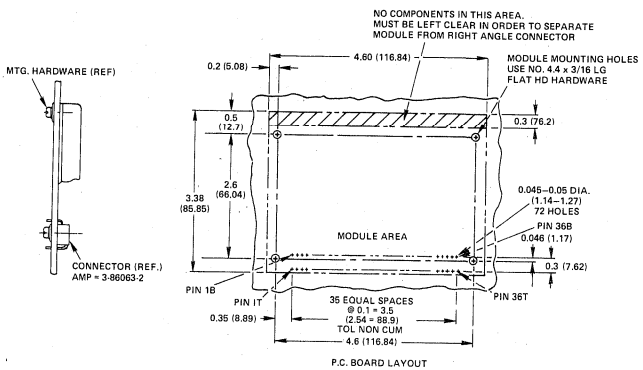
+15V	1T	1B	-15V
ANA RTN	2T	2B	ANA RTN
CH 0 IN	3T	3B	CH 8 IN (CH 0 RTN)
CH 1 IN	4T	4B	CH 9 IN (CH 1 RTN)
CH 2 IN	5T	5B	CH 10 IN (CH 2 RTN)
CH 3 IN	6T	6B	CH 11 IN (CH 3 RTN)
CH 4 IN	7T	7B	CH 12 IN (CH 4 RTN)
CH 5 IN	8T	8B	CH 13 IN (CH 5 RTN)
CH 6 IN	9T	9B	CH 14 IN (CH 6 RTN)
CH 7 IN	10T	10B	CH 15 IN (CH 7 RTN)
MUX HI OUT	11T	11B	MUX LO OUT
RANGE SEL	12T	12B	AMP IN LO
S & H OUT	13T	13B	AMP OUT
ADC IN 1	14T	14B	ADC IN 2
+10V REF	15T	15B	BINARY SCALE
EXT OFFSET	16T	16B	REF ADJ
OUTPUT CODING	17T	17B	ENABLE LO
ENABLE HI	18T	18B	$\overline{8}$ OUT
8 OUT | MUX	19T	19B	8 IN | MUX
4 OUT | ADDRESS	20T	20B	4 IN | ADDRESS
2 OUT | LINES	21T	21B	2 IN | LINES
1 OUT	22T	22B	1 IN
DLY OUT	23T	23B	DLY TRIM
$\overline{\text{STROBE 1}}$	24T	24B	$\overline{\text{LOAD ENB}}$
$\overline{\text{STROBE 2}}$	25T	25B	CLR ENB
TRIG	26T	26B	CLK TRIM
$\overline{\text{TRIG}}$	27T	27B	$\overline{\text{EOC}}$
SHT CYC	28T	28B	$\overline{\text{B1}}$ OUT
B1 OUT	29T	29B	B2 OUT
B3 OUT	30T	30B	B4 OUT
B5 OUT	31T	31B	B6 OUT
B7 OUT	32T	32B	B8 OUT
B9 OUT	33T	33B	B10 OUT
B11 OUT	34T	34B	B12 LSB OUT
DIG RTN	35T	35B	DIG RTN
+5V	36T	36B	+5V

TOP VIEW



BASIC MODULE CONFIGURATION

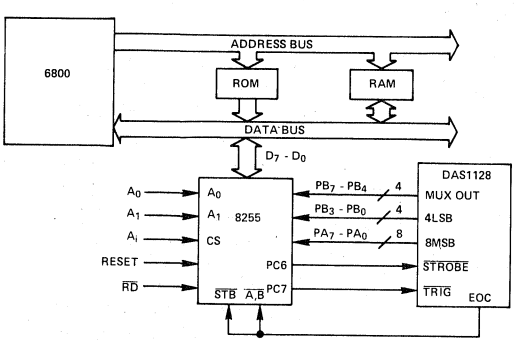
Dimensions shown in inches and (mm).



P.C. BOARD LAYOUT

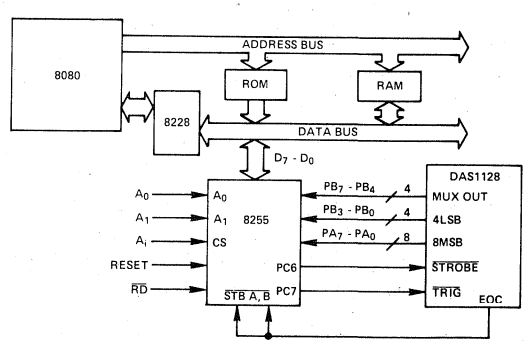
Typical Applications

DAS1128 WITH MOTOROLA 6800



NOTE:
1. 8255 USED IN MODE 1 (STROBED I/O)
2. PC6 INDEXES MUX TO DESIRED CHANNEL
3. CS TO A_i (WHERE, A_i IS AN ADDRESS BIT OTHER THAN A_0 OR A_1)
4. PC7 INITIATES CONVERSION
5. EOC STROBES IN DATA AND MUX INFO
6. 8255 SHOWN, HOWEVER 6820 CAN ALSO BE USED

DAS1128 WITH INTEL 8080



NOTE:
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5. EOC STROBES IN DATA AND MUX INFO

Low Level Input, 12-Bit Data Acquisition Modules

DAS1150, DAS1151

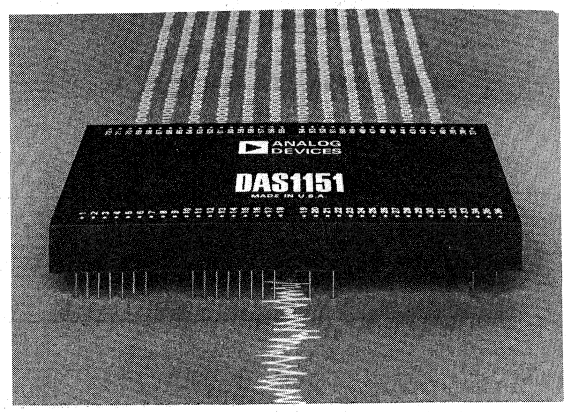
FEATURES

DAS1150

- Resistor-Programmable Gain (1 = 1000V/V)
- High Accuracy with Low Level Input Signals
- Low Cost
- High Throughput Rate and High Gain

DAS1151

- Software-Programmable Gain (1, 2, 4, 8V/V)
- Provides Gain for Signal Conditioning and High Throughput Rate
- Gain Ratio Error: ±0.02% FS max



GENERAL DESCRIPTION

The DAS1150 and DAS1151 are two data acquisition modules designed, built and tested to meet system data acquisition requirements. The designs are comprised of an instrumentation amplifier, sample-hold amplifier and 12-bit successive approximation A/D converter. These products are used on Analog Devices Real Time Interface boards as data acquisition systems to interface with microcomputer boards.

With the DAS1150 and DAS1151, users can apply gain to the instrumentation amplifier for signal conditioning and still achieve high speed data conversion. The difference between models is how the gain is controlled. With the DAS1150, the designer sets the gain from 1 to 1000 V/V with a resistor, R_G. The DAS1151 has gains of 1-2-4-8 that are software-programmable.

DESIGN FEATURES AND USER BENEFITS

The DAS1150 and DAS1151 offer true high-speed 12-bit performance with maximum overall error at unity gain of ±1 least significant bit (LSB). This performance is guaranteed at a 25kHz throughput rate. There is very little performance lost at high gains. For example, at gain of 1000, the DAS1150 has a throughput of 13kHz and an overall accuracy of ±2LSB. The DAS1151 with its software-programmable gain provides dynamic range expansion through subranging as well as the flexibility of using different gain settings to accommodate different input signal levels. The resistor-programmable-gain DAS1150 may be used for input ranges from 10mV full scale to ±10V full scale with very little loss of speed and no degradation of linearity at high gains.

THEORY OF OPERATION

Block diagrams of the DAS1150 and DAS1151 are shown in Figures 1 and 2. Analog input signals are applied to the input of the instrumentation amplifier. The instrumentation amplifier is gain-programmable by the user via a resistor (DAS1150) or TTL/CMOS logic (DAS1151). This feature permits the user to operate the module on any input voltage range from ±10mV to ±10V with the DAS1150 or any of 4 input voltage ranges with the DAS1151. The instrumentation amplifier drives a sample-hold amplifier, whose function is to hold the selected analog input signal at a constant level while the A/D converter is making a conversion.

The A/D converter is a high speed 12-bit successive approximation device that has been designed using Analog Devices AD562 integrated circuit D/A converter with a precision reference source, a high speed comparator and successive approximation logic; the laser trimmed AD562 which contains precision current switches and a very stable thin film resistor network provides excellent performance over temperature.

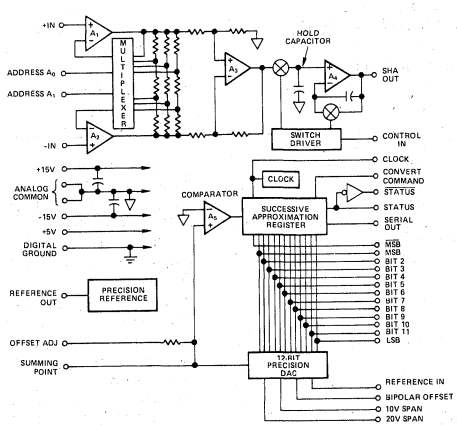


Figure 1. DAS1151 Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise noted)

MODELS	DAS1150	DAS1151
RESOLUTION	12 Bits	*
DYNAMIC CHARACTERISTICS		
ADC Conversion Time	25μs max	*
IA Settling Time, 20V Input Step		
to 0.01% @ G = 1	15μs max	(G = 1-8) 10μs max
to 0.01% @ G = 10	15μs	N.A.
to 0.05% @ G = 1000	50μs	N.A.
Throughput Rate G = 1	25kHz	(G = 1-8) 28.5kHz
G = 10	25kHz	N.A.
G = 1000	13.3kHz	N.A.
Sample-Hold		
Aperture Delay Time	90ns	*
Aperture Time	20ns	*
Aperture Uncertainty Time	5ns	*
Droop Rate	2mV/s	*
ACCURACY		
Overall Error @ G = 1	±1LSB max	*
@ G = 1000	±2LSB max	(G = 8) ±2LSB max
Nonlinearity Error	±1/2LSB (±1LSB max)	*
Offset Error	Adjust to Zero	*
Gain Error	Adjust to Zero	*
TEMPERATURE COEFFICIENTS		
Offset (RTI)	$\pm\left(1+\frac{50}{G}\right)\mu V/^{\circ}C$	±30μV/°C
Gain (RTI)	±20ppm of Reading/°C	*
Differential Nonlinearity	2ppm/°C	*
ANALOG INPUTS		
Voltage Input Range $\left(\frac{\text{ADC FS}}{\text{GAIN}}\right)$	10mV to ±10V	0.625V to ±10V
ADC Input Ranges	0 to +5V	*
	0 to +10V	*
	±2.5V	*
	±5V	*
	±10V	*
Instrumentation Amplifier		
Gain	Resistor-Programmable	Software-Programmable
Gain Range	1 to 1000	1, 2, 4, 8
Gain Equation	$G = 1 + \left(\frac{20k\Omega}{R_G}\right)$	See Table 4
Gain Ratio Error	N.A.	±0.02% FS max
Input Impedance	$10^8\Omega$	*
Bias Current	20nA	2nA
Offset Current	2nA	500pA
Offset Voltage (RTI)	±50μV	±200μV
DIGITAL INPUTS		
ADC Convert Command	Positive Pulse, TTL Compatible, 100ns min Width	*
SHA Mode Control	Positive Pulse TTL Compatible Logic "1" = Hold, Logic "0" = Sample	*
PGA Gain Control	N.A.	TTL Compatible, Positive True
DIGITAL OUTPUT		
Parallel Data Output	6TTL Loads/Bit	*
Unipolar	Positive True Binary	*
Bipolar	Positive True Offset Binary or Two's Complement	*
Serial Data Output	6 TTL Loads	*
Unipolar	Positive True Binary NRZ Format, MSB First	*
Bipolar	Positive True Offset Binary, NRZ Format, MSB First	*
Status Output	Logic "1" During Conversion, TTL Compatible, 4TTL Loads, Complement also Available	*
Clock Output	480kHz, TTL Compatible, 6TTL Loads	*
POWER REQUIREMENTS[1]	+5V dc ±5% @ 130mA (170mA max)	*
	±15V dc ±3% @ 30mA (40mA max)	*
	±15V dc ±3% @ 30mA (40mA max)	*
TEMPERATURE RANGE		
Operating	0 to +70°C	*
Storage	-55°C to +85°C	*

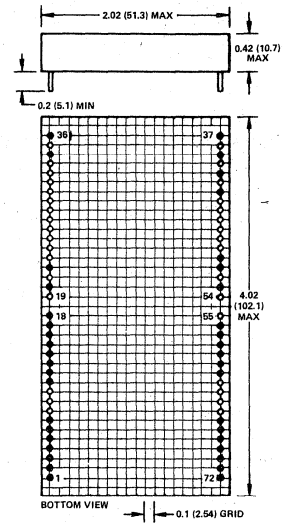
*Specifications same as model DAS1150.

[1] Recommended power supply, model 923, ±15V @ ±100mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

SEE TABLE BELOW FOR PIN DELETIONS.

MODULE WEIGHT: 3.5 OUNCES (99.3 GRAMS). ALL PINS ARE GOLD PLATED HALF-HARD BRASS (MIL-G-45204), 0.019" ±0.001" (0.48 ±0.03mm) DIA.

MODEL	DELETED PINS
DAS1150	PINS 50, 51
DAS1151	PINS 41, 43

MATING SOCKET: AC1577
(4 Required)

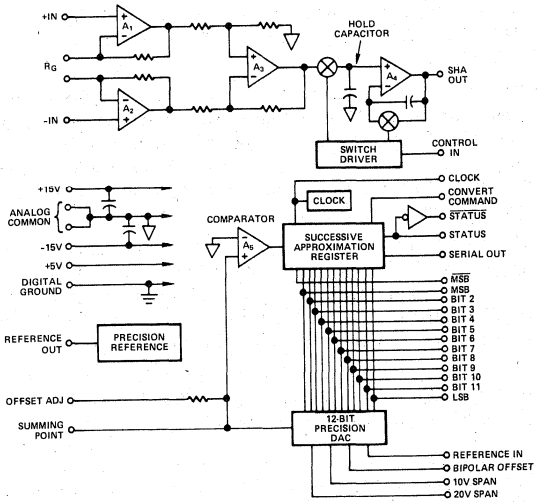


Figure 2. DAS1150 Block Diagram and Pin Designations

GROUNDING PRACTICE

Attention should be given to the methods of connection for electrical returns and voltage reference points. Analog ground and digital ground are provided. These data acquisition systems do not have an internal connection between analog ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops between the high current carrying logic supply ground and the sensitive analog circuit sections.

1. If the ±15V power supply is floating (for optimum analog accuracy), connect its common to analog ground. If the ±15V power supply is not floating, connect its common to digital ground.
2. Connect the +5V supply common to digital ground. If this supply also powers additional equipment, run separate, parallel returns to the equipment ground and to digital ground.
3. Single-ended input signals should only be returned to analog ground. If this is not possible, then connect the input signals in the differential configuration.
4. Connect computer ground to digital ground. Use heavy wire or ground planes.
5. The computer chassis should be connected to the computer and power supply grounds at only one point.
6. Connect the third wire ground from main ac power input to the computer power supply return.
7. Bias return path should always be provided.

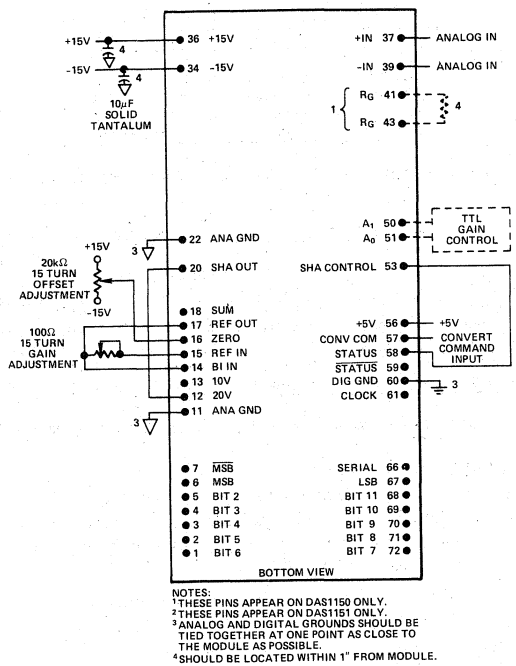


Figure 3. Module Connections for ±10V Range

Figure 3 shows the connections required to operate the DAS1150 or DAS1151 with a ±10V input range. Table 1 shows connections for ADC input ranges.

Input Range	Jumper
0 to +5V	Pin 20 to Pin 13, Pin 12 to Pin 18
±2.5V	Pin 20 to Pin 13, Pin 12 to Pin 18 Pin 17 to Pin 14
0 to +10V	Pin 20 to Pin 13
±5V	Pin 17 to Pin 14, Pin 20 to Pin 13
±10V	Pin 17 to Pin 14, Pin 20 to Pin 12

Table 1. ADC Input Range Connections

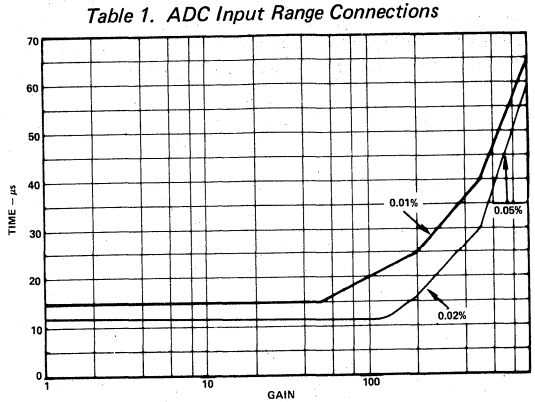


Figure 4. Typical Settling Time Curves for DAS1150

GAIN AND OFFSET ADJUSTMENT PROCEDURE

ADC ANALOG INPUT		DIGITAL OUTPUT
+5V RANGE	+10V RANGE	BINARY CODE
+4.9988V	+9.9976V	111111111111
+2.5000V	+5.0000V	100000000000
+0.6250V	+1.2500V	001000000000
+0.0012V	+0.0024V	000000000001
+0.0000V	+0.0000V	000000000000

Table 2. Nominal Unipolar Input-Output Relationships

ADC ANALOG INPUT			DIGITAL OUTPUT	
±2.5V RANGE	±5V RANGE	±10V RANGE	OFFSET BINARY CODE	TWO'S COMPLEMENT CODE
+2.4988V	+4.9976V	+9.9951V	111111111111	0111111111111
+1.2500V	+2.5000V	+5.0000V	100000000000	0100000000000
+0.0012V	+0.0024V	+0.0049V	000000000001	0000000000001
+0.0000V	+0.0000V	+0.0000V	000000000000	0000000000000
-2.5000V	-5.0000V	-10.0000V	000000000000	1000000000000

Table 3. Nominal Bipolar Input-Output Relationships

OFFSET CALIBRATION

For unipolar mode set the input voltage precisely to the value of 1LSB (see Table 2) and adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For bipolar mode set the input voltage precisely to zero volts. Adjust the offset potentiometer until the offset binary coded units are just on the verge of switching from 011111111111 to 100000000000 and two's complement coded units are just on the verge of switching 111111111111 to 000000000000.

GAIN CALIBRATION

The analog input values given in Tables 2 and 3 are values that should be present at the input to the internal ADC. The value of the analog input will be affected by the gain of the module, i.e., $\text{ANALOG IN} = \left(\frac{\text{ADC FULL SCALE}}{\text{GAIN}}\right)$

Set the ADC input voltage precisely to plus full scale minus 1 1/2 LSB's: +4.9982V for 5V units, +9.9963V for ±10V units, +2.4982V for ±2.5V units, +4.9963V for ±5V units, or +9.9926V for ±10V units. Adjust the 100Ω variable gain resistor until binary and offset binary coded units are just on the verge of switching from 111111111110 to 111111111111 and two's complement coded units are just on the verge of switching from 011111111110 to 011111111111.

TIMING

The "0" to "1" transition of the CONVERT COMMAND input resets the MSB output to Logic "0" and the CLOCK STATUS, MSB, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the CONVERT COMMAND returns to Logic "0", at which time the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's (D/A) output is compared with the analog input (SHA OUT). If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 12 (LSB) comparison is completed. At this time the STATUS output returns to Logic "0" and the conversion cycle ends.

The SERIAL DATA output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, 40ns after each of the twelve "0" to "1" clock transitions.

AMPLIFIER GAIN

The DAS1150 instrumentation amplifier gain may be set to any any value between 1 and 1000 by connecting an external gain resistor between pins 41 and 43. The resistance is determined by the formula $G = 1 + \left(\frac{20k\Omega}{R_G}\right)$. R_G should be located as close as possible to the module pins. It must be noted that the TC of R_G directly affects the gain temperature coefficient of the DAS1150. A high quality metal film resistor 0.1% is recommended.

The gain of the DAS1151 is programmed by loading the proper code into the gain address, as shown in Table 4.

ADDRESS INPUTS		DAS1151
A_1	A_0	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

Table 4. DAS1151 Gain State Truth Table

Microcomputer Interface Boards

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Selection Guide
Microcomputer Interface Boards

Analog Devices Real-Time Interfaces make possible direct memory-mapped interfacing between popular microcomputers and analog I/O signals. For each computer, input-only, output-only, and combination input/output cards are available, with a variety of inherent features and options to extend their usefulness.

The chart below provides selection information in capsule form, matching cards to features. Additional information and specifications are provided on the individual card/family data sheets.

	MULTIBUS INTEL SBC-80			MICROMODULE MOTOROLA			TM-990 TEXAS INSTRUMENTS				PRO-LOG 4 1/2" × 6 1/2"		STD BUS	D.E.C. LSI-11/2		
	RTI-1200	RTI-1201	RTI-1202	RTI-1230	RTI-1231	RTI-1232	RTI-1240	RTI-1241	RTI-1242	RTI-1243	RTI-1220	RTI-1221	RTI-1225	RTI-1250	RTI-1251	RTI-1252
INPUT																
Input Protection	●		●	●	●		●	●			●		●	●	●	
16 Channels	●		●	●	●		●	●			●		●	●	●	
32 Channels	●		●	●	●		●	●						●		
0-20mA Inputs	●		●	●	●		●	●			●			●	●	
10mV to 10V FS			●	●	●		●	●			●			●	●	
Programmable Gain	●			●	●		●	●						●		
8-Bit ADC			●	●	●						●					
12-Bit ADC	●		●	●	●		●	●			●			●	●	
10-Bit ADC													●			
OUTPUT																
2 Channels	●	●			●			●					●		●	●
4 Channels		●				●			●			●				●
8 Channels										●						
4-20mA Outputs	●	●				●		●								●
8-Bit DAC												●	●			
10-Bit DAC												●				
12-Bit DAC	●	●			●	●		●	●	●					●	●
DAC Data Readback		●							●	●						
Remote Load Sensing	●	●			●	●			●	●			●		●	●
4 Quadrant Multiplication					●	●						●			●	
Digital Logic Outputs	●	●				●			●	●						●
COMMON FEATURES																
Single +5V Power	●	●	●	●		●	●	●	●	●			●	●	●	●
Memory Mapped Interface	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Wire Wrap Feature Selection	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Selection																
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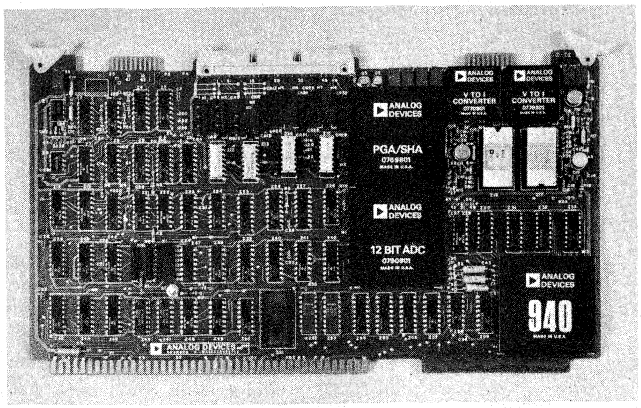
MULTIBUS
Intel Compatible
Combination Analog I/O Subsystem
MODEL RTI-1200

FEATURES
- **Complete Analog I/O Subsystem**
- **Intel SBC-80/10, 80/20, and MDS Compatible**
- **Memory Mapped I/O Interface**
- **Data Acquisition:**
  - **Up to 32 Input Channels**
  - **Sample and Hold Amplifier**
  - **Programmable Gain Amplifier**
  - **12-Bit A/D Converter**
  - **Input Fault Protection**
- **Real-Time Pacer Clock System**
- **On-Board PROM Socket**
- **Two Optional 12-Bit DAC's**
- **Optional 4-20mA Current Outputs**
- **Optional Single +5V Power**
- **Memory Overlay – RAM and ROM Inhibit**



GENERAL DESCRIPTION

The RTI-1200 is a complete analog input/output subsystem that greatly simplifies the task of interfacing analog signals to Intel SBC-80 Single Board Computers, or other 8080-based microcomputers. It is functionally, electrically, and mechanically compatible with the SBC-80, and all connections to it are made simply by plugging the RTI-1200 into a slot in a card cage that also contains an SBC-80. The RTI-1200 can also be readily interfaced to other 8080-based microcomputers whose address, data, and control busses are accessible.

The RTI-1200 is interfaced to an SBC-80 or other 8080 based microcomputer as a block of contiguous memory locations. It combines on a single printed circuit card many features and capabilities which reduce the hardware required to interface analog signals to a microcomputer, and significantly ease the programming effort associated with inputting and outputting analog signals.

DATA ACQUISITION

The RTI-1200's most basic function is data acquisition. This is accomplished with an analog input multiplexer, a programmable gain amplifier, a sample-and-hold amplifier, and a 12-bit A/D converter. The standard RTI-1200 offers either 16 single ended or 8 differential input channels (user selected). An optional multiplexer expander allows for up to 32 single ended or 16 differential input channels. All of the analog inputs are fully protected up to ±28 volts, and additional protection against larger, potentially destructive overloads is afforded by fusing resistors located at the inputs.

The RTI-1200's A/D Converter can be configured by the user to accept 0 to +10V, ±5V, or ±10V full scale input signals. A programmable gain amplifier preceding the A/D converter has software selectable gains of 1, 2, 4 and 8. This expands the dynamic range of the A/D converter to 15 bits, and results in greater input sensitivity. For example, when operating on the 0 to +10V input range with a programmable gain amplifier gain of 8, the actual input range is 0 to +1.25V. The programmable gain amplifier allows the user to program different gains for different input channels, or to have different gains for varying input levels on the same channel. It is even possible to write software to implement automatic gain ranging operation.

Eight of the input channels have provisions for resistors provided by the user that allow the inputs to accept 4-20mA current loop signals. Output data from the A/D converter is in natural binary code for unipolar input ranges, and at the user's option can be either offset binary or two's complement coding when using bipolar input ranges. A special feature of the RTI-1200's data acquisition operation is that the controlling microcomputer's CPU (i.e., the 8080) is not tied up while a conversion is taking place. This significantly enhances system throughput capability and flexibility, as the CPU is free to pursue other tasks while an A/D conversion is in progress.

ANALOG OUTPUTS

The RTI-1200 has provisions for two optional 12-bit D/A converters which are software driven via double buffered registers. They can be used for such functions as driving an analog recorder, or generating analog control signals. Both D/A converters can be user set to any of five voltage output ranges. The D/A input data is natural binary for unipolar output ranges, and at the user's choice can be offset binary or two's complement for bipolar output ranges. Both analog output channels can also be optionally equipped with 4-20mA current loop outputs. This permits them to drive directly the 4-20mA control loops often used in process and industrial controls.

SPECIFICATIONS (typical @ +25°C and with +5V and ±15V, unless otherwise noted)

DATA ACQUISITION

Number of Analog Inputs	
Standard	16 Single-Ended or 8 Diff.
With Multiplexer Expander[1]	32 Single-Ended or 16 Diff.
Multiplexer Switching Characteristics	Break-Before-Make. All Switches Open When Power is Off.
Input Voltage Ranges[2]	0 to +10V, ±5V, ±10V
Programmable Gains[3]	1, 2, 4, 8 Software Selectable
Input Impedance	$>10^9$ Ohms
Input Bias Current	
at +25°C	5nA
over 0 to +70°C	50nA
Diff. Input Bias Current	
at +25°C	3nA
over 0 to +70°C	3.5nA
Input Overvoltage Protection	
Continuous Overvoltage	±28 Volts maximum
Overvoltage >±28V	Fusing Resistors
Accuracy	
Resolution	12 Bits
Nonlinearity Error[4]	±1/2LSB typ, ±1LSB max
Diff. Nonlinearity Error	±1/2LSB typ, ±1LSB max
Quantization Error	±1/2LSB max
Input Offset Voltage[5]	Adjustable to Zero
Gain Error[5]	Adjustable to Zero
CMRR	75dB min
CMV	±10V
Noise Error[6]	±1/2LSB max
Temperature Coefficients	
Gain	±15ppm/°C typ, ±25ppm/°C max
Offset	±25μV/°C Referred to Input
Diff. Nonlinearity	±3ppm/°C max
Settling Time to ±0.01%[7]	10μs max at any Gain
SHA Aperture Time	90ns
SHA Aperture Width	20ns
SHA Aperture Uncertainty	±5ns
Conversion Time	25μs max
Maximum Throughput Rate[8]	28kHz

ANALOG OUTPUTS

Number of DAC Channels[9]	2
Accuracy	
Resolution	12 Bits
Nonlinearity Error[4]	±1/2LSB
Diff. Nonlinearity Error	±1/2LSB
Voltage Output Characteristics	
Voltage Output Ranges[2]	±2.5V, 0 to +5V, ±5V, 0 to +10V, ±10V
Output Current	5mA min @ ±10V
Settling Time [10]	10μs max
Gain TC	±8ppm/°C typ, ±15ppm/°C max
Offset TC	±5μV/°C typ, ±20μV/°C max
Current Loop Characteristics[11]	
Current Output Range	4 to 20mA
Load Resistance Range	0 to 500Ω
Loop Supply Voltage	+15V to +30V
Settling Time [12]	50μs max
Gain TC	±10ppm/°C typ, ±25ppm/°C max
Offset TC	±0.4μA/°C
Reference Voltage Output	+5.00V ±0.02% @ 5mA max

REAL-TIME PACER CLOCK SYSTEM

Modes of Operation	Pacer-Timed Conversion Trigger, Pacer-Timed Interrupt, Pacer Off
Types of Clocks	Variable Frequency R-C, Fixed Frequency Crystal, External
Crystal Clock Freq. [13]	Determined by User Supplied Crystal
Variable Freq. Clock Range	30Hz to 30kHz, User Adjustable

LOGIC DRIVER OUTPUTS

Number Available	2
Characteristics	Open Collector, 30V max, 300mA max Continuous Sink Current per Output

MICROCOMPUTER INTERFACE

Compatibility	Completely Compatible with Intel SBC-80/10, SBC-80/20, and MDS Bus System
Type of Interface	Interfaces as a Block of Memory Locations, Using Address, Data and Control Busses.
Position in Memory	User Selectable Among any of 14 Possible Locations.
On-Board PROM	Socket for Intel 2708 or Equivalent 1024 Byte x 8 Bit PROM, of which 1008 Bytes are Usable.
Memory Overlay (Inhibit)	RAM or ROM

POWER REQUIREMENTS[14, 16]

Without DC/DC Option[15]	+15V ±3% @ 40mA -15V ±3% @ 40mA +5V ±5% @ 1.2A
With DC/DC Option	+5V ±5% @ 1.7A

TEMPERATURE RANGE

Operating	0 to +70°C
Storage	-55°C to +85°C

MECHANICAL 6.75″ x 12.00″ with 0.6″ Board-to-Board Spacing (171.5 x 304.8 x 15.24mm)

NOTES

[1] The multiplexer expander is an option, and is shown in the ordering guide as MUX EXP.
[2] The desired range is user selectable with straps.
[3] The input gain of a channel is multiplied by the gain setting of the programmable gain amplifier (e.g., the input range of the 0 to +10V range when using a gain of 8 is 0 to +1.25V).
[4] Defined as deviation from a straight line passing through the end points of the range.
[5] For any one software programmable gain setting. Maximum offset shift of ±1LSB or gain shift of ±0.02% when using a programmable gain setting other than the one used during calibration.
[6] When using a programmable gain setting of 1. It is ±1.5LSB max when using a programmable gain setting of 8.
[7] For a 20V step. This specification is valid for a step change on one input, or following a channel change, or following a programmable gain change, or simultaneous changes involving any combination of these changes.
[8] Based on a 10μs settling time, followed by a 25μs A/D conversion time. Overall system throughput rate is enhanced because the CPU is not held up during conversions.
[9] Two channels of D/A converters and two channels of current loops are available on an option basis. See Ordering Guide.
[10] To ±0.01% of full scale range following a 20V step.
[11] The current loop characteristics include the effects of the driving D/A converter.
[12] To ±0.02% of full scale current following a full scale step.
[13] Space provided for HC-18/U crystal cut for a frequency of up to 50MHz. User can select to divide crystal frequency by 10^3 or 10^4 on-board the RTI-1200.
[14] Power requirements shown are for an RTI-1200 with no DAC or current loop options.
[15] The DC/DC power converter is an option that converts +5VDC power to ±15V. It is shown in the ordering guide as DC/DC.
[16] +12V and -5V power is required only if optional PROM is used. This power is supplied by the SBC bus.

Specificatons subject to change without notice.

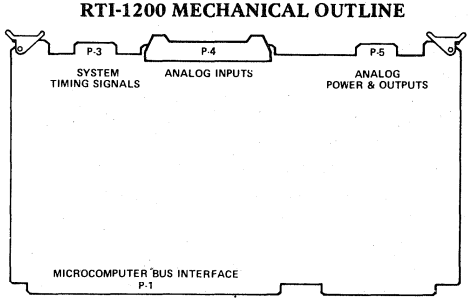
RTI-1200 ORDERING GUIDE

MODEL NUMBER	MUX EXP	DACS
RTI-1200-001		
-004		X
-011	X	
-014	X	X

ACCESSORIES	
0A08	4-20mA V/I Module
0A09	DC/DC Converter

X DENOTES OPTIONS INCLUDED WITH THE CORRESPONDING MODEL NUMBER. THE OPTIONS ARE DESCRIBED IN NOTES 1, 9, AND 15.

RTI-1200 MECHANICAL OUTLINE



MATING CONNECTORS FOR RTI-1200

PART NO.	MATES TO	DESCRIPTION
AC1551	P3 or P5	Flat Cable Connector 20 Pin, 0.1″ Center
AC1552	P4	Flat Cable Connector 50 Pin, 0.1″ Center
AC1553	P4	Flat Cable Connector 50 Pin, 0.1″ Center with 2′ Color Coded Assembly Attached

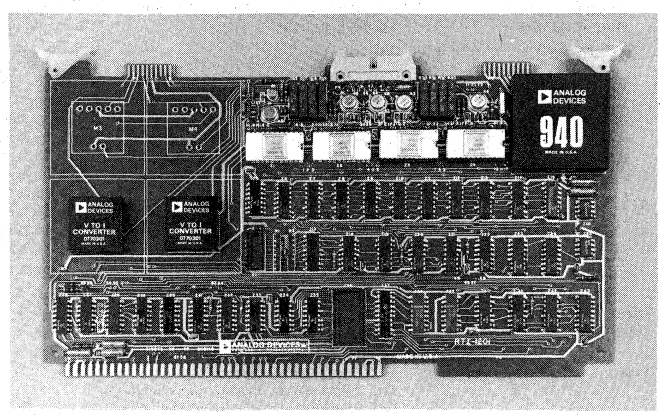
ANALOG DEVICES

MULTIBUS Intel Compatible Analog Output Subsystem

MODEL RTI-1201

FEATURES

- Complete Output Subsystem
- SBC-80, SYSTEM-80, MDS, BLC-80 Compatible
- Memory Mapped I/O Interface
- Wire Wrap Feature Selection
- Four Software Controlled Logic Driver Outputs
- Four Channels of 12-Bit Analog Output
- DAC Data Read Back
- DAC Reset Function
- Optional 4-20mA Current Loop Outputs
- Precision +10V Reference
- Optional Single +5V Power
- Memory Overlay – RAM and ROM Inhibit
- Multiple Card Select Function
- On-Board PROM Socket



GENERAL DESCRIPTION

The RTI-1201 is a complete 8 channel output subsystem comprised of 4 digital and 4 analog channels. This subsystem is electrically and mechanically compatible with the Intel SBC-80 series of single board computers. It is also compatible with the Analog Devices RTI-1200 Analog I/O Interface board, the Intel System-80 microcomputer series, the MDS-800 microcomputer development system and the National Semiconductor BLC-80/10 board level computer.

The RTI-1201 combines on a single printed circuit board many features and capabilities which reduce both the hardware and software effort required to interface a microcomputer to the real world. The RTI-1201 was designed to be extremely versatile, efficient and easy to use in the end user's application. All connections to the microcomputer are made by simply plugging the RTI-1201 into the digital bus connector in the user's card cage. The analog interface is made through a high quality pin connector mounted at the opposite board edge from the digital bus connection. Digital outputs are made at a card edge connector.

DIGITAL OUTPUTS

The RTI-1201 contains four digital output channels. These digital outputs are comprised of high-current logic drivers which can be used for simple "on/off" control of various system functions. These open collector driver outputs are software controlled and have a 30V, 300mA capability.

ANALOG OUTPUTS

The RTI-1201 is configured with four 12-bit D/A converters which are software driven via double buffered registers. They can be used for such functions as driving an analog recorder or generating analog control signals. By using the +10V onboard reference, each of the D/A converters can be individually set by the user to any of five output ranges. The D/A input code for each channel can also be individually set for natural binary, offset binary, or two's complement. The desired configuration is user selectable at convenient wire wrap posts.

REFERENCE

The RTI-1201 inherently guarantees superb tracking capability of all analog output channels since they all share a single onboard reference. This reference is also buffered and brought out for user convenience. The user may also choose to disconnect the internal reference and use the provision for an external reference.

REMOTE SENSING

Sense inputs of the D/A converter are present at the output connector for applications where the load is to be located a considerable distance from the RTI-1201. Without this feature, IR drops in the output line could rapidly degrade overall accuracy. The board is shipped with jumpers connecting the D/A converter sense inputs to local sense points.

DAC DATA REGISTERS

The D/A converters are software driven via double buffered registers. The buffers allow two data bytes to be loaded simultaneously into the D/A converter so that the output changes directly from one 12-bit value to another. The RTI-1201 also has a provision for writing the 8 MSB's in a single byte word to each D/A converter. This allows fast, highly accurate, eight bit operation.

CURRENT LOOP OUTPUTS

Each of the four analog output channels can be optionally equipped with a voltage to current converter. With this option, a 4-20mA current loop signal is available for process and industrial control applications.

SPECIFICATIONS (typical at +25°C and with nominal voltages, unless otherwise noted)

RTI-1201 ANALOG/DIGITAL OUTPUT BOARD

ANALOG OUTPUTS[1]	
Number Available	4 DAC's
Accuracy[2]	
Resolution	12 Bits
Overall Error	±1/2LSB (0.0125% FSR)
Voltage Output Characteristics	
Ranges[3]	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Output Current	5mA min @ ±10V
Settling Time (to 0.02% FS for 10V Step)	5μs
Offset T.C.	±10μV/°C
Gain T.C.	±10ppm/°C
Current Loop Characteristics[1,4]	
Number	0, 2, or 4
Range	4–20mA Nonisolated
Compliance Voltage[5]	10V @ 20mA with 18V to 30V Supply
Loop Supply Voltage Range	+15V to +30V
Settling Time (to ±0.01% for Full Scale Step)	50μs max
Offset T.C.	±0.4μA/°C
Gain T.C.	±15ppm/°C
Load Resistance Range	0 to 500 ohms
Digital Input Coding[3]	BIN, OBN, 2SC
DAC Load Sense	Provision is made for Local (on-board) or External Load Sensing for each DAC.
Reset[3]	All DAC's can be Reset to 0V Output with a Single Write Instruction or upon System Reset. All logic drivers can be turned "off" upon system reset.
DAC Readback	DAC Data can be written to and read from the same location
On-Board Reference[6]	
Voltage Output	+10.00V ±0.02% @ 2mA
T.C.	±10ppm/°C
External Reference Input[6]	
Range	1V to +10V
Input Impedance	20kΩ ±15%
LOGIC DRIVER OUTPUTS	
Number	4
Characteristics	Open Collector, 30V max, 300mA max Continuous Sink Current per Output
MICROCOMPUTER INTERFACE	
Compatibility	Completely Compatible with Intel SBC-80/10, SBC-80/20, and MDS Bus System; RTI-1200; BLC-80/10
Type of Interface	Interfaces as a Block of Memory Locations, Using Address, Data and Control Busses.
Position in Memory[7]	User Selectable Among any of 16 Possible Locations.
Card Select Feature[7]	16 Cards per 1K Memory Position
On-Board PROM Socket	Socket for Intel 2708 or Equivalent 1024 Byte x 8-Bit PROM, of which 1008 Bytes are Usable. +12V and -5V are supplied from the Digital Bus.
Memory Overlay (Inhibit)[3]	RAM or ROM
POWER REQUIREMENTS[8]	
Without DC/DC Options	
RTI-1201-040	+15V ±3% @ 45mA −15V ±3% @ 95mA +5V ±5% @ 800mA
Per V/I (0A08)	+15V ±3% @ 5mA −15V ±3% @ 1mA
With DC/DC (0A09) Option[9] RTI-1201-040, 0A09 and 4, 0A08's	+5V ±5% @ 1700mA max
TEMPERATURE RANGE	
Operations	0 to +70°C
Storage	−55°C to +85°C
MECHANICAL	
Size	6.75" x 12.00" with 0.6" min Board Spacing (171.5 x 304.8 x 15.2mm)
Connectors	See Ordering Guide Below

NOTES
[1] See ordering guide for information on allowable combinations.
[2] Overall error is specified with gain and offset trimmed and is defined as the deviation from a straight line passing through the end points of the range. It is expressed in terms of bits and in terms of the deviation as a percent of the full scale range, (i.e., 2.5mV is 0.0125% FSR of a −10V to +10V range).
[3] User selectable with wire-wrap jumpers.
[4] The current loop specifications include the effects of the driving D/A converter.
[5] Up to 11V compliance is possible @ 20mA with a +18V minimum loop supply.
[6] The reference is trimmed to within 0.02% accuracy at no load. Long term drift is less than 1/2LSB/1000 Hours operation. DAC accuracy is reduced with lower reference levels. Overall error is 0.1% with a 1V external reference input.
[7] The memory map shows in detail where the data and control functions appear in memory.
[8] Power requirements shown are for RTI-1201-040 with 4 DAC's and no Current Loop options. Power requirements for each additional pair of V/I converters are also shown.
[9] The DC/DC converter option provides ±15V for the analog circuits from the SBC system's +5V bus.

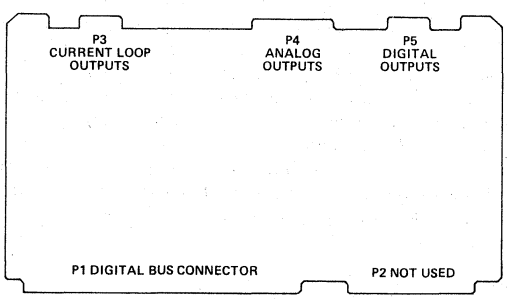
Specifications subject to change without notice.

RTI-1201 ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1201-040	**Output Subsystem With 4 DAC's**
ACCESSORIES	
0A08	**4-20mA V/I Converter (order 0, 2 or 4)**
0A09	**DC/DC Converter (+5V to ±15V)**

NOTE: ALL OPTIONS HAVE 4 LOGIC DRIVER OUTPUTS

MECHANICAL OUTLINE



MATING CONNECTIONS

	Mates to	Description
AC1551	P3 or P5 (Card Edge Connector)	Solder Tail Connector 20 pin, 0.1" centers w/o connecting cable
AC1555	P4 (Analog Pin Connector)	Flat Cable Connector 20 pin, 0.1" centers with 2' color coded cable attached
AC1556	P3 or P5 (Card Edge Connector)	Flat Cable Connector 20 pin, 0.1" centers with 3' color coded cable attached

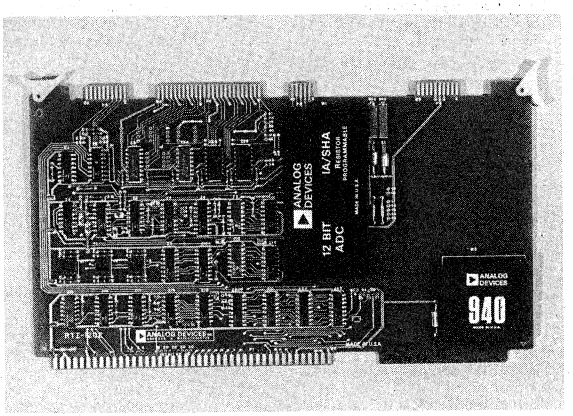
ANALOG DEVICES

MULTIBUS Intel Compatible Analog Input Subsystem

MODEL RTI-1202

FEATURES

- Complete Analog Input Subsystems for OEM Applications
- SBC-80, System-80, MDS, BLC-80 Compatible
- Memory Mapped I/O Interface
- Wire-Wrap Feature Selection
- Data Acquisition:
  - Up to 32 Input Channels On-Board
  - Auto Scan Operation Mode
  - Input Fault Protection
  - Instrumentation Amplifier
  - Sample and Hold Amplifier
  - 4-20mA Current Loop Inputs
  - 12-Bit ADC (RTI-1202-R)
  - 8-Bit ADC (RTI-1202-8R)
- Interrupt Operation Mode
- Memory Overlay – RAM and ROM Inhibit
- Optional Single +5V Power



GENERAL DESCRIPTION

The RTI-1202-R and RTI-1202-8R represent complete cost effective solutions to *OEM* applications. These analog input systems are electrically and mechanically compatible with the Intel SBC-80 series of single board microcomputers. In addition, the RTI-1202 series is compatible with the Intel MDS microcomputer development system, the National Semiconductor BLC-80 microcomputer board and many other Multibus compatible microcomputers.

The RTI-1202 series offers on a single printed circuit board many features that significantly simplify interfacing microcomputers to real world analog signals. These analog input subsystems are versatile, easy to use and cost effective. All connections to the microcomputer are made by simply plugging the subsystem into the digital bus connector in the user's card cage. The analog signals are connected to the system via a printed circuit board connector.

The RTI-1202 series of analog input subsystems offer up to 32 channels of protected multiplexer input, a selectable gain instrumentation amplifier, a sample and hold amplifier, and either an 8- or 12-bit A/D converter.

INPUTS

The basic RTI-1202-R offers 16 single-ended, 16 pseudo-differential, or 8 differential input channels (jumper selectable). Each input channel is fully protected to 20 volts beyond the supply voltages ($\pm V_{CC}$ ±20V). The number of input channels can be expanded on board to 32 channels and off board to 256 channels.

The multiplexer outputs are connected to the inputs of a resistor programmable instrumentation amplifier. A single metal film or wire-wound resistor can be used to set the amplifier gain to any value between 1 and 1000. The instrumentation amplifier provides low level signal acquisition with a system CMRR (Common Mode Rejection Ratio) consistent with 8- or 12-bit resolution.

A/D CONVERSION

The RTI-1202-8R offers a fast 8-bit ADC (2μs) and the RTI-1202 comes with a higher resolution 12-bit ADC (25μs). Data is made available to the microcomputer in both a two byte format (8 LSB and 4 MSB) and a single byte format (8 MSB). For synchronization with external events, a TTL level sync signal can be hardwired to the P-3 edge connector to create an external convert command. A wire-wrap jumper offers the user a choice between autoscan operation and random channel addressing. In the autoscan mode each convert command automatically increments the multiplexer register to the next channel. After a channel is addressed, a built-in convert command delay provides ample time for the input signal to fully settle, before the A/D conversion.

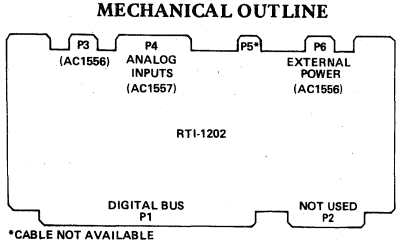
In the memory mapped mode of operation, the user may opt to have the processor continue operation during each conversion, or halt the processor completely during the A/D conversion. The halt mode allows the operator to avoid jumping to an interrupt service routine to read the converted data. By simply addressing the selected channel as a location in memory, the data is automatically transferred to the processor at the completion of the A/D conversion. In the interrupt mode, the optional end of conversion signal sets the EOC bit in the status word, activating any one of eight jumper selectable interrupts. Upon recognition of the interrupt, the microcomputer branches to a service routine to read the converted data. At the end of the service routine the microcomputer continues with the mainline program operation. In addition to end of conversion interrupt and CPU hold, the user can simply loop to check the EOC status bit or wait a sufficient amount of time for the A/D conversion to take place. All four methods are available on these subsystems for maximum user flexibility. The converted data is available in either natural binary, offset binary, or two's complement code.

SPECIFICATIONS (typical at +25°C with nominal supply voltages unless otherwise noted)

MODEL	RTI-1202-R	RTI-1202-8R
INPUT		
Number of Analog Inputs		
Standard	16 Single Ended, 16 Pseudo-Differential, or 8 Differential[1]	*
With Multiplexer Expander Option	32 SE, 32 PD or 16 Diff.[1]	*
Total Channel Addressing Capability		
Using On Board Logic	256 Total	*
Multiplexer Switching Characteristics	Break-Before-Make. All Channels Off When No Power Applied	*
Input Overvoltage Protection	$\pm(V_{CC}+20V)$	*
Input Full Scale Range at Connector[2]	10mV FS to ±10V FS	*
Current Loop Inputs	16 Locations For User Installed Conversion Resistors	*
INSTRUMENTATION AMPLIFIER		
Gain Range	1V/V to 1000V/V	*
Gain Equation	$G=\left(1+\frac{20k\Omega}{R_G}\right)$	*
CMV Range	±10V min	*
CMRR (dc to 100Hz)	74dB min	70dB min
Input Impedance	$>10^8\,\Omega$	*
Input Bias Current	±50nA max	*
0 to +70°C	±70nA	*
Input Offset Current	±5nA max	*
0 to +70°C	±7nA	±30nA
Offset Error	Adjustable to Zero	*
Gain Error	Adjustable to Zero	*
Offset T.C.	$\pm\left(1+\frac{35}{G}\right)\mu V/^\circ C$ (RTI)	$\pm\left(5+\frac{100}{G}\right)\mu V/^\circ C$ (RTI)
Gain T.C.	±25ppm of rdg./°C (RTI)	±200ppm of rdg./°C (RTI)
Settling Time[3]	15µs max to 0.01%	6µs max to 0.2%
SAMPLE/HOLD AMPLIFIER		
Aperture Delay	90ns	*
Aperture Width	20ns	*
Aperture Uncertainty	5ns	*
CONVERSION CHARACTERISTICS		
Resolution	12 Bits	8 Bits
Conversion Time	25µs max	2µs max
Throughput Rate[4]	40,000 Channels/sec	125,000 Channels/sec
Nonlinearity Error	±1/2LSB typ, ±1LSB max	*
Nonlinearity T.C.	±3ppm/°C	*
Noise Error	±1/4LSB max (G=1)	*
	±1LSB max (G=100)	±1LSB max (G=1000)
Overall Error	±1LSB max (G = 1) ±2LSB max (G = 200)	*
Output Codes[1]	Bin, OBN, 2SC	*
THE FOLLOWING SPECIFICATIONS APPLY TO ALL BOARDS		
POWER REQUIREMENTS		
Without dc-dc Converter	650mA	
+5V, ±5%		
+15V, ±3%	40mA	
−15V, ±3%	40mA	
With dc-dc Converter		
+5V ±5%	1100mA	
MICROCOMPUTER INTERFACE		
Digital Bus Connections	SBC-80 "Multibus" Compatible (1TTL Load max)	
Type of Interface	Memory Mapped Using Data, Address and Control Buses	
Position in Memory	Selectable by the Use of 3 on-board sockets	
Memory Overlay (Inhibit)	RAM or ROM	
TEMPERATURE RANGE		
Operating	0 to 70°C	
Storage	−55°C to +85°C	
MECHANICAL		
Size	6.25" (171.5mm) x 12.00" (304.8mm)	
Board-Board Spacing	0.7" (15mm)	
max Weight	14 ounces (400 grams)	

NOTES:
[1] Selectable with wire-wrap jumpers.
[2] The input range at the connector is the A/D converter full scale input range divided by the gain of the instrumentation amplifier.
[3] Settling time is for a 20V step or any channel change at G = 1. Settling time will increase to 55µs at G = 1000.
[4] The effective throughput rate is determined by the user's software data handling capability. The maximum throughput rate listed is exclusive of the CPU interface operations which may or may not be completed during the subsystem's conversion time. In the CPU hold mode, the user's software and interface time must be added to the conversion time to determine the maximum effective throughput rate.
Specifications subject to change without notice.

MECHANICAL OUTLINE



ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1202-R	Input Board with 12-Bit ADC and Resistor Programmable Gain IA
RTI-1202-8R	Input Board with 8-Bit ADC and Resistor Programmable Gain IA
ACCESSORIES	
0A09	DC-DC Converter (5V to ±15V)
0A10	Multiplexer Expansion Kit (2 ea. HI-508A)
CONNECTORS	
AC1556	20 Pin, Card Edge, with 3' Cable
AC1557	50 Pin, Card Edge, with 3' Cable

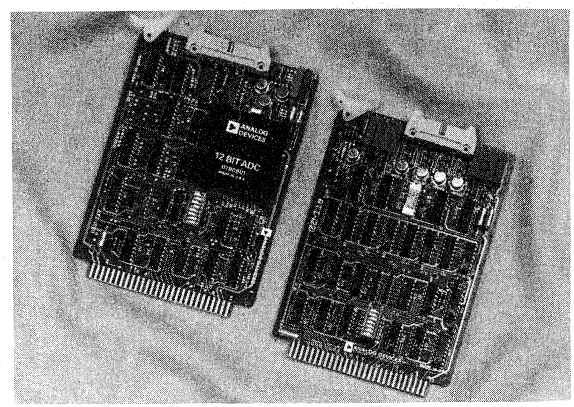
ANALOG DEVICES

Pro-Log Compatible Analog I/O Subsystems

MODELS RTI-1220, RTI-1221

FEATURES

- **Compatible with Pro-Log 8-Bit and 4-Bit Microcomputers**
- **Complete Analog Input and Output Subsystems**
- **Memory Mapped or I/O Port Interface**
- **Card Select Feature**
- **Wire Wrap Feature Selection**
- **Data Acquisition (Model RTI-1220)**
  - **16 Input Channels**
  - **4-20mA Current Input Capability**
  - **Sample and Hold Amplifier**
  - **Adjustable Gain Instrumentation Amp.**
  - **8-Bit or 12-Bit A/D Converter Option**
  - **Input Fault Protection**
- **Analog Output (Model RTI-1221)**
  - **4 Channel Output**
  - **Full 4-Quadrant Multiplying DAC's**
  - **-5V and -10V Precision References Available at Pin Connector**



GENERAL DESCRIPTION

The RTI-1220, Analog Data Acquisition Board and the RTI-1221, Analog Output Board comprise complete analog I/O subsystems. They simplify system development between real-time analog signals and Pro-Log microcomputers or other 8080 and 6800 based systems. The RTI-1220 and RTI-1221 are functionally, mechanically, and electrically compatible with the Pro-Log series of microcomputers. All address, control, and data bus connections are made by simply plugging these cards into a user wired Pro-Log card cage. The analog interface to each card is made through a high quality pin connector mounted at the opposite board edge from the digital bus.

DATA ACQUISITION – RTI-1220

The basic functions of the RTI-1220 are analog signal data acquisition, and conversion into digital information acceptable to a microcomputer. This is accomplished with a protected analog multiplexer, an adjustable gain instrumentation amplifier, a sample and hold amplifier, and either a 12-bit or an 8-bit A/D converter.

The input of model RTI-1220 may be configured for either 16 channel single-ended, or pseudo-differential operation, or for 8 channel full differential operation. The desired configuration is user selectable at convenient wire wrap posts.

The RTI-1220 has a special feature that prevents erroneous data acquisition. Each time an input channel is switched an automatic convert command delay is enabled. This delay allows for signal settling at the front end before initiation of conversion. The controlling microcomputer is not held up during either the delay time or the conversion time.

The RTI-1220 can be easily configured by wire wrap jumpers at the ADC to accept 0 to +10V, -10V to 0V, ±5V, or ±10V full scale ADC input signals. Output data from the A/D converter is natural binary code for unipolar input ranges and at the user's option, can be either offset binary or two's complement coding when using bipolar input ranges. Another feature of the RTI-1220 is that all of the resulting ADC data appears in both single and double byte format.

ANALOG OUTPUTS – RTI-1221

The basic function of the RTI-1221 is to provide Analog outputs corresponding to digital information available from the microcomputer. The RTI-1221 is a complete four channel analog output system that consists of double-buffered registers, 10-bit resolution DAC's, and output amplifiers. Two precision voltage references are also available for on-board or external system utilization.

Double-buffered input registers are used so that digital data from the microcomputer may be presented in two byte format for 10-bit resolution or in single byte format for a highly accurate 8-bit output. The D/A input data is natural Binary for unipolar output ranges and can be user configured for Offset Binary or Two's Complement for bipolar output ranges.

All four D/A converters can be set to virtually any voltage range desired. By using the on-board references, 4 output ranges may be selected by wire wrap jumpers (±10V, 0 to 10V, ±5V, 0 to 5V). If an external reference is used, the user has complete freedom to set the full scale output to any value from a few millivolts to ±10 volts. This feature is made possible by the utilization of true four quadrant multiplying DAC's. If a varying reference signal is used, the DAC becomes a programmable attenuator. For more sophisticated applications flexibility, the output of one D/A channel can be used as a reference for a second D/A channel. The resulting Analog output is then directly proportional to the product of two variables and is completely under software control.

SPECIFICATIONS (typical @ +25°C with +5V and ±15V unless otherwise noted)

MODEL	RTI-1220
ANALOG INPUT	
Number of Analog Inputs	16 Single-Ended, 8 Differential, or 16 Pseudo-Differential
Multiplexer Switching Characteristics	Break-Before-Make. All Channels Open When Power is Off.
Input Voltage Ranges[1]	±10mV to ±10V
Input Current Loop Ranges (Resistor Programmable)	4-20mA, 10-50mA, etc.
ADC Input Ranges[2]	0V to +10V, 0V to -10V, ±5V, ±10V
Amplifier Gain Range (Resistor Programmable)	1 to 1000V/V
Amplifier Gain Equation	$G = (1 + \frac{10K}{R})$
Input Impedance	$>10^8\Omega$
Settling Time[3]	30µs max @ G = 1
Input Bias Current (0 to +70°C)	300nA
Amplifier Input Offset Voltage	±0.3mV max
Amplifier Input Offset Voltage Drift	±25µV/°C
CMRR	75dB min
CMV	±10V
Noise Error[4]	±1/2LSB max @ G = 1
Input Overvoltage Protection Continuous Overvoltage	$\pm V_{CC}$ ±20V

CONVERSION CHARACTERISTICS	8-BIT ADC	12-BIT ADC
Accuracy		
Resolution	8 Bits	12 Bits
Overall Error[5], G = 1	±0.2% max	±0.025% max
G = 10	±0.3%	±0.03%
G = 200	±0.4%	±0.2%
T.C. of Overall Error, G = 1	±0.02%/°C max	±0.005%/°C
Conversion Time[6]	2µs	25µs
Delay Time[6]	35µs	35µs
Throughput Rate[7]	27.0kHz	16.7kHz
SHA Aperture Time	150ns	150ns
SHA Aperture Uncertainty	±15ns	±15ns
Gain Error	Adjustable to Zero	
Input Offset Voltage	Adjustable to Zero	
Digital Output Coding	Binary, Offset Binary, Two's Complement	

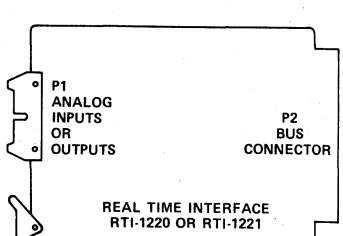
MICROCOMPUTER INTERFACE	
Compatibility	All Pro-Log 4- or 8-Bit Bus or I/O Port-Oriented Microcomputer Cards
TYPE OF INTERFACE	Memory Mapped or I/O Port-Interface
Address[8]	User Selectable
Power Requirements	+15V ±3% @ 30mA -15V ±3% @ 40mA +5V ±5% @ 600mA
Mechanical Size	4.5" x 6.5" with 0.5" min Board Spacing (114.3mm x 152.4mm x 12.7mm)
Temperature Range	
Operating	0 to +70°C
Storage	-55°C to +85°C
Mating Connectors Analog Connector (P-1) with 2' Color Coded Flat Cable Attached.	AC1554

MODEL	RTI-1221	
ANALOG OUTPUT		
Number of DAC Channels	4	
Accuracy	8-BIT OPTION	10-BIT OPTION
Resolution	10 Bits	10 Bits
Overall Error	±0.4% max	±0.1% max
Offset Error	Adjustable to Zero	
Gain Error	Adjustable to Zero	
Voltage Output Characteristics		
Voltage Output Range[2,9]	0 to +5V, ±5V, 0 to +10V, ±10V	
Output Current	5mA min @ ±10V	
Settling Time to 0.05% (20V Step)	30µs max	
Gain T.C.	±30ppm/°C max	
Offset T.C.	±25µV/°C max	
Reference Voltage Outputs	-10.00V @ 2mA (±0.02%) -5.00V @ 2mA (±0.07%)	
External Reference Input[10]		
Voltage Range	-10V to +10V	
Input Resistance	10kΩ Nominal	
Digital Input Coding[2]	Binary, Offset Binary, Two's Complement (All digital inputs are double buffered)	
Address[8]	User Selectable	
Power Requirements		
+15V	35mA	
-15V	25mA	
+5V	265mA	
Temperature Range		
Operating	0 to +70°C	
Storage	-55°C to +85°C	
Mating Connector Analog Connector (P-1) with 2' Color Coded Flat Cable Attached.	AC1555	

NOTES
[1] The input signal range is the A/D converter range divided by the gain of the instrumentation amplifier.
[2] User selectable with wire wrap jumpers.
[3] Settling time is a function of gain and increases to 1.5 milliseconds at G = 200.
[4] Typically 1/2LSB for G = 1 to 200 with an 8-bit ADC and 1/2LSB for G = 1 to 50 with the 12-bit ADC.
[5] When offset and gain error are trimmed to zero. Noise error is specified separately.
[6] Neither delay time nor conversion time will hold up the CPU.
[7] The throughput rate is based on a 35µs delay time followed by a 25µs conversion time for the 12-bit ADC or 2µs conversion time for the 8-bit ADC.
[8] The memory map shows in detail where the data and control functions appear in memory.
[9] The address is selected at an on board socket by a user provided DIP switch (or shorting plugs).
[10] These ranges are possible by using the on board reference voltages. Other ranges may be obtained with an external reference.
[11] Each DAC used on model RTI-1221 is a true four quadrant multiplying DAC which can be used with an independent reference voltage or ac signal for programmable attenuation.

Specifications subject to change without notice.

RTI-1220/1221 MECHANICAL OUTLINE



RTI-1220 AND RTI-1221 ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1220-8	Analog Input Board with 8-Bit ADC
RTI-1220-12	Analog Input Board with 12-Bit ADC
RTI-1221-8	Analog Output Board with Four 10-Bit DAC's Having 8-Bit Accuracy.
RTI-1221-10	Analog Output Board with Four 10-Bit DAC's Having 10-Bit Accuracy.

STD Bus
Mostek and Pro-Log Compatible
Analog I/O Subsystem

MODEL RTI-1225

FEATURES

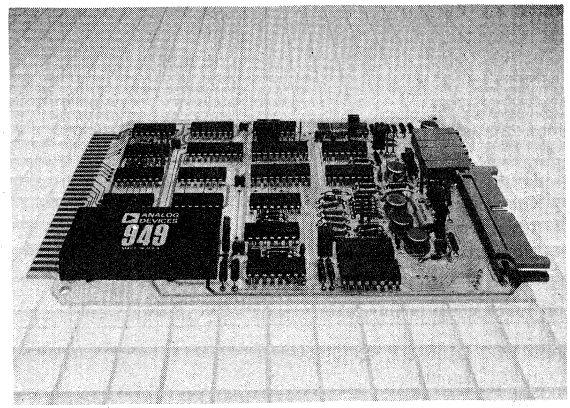
- Directly Compatible with Pro-Log and Mostek STD Bus Microcomputer Systems
- Memory Mapped I/O
- Operates Directly from Microcomputer +5 Volt Supply
- Convenient Wire Wrap Feature Selection
- Combination Analog Input and Output
  - 16 Channels of Analog Input
  - 2 Channels of Analog Output

ANALOG INPUT

- Input over Voltage Protection to ±35 Volts
- Sample and Hold Amplifier
- Monolithic 10-Bit A/D Converter
- Differential or Single Ended Inputs

ANALOG OUTPUTS

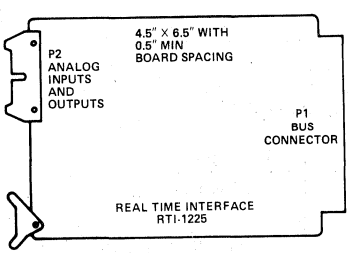
- 2 High Quality 8-Bit Analog Outputs
- Single On-Board Precision Reference Circuit

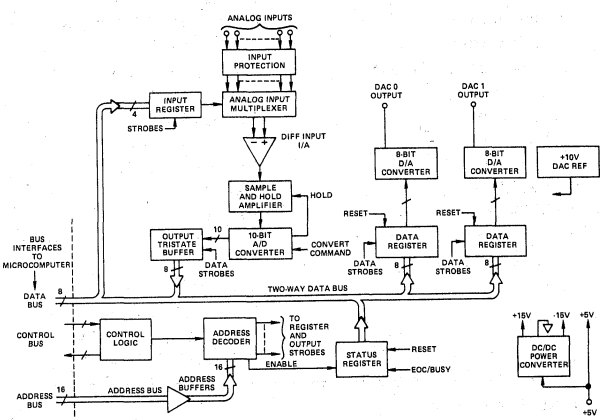


GENERAL DESCRIPTION

The RTI-1225 Analog Data Acquisition and Control Board comprises a complete analog I/O subsystem which simplifies the interface of REAL TIME ANALOG SIGNALS to STD BUS compatible microcomputer systems from MOSTEK and PRO-LOG. The RTI-1225 is functionally, mechanically and electrically compatible with the STD BUS. Address, control, and data bus connections are made by simply plugging the card into the microcomputer chassis. The analog signals are connected to the board through a high quality pin connector mounted at the opposite board edge from the digital bus. The RTI-1225 comes complete with its own dc/dc converter so that the board can operate directly from the microcomputer +5 volt supply.

Each board is configured as a block of five contiguous memory locations (MEMORY MAPPED INTERFACE). The RTI-1225 combines on a single printed circuit board, features and capabilities found only in systems costing twice as much. These features simplify the task of using microcomputers in real world measurement and control applications.





RTI-1225 Block Diagram

BYTE FORMAT

BYTE ADDRESS	MSB B_0	B_1	B_2	B_3	B_4	B_5	B_6	LSB B_7	BYTE FUNCTION	OPERATION
X F Y B	ϕ	ϕ	ϕ	ϕ	M_0	M_1	M_2	M_3	MUX ADDR & CONV. CMD	WRITE
X F Y C	D_2	D_3	D_4	D_5	D_6	D_7	D_8	LSB	LOWER ADC DATA BYTE	READ
X F Y D	BUSY	ϕ	ϕ	ϕ	ϕ	ϕ	MSB	D_1	STATUS & UPPER ADC DATA BYTE	READ
X F Y E	MSB	← DAC 0 DATA →						LSB	DAC 0 DATA BYTE	WRITE
X F Y F	MSB	← DAC 1 DATA →						LSB	DAC 1 DATA BYTE	WRITE

NOTES:
1. "X" HEX ADDRESS DIGITS ARE USER SELECTABLE.
2. ϕ BITS ARE IGNORED ON WRITE AND INDETERMINATE ON READ.
3. BUSY BIT IS "1" DURING CONVERSIONS AND "0" WHEN DONE.
4. WRITING THE MUX NUMBER TO LOCATION XFYB SETS THE INPUT CHANNEL AND INITIATES A CONVERSION.

RTI-1225 Memory Map

SPECIFICATIONS (typical @ +25°C with ±10V F.S.R. unless otherwise noted)

ANALOG INPUT SECTION	
Input Channels[1]	16 Single-Ended or 8 Differential
Input Protection	±35V Power On, ±20V with System Power Off
Input Range[1]	0V to 10V, ±5V, ±10V
Input Impedance	100MΩ min
IA Gain	1V/V
Input Bias Current	50nA
CMV Range	±10V
CMRR @ 60Hz	60dB min
ADC Resolution	10 Bits
Conversion Time[2]	40μs
Monotonicity	Guaranteed 0 to +50°C
Overall System Error	±0.15% F.S.R.
Offset Error	Adjustable to Zero
Gain Error	Adjustable to Zero
Noise Error RTI	±1/2LSB
Nonlinearity	±1LSB max
Offset Drift	50ppm/°C
Gain Drift	100ppm/°C

ANALOG OUTPUT SECTION	
Output Channels	2
Resolution	8 Bits
Output Ranges	0V to 10V, ±5V, ±10V
Output Current	5mA @ ±10V
Settling Time (20V Step)	50μs to ±1/2LSB
Monotonicity	Guaranteed 0 to +50°C
Nonlinearity	±1/2LSB max
Offset Error	Adjustable to Zero
Gain Error	Adjustable to Zero
Offset Drift	30μV/°C
Gain Drift	50ppm/°C

ENVIRONMENTAL	
Operation	0 to +50°C 5% to 95% R.H. without Condensation 25 to 32 inches of Mercury
Storage	-25°C to +85°C

MECHANICAL	
Size	4.5" X 6.5" (compatible to the STD BUS chassis)
Spacing	0.5" min
Analog Connector	3M Type Ribbon Cable Connector (ADI P/N AC1562) 34 Pins Total (Optional)

POWER REQUIREMENT	
+5V	750mA

NOTES:
[1] User selectable with wire wrap jumpers.
[2] The conversion time includes the time required for the input section to settle to the required accuracy when switching from one channel at 20V potential difference from the next channel to be sampled.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Description
RTI-1225	Analog I/O Board
Connector	
AC1562	34 Pin, Ribbon Cable Connector

ANALOG DEVICES

Micromodule Motorola Compatible Analog I/O Subsystems

MODELS RTI-1230, 1231, 1232

FEATURES

- **Complete Analog I/O Systems for OEM Applications**
- **Motorola Micromodule and EXORcisor Compatible**
- **Memory Mapped I/O Interface**
- **Convenient Address and Features Selection**
- **12-Bit or 8-Bit ADC**
- **Direct Operation from ±12V, +5V Bus Power**
- **Analog Input Subsystem RTI-1230**
  - **Up to 32 Input Channels**
  - **Each Input Channel Protected to V_{CC} +20 Volts**
  - **Software or Resistor Programmable Gain**
  - **Software Controlled EOC Interrupt**
  - **Auto Scan Capability**
  - **0-20mA Current Loop Input**
- **Analog Combination I/O Subsystem RTI-1231**
  - **Same Analog Input Features Plus:**
    - **Two 12-Bit D/A Converters**
    - **4 Quadrant Multiplication**
    - **On-Board or External Reference Capability**
- **Analog Output Subsystem RTI-1232**
  - **Four Independent 12-Bit Analog Outputs**
  - **Four Software Controlled, High Current Logic Driver Outputs**
  - **Optional 4-20mA Current Loop Converter Outputs**
  - **DAC and Logic Driver Reset**
  - **Remote Load Sensing**

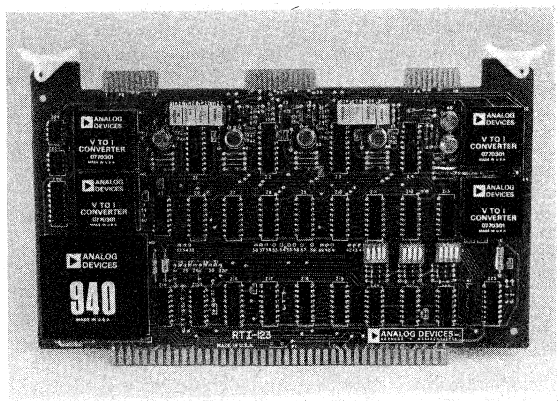
SERIES DESCRIPTION

The RTI-1230 series are complete, 8-bit and 12-bit analog I/O subsystems which are electrically and mechanically compatible with the Motorola EXORcisor Development System and Micromodule single board microcomputer. The series is comprised of an input only board (RTI-1230), an output only board (RTI-1232), and a combination I/O board (RTI-1231); each of which interfaces to the microcomputer as a block of 16 address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional features and options reduce both the hardware and the software effort required to interface analog signals to the microcomputer; freeing the designer to spend more time and effort on his particular application.

RTI-1230 ANALOG INPUT SUBSYSTEM

The basic function of the RTI-1230 input subsystem is to digitize analog signals and transfer the converted digital data to the microcomputer. The design includes protected input multiplexers, either a resistor-programmable-gain or a software programmable-gain instrumentation amplifier, a sample and hold amplifier, a 12-bit analog to digital (A/D) converter (RTI-1230-R and RTI-1230-S) or an 8-bit A/D converter (RTI-1230-8R) and the associated digital interface logic.



RTI-1231 COMBINATION ANALOG I/O SUBSYSTEM

The RTI-1231 provides the same analog input functions as the RTI-1230 *plus* two channels of high resolution, 12-bit analog voltage output. The 12-bit digital to analog converters are capable of full 4 quadrant multiplication. Four output voltage ranges can be jumper selected independently for each output channel, by using the on-board references.

RTI-1232 ANALOG OUTPUT SUBSYSTEM

The RTI-1232 output subsystem provides 4 channels of 12-bit analog output and 4 high current, digital logic driver outputs. The four digital outputs are software controlled, open collector drivers capable of sinking 300mA and sustaining voltages up to +30V. They can be used to provide "ON/OFF" system functions for driving relays, solenoids, and valve control.

The DAC's used are 4 quadrant multiplying 12-bit DAC's. Each DAC input code and output range are jumper selectable.

The analog output channels can also be ordered with optional 4-20mA current loop outputs ideal for use in process and industrial control applications. These high compliance voltage to current (V/I) converter modules (P/N 0A08) meet all the requirements of ISA-S50.1 compatibility of signal for Type 3, Class L, nonisolated 4-20mA current loop transmitters.

SPECIFICATIONS (typical @ +25°C and +5V, ±15V unless otherwise noted)

ANALOG INPUT

Model Numbers - Input Boards:	RTI-1230-R	RTI-1230-S	RTI-1230-8R
Combo I/O Boards:	RTI-1231-R	RTI-1231-S	RTI-1231-8R
Input Channels: Basic Board	16 SE, 16 PD, 8 Diff.	*	*
with On-Board Expansion	32 SE, 32 PD, 16 Diff.	*	*
with Off-Board Expansion	256 Total	*	*
Input Range at Card Edge	10mV F.S. to ±10V F.S.	0.625V F.S. to ±10V F.S.	*
Current Loop Inputs	Resistor Selectable	*	*
Input Protection	±(V_{CC} +20V)	*	*
Switching Characteristics	Break-Before-Make	*	*
Instrumentation Amplifier Gain	Resistor Programmable	Software Programmable	*
Gain Range	1V/V to 1000V/V	1, 2, 4, 8V/V	*
CMV Range	±10V min	*	*
CMRR (dc to 500Hz)	78dB min	*	70dB min
Input Settling Time (G = 1)	15µs max	10µs max	6µs max
Input Impedance	$>10^8\Omega$	*	*
Input Bias Current	±50nA	±5nA max	±50nA max
0 to +70°C	±70nA max	±50nA max	±70nA max
ADC Resolution	12 Bits	12 Bits	8 Bits
Conversion Time	25µs max	*	2µs max
Throughput Rate	40K Channels/sec	*	125K Channels/sec
ADC Input Ranges	±5V, ±5.12V, ±10V, ±10.24V ±2.5V, +5V, +10V, +10.24V	*	*
ADC Output Codes	BIN, OBN, 2SC	*	*
Nonlinearity Error	±1/2LSB typ. (±1LSB max)	*	*
Offset Error	Adj. to Zero	*	*
Offset TC (RTI)	$\left(1+\frac{50}{G}\right)$ µV/°C	±50µV/°C	$\left(5+\frac{100}{G}\right)$ µV/°C
Gain Error	Adj. to Zero	*	*
Gain TC (RTI)	±25ppm of RDG./°C	*	±200ppm of Rdg./°C
Noise Error (G = 1)	±1/4LSB max	*	*
Overall Error (G = 1)	±1LSB max	*	*
Overall Error	±1LSB at G = 100	±1.5LSB at G = 8	±1LSB at G = 100

ANALOG OUTPUT

Model Numbers - Combo I/O Boards:	RTI-1231-R, S, -8R	
Output Boards:		RTI-1232
Output Channels	2	4
DAC Resolution	12 Bit (8 Bit for -8R)	12 Bit
Nonlinearity Error	±0.05% FSR	*
Settling Time for a 20V Step	10µs max	*
Output Ranges	±5V, ±10V, +5V, +10V	*
Output Current	5mA @ 10V	*
Offset Error	Adj. to Zero	*
Offset TC	±25µV/°C	*
Gain Error	Adj. to Zero	*
Gain TC	±25ppm/°C	*
External Reference Range	-10V to +10V	*
Input Impedance	10kΩ Each DAC	*
DAC Input Codes	BIN, OBN, 2SC	*
DAC Updating	Double Buffered	*
Load Sensing	Each DAC	*

CURRENT LOOP OUTPUTS (RTI-1232) (Option P/N 0A08)

Type	ISA-S50.1, Type 3, Class L
Number	One per DAC
Output Current Range	4-20mA (Nonisolated)
Supply Voltage Range	+15V to +30V
Load Resistance Range	0Ω to 475Ω
Offset TC	±0.4µA/°C
Gain TC	±30ppm/°C
Nonlinearity	±1/2LSB
Settling Time	50µs max to 0.05%

DIGITAL OUTPUTS (RTI-1232)

Type	Open Collector Peripheral Driver
Number	4(Independently Controlled)
Current Range	300mA max Sink Current at 0.1V
Supply Voltage Range	30V max at the Collectors

MECHANICAL

Size	9.75" x 6.00" x 0.6" (247.6mm x 156.2mm x 15.2mm)
Weight	14 oz (500gm)

TEMPERATURE RANGE

Operating 0 to +70°C	0 to +70°C
Storage	-25°C to +85°C

*Same specifications as for RTI-1231-R.
Specifications subject to change without notice.

POWER REQUIREMENTS

Without dc-dc Option	Input Boards	Output Boards	Combo Boards	0A08(2)
±15V/±3%	30mA	50mA	50mA	10mA
-15V/±3%	30mA	40mA	45mA	2mA
+5V/±5%	700mA	350mA	900mA	0mA
With dc-dc Option				
+5V/±5%	1100mA	950mA	–	-

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1230-R	Input Board with 12 Bit A/D and Resistor Programmable Gain Amplifier
RTI-1230-S	Input Board with Software PGA
RTI-1231-R	I/O Board with Resistor Programmable Gain Amplifier
RTI-1231-S	I/O Board with Software PGA
RTI-1232	Output Board with 4 DAC's
RTI-1230-8R	Input Board with 8 Bit A/D and Resistor Programmable Gain Amplifier
RTI-1231-8R	I/O Board with 8 Bit A/D and Resistor Programmable Gain Amplifier

ACCESSORIES

0A08	4–20mA V/I Module
0A09	DC-DC Converter
0A10	Multiplexer Expansion Kit

CONNECTORS

AC1556	20 Pin, Card Edge*
AC1557	50 Pin, Card Edge*
AC1559	26 Pin, Card Edge*

*ALL CONNECTORS HAVE 3' OF COLOR CODED CABLE ATTACHED

TM-990/100M
Texas Instruments Compatible Analog I/O Subsystems

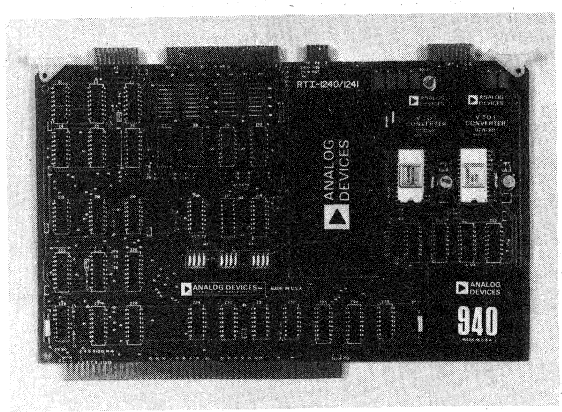
MODELS RTI-1240, 1241, 1242, 1243

FEATURES
- **Complete Analog I/O Subsystems**
- **T.I. 16-Bit TM-990/100M Compatibility**
- **Memory Mapped I/O Interface**
- **12-Bit Resolution and Accuracy**
- **Optional Single +5V Power**
- **Wire Wrap Feature Selection**

INPUT SUBSYSTEMS
- **256 Channel Expansion Capability**
- **Input Overvoltage Protection**
- **Software or Resistor Programmable Gain**
- **Interrupt Operation Capability**
- **Optional Analog Output Channels**

OUTPUT SUBSYSTEMS
- **8 High Current Logic Driver Outputs**
- **4 or 8 Analog Output Channels**

Detailed User's Guide



SERIES DESCRIPTION

The RTI-1240 Series are complete, 12-bit resolution, analog I/O subsystems which are electrically and mechanically compatible with the Texas Instruments 16-bit TM-990/100M single board microcomputer. The series is comprised of an input board, two output boards, and a combination I/O board; each of which interfaces to the microcomputer as a block of 8 or 16 address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional capabilities, features and options are included to reduce both the hardware and the software effort required in interfacing analog signals to the microcomputer. The designer is then free to spend more time and effort on the particular application instead of on designing basic building block functions.

RTI-1240 ANALOG INPUT SUBSYSTEM

The basic function of the RTI-1240 is to acquire signals and present them to the microcomputer in digital form. The design is comprised of a protected input multiplexer, either a resistor or a software programmable gain instrumentation amplifier, a sample and hold amplifier, a 12-bit A/D converter and the associated digital interface logic.

RTI-1241 COMBINATION ANALOG I/O SUBSYSTEM

The RTI-1241 provides the same analog input functions as the RTI-1240 and in addition has two channels of 12-bit analog output.

The RTI-1241 has two 12-bit resolution D/A converters (DAC's) providing up to ±10V analog output in several ranges. The input coding and output range of each DAC are independently selectable by wire-wrap jumpers.

The +10V reference for the DAC's is located on-board. However, should the user desire, an external reference between +1V and +10V may be used.

The two analog output channels can also be ordered with optional 4-20mA current loop outputs for use in process and industrial control applications. These voltage to current (V/I) converter modules (P/N 0A08) meet all the requirements of ISA-S50.1 for Type 3, Class L, non-isolated 4-20mA current loop transmitters.

RTI-1242 AND RTI-1243 OUTPUT SUBSYSTEMS

The RTI-1242 and 1243 output subsystems provide 4 or 8 channels of analog output and 8 high current, logic driver outputs.

The eight digital outputs are software controlled, open collector, drivers capable of 300mA maximum sink current and voltages up to +30V. They can be used to provide "on/off" system functions for relay, solenoid, and valve control.

The RTI-1242 and RTI-1243 have four or eight 12-bit DAC's respectively. Each DAC's input code and output range is independently selectable.

SPECIFICATIONS (typical @ +25°C and nominal supply voltage)

ANALOG INPUT	COMBINATION I/O BOARDS		INPUT ONLY BOARDS	
Model Numbers	RTI-1241-R	RTI-1241-S	RTI-1240-R	RTI-1240-S
Input Channels				
Basic Board	16 SE, 16 PD, 8 Diff.	*	*	*
Expansion: On-Board	32 SE, 32 PD, 16 Diff.	*	*	*
Off-Board	256 Total	*	*	*
Input Range at Card Edge	10mVFS to ±10VFS	0.625 to ±10VFS	*	**
Current Loop Inputs	0 to 50mA, 0 to 20mA, etc.	*	*	*
Input Protection	±(V_{CC} +20V)	*	*	*
Switching	Break-Before-Make	*	*	*
Input Impedance	$>10^8\Omega$	*	*	*
Input Bias Current	±50nA max	±5nA max	*	**
0 to +70°C	±70nA	±50nA	*	**
Instrumentation Amplifier	Resistor Programmable Gain	Software Programmable Gain	*	**
Gain Range	1 to 1000 V/V $\left[G = 1 + \frac{20k}{R}\right]$	1, 2, 4, 8 V/V	*	**
CMV	±10V min	*	*	*
CMRR (dc–500Hz)	76dB min	*	*	*
Input Settling Time	15µs max (G = 1)	10µs max (G = 1 to 8)	*	**
ADC Input Ranges	±5V, ±5.12V, ±10V, ±10.24V, +10V, +10.24V	*	*	*
Resolution	12 Bits	*	*	*
Conversion Time	25µs max	*	*	*
Throughput Rate	40,000 Channels/sec	*	*	*
Output Codes	Binary, Offset Binary, Two's Complement	*	*	*
Nonlinearity Error	±1/2LSB typ (±1LSB max)	*	*	*
Offset Error	Adj. to Zero	*	*	**
Gain Error	Adj. to Zero	*	*	*
Offset TC	$\pm(1 + \frac{50}{G})\mu V/°C$ (RTI)	±50µV/°C (RTI)	*	**
Gain TC	±20ppm of rdg/°C (RTI)	±25ppm of rdg/°C (RTI)	*	**
Noise Error	±1/4LSB max	*	*	*
Overall Error @ G = 1	±1LSB max	*	*	*
SHA Aperture Delay	90ns	*	*	*
SHA Aperture Width	20ns	*	*	*
SHA Aperture Uncertainty	5ns	*	*	*

ANALOG OUTPUT		OUTPUT ONLY BOARDS	
Model Number	RTI-1241-R	RTI-1241-S	RTI-1242	RTI-1243
Output Channels	2	2	4	8
Resolution	12 Bits	*	*	*
Output Ranges (with on board Ref)	+5V, +10V, ±2.5V, ±5V, ±10V	*	*	*
Output Current	±5mA min @ ±10V	*	*	*
Nonlinearity Error @ +10V Ref	±0.01% max	*	*	*
Offset Error	Adj. to Zero	*	*	*
Gain Error	Adj. to Zero	*	*	*
Offset TC	±15µV/°C	*	*	*
Gain TC	±15ppm/°C	*	*	*
Settling Time (for 20V step to ±0.01%)	10µs	*	*	*
Reference Range External	1V to +10V	*	*	*
Input Codes	Binary, Two's Complement, or Offset Binary	*	*	*

OTHER OUTPUTS				
Type	2 Optional Current Loops	*	8 Logic Drivers	***
Output Current Range	ISA-S50.1, Type 3, Class L	*	Open Collector	***
Supply Voltage Range	4-20mA	*	300mA sink @ 0.7V	***
Input Voltage Range	+15V to +30V	*	+30V max	***
Offset Error	0V to +10V	*		
Gain Error	Adj. to Zero	*		
Offset TC	Adj. to Zero	*		
Gain TC	±0.4µA/°C	*		
Nonlinearity Error	±30ppm/°C	*		
Settling Time	±0.01% max	*		
	50µs max to 0.02%	*		

POWER REQUIREMENTS					
Model Number	RTI-1240	RTI-1241	RTI-1242	RTI-1243	V/I
Without Optional dc-dc					
+15V ±3%	40mA	50mA	45mA	50mA	10mA
−15V ±3%	40mA	80mA	80mA	150mA	2mA
+5V ±5%	1100mA	1100mA	900mA	1000mA	0mA
With dc-dc Option					
+5V ±5%	1.4A	1.5A	1.3A	1.6A	mA

MECHANICAL (All Models)	
Size	7.5" x 11.0" (190.5mm x 279.4mm)
Card Outline	Conforms to Texas Instruments Drawing SK922321
Card Spacing	0.6" min (15.2mm)
Operating Temperature	0 to 70°C
Storage Temperature	−25°C to +85°C

*Same as for RTI-1241-R
**Same as for RTI-1241-S
***Same as for RTI-1242
Specifications subject to change without notice.

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1240-R	Input Board with Resistor Programmable Gain Amplifier
RTI-1240-S	Input Board with Software PGA
RTI-1241-R	I/O Board with Resistor PGA
RTI-1241-S	I/O Board with Software PGA
RTI-1242	Output Board with Four DAC's
RTI-1243	Output Board with Eight DAC's
ACCESSORIES	
0A08	4-20mA V/I Module
0A09	DC-DC Converter
0A10	Multiplexer Expansion Kit (2 ea. HI-508A)
CONNECTORS	
AC1556	20 pin, Card Edge*
AC1557	50 pin, Card Edge*
AC1559	26 pin, Card Edge*

*ALL CONNECTORS HAVE 3' OF COLOR CODED CABLE ATTACHED

ANALOG DEVICES

DEC LSI-11
LSI-11/2 and LSI-11/23 Compatible Analog I/O Subsystems

MODELS RTI-1250, 1251, 1252

FEATURES

Complete Analog I/O Subsystems
Digital Equip. Corp. 16-Bit LSI-11/2 and 11/23 Compatibility
Memory Mapped I/O Interface
12-Bit Resolution and Accuracy
Single +5V Power Requirement
4-20mA Current Loop I/O Capability
Convenient Wire Wrap Feature Selection

RTI-1250 Analog Input Subsystem
- **16 Input Channels — Expandable On-Board to 32 Channels**
- **Input Overvoltage Protection to ±35 Volts**
- **Resistor or Software Programmable Gain Amplifier**
- **Software Control of Interrupt, Channel Scanning and External Trigger**

RTI-1251 Analog I/O Subsystem
- **16 Input Channels and 2 12-Bit Analog Output Channels**
- **Four Quadrant Multiplying DAC's**
- **On-Board Reference**

RTI-1252 Analog Output Subsystem
- **2- or 4-, 12-Bit Analog Output Channels**
- **Field Expandable from 2 to 4 DAC Outputs**
- **4 High Current Digital Logic Drivers**
- **Optional 4-20mA Current Loop Outputs**
- **Optional DAC and Logic Driver Reset**

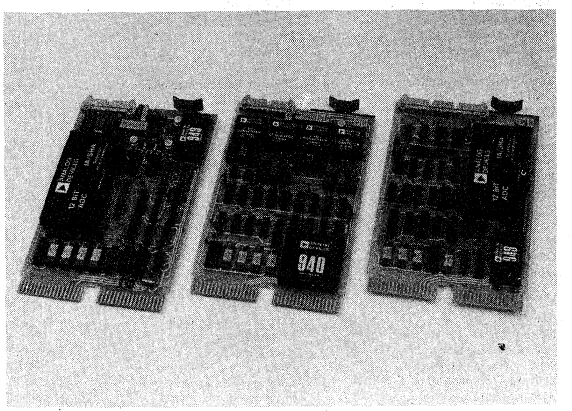
SERIES DESCRIPTION

The RTI-1250 Series products are complete, 12-bit resolution, analog I/O subsystems which are electrically and mechanically compatible with the Digital Equipment Corp. LSI-11, LSI-11/2, and LSI-11/23 single board microcomputers. The series is comprised of an input only board, an output only board, and a combination I/O board; each of which interfaces to the microcomputer as a block of 4 address locations (memory mapped interface). All bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional capabilities, features and options are included to reduce both the hardware and software effort required to interface analog signals to the microcomputer.

RTI-1250 ANALOG INPUT SUBSYSTEM

The basic function of the RTI-1250 is to convert analog signals into a digital format and to present this digital data to the microcomputer. The design includes a protected input multiplexer for switching up to 32 single-ended inputs, either a software or resistor programmable gain instrumentation amplifier, a sample and hold amplifier, a 12-bit A/D converter and the associated digital interface logic.



RTI-1251 COMBINATION ANALOG I/O SUBSYSTEM

The RTI-1251 provides 16 channels of analog input and two channels of 12-bit analog output.

The RTI-1251 has two 12-bit resolution multiplying D/A converters (MDAC's) providing up to ±10V analog output in several ranges. The input coding and output range of each MDAC are independently selectable by wire-wrap jumpers.

A -5V and a -10V reference for the MDAC's are located on-board. However, should the user desire, an external reference or signal between -10V and +10V may be used for multiplying applications for each MDAC.

RTI-1252 OUTPUT SUBSYSTEM

The RTI-1252 output subsystems provide either 2 or 4 channels of analog output, and 4 high current logic driver outputs. The 2 channel board (RTI-1252-2) may be expanded to either 3 or 4 channels by purchasing option 0A12.

Each DAC's input code and output range are independently selectable. Optional 4-20mA current loop outputs are available for use in process and industrial control applications. These socketed voltage to current (V/I) converter modules (P/N 0A08) meet all the requirements of the ISA-S50.1 standard for Type 3, class L, nonisolated 4-20mA current loop transmitters.

The four digital outputs are software controlled, open collector drivers capable of 300mA maximum sink current and sustaining voltages up to +30V. They can be used to provide "on/off" system functions for relay, solenoid, and valve control.

SPECIFICATIONS (typical @ +25°C and nominal supply voltages unless otherwise noted)

	INPUT ONLY BOARDS		COMBINATION I/O BOARDS
ANALOG INPUT			
Model Numbers	RTI-1250	RTI-1250-S	RTI-1251
Input Channels			
Basic Board	16 SE, 16 PD, 8 Diff.	*	*
Expansion On-Board	32 SE, 32 PD, 16 Diff.	*	None
FS Input Range	±10mVFS to ±10VFS	±0.625VFS to ±10VFS	±10mVFS to ±10VFS
Current Loop Inputs	0 to 50mA, 0-20mA, etc.	*	*
Input Protection	±(V_{CC} +20V)	*	*
Mux Switching	Break-Before-Make	*	
Input Impedance	$>10^8\ \Omega$	*	*
Input Bias Current 0 to +70°C	±50nA max	±5nA max	±50nA max
	±70nA	±50nA	±70nA
Instrumentation Amplifier	Resistor Programmable Gain	Software Programmable Gain	Resistor Programmable Gain
Gain Range	1 to 1000V/V	1, 2, 4, 8V/V	1 to 1000V/V
CMV Range	±10V min	*	*
CMRR (dc – 500Hz)	76dB min	*	*
Input Settling Time	20µs max (G = 1)	15µs max (G = 1 to 8)	20µs max (G = 1)
ADC Input Ranges	±2.5V, ±5V, ±10V, 0 to 10V, 0 to 5V	*	±5V, ±10V, 0V to +10V
Resolution	12 Bits	*	*
Conversion Time	25µs max	*	*
Throughput Rate	30,000 Channel/sec.	*	*
Output Codes	Binary, Offset Binary, Two's Complement	*	*
Nonlinearity Error	±1/2LSB typ (±1LSB max)	*	*
Offset Error	Adj. to Zero	*	*
Gain Error	Adj. to Zero	*	*
Offset TC	$\pm\left(1+\frac{50}{G}\right)\mu V/^{\circ}C$ (RTI)	±30µV/°C (RTI)	$\pm\left(1+\frac{50}{G}\right)\mu V/^{\circ}C$ (RTI)
Gain TC	±20ppm of rdg./°C (RTI)	±25ppm of rdg./°C (RTI)	±20ppm of rdg./°C (RTI)
Noise Error	±1/4LSB max	*	*
Overall Error @ G = 1	±1LSB max	*	*
SHA Aperture Delay	90ns	*	*
SHA Aperture Width	20ns	*	*
SHA Aperture Uncertainty	5ns	*	*

ANALOG OUTPUT		
Model Number	RTI-1251	RTI-1252-2
Output Channels	2	2 expandable to 4
Resolution	12 Bits	**
Output Ranges (with on board Ref)	+5V, +10V, ±5V, ±10V	+5V, +10V, ±2.5V, ±5V, ±10V
Output Current	±5mA min. @ ±10V	**
Nonlinearity Error	±0.01% max	±0.01%
Offset Error	Adj. to Zero	**
Gain Error	Adj. to Zero	**
Offset TC	±25µV/°C	±25µV/°C
Gain TC	±25ppm/°C	±15ppm/°C
Settling Time (for 20V step to ±0.01%)	10µs max	**
Input Codes	Binary, Two's Complement, or Offset Binary	**
Reference	-10.00V or -5.00V	+6.3V ±2%

OTHER OUTPUTS		
Type	V/I Current Loop Converter (Option 0A08)	4 Logic Drivers (RTI-1252 Only)
Output Current Range	ISA-S50.1, Type 3, Class L	Open Collector
Supply Voltage Range	4-20mA	300mA sink @ 0.7V
Input Voltage Range	+15V to +30V	+30V max
Offset Error	0V to +10V	
Gain Error	Adj. to Zero	
Offset TC	Adj. to Zero	
Gain TC	±0.4µA/°C	
Nonlinearity Error (V/I Only)	±30ppm/°C	
Settling Time	±0.01% max	
	50µs max to 0.02%	

POWER REQUIREMENTS

Model Number	RTI-1250	RTI-1251	RTI-1252	0A08 (V/I)
+5V ±5%	1.4A	1.5A	1.4A	10mA

MICROCOMPUTER INTERFACE
Complies with D.E.C. bus loading and electrical specifications

TEMPERATURE RANGE

Operation	0 to +70°C (0 – 95% RH non-condensing)
Storage	-55° C to +85°C

MECHANICAL

Size	5" X 8.5" (per D.E.C. Drawing)
Weight	10 ounces
Connectors	See Ordering Guide

*Same as for RTI-1250-R
**Same as for RTI-1251-R

Specifications subject to change without notice.

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1250-R	Input Board with Resistor Programmable Gain Amplifier
RTI-1250-S	Input Board with Software Programmable Gain Amplifier
RTI-1251	I/O Board with Resistor Programmable Gain Amplifier and Two Multiplying DAC's
RTI-1252-2	Output Board with Two Trimmed DAC's
RTI-1252-4	Output Board with Four Trimmed DAC's
ACCESSORIES	
0A08	4-20mA V/I Module
0A10	Multiplexer Expansion Kit (2 ea. HI-0508A-5)
0A12	12-Bit DAC for RTI-1252-2
CONNECTORS	
AC1553	50 Pin, Flat Cable Connector*
AC1554	26 Pin, Flat Cable Connector*
AC1560	14 Pin, Dip Plug Connector*

*All Connectors Have 3' of Color Coded Cable Attached

Prices subject to change without notice.

Testers for Linear Circuits

BIG SYSTEM PERFORMANCE IN A BENCHTOP SYSTEM AT 1/4 THE PRICE

The LTS-2000 is an easy-to-use, flexible linear test system that allows you to test any component to the manufacturer's own specifications—ADS's, DAC's and linear amplifiers including op amps, voltage regulators, current regulators, voltage comparators, voltage followers, current mirror op amps, instrumentation and isolation amplifiers and similar devices. Future system capabilities will include such data acquisition components as multipliers, dividers, log amplifiers, CMOS switches and more.

Far more than a simple tester, the LTS-2000 is a powerful instrument you can use for basic go/no-go testing, for component selection and grading, for engineering analysis, for qualification testing, or as a diagnostic tool for component evalution. Test results are immediately displayed and printed on the standard LTS-2000, and full reports, including statistical analysis are available through the RS232 ports.

We've included features in the LTS-2000 that you would expect to find only in "big systems": a software-controlled automatic handler interface, IEEE-488 interface, integral printer, integral statistical analysis package, and "big system" performance.

The LTS-2000 is the only compact linear test system that offers these kinds of "big system" advantages at less than 1/4 the "big system" price.

EASY TO USE SOFTWARE AND HARDWARE

Your Test Supervisor can set up the LTS-2000 in minutes by using either a program from the device library, or the complete test menu of fill-in-the-blanks software. Prompts for each step of the fill-in-the-blanks test programs are conveniently displayed directly over the associated function switches. Your Test Supervisor just plugs in the appropriate Family Board Module (ADC, DAC or linear amplifier) and socket module, and the LTS-2000 is ready to go.

The operator just plugs in the device and presses the Go button—the LTS-2000 does the rest.

Standard test programs can be easily altered to suit your needs. Select the tests you want—arrange them in the order you want. There's a full edit capability included too, so that you can change test parameters easily and quickly.

The system hardware is as easy to use as the system software. The large character digital display, the slope of the operator panel, the arrangement of the keyboard and switches are all human-engineered to ensure maximum throughput and minimum operator fatigue. This attention to detail is carried throughout the system. The socket assemblies, including the do-it-yourself socket assembly which accommodates a variety of device packages, can be assembled quickly and easily. There's no need to solder in a lot of pins—the connector included with the socket assemblies is soldered in for you. Just a few jumpers are all that is required.

SPECIFICATIONS

Accuracy: Overall measurement accuracy greater than 16 bits.

Sample Test Specifications:
- Op Amps:
  - Gain Bandwidth Product to 100MHz
  - Slew Rate to 1000V/μs
  - Input Bias Current from 10fA
- Voltage Regulators (Fixed, Adj., Positive, Negative, Dual Tracking):
  - Load Current to 15 Amp
  - Load Reg to 0.01%/V_{OUT}
- DAC's and ADC's:
  - Accuracy to 12 bit
  - Resolution to 16 bit

CPU: TI, TM990-101, 16 bit

Memory: TI, TM990/203, 64Kb RAM

Storage: 5-1/4" Floppy Disk, 92Kb capacity

Display: 40 character, dot matrix

Operator Keyboard: 30 alpha-numeric keys for data entry
6 fixed function keys
5 programmable function keys with indicator lights

Strip Printer: 20-column, alpha-numeric thermal printer

Power Requirements: Switch selectable, 115V ac or 230V ac 50Hz/60Hz 250 watts

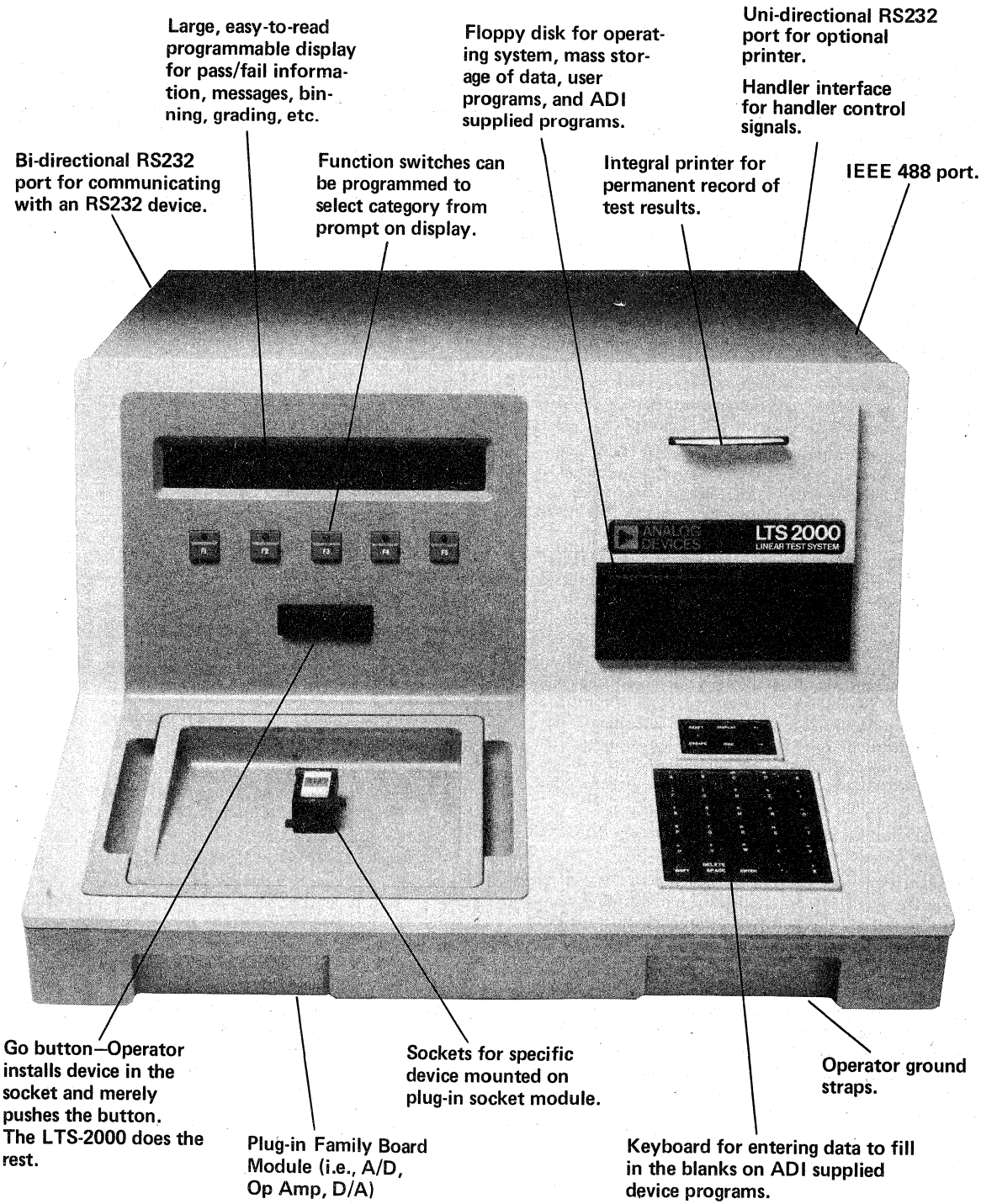
Dimensions: 48cm wide X 66cm deep X 31cm high
19" wide X 26" deep X 12" high

Weight: 39 Kgs
75 lbs

Operating Temperature: +10°C to +40°C

Humidity: Noncondensing

Options:
- Printer: TI Model 820KSR, 150 char/sec/132 col 110 to 9600 baud
- CRT Terminal: Perkin-Elmer Model 550
  12" diagonal screen,
  24 lines of 80 char/line
  Full 128 char ASCII, 110 to 9600 baud


Large, easy-to-read programmable display for pass/fail information, messages, binning, grading, etc.
Floppy disk for operating system, mass storage of data, user programs, and ADI supplied programs.
Uni-directional RS232 port for optional printer.
Handler interface for handler control signals.
Bi-directional RS232 port for communicating with an RS232 device.
Function switches can be programmed to select category from prompt on display.
Integral printer for permanent record of test results.
IEEE 488 port.
ANALOG DEVICES
LTS 2000
LINEAR TEST SYSTEM
Go button—Operator installs device in the socket and merely pushes the button. The LTS-2000 does the rest.
Sockets for specific device mounted on plug-in socket module.
Operator ground straps.
Plug-in Family Board Module (i.e., A/D, Op Amp, D/A)
Keyboard for entering data to fill in the blanks on ADI supplied device programs.

Modular AC/DC Power Supplies

Analog Devices ac/dc Power Supplies are designed to provide OEM's and circuit designers with a broad line of high reliability, regulated and short circuit protected power supplies at low overall cost. These modules are available with 5 volt to 12 volt outputs (single, dual and triple) and current ratings from 25mA to 2 amps. Most Analog Devices' Power Supplies are available from stock in both large and small quantities. Substantial discounts apply on quantity orders.

ADVANTAGES

Packaged circuit modules have found wide acceptance. Engineers have discovered the convenience and economy of plug-in building blocks . . . op amps, logic cards, miniature A/D and D/A converters are now available in wide varieties. Now a complete line of modular power supplies is available from Analog Devices. These encapsulated units are shipped ready to use, at prices below the internal manufacturing cost of most OEM users.

TRIPLE OUTPUT SUPPLIES – NEW

Analog Devices offers two new triple output ac/dc designs which are particularly useful in A/D, D/A and signal conditioning applications. Using a triple output supply is often less expensive than purchasing two separate supplies and also saves on space.

Model 923 is designed to provide power to data acquisition systems as well as A/D and D/A converters. The ±15V @ ±100mA outputs can drive linear circuits such as op amps, while the +5V @ 500mA output can power the digital logic.

Model 2B35 is designed to provide regulated excitation to transducers such as strain gages, pressure transducers or load cells, as well as ±15V power for amplifiers and other analog circuits. The single-resistor programmable transducer excitation output may be operated in two modes: constant voltage, providing a +1V to +15V output or a constant current, adjustable from 100μA to 10mA.

AC/DC POWER SUPPLIES FEATURES

- Current limited short circuit protection
- PC mounted and chassis mount designs
- Single, dual and triple output designs
- Current outputs of 25mA to 500mA for dual output supplies, 250mA to 2A for single output supplies
- Free-air convection cooling—no external heat sink required

GENERAL SPECIFICATIONS FOR ALL MODELS

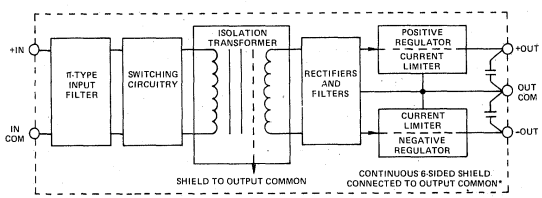
Input Voltage: 105V ac to 125V ac, 50 to 400Hz
Temperature Coefficient: 0.02%/°C
Input Isolation: 50 megohms
Breakdown Voltage: 500V rms, minimum
Operating Temperature: -25°C to +71°C
Operating at elevated temperatures may require derating. Consult factory.
Storage Temperature: -25°C to +85°C
Short Circuit Protection: All of the ac/dc Power Supplies employ current limiting. They can withstand substantial overload including direct shorts. Prolonged operation should be avoided since excessive temperature rises will occur.

Modular DC/DC Converters

Analog Devices' compact dc-dc converters satisfy a wide variety of floating power requirements in analog (Computational Circuits, Op Amps, Instrumentation Amps) and digital (a-d/d-a) applications. Available in three power levels of 1.8 watt (models 949), 4.5 watt (models 940, 941, 943, 945 and 953) and 12 watt (model 951), these designs offer accurate (±0.05% max error), regulated outputs with very low noise. Most models are high efficiency (typically over 60% at full load) that feature complete 6-sided continuous shielding for EMI/RFI protection.

DUAL OUTPUT MODELS

Logic to analog power conversion is available with models 940, 941, 949 and 951. These modules deliver floating power (±12V and ±15V) from logic power sources (+5V). This permits analog networks to be separated from digital systems in order to avoid intersystem grounding problems. Model 945 derives regulated ±15V outputs from any combination of inputs between 23 and 31 volts. The 945 can be powered from dual 12 volt, dual 15 volt, +24 volt or +28 volt power supplies.



Block Diagram – Models 940, 941, 945, 951 and 953

DC/DC CONVERTERS FEATURES

- Inaudible (>20kHz) converter switching frequency
- Continuous, Six-Sided EMI/RFI shielding except on model 949
- Free air convection cooling—no external heat sink or specification derating is required over operating temperature range
- Output short circuit protection(either output to common) for at least 8 hrs. at T_A = +71°C
- Automatic restart after short condition removed
- Automatic starting with reverse current injected into outputs

GENERAL SPECIFICATIONS FOR ALL MODELS

Line Regulation—full range: ±0.05% max (±1% max, 949)
Load Regulation—no load to full load: ±0.05% max (±0.5% max, 949)
Output Noise and Ripple: 1mV rms max (2mV rms max, 949)
Breakdown Voltage: 500V dc minimum
Input Filter Type: π (except model 949)
Operating Temperature Range: -25°C to +71°C
Storage Temperature Range: -40°C to +100°C

MODULAR AC/DC POWER SUPPLIES

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

Type		Model	Output Voltage Volts	Output Current mA	Line Reg. Max %	Load Reg. Max %	Output Voltage Error Max	Ripple and Noise mV rms Max	Inches Dimensions
PC Board Mounted	Dual Output	915	±15	±25	0.2	0.2	±1%	1	3.5X2.5X0.875
		904	±15	±50	0.02	0.02	+200mV -0mV	0.5	3.5X2.5X0.875
		902	±15	±100	0.02	0.02	+300mV -0mV	0.5	3.5X2.5X1.25
		902-2	±15	±100	0.02	0.02	+300mV -0mV	0.5	3.5X2.5X0.875
		920	±15	±200	0.02	0.02	+300mV -0mV	0.5	3.5X2.5X1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5X2.5X1.62
		921	±12	±240	0.02	0.02	+300mV -0mV	0.5	3.5X2.5X1.25
	Single Output	906	5	250	0.02	0.04	±1	1	3.5X2.5X0.875
		903	5	500	0.02	0.04	±1	1	3.5X2.5X1.25
		905	5	1000	0.02	0.05	±1	1	3.5X2.5X1.25
		922	5	2000	0.02	0.05	±1	1	3.5X2.5X1.62
	Triple Output	923	±15	±100	0.02	0.02	±1	0.5	3.5X2.5X1.25
			+5	500	0.02	0.05	±1	0.5	
		2B35J	±15	±65	0.08	0.1	(-0, +300mV)	0.5	3.5X2.5X1.25
			+1 to +15*	125	0.08	0.1	*	0.25	
		2B35K	±15	±65	0.01	0.02	(-0, +300mV)	0.5	3.5X2.5X1.25
			+1 to +15*	125	0.01	0.02	*	0.25	
	Chassis Mounted	952	±15	±100	0.05	0.05	±2	1	4.4X2.7X1.44
		970	±15	±200	0.05	0.05	±2	1	4.4X2.7X1.44
		973	±15	±350	0.05	0.05	±2	1	4.4X2.7X2.00
		975	±15	±500	0.05	0.05	±2	1	4.4X2.7X2.00
		955	5	1000	0.05	0.15	±2	2	4.4X2.7X1.44

*Resistor Programmable

MODULAR DC/DC CONVERTERS

SPECIFICATIONS (typical @ +25°C over the full range of input voltages unless otherwise noted)

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input Voltage Range Volts	Input Current Full Load	Output Voltage Error Max	Temperature Coefficient /°C Max	Efficiency Full Load Min	Dimensions Inches
943	5	1000	5	4.65/5.5	152A	±1%	±0.02%	62%	2.0 X 2.0 X 0.375
941	±12	±150	5	4.65/5.5	1.17A	±0.5%	±0.01%	58%	2.0 X 2.0 X 0.375
949	±15	±60*	5	4.65/5.5	0.6A	±2%	±0.03%	58%	2.0 X 1.0 X 0.375
940	±15	±150	5	4.65/5.5	1.35A	±0.5%	±0.01%	62%	2.0 X 2.0 X 0.375
953	±15	±150	12	11/13	0.6A	±0.5%	±0.01%	62%	2.0 X 2.0 X 0.375
945	±15	±150	28	23/31	250mA	±0.5%	±0.01%	61%	2.0 X 2.0 X 0.375
951	±15	±410	5	4.65/5.5	3.7A	±0.5%	±0.01%	62%	3.5 X 2.5 X 0.88

*Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120mA.

Technical Publications

Analog Devices provides a wide array of FREE technical publications. These include data sheets for all products, catalogs, Application Notes and Guides, and two serial publications: *Analog Productlog*, a digest of new-product information, and *Analog Dialogue*, our technical journal, with in-depth discussions of products, technologies, and applications.

In addition to the free publications, three technical handbooks and a set of *Analog-Digital Conversion Notes* are available at reasonable cost. The most-recent of these books is the *Transducer Interfacing Handbook*, published in Spring, 1980.

A brief description of this literature appears below. If you would like copies, or if you want to receive *Analog Productlog* and *Analog Dialogue*, please get in touch with Analog Devices or your nearby sales office.

CATALOGS

DATA ACQUISITION PRODUCTS CATALOG (this book)
Eight-hundred-eighty page book of data sheets for all Analog Devices circuit cards and components recommended for new designs.

DIGITAL PANEL INSTRUMENT CATALOG
Ninety-six-page data book for Analog Devices digital panel instruments and signal conditioning products.

POWER SUPPLY CATALOG (Short Form)
A concise eight-page brochure which describes and specifies Analog Devices ac to dc and dc to dc power supplies.

SYNCHRO CONVERTER SHORT-FORM GUIDE
Twelve pages of specifications and application material relative to synchro-to-digital and digital-to-synchro converters.

INTEGRATED CIRCUIT CHIPS FOR PRECISION HYBRIDS
One-hundred-twenty pages of support information for Analog Devices' precision chip program (55 products).

APPLICATION NOTES AND GUIDES

ISOLATION AND INSTRUMENTATION AMPLIFIER DESIGNERS GUIDE
This guide explains, in detail, the differences between isolation and instrumentation amplifiers, and the applications for which each type is optimized (24 pages).

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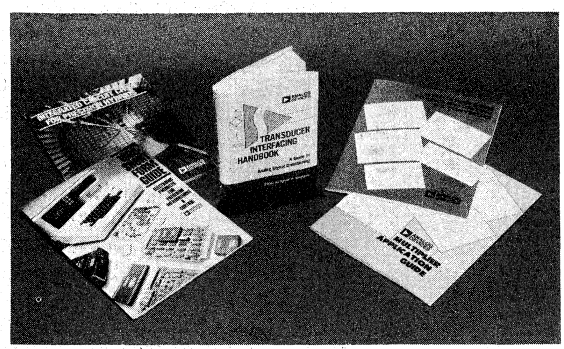
Over 30 workable applications for the ubiquitous multiplier. Circuits, specifications and theory (50 pages).

APPLICATION GUIDE TO CMOS MULTIPLYING D TO A CONVERTERS
This 44-page guide includes detailed information on the internal design and successful application of CMOS MDACs. Typical circuits discussed include measurement, function generation, programmable filters, and audio control.

VOLTAGE TO FREQUENCY CONVERTER APPLICATION NOTES
Twenty-four pages of V to F converter applications.

A USER'S GUIDE TO IC INSTRUMENTATION AMPLIFIERS
Application note tells how they work, explains their specifications and provides an example of error budget computation (12 pages).



AN IC AMPLIFIER USER'S GUIDE TO DECOUPLING, GROUNDING, AND MAKING THINGS GO RIGHT FOR A CHANGE (8 pages)
A down-to-earth application note on the often ignored topic of ground management in combined analog and digital systems.

UNDERSTANDING HIGH SPEED (Video) A/D CONVERTER SPECIFICATIONS
A sixteen-page profusely illustrated application note.

BOOKS

TRANSDUCER INTERFACING HANDBOOK (1980)
A Guide to Analog Signal Conditioning
Edited by D. H. Sheingold
A book for the electronic engineer who must interface temperature, pressure, force, level or flow transducers to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. This includes excitation, isolation, amplification, linearization, filtering, multiplexing, offsetting and display. The viewpoint is that of the practical, working scientist, engineer, or technician. Hardcover $14.50

MICROPROCESSOR SYSTEMS HANDBOOK (1977)
by Dr. D. Philip Burton and Dr. A. L. Dexter
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ANALOG-DIGITAL CONVERSION NOTES (1977)
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